

Capacitor Voltage Balancing of Four-Level ANPC and π -type Converters Based on Simplified Virtual-Vector PWM

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Abstract—Multilevel π -type and ANPC converters without flying capacitors and clamping diodes are emerging candidates for industrial applications due to their simple structure, less number of devices, and better harmonic performance. However, the voltage balancing difficulty is the key issue of these topologies similar to diode-clamped topology under conventional PWM methods. The unbalance of capacitor voltages may affect the system integrity and stability, and may degrade harmonic performance. To sort out this issue, a simplified virtual vector PWM method to balance the dc-link capacitor voltage of four-level three-phase π -type and ANPC converters is presented in this paper. Simulation results demonstrate that the proposed modulation strategy is easy to implement and effectively controls the balance of the capacitor voltages for the whole range of modulation index and load power factor under balanced and unbalanced loads.

Keywords— *simplified virtual-vector pulse-width modulation (SVVPWM), capacitor voltage balancing, four level ANPC converter, four level π -type converter*

I. INTRODUCTION

Multilevel converters are very common in high power and medium voltage applications in industry [1]. However they are also considered nowadays a good replacement of two level converters for low voltage applications [2, 3]. For instance, for a given dc-link voltage rating, multilevel converters allow operating with lower-voltage-rated devices with better performance features, reducing both switching and conduction losses, reducing the total harmonic distortion of voltage and current waveforms and thus reducing the output-filter size, and improving the converter fault-tolerance capacity. Another advantage of multilevel converters is their modularity. As shown in [4] for electric vehicle (EV) applications, multilevel topologies allow the use of single battery modules and power switches as a building block to conceive modular and scalable powertrain solutions for a wide

range of electric vehicle solutions, taking full advantage of scale economies.

Neutral-point-clamped (NPC) converter topologies are one of the most commonly used multilevel converter topologies because of their simple structure and easy control. Three main types of NPC converters are the diode clamped (DC), active NPC (ANPC) and π -type. Fig. 1 shows one phase leg of the four-level DC, ANPC and the π -type converters. As shown in Fig. 1, DC topology has six additional diodes, known as clamping diodes, in a single leg as compared to ANPC and π -type converters. The number of clamping diodes increases significantly when the leg number of levels increases, which limits the application of DC converters in industry. ANPC [5, 6] and π -type [7, 8] converters are more attractive due to their simple structure, with only six power switches per phase leg in the four-level case. Due to the reduced number of switching devices, the circuitry of ANPC and π -type converters becomes simple, and it is appropriate for low-voltage applications as well.

The inherent issue of NPC converter family is the voltage balancing of dc-link capacitors for higher level (greater than three) converter. The unbalance of capacitor voltages may affect the system integrity and stability, and may degrade harmonic performance. To sort out the issue of voltage unbalancing, many solutions have been discussed so far. In a general way they can be summarize as solutions based on hardware amendments and on software improvements. The hardware-based solutions are more expensive and complex because they use auxiliary hardware circuits [9] or back-to-back connections [10]. On the other hand, the software-based solutions use novel modulation algorithms to achieve the capacitor voltage balancing [11, 12].

A carrier-overlapped PWM method to balance the capacitor voltage of DC and ANPC four-level converter is proposed in [12] and [6], respectively. The main advantage of

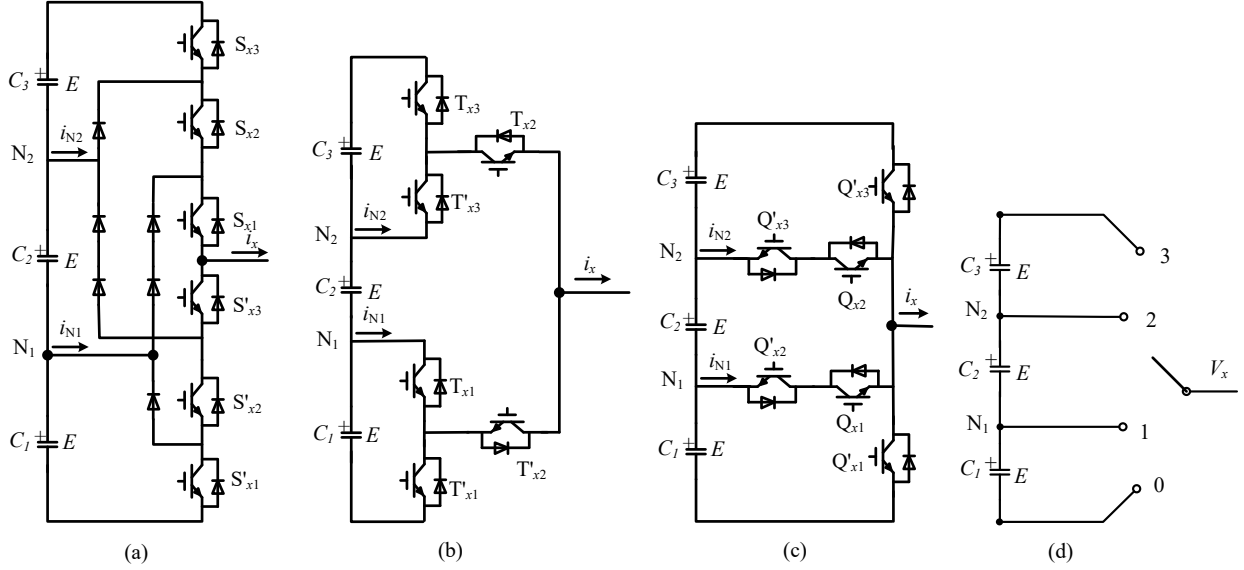


Fig. 1. A phase leg of four-level NPC converters: (a) DC, (b) ANPC, (c) π -type NPC, (d) equivalent single-pole four-throw switch

TABLE I. SWITCHING STATES OF 4L-ANPC AND π -TYPE CONVERTER

$T_{x1}/$ Q_{x1}	$T_{x2}/$ Q_{x2}	$T_{x3}/$ Q_{x3}	$T'_{x1}/$ Q'_{x1}	$T'_{x2}/$ Q'_{x2}	$T'_{x3}/$ Q'_{x3}	i_{N1}	i_{N2}	Voltage Level
1	1	1	0	0	0	0	0	3E
1	1	0	0	0	1	0	i_x	2E
1	0	0	0	1	1	i_x	0	E
0	0	0	1	1	1	0	0	0

this method is its simple implementation because all the switching signals can be generated by comparing multiple carriers with one reference signal, similar to classic carrier-based modulations. Another carrier-based solution for hybrid-clamped π -type four level converter is presented in [13] to regulate the neutral-point voltage. A flying capacitor and two additional power switches are added to the basic version of π -type converter demonstrated in [7] to address the balancing issue of dc-link capacitors. A redundant-level modulation algorithm has been discussed in [14] to control the capacitor voltage of four-level π -type converter by using an additional voltage level in a carrier cycle. Similar approach has been applied on four-level ANPC converter in [15] for EV applications.

Virtual-space-vector-based solutions are also very promising in controlling the neutral-point voltage of multilevel NPC converters. A virtual-vector PWM (VVPWM) is implemented on four-level DC in [16] and for multilevel active clamped converter in [17, 18] by defining new virtual vectors consisting of more than two switching states that guarantees zero average neutral-point current in each switching cycle. However, the harmonic distortion and switching losses are increased due to the increase of switching transitions in each switching cycle.

Another virtual-vector-based solution is the simplified virtual-vector PWM (SVVPWM), proposed in [19] and experimentally validated in [20] under steady-state and dynamic regimes for multiple operation conditions for four-level DC. The SVVPWM can be easily implemented as it transforms the four-level space-vector diagram to a three-level space-vector diagram. Moreover, SVVPWM is advantageous in sense of harmonic distortion and switching losses as compared to its counterpart [21].

The main focus of all aforementioned virtual-vector-based modulations is DC converter. Very limited efforts have been reported so far in the literature regarding the capacitor voltage control in ANPC and π -type converters. Four-level DC, ANPC and π -type converter topologies can be represented as single-pole four-throw switches as shown in Fig. 1. The voltage balancing control implementation is identical as DC for ANPC and π -type converters. The only difference is the correspondence between the PWM signals and switches. The contribution of this paper is to implement the SVVPWM algorithm to balance the dc-link capacitor voltage of four-level three-phase ANPC and π -type converters as these topologies are getting more attention nowadays in EV applications due to their simple structure and reduced number of switching devices. The converters operation is validated through simulation results.

II. VOLTAGE BALANCING PROBLEM AND MODULATION

Fig. 1 shows a phase leg of four-level DC, ANPC and π -type converters. Each phase leg is composed of six complementary switches named as $(S_{x1}-S_{x3}$ and $S'_{x1}-S'_{x3}$) for the DC topology, $(T_{x1}-T_{x3}$ and $T'_{x1}-T'_{x3}$) for the ANPC topology, and $(Q_{x1}-Q_{x3}$ and $Q'_{x1}-Q'_{x3}$) for π -type topology. Neutral point currents are denoted as i_{N1} and i_{N2} passing through the two neutral points N_1 and N_2 respectively. Dc-link capacitors are represented as C_1-C_3 . ANPC and π -type

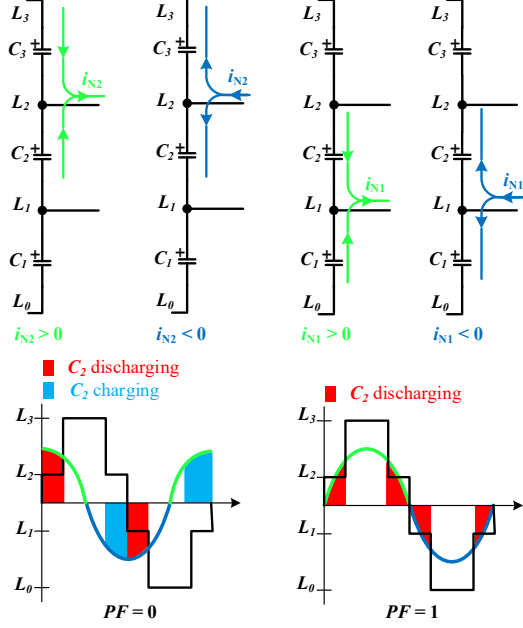


Fig. 2. Effect of neutral point currents on C_2 .

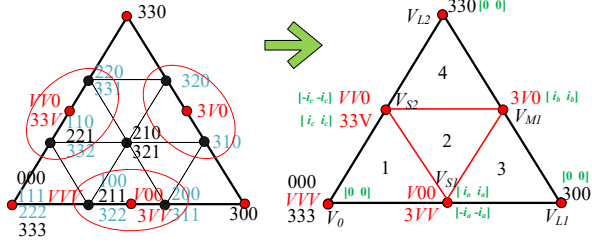


Fig. 3. First sector of the space diagram for the CSPWM (left) and the SVVPWM (right).

topologies are a simplified form of four-level converters with a lower number of devices. However, the cost to be paid in simplification is complications in voltage balancing and higher blocking voltage of some devices. Four-level ANPC is a simplified form of four-level hybrid clamped converter. Switching devices T_{x2} and T'_{x2} in 4L-ANPC have to withstand higher voltages as compared to other devices. The solution of this problem has been presented in [22] by using hybrid Si/SiC configuration. In case of π -type converter, common collector configuration is used to connect the power switches Q_{x2} and Q'_{x3} , to form a four-quadrant switch. The benefit of this configuration is that a same gate driver supply can be used for three devices Q_{x1} , Q_{x2} and Q_{x3} . Table I shows the relation between neutral point currents, switches of ANPC and π -type converters, and output voltage levels.

As discussed earlier, ANPC and π -type converters face a voltage balancing problem under certain operational conditions specifically for high modulation index and unity power factor by using conventional PWM methods. In case of four-level NPC converters, the middle capacitor discharges and the converter starts behaving like a three-level converter. Fig. 2 shows the effect of neutral point currents on charging and discharging of middle capacitor C_2 in a fundamental cycle

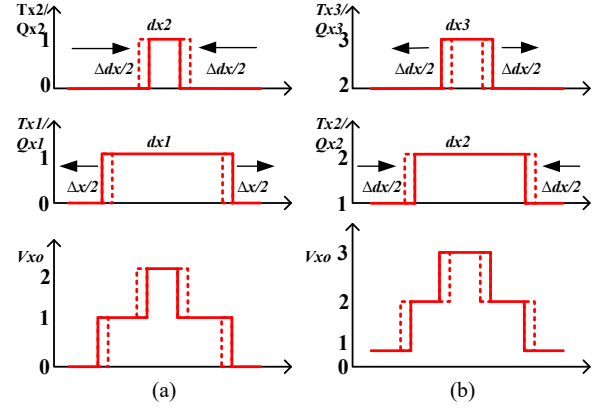


Fig. 4. Duty ratio adjustment to balance the voltage of C_2 . (a) $0 \leq V_{ref} < V$. (b) $V \leq V_{ref} \leq 3$

TABLE II. DUTY RATIO ADJUSTMENT OF SWITCHES FOR $V_{C2} < E$

V_{refx}	i_x	d'_{x3}	d'_{x2}	d'_{x1}
$0 \leq V_{refx} < V$	$i_x > 0$	0	$-\Delta d_x$	$+\Delta d_x$
	$i_x < 0$	0	$+\Delta d_x$	$-\Delta d_x$
$V \leq V_{refx} \leq 3$	$i_x > 0$	$+\Delta d_x$	$-\Delta d_x$	0
	$i_x < 0$	$-\Delta d_x$	$+\Delta d_x$	0

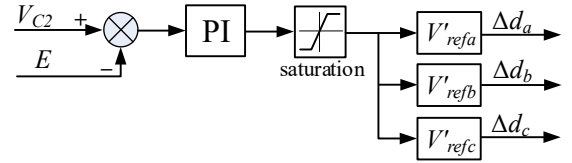


Fig. 5. The diagram of obtaining the factor Δd_x

at two extreme cases; i.e., zero and unity power factor. For the sake of simplification, phase-leg switching frequency is equal to the output-voltage fundamental frequency. In case of zero power factor, when phase-leg output is connected to L_2 dc-link point and the direction of the output current is positive ($i_{N2} > 0$), capacitor C_2 discharges. When direction of current is negative ($i_{N2} < 0$), the capacitor C_2 charges. Similarly, when output is connected to level L_1 and $i_{N1} < 0$, capacitor C_2 discharges and when $i_{N1} > 0$ the capacitor C_2 charges. Under this condition, due to the equal charging and discharging of middle capacitor C_2 in a fundamental cycle, the dc-link capacitor voltages are balanced automatically.

In case of unity power factor, the middle capacitor continuously discharges in a fundamental cycle regardless the direction of the output current, as shown in Fig. 2. Therefore, the balancing of dc-link capacitors becomes harder for unity power factor case by using conventional modulation methods.

A virtual vector based modulation method named as SVVPWM proposed in [21] is implemented on four level three-phase ANPC and π -type converters in this article. Compared to the conventional space vector PWM (CSVPWM), the SVVPWM employs a set of virtual switching states defined by a linear combination of two or more adjacent switching states. The derivation of the four-level simplified virtual space vector diagram from the

conventional space vector diagram is shown in Fig. 3. The nine small regions of a given triangular sector of the conventional diagram are converted into four regions, resembling the three-level-case conventional diagram, which makes the duty ratio calculations and identification of reference vector very simple. The value of the neutral point currents is denoted between brackets, with $[i_{N1}, i_{N2}]$.

Each virtual switching state of the SVVPWM diagram in Fig. 3, features equal neutral point currents ($i_{N1} = i_{N2}$), which can take the value of either zero or any of the three phase currents ($\pm i_a, \pm i_b, \pm i_c$). Similar neutral point currents do not affect the voltage of capacitor C_2 . So, voltage of middle capacitor balanced naturally in a carrier period. The voltage of other two capacitors can be balanced by adjusting the application time of two virtual switching states of any small vector as they have opposite neutral point currents. The sub sector identification, duty ratio calculations and switching sequence in any triangular region is the same as the three-level converter case, discussed in detail in [20].

III. CAPACITOR VOLTAGE BALANCING CONTROL

The presence of neutral point currents is the main reason for voltage unbalancing of dc-link capacitors. SVVPWM is capable of balancing the capacitor voltage naturally for steady state operation. However, the dc-link capacitor voltages may unbalance under dynamic operation and due to converter non idealities. Thus, a closed-loop control is necessary, such that by modifying certain modulation variables, maintains the capacitor voltages balanced. Considering $C_1 = C_2 = C_3 = C$, the variation of the capacitor voltages (ΔV_{C1} , ΔV_{C2} , and ΔV_{C3}) for a given time period (T_s) due to the neutral-point currents can be expressed as

$$\begin{aligned}\Delta V_{C1} &= -\frac{2}{3} \cdot \left(\frac{i_{N1} \cdot T_s}{C} \right) - \frac{1}{3} \cdot \left(\frac{i_{N2} \cdot T_s}{C} \right) \\ \Delta V_{C2} &= \frac{1}{3} \cdot \left(\frac{(i_{N1} - i_{N2}) \cdot T_s}{C} \right) \\ \Delta V_{C3} &= \frac{1}{3} \cdot \left(\frac{i_{N1} \cdot T_s}{C} \right) + \frac{2}{3} \cdot \left(\frac{i_{N2} \cdot T_s}{C} \right).\end{aligned}\quad (1)$$

As shown in (1), the voltage of each capacitor is affected by both neutral point currents. The voltage balancing task can be separated in two parts, as the voltage deviation in C_1 and C_3 is due to sum of both neutral-point currents, while C_2 deviation is only due to the difference of both currents.

A. Voltage Balancing of Capacitors C_1 and C_3

Voltage balancing procedure of capacitors C_1 and C_3 is identical to three-level converter case as the four-level space vector diagram is similar to three-level case, which has been discussed by many authors [23]. Voltage deviation between these capacitors can be written as

$$\Delta V_{C31} = V_{C3} - V_{C1} = \frac{(i_{N1} + i_{N2})T_s}{C} = \frac{i_{NP}T_s}{C}. \quad (2)$$

To diminish the voltage variations between two capacitors, the demanded neutral point current can be expressed as

$$i_{NP,ref} = \frac{C(V_{C1} - V_{C3})}{T_s}. \quad (3)$$

The average current in a carrier period should be zero to guarantee the voltage balancing between the two outer capacitors. The SVVPWM guarantees that the average current is zero in each carrier cycle. For example, in region 4 of simplified virtual vector diagram shown in Fig. 3, small vector V_{S2} is composed of virtual states “ $VV0$ ” and “ $33V$ ” which have opposite neutral point currents. So, by adjusting the application time of these virtual states, nonzero current produced by medium vector can be controlled same as three-level converter. The duty ratio of these virtual switching states can be expressed as

$$\begin{aligned}d_{VV0} &= k \cdot d_{VS2} \\ d_{33V} &= (1-k) \cdot d_{VS2}\end{aligned}\quad (4)$$

where $k \in [0, 1]$ is the sharing factor between two redundant switching states and can be calculated similar to three-level converter.

B. Voltage Balancing of Capacitor C_2

The voltage variation in capacitor C_2 is due to the difference of both neutral-point currents. Neutral-point currents i_{N1} and i_{N2} in a carrier cycle for phase x , where $x \in (a, b \text{ and } c)$, can be expressed as

$$\begin{aligned}i_{N1x} &= (d_{x2} - d_{x1}) \cdot i_x \\ i_{N2x} &= (d_{x3} - d_{x2}) \cdot i_x.\end{aligned}\quad (5)$$

Here d_{x1} , d_{x2} and d_{x3} represent the duty ratio of switches T_{x1}/Q_{x1} , T_{x2}/Q_{x2} and T_{x3}/Q_{x3} of the ANPC and π -type converters respectively as shown in Fig. 1. From (1) and (5), the average current of capacitor C_2 in a carrier cycle can be derived as

$$i_{C2x} = i_{N1x} - i_{N2x} = (2d_{x2} - d_{x1} - d_{x3}) \cdot i_x \quad (6)$$

Thus, C_2 voltage can be controlled by changing d_{x1} , d_{x2} and d_{x3} duty ratio. For instance, let us suppose that the voltage of capacitor C_2 is less than its nominal voltage E . To set its voltage back to E , C_2 must be charged. Depending on the position of reference vector V_{ref} , and assuming $i_x > 0$, two different procedures to regain the voltage balance can be taken:

1) $0 \leq V_{refx} < V$: Here V is the virtual dc-link connection representing dc-link points 1 and 2. In this case, switch T_{x3}/Q_{x3} is in off state for the whole carrier cycle. To charge capacitor C_2 , the on time of switch T_{x2}/Q_{x2} must be decreased and the on time of switch T_{x1}/Q_{x1} must be increased with factor Δd_x as shown in Fig. 4. The solid line represents the modified duty ratio while the dotted line is the original duty ratio of the switches.

2) $V \leq V_{refx} \leq 3V$, in this case, the switch T_{x1}/Q_{x1} is in on position for whole carrier cycle so $d_{x1} = 1$. To charge the capacitor C_2 , the on time of switch T_{x2}/Q_{x2} must be decreased and the on time of switch T_{x3}/Q_{x3} must be increased with factor Δd_x .

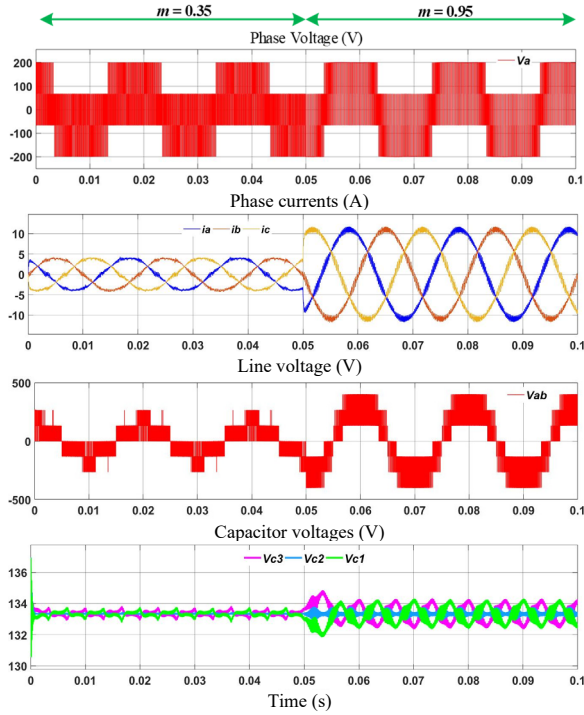


Fig. 6. Simulation results of ANPC converter for PF = 0.999.

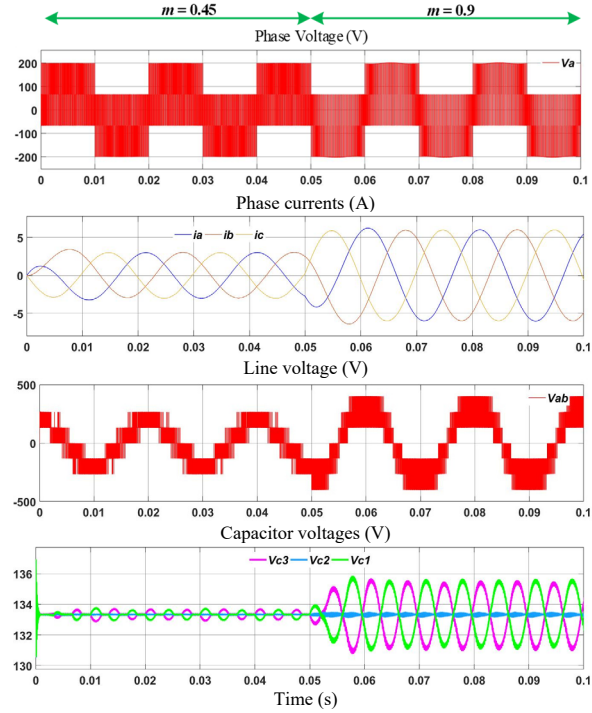


Fig. 7. Simulation results of π -type converter for PF = 0.577.

This process is summarized in Table II. PI regulator is used to obtain the factor Δd_x as shown in Fig. 5. The new adjusted values of duty ratio for switches T_{x1}/Q_{x1} , T_{x2}/Q_{x2} and T_{x3}/Q_{x3} is $d_{x1} + d'_{x1}$, $d_{x2} + d'_{x2}$, and $d_{x3} + d'_{x3}$. The balancing of the capacitor voltage under transients can be achieved by following above procedure.

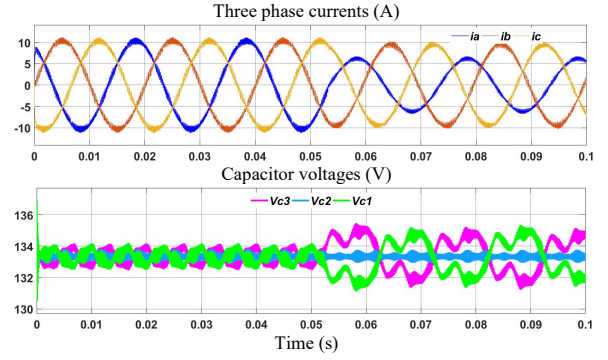


Fig. 8. Simulation results for unbalanced load.

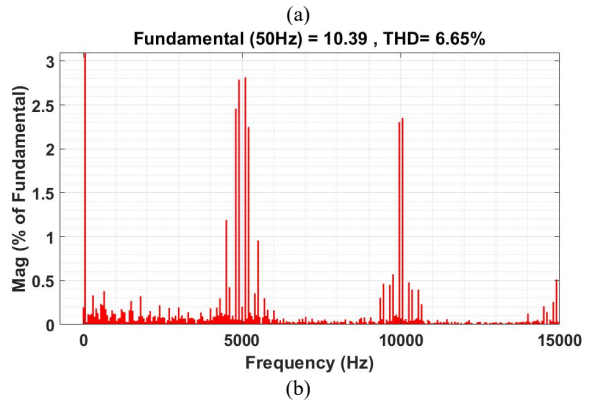
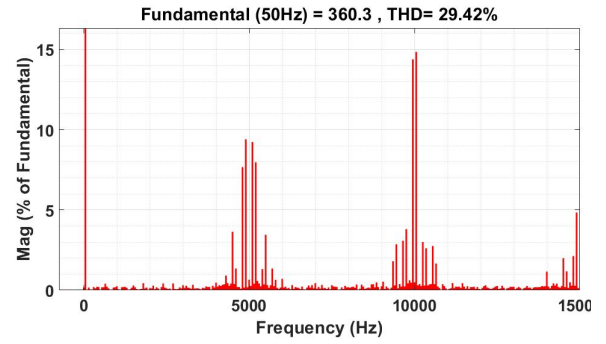


Fig. 9. Harmonic spectrum of (a) line voltage (b) phase current.

IV. SIMULATION RESULTS

The performance analysis of the SVVPWM algorithm is done by conducting MATLAB simulations for four level three-phase ANPC and π -type converters. The value of dc-link voltage is 400 V and 800 μ F capacitors are used to perform simulations for different operational conditions under a carrier frequency of 5 kHz.

Fig. 6 presents the simulation results for the ANPC converter. Dynamic performance of SVVPWM has been demonstrated in these results by making a change in modulation index from $m = 0.35$ to $m = 0.95$ under a large power factor of 0.999 ($R = 20 \Omega$, $L = 2$ mH). From the results, it is fair to infer that the capacitor voltages balancing can be guaranteed for the whole modulation index range. The line

voltage and phase currents amplitude increase due to the change in modulation index.

Simulations are also conducted for the four-level π -type converter by using SVVPWM (Fig. 7). Results are shown for a low power factor of 0.577 ($R = 20 \Omega$, $L = 90 \text{ mH}$). The average value of the capacitor voltage is kept to its nominal value for both modulation index, with a voltage ripple at three times the fundamental frequency, whose amplitude increases with the modulation index. Fig. 8 shows simulation results under an unbalanced three-phase load. A 20Ω resistor is added in phase a at time 0.05 s, reducing the phase current. It can be seen that the capacitor voltages remain balanced in average during a fundamental period, even when the load is unbalanced, proving the effectiveness of the presented SVVPWM and closed-loop control.

The line voltage and phase current harmonic performance of the SVVPWM is presented in Fig. 9 for modulation index $m = 0.9$. The harmonic content is concentrated around the carrier frequency and integer multiples of the carrier frequency. Thanks to the high-frequency harmonic content, this can be easily filtered with a reduced-size filter.

V. CONCLUSIONS

In this paper, a simplified VVPWM is implemented on four-level three-phase ANPC and π -type converters that guarantees the dc-link capacitor voltages balancing. The modulation for the four-level converters is simple in its implementation since it allows the simplification to the less complex three-level case. Simulations are conducted for both ANPC and π -type converters, proving that the SVVPWM is capable of balancing the capacitor voltages for multiple modulation indexes and for low and high power factor, as well as under balanced and unbalanced loads.

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