CMOS Inverter performance degradation and its correlation with BTI, HCI and OFF State MOSFETs aging

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***Abstract*— In this work, CMOS inverters are subjected to electrical stress emulating a complete operation cycle and the shifts in the performance parameters (i.e., peak current and inversion voltage) evaluated. Moreover, degradation of the two MOSFETs is also measured as variations of their threshold voltage and mobility. The relationships between the observed transistors and circuit parameter shifts are explained in terms of the different device aging mechanisms (i.e., BTI, CHI and OFF-state) that are active depending on the voltages at the circuit terminals. Moreover, the combined effects of the aging mechanisms that are sequentially activated, at device and circuit levels, and their voltage dependence, are also discussed. Finally, a power law fitting of the inversion voltage degradation of the inverter is used to evaluate its variation at operating conditions.**

I. INTRODUCTION

Device aging mechanisms such as Bias Temperature Instabilities (BTI) and Hot-Carrier Injection (HCI) degradation are of increasing importance in deep CMOS scaled technologies, significantly reducing device and circuit reliability [1]. Customary, BTI and HCI aging are studied in stand-alone devices [2-7] and aging models are formulated for device and circuit lifetime predictions [7-10]. However, to develop realistic and accurate device aging models, it is necessary to take into account the actual operation conditions of the devices when integrated in a circuit. This is not a simple task, since normally it is difficult to access the device terminals in a circuit to observe the aging impact on the device electrical parameters, so that it can be correlated to circuit performance changes. With this aim, dedicated circuit test structures could be designed and measured [22]. But also, because the stress conditions of the device in the circuit dynamically change by the aging suffered by the devices themselves, what is difficult to reproduce in stand-alone experiments. This aging is actually the result of the combined effect of the several aging mechanisms that are activated depending on the actual biasing of the device in the circuit. The effect of two different stress configurations that sequentially activate two aging mechanisms (one after the other) in an isolated device has been analyzed previously in the literature [11-13]. However, device aging in a circuit may differ from that actually experienced in this kind of tests. As an example, interestingly, for example, the relevance of off-state degradation [14-19] is not revealed. Other works analyze the sequential effect of several aging mechanisms by applying pulsed stress conditions, which are closer to circuit operation. However, these experiments do not allow the observation of the device and circuit parameters shifts during the stress, but only at the end of the stress [20-22]. This can be useful for circuit lifetime prediction, but relevant information on the aging suffered by the devices in the circuit as a consequence of the different activated aging mechanisms is lost, as well as how they could be mutually compensated. In this regard, experimental studies of the circuit performance degradation are rather limited and device-circuit aging correlations are still unclear [21-25].

In this work, the aging of the transistors in a CMOS inverter during a complete cycle of operation and their impact on the circuit performance is experimentally studied. Several stress configurations have been considered, to evaluate the impact of NBTI, PBTI, HCI and OFF-state aging mechanisms, and their interdependences, on the pMOSFET and nMOSFET threshold voltages (V_{TH}) and mobilities (μ), as well as the circuit performance degradation (measured as changes in the inversion voltage and peak current). In this sense, the correlation of the device aging and the CMOS inverter performance shifts is studied. The voltage dependence of the observed degradation is also analyzed. Finally, the degradation of the CMOS inverter at operating conditions is evaluated, by fitting of the Inversion Voltage (V_{INV}) to a power law that accounts for the stress time and voltage conditions.

II. Device and Stress Procedure Description

The circuits used in this work (see Figure 1) were fabricated on a commercial 65-nm technology with 1.2 V nominal operation voltage and purposely designed to evaluate aging of RF Low Noise Power Amplifier [at 2.45GHz] [22, 26], but in this work they will be operated as inverter under DC stress conditions. The pMOSFET and nMOSFET W/L dimensions were 180µm/60nm, and the gate was split in 45 fingers. To avoid detrimental series resistance effects during the high-voltage HCI stresses, high conductive tips were used in combination with a Semiconductor Parameter Analyzer that allows Force/Sense measurements, to minimize IR-drops. In order to exactly fix the inversion point (i.e, the input voltage at which output and input are equal), the structure includes an external resistive feedback between the circuit input and output that can be connected or disconnected. When connected, it provides self-biasing (see Fig. 1.B) [22] of the structure, emulating the transitions during the inverter operation. When disconnected, the structure behaves as a standard CMOS inverter. This topology was purposely chosen to allow access to all the transistor terminals, so that the aging of the individual devices, as well as their impact on the performance of the circuits when operated as a Power Amplifier under RF conditions could be evaluated [23]. However, in this work, these circuits will be operated as CMOS inverters, to analyze the shifts of the device/circuit performances in more detail, using a sequence of constant voltages at the gates (input terminal) that emulates the inverter operation.

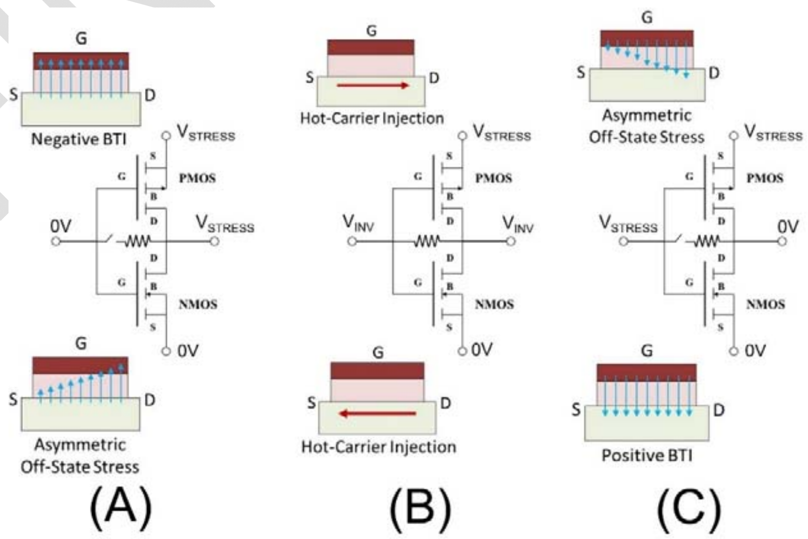


Figure 1. CMOS inverter voltage configuration and active aging mechanisms at (A) low input, (B) inversion point, and (C) high input. The vertical electric field at the gate dielectric during BTI and OFF-State aging (blue arrows) and the currents for HCI (red arrows), for the different inverter stress conditions, are also depicted.

Different electrical stress configurations of the devices were identified in a complete inverter operation cycle (Figures 1 A, B and C). When a low voltage (logic '0') is applied to the input (case A), a negative voltage drop between the gate-source and gate-drain terminals of the pMOSFET is forced, so that pMOSFET suffers NBTI stress. The nMOSFET is OFF, but a non-uniform electric field is applied to the gate dielectric, due to the large V_{DS} forced by the '1' logic output, so that actually the nMOSFET suffers OFF-state aging [14-19]. It must be emphasized that usually this stress mode is overlooked in stand-alone device reliability tests, but it is actually acting in an inverter. When the input voltage is switched to '1' (high input voltage), the output voltage shifts from '1' to '0'. During the transition, both transistors are ON and significant current flows through their channels, being subjected to HCI stress (case B). The worst case HCI stress corresponds to the inversion voltage (V_{INV}) where V_{IN}=V_{OUT} (V_{DS}=V_{GS}), for this short channel devices [27], which in our circuit configuration can be evaluated by connecting the resistor. Finally, case C represents the situation when a logic '1' (i.e. high voltage) is applied to the input, so that the nMOSFET suffers from PBTI and the pMOSFET from OFF-state aging (case C, complementary to case A).

This stress sequence has been emulated using the voltage sequence 'S0V1' in Fig. 2A. Note however, that the actual fast '0' to '1' (or vice versa) state transitions have been replaced by a constant voltage at V_{INV} (Input/Output voltages at the inversion point, thanks to the self-biasing). To induce a measurable degradation in a short period of time, the supply voltage was increased over the nominal operation voltage (i.e. 1.2V). To evaluate the voltage dependence of the degradation, several supply voltages were applied, ranging from 2.3V to 2.6V. The high (supply voltage) and low (0 V) input stresses are applied for 300 seconds and the stresses at V_{INV} for 30 seconds. The stress effects on the devices and circuit parameters have been evaluated by measuring the transistors curves (I_D-V_{GS} and I_D-V_{DS}, to extract V_{TH} and μ) and the CMOS inverter characteristics (transfer curve and peak current) before any stress (pristine samples) and after each stress phase (marked with orange flags in Fig. 2A). V_{TH} and μ were obtained from the I_D-V_{GS} curves using a least-squares method that minimizes the error between measurements and the equational transistor model provided by the manufacturer for the triode region [23]. To explain the results obtained during this stress sequence, simpler stress configurations have been considered. To evaluate the effects of NBTI, PBTI, OFF-state and HCI aging in the transistors and the inverter performance, only low input (S0) and only high input (S1) have been considered. To analyze the effects of the sequential activation of mechanisms, low-high inputs (S0-1) have also been alternatively applied. For comparison, the duration of all the stress phases in the sequence has been kept equal (300 s). The stress sequences have been applied several times (namely, iterations), to evaluate the evolution of the degradation with time.

On the other hand, Figure 2B shows the CMOS inverter transfer curves of the pristine device (continuous lines). Typical curves measured after stress (dashed lines) are also included. Note that the stress has introduced a shift of the transfer curve (i.e. of the inversion voltage) and a decrease of the peak current [28]. In the next sections, the dependences of these shifts with the applied stress and their correlation with the MOSFETs aging are evaluated in detail.

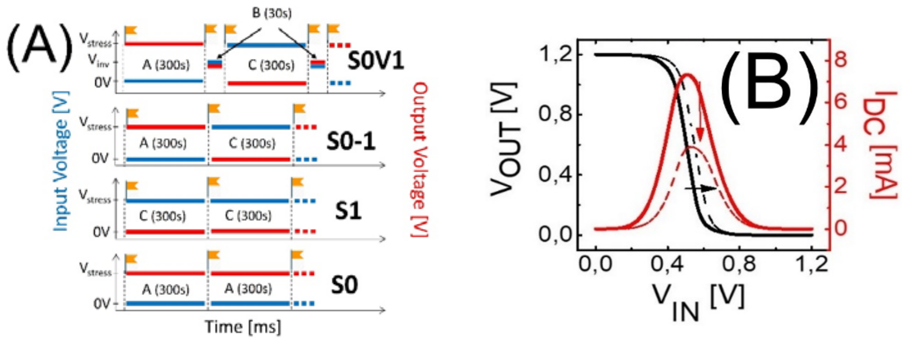


Figure 2. (A) Applied input (blue) and output (red) voltages for each stress sequence. V_{STRESS} was varied to evaluate the voltage dependence of the degradation. Labels indicate the stress voltage configurations of the transistors: (S0V1) alternation of low and high inputs, with and intermediate 30 seconds stage where input and output voltages are coincident thanks to the inverter self-bias, (S0-1) alternation of low and high inputs, (S1) high input, and (S0) low input. Flags indicate the times at which the electrical characterization of the CMOS inverter and MOSFET transistors is performed. (B) Typical inverter transfer curve (black) and peak current (red) for pristine (solid lines) and damaged (dashed lines) CMOS inverter.

III. RESULTS AND DISCUSSION

A. *MOSFETs and circuit degradation: dependence on the stress history*

The degradation of the MOSFETs and CMOS inverter has been analysed in detail. Unless contrarily indicated, all the results shown in this section correspond to V_{STRESS} =2.4V. Shifts of V_{TH} and μ of the nMOSFET and pMOSFET, V_{INV} in the inverter transfer curve, and inverter peak current (I_{DC}) as a function of the stress time (i.e. #iteration) for the different stress sequences have been evaluated. Figure 3 shows the evolution of the relative variation of V_{INV} and I_{DC} of the CMOS inverter (Fig. 3A and 3B, respectively) and V_{TH} and μ of the nMOSFET and pMOSFET transistors (Fig. 3C-3E, and Fig. 3D-3F, respectively) as a function of the stress iteration.

For S0 (low input, open triangles), the nMOSFET is under OFF-State stress, whereas the pMOSFET is under NBTI. Then, as expected for this technology, V_{TH} shift of the pMOSFET is larger than for the nMOSFET, (~1.2% vs ~0.8%). However, surprisingly, ΔV_{TH} and Δμ of the nMOSFET are relevant, especially for Δμ (~7% versus ~4% for the pMOSFET), which could be related to the generation of interface traps and positive oxide charges at the gate-drain region during the OFF-state stress [14, 15, 16]. At circuit level, ~8% I_{DC} reduction and ~0.8% inversion point shift are observed. These results suggest that (i) I_{DC} variation is dominantly controlled by Δμ, whereas the transfer curve shift is mainly determined by ΔV_{TH} of the transistors, and (ii) the inverter degradation is mainly controlled by the OFF-state nMOSFET aging.

For S1 (high input, solid triangles), no significant variations of the inverter performance are observed (Fig. 3A and 3B), clearly related to the negligible variations of μ and V_{TH} of both transistors. Regarding the nMOSFET, this can be explained by the negligible effect of PBTI stress expected on our Poly/SiON gate stacks in 65nm technology [29]. Moreover, results also suggest that, contrarily to the nMOSFET, the OFF-state stress in the pMOSFET is not as relevant. Therefore, unexpectedly, a low input (S0) is much more detrimental than a high input (S1), from the circuit perspective. This is because the device aging mechanisms activated when a low input (S0) is applied produce larger device degradations, and therefore, larger circuit performance shifts.

The results obtained when sequence S0-1 (solid circles) is applied, i.e., there is an alternation of high and low inputs, are depicted in Fig. 3 with red circles. For the nMOSFET, small fluctuations of ΔV_{TH} around 0% are registered, what suggests that the application of a high voltage (PBTI) after a low voltage (OFF-state) mostly compensates the effects of the previous OFF-state stress on the V_{TH}. However, this does not hold for $\Delta\mu$, since a large decrement of μ is observed, following a similar trend as in S0. On the other hand, μ and V_{TH} of the pMOSFET are clearly degraded during low input stage (NBTI), but largely relaxed during the next high input phase (OFF-state) [15], as observed in Fig. 3D and 3F, producing oscillating variations of the pMOSFET parameters. All those changes at device level are observed as small variations of the inversion voltage (< ~0.2%) around the fresh value, but ~6% variation of I_{DC} (as for sequence S0) due to the large μ reduction of both transistors. The large pMOSFET relaxation (during high input stress) is reflected in the peak current evolution, which oscillates as observed for S0. These results seem to directly relate the μ variations of both transistors with peak current, and V_{TH} with inversion voltage.

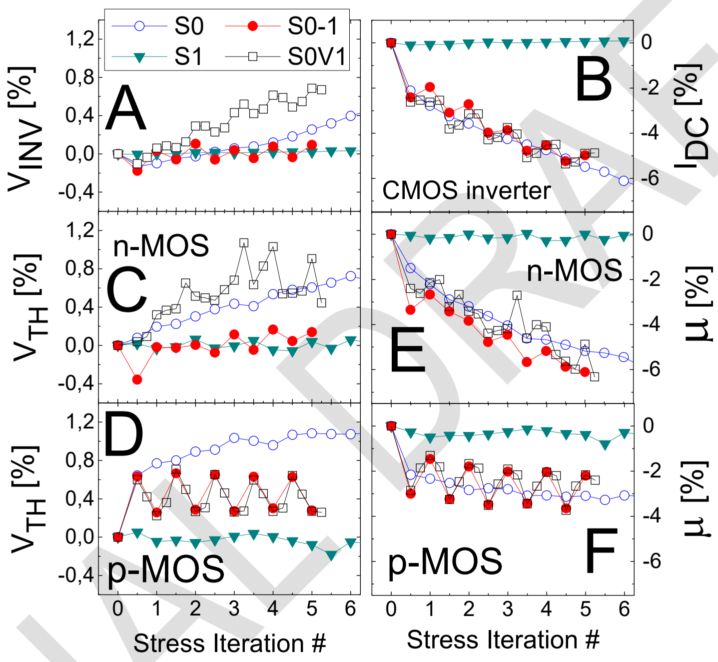


Figure 3. Relative variations of the inversion voltage (A), peak current at the inversion point (B) of the CMOS inverter, threshold voltage (C and D) and carrier mobility (E and F) of the nMOS (C and E) and pMOS (D and F), for the different sequences defined (S0, S1, S0-1 and S0V1) shown in figure 2-A.

Finally, results corresponding to S0V1 (open squares), where the intermediate HCI stress is introduced, are shown with open squares in Fig. 3. For the pMOSFET parameters, degradation and relaxation are alternatively observed again, and the self-bias stage (HCI) simply acts as an intermediate degradation state between the maximum and minimum. Therefore, during inverter operation, in this technology, NBTI is the main aging mechanism for the pMOSFET, which is largely relaxed when the voltage drops at its terminals change (with or without current flow), having HCI a negligible effect. Regarding the nMOSFET parameters, similar trends as for S0 are observed for S0V1. For ΔV_{TH}, since the alternation of high and low voltages compensates the V_{TH} shift (S0-1 in Fig. 3C), and the inclusion of the HCI state provokes a degradation of V_{TH}, this suggests that HCI aging mechanism plays an important role in the V_{TH} degradation of the NMOS transistors (and then in the variation of inversion voltage). Then, the damage becomes permanent, so that a similar trend as for S0 is observed, also at circuit level (i.e., large increase of ΔV_{INV}). As far as $\Delta\mu$ is concerned, no remarkable difference is observed with respect to the case S0-1, and only similar fluctuations as for S0 are measured. Consequently, no significant differences are observed for I_{DC} in the S0, S0-1 and S0V1 cases, being dominated by the nMOSFET Δμ (see fig. 3B).

B. *Stress voltage dependence*

To analyse the effect of the stress voltage conditions, circuits have been measured when the sequence S0V1 is applied at different supply/input voltages (2.3V, 2.5V and 2.6V), in addition to the 2.4V case previously studied. Figure 4 shows the relative variations of the circuit parameters shifts (V_{INV} and I_{DC}, figures 4A and 4B, respectively) and of the device parameters (V_{TH} and μ of the N-type and P-type transistors, figures 4C to F) as a function of the stress time. As shown in figure 4, similar temporal evolutions of the parameters shifts than for the case of 2.4V (shown in figure 3) is observed for the 2.3V, 2.5V and 2.6V input voltages. The cumulative effect of the aging mechanisms is also observed for device and circuit parameters shifts, with larger relative variations as the stress voltage increases. When observing the correlations between device (V_{TH} and μ) and circuit parameters (V_{INV} and I_{DC}) shifts, again V_{INV} (figure 4A) seems to be dominated by the V_{TH} variations, especially by those of the nMOSFET (Figure 4C). Nonetheless, the strong relaxation of the pMOSFET degradation under the OFF-state stress (figure 4D) is also observed in the V_{INV} variation as small relaxations (Figure 4A). On the other hand, the I_{DC} reduction (~15% in the case of 2.6V, pink triangles) is determined by the reduction of the mobility of both transistors, being closer to the nMOSFET Δμ (~20% in the case of 2.6V, pink triangles).

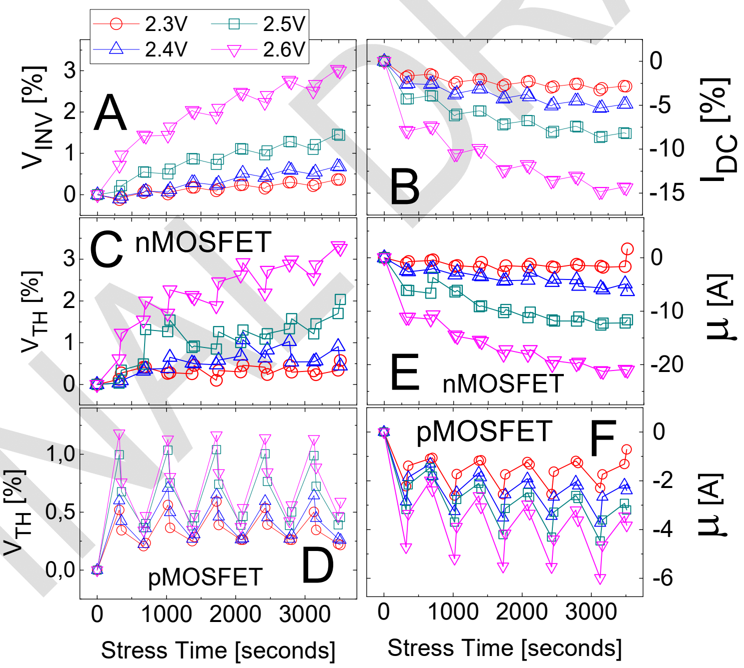


Figure 4. Relative variations measured during a S0V1 sequence of the inversion voltage (A), peak current at the inversion point (B) of the CMOS inverter, threshold voltage (C and D) and carrier mobility (E and F) of the nMOS (C and E) and pMOS (D and F) for different stress voltage conditions: 2.3V (Red Circles), 2.4V (blue triangles), 2.5V (green triangles), and 2.6V (pink triangles) during the application of S0V1 sequences.

These results indicate that the combined effects of the different aging mechanisms activated along the application of the S0V1 stress sequence under different stress voltages are qualitatively similar but with larger variations for larger applied stress voltages. This fact suggests that, for the analysed stress voltage range, the particular effects of each aging mechanism (BTI, HCI or OFF-State degradation) are accelerated by the same factor.

C. *Power law fitting: extrapolation to operation conditions*

In this section, a fitting of the degradation of the circuit parameters, V_{INV} and I_{DC}, using a power law that accounts for the stress time and voltage dependences is carried out, to analyse and predict the lifetime of the CMOS inverter at operating conditions. Figure 5 shows the relative variations (symbols) of V_{INV} (Figure 5 Left) and I_{DC} (Right) as a function of time, for the different stress voltages, when the stress sequence S0V1 is applied to different samples. Lines in figure 5 are the result of the power law fittings (see equations in figure 5), being A, B and C (for V_{INV}) and A´, B´ and C´ (for I_{DC}) are the fitting parameters of the equations. For this particular technology (65nm bulk), the values of the power-law exponents for both, device and circuit parameters, are indicated in Table 1. As shown in table 1, the exponents of V_{TH} shifts of the nMOSFET are close to those of the V_{INV} shift, while those for the mobility reduction are close to those observed for I_{DC}, suggesting that the circuit performance degradation is mainly dominated by the nMOSFET aging.

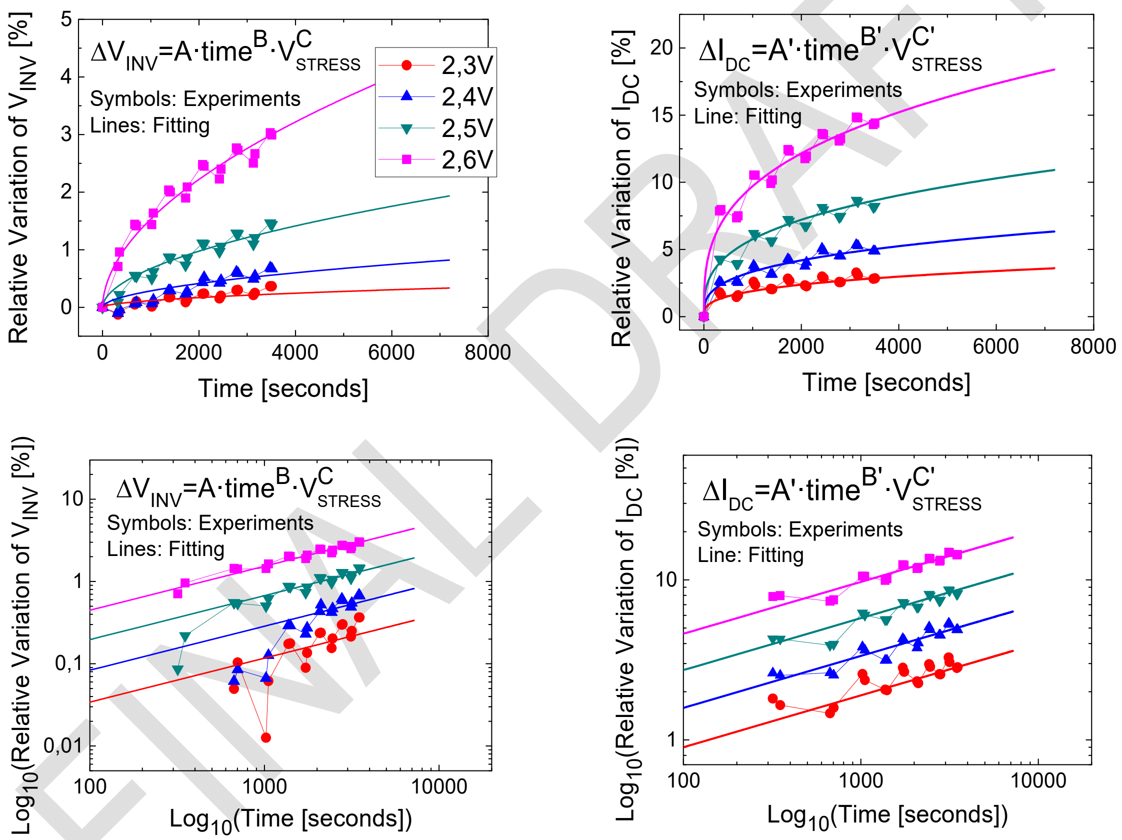


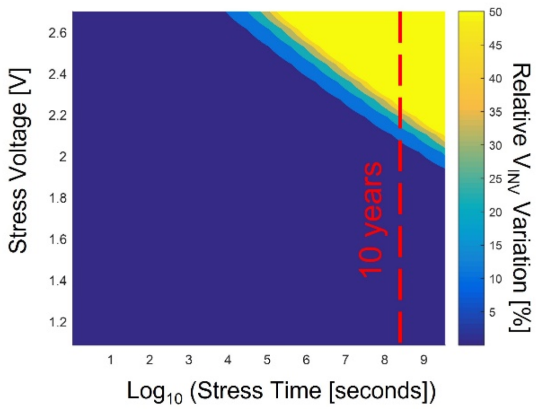
Figure 5: Top figures. Relative variation of V_{INV} (Left) and I_{DC} (Right) when applying the stress sequence S0V1 with stress voltages 2.3V (red circles), 2.4V (blue triangles), 2.5V (green triangles) and 2.6V (pink squares). Thick lines are the fittings to the power law equations indicated in the figures, that take into account the stress time and voltage conditions. Bottom figures show the same data in log-log plots

ΔV_{INV}	$A = 0.7517 \cdot 10^{-10}$	B = 0.5347	C = 20.978
ΔI_{DC}	$A' = 3.112 \cdot 10^{-6}$	B' = 0.3239	C' = 13.3076
VthN	A = 5.6407·10-9	B = 0.4372	C = 17.3377
VthP	A = 0.0019	B = 4.0994·10-5	C = 6.2294
MovN	A = 9.3881·10-8	B = 0.3469	C = 17.2072

MovP	A = 0.0026	B = 0.1132	C = 6.764

Table 1: Parameters values of the equations used to fit the V_{INV} and I_{DC} shifts

Taking into account the observed voltage and time dependences of the circuit parameters shifts, the expected shifts at operation conditions have been estimated. To do so, from equations in figure 5, with the obtained parameter set (table 1), the variation of V_{INV} and I_{DC} has been evaluated as a function of the stress voltage and the stress time and represented in Figure 6. Only circuit parameter shifts up to 50% are considered and shown in figure 6. From these maps, considering the voltage dependence, it is possible to extrapolate the V_{INV} and I_{DC} degradation to the circuit operating conditions (i.e., 1.2V), while the time dependence allows analyzing the circuit lifetime. As observed in figure 6, both circuit parameters are shifted by less than 5% after 10 years when the circuit is operated at voltages lower than 1.6V. This small degradation of the circuit performance is expected for this commercial technology and is consistent with the low degradations of both transistors (see figures 4C, 4D, 4E and 4F) in this particular circuit due to the circuit topology itself.



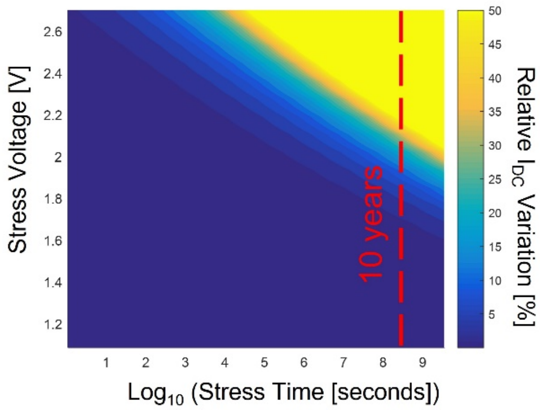


Figure 6: Colored map of the V_{INV} (Left) and I_{DC} (Right) relative degradation as a function of the stress voltage and stress time, evaluated using the equations indicated in figure 5 and parameters in table 1. The red dashed line corresponds to the expected 10 years lifetime.

IV. CONCLUSIONS

CMOS inverters have been subjected to electrical stress, to evaluate their degradation during a complete cycle of operation. Correlations between devices and circuit degradations have been analysed. To unravel the impact of the degradation of both nMOSFET and pMOSFET transistors on the CMOS inverter performance, several stress-measurement sequences have been defined that, on the one hand, emulate the voltages applied during a complete '0-1' input cycle and, on the other, consider particular stress cases (at device level) along the sequence. Measurements confirm that the shift of the inversion voltage in the CMOS inverter transfer curve is mainly determined by the V_{TH} shifts of the transistors, whereas the peak current is mostly related to the degradation of μ.

The device degradation is strongly dependent on the 'stress history', which depends on its actual operation in the circuit. Degradation can become permanent or compensated, depending on the order that aging mechanisms are activated during the circuit operation. The relative variations of the device parameters under the combined effects of the BTI, HCI and OFF-state depend on the stress voltage and, consequently, circuit level parameters (i.e., V_{INV} and I_{DC}) as well. So that, lifetime prediction procedures must take into account these aging mechanisms interdependencies. For this particular commercial technology, the extrapolation of the circuit degradation to lower voltages suggests a relative variation of the circuit performance smaller than 5%, after 10 years of operation for voltages lower than 1.6V.

The results highlight the importance of the OFF-state induced degradation on the device/circuit performance. Therefore, on the one hand, models for this mechanism will have to be included in aging prediction CAD tools and, on the other, it may have to be accounted for when designing idle or off-state configurations in digital and analog circuits (i.e. high inputs may be less detrimental than low ones).

Acknowledgments

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