Summary

Anti-islanding, islanding detection algorithm for inverters connected to the utility grid. Any inverter connected to the grid must be able to detect disconnection quickly and reliably under any circumstance.

Most inverters designed to feed energy at the utility grid are current controlled voltage source converters (CC-VSC), only able to work if the grid or a voltage controlled voltage source converter (VC-VSC) is connected. CC-VSCs are unable to generate controlled voltages as an island by themselves.

This project aims to study and design an anti-islanding algorithm for voltage controlled voltage source converters (VC-VSC), able to work connected to the grid and as an island.

During the first chapter the main parts of the simulated plant model are explained focusing on converters working principles and the pulse width modulation method. Also some simplifications regarding simulation limitations are introduced, such as implementing an averaged model over a commutated one.

In the second chapter the control loops for both CC-VSC and VC-VSC are explained, this aims to give the lector an idea about cascaded control loops design and control of alternating variables with resonant controllers. This chapter also covers the main differences in design and nature of both kinds of converters.

The third chapter analyses the most important anti islanding algorithms for both CC-VSC and VC VSC. It also explains the resonant load situation and the need to develop active methods to cover this particular situation. It focuses on impedance measurement and harmonic injection the main method studied during this project.

Fourth and final chapter studies and analyses the harmonic injection method based on impedance measurement. First, it aims to give the lector a general idea of the working principles to later on conduct a study to determine its optimal values and extract some conclusions.

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Glossary

Symbols

C	capacity
f	frequency
G	transfer function
I	current
k	constant or proportional gain
L	inductance
P	active power
Q	reactive power
q	quality factor
R	resistance
S	apparent power
U	controllable voltage
V	non-controllable voltage
X	reactance
Y	admittance
Z	impedance
ω	angular frequency
θ	phase or angle

Subscripts

0	relative to fundamental frequency in case of ω
C	relative to a capacitor
RL	relative to a resonant lad
ctr	relative to a controller
DG	relative to distributed generation
h	relative to an harmonic
island	relative to an islanding situation
L	relative to an inductance
n	relative to the natural frequency
PCC	relative to the Point of Common Coupling
PI	relative to a proportional integral controller
PR	relative to a proportional resonant controller
PV	relative to active power - voltage
Qω	relative to reactive power - frequency
r	relative to resonance
ref	relative to reference
RMS	Root Mean Square
S	relative to converter output Source
s	relative to settling time
SFS	relative to Sandia Frequency Shift
SVS	relative to Sandia Voltage Shift
G	relative to the grid

Acronyms

AC	Alternating Current
AFD	Active Frequency Drift
CC-VSC	Current Controlled –Voltage Source Converter
CC-VSI	Current Controlled – Voltage Source Inverter
CITCEA	Centre d'Innovació Tecnològica en Convertidors Èstatics i Accionaments
DC	Direct Current
DFT	Discrete Fourier Transformation
HI	Harmonic Injection
PCC	Point of Common Coupling
PI	Proportional Integral
PJD	Phase Jump Detection
PR	Proportional Resonant
SFS	Sandia Frequency Shift
SMS	Slip-Mode frequency Shift
SVS	Sandia Voltage Shift
THD	Total Harmonic Distortion
UPC	Universitat Politència de Catalunya
VC-VSC	Voltage Controlled – Voltage Source Converter
VC-VSI	Voltage Controlled – Voltage Source Inverter

Preface

Origin of the project

Nowadays, for the most part, energy generation is still carried by big energy suppliers based on big centralized sources such as nuclear plants, wind farms, gas plants and hydroelectric power plants. However, with the constantly increasing demand of energy and the quick evolution of renewable energies we are on the road for a more diversified energy generation model.

This model will strongly rely on micro grids, small grids formed by sources and/or loads connected to the utility grid. In order to achieve such distributed generation we will need to work with a multitude of micro grids synchronized with the utility grid. For this purpose we will need a convenient control of the inverter that connects them both.

In this context appears the islanding phenomenon, a critical condition attributed to micro grids. Islanding occurs when a distributed generator (such as solar powered system) continues to power a micro grid after the utility grid has been disconnected. This causes the local micro grid to resemble an island where power can flow disconnected from the rest of the utility grid, thus the name.

In an islanding situation the point of common coupling (PCC) between the micro grid and the utility grid will still be powered and can be dangerous to users and utility workers who don't expect a live wire. Also it can prevent synchronization of devices to the grid, which may turn damaging in case of sudden reconnection.

In order to avoid these situations, anti-islanding methods must be applied to detect the disconnection and act accordingly. Moreover from a legal point of view, anti-islanding detection is strictly mandatory.

Voltage Controlled Voltage Source Inverters (VC-VSI) offer the duality to work as an island and connected to the grid. However, due to the control nature and less popularity, islanding algorithms are far less developed. For that reason, the project main goal is to develop an anti islanding algorithm based on impedance measurement for VC-VSI adjusting the variables accordingly.

Motivation

During the degree I'm about to end I've been learning about multitude of disciplines related to engineering. I've studied from mechanics to electronics all based on the same learning process, study the theory first to later establish the concepts through solved problems.

However I've hardly ever faced an interdisciplinary problem without a clear path to resolution. That's why with this project I plan to get a more global vision of engineering, working on my soft skills learned as a student using my criteria and rigor to apply all I've learnt thus far.

To achieve this I will have to define the boundaries of each problem I face identifying the disciplines it involves. I will then learn with the help of my instructor what I need to know in order to solve it.

CITCEA-UPC, a technology transfer centre specialized in converters and power electronics, offered me this opportunity to help complete a part of a finished project by demonstrating some of its conclusions [1]. Hopefully this project will come as a challenge to prove myself professionally and decide which disciplines I would and I wouldn't continue studying or working. Particularly I would like learn about power electronics, control dynamics and simulations.

Introduction

Project objectives

The main objective of this project is to demonstrate and corroborate some of the conclusions already drawn on a finished project of CITCEA-UPC [1].

To achieve this, we will simulate active anti-islanding algorithms based on impedance measurement by harmonic injection on voltage controlled inverters working as a voltage source. Particularly the study will be conducted on a 90 kVA, three-leg four-wire split capacitor Inverter with a 50 Hz resonant load of 90 kW with a quality factor q = 2.

For that matter we will perform a theoretical study to determine which variables affect the detection and how we can tune the ones we can control to do it faster. Later we will corroborate these suppositions by performing simulations of the model on Matlab Simulink.

Project extent

As a relatively open project the complexity of the study we are conducting is only limited by our time and knowledge. For that matter we need to define solid boundaries and acknowledge its limitations.

The project is divided in the following tasks.

- Build a representative Simulink-Matlab model of the three-leg split capacitor inverter
- Study and implement the three cascade control loops of the VC VSC. Current, voltage and apparent power.
- Study the already existing anti-islanding algorithms.
- Implement the harmonic injection algorithm.
- Make a theoretical study and perform simulations.
- Draw conclusions and tune the algorithm accordingly

PROJECT REPORT

1. MODEL BUILDING

In order to implement the anti-islanding algorithm it's imperative to first understand the working model. For that reason, the main parts of the model will be explained sequentially in a logical manner.

1.1. Inverter internal electronics

An inverter is a device that transforms DC current into AC current. As a black box (Figure 1.1), it has 2 inputs from the DC voltage source, 4 outputs for the three AC phases, the ground and the Duty Cycle control signal.

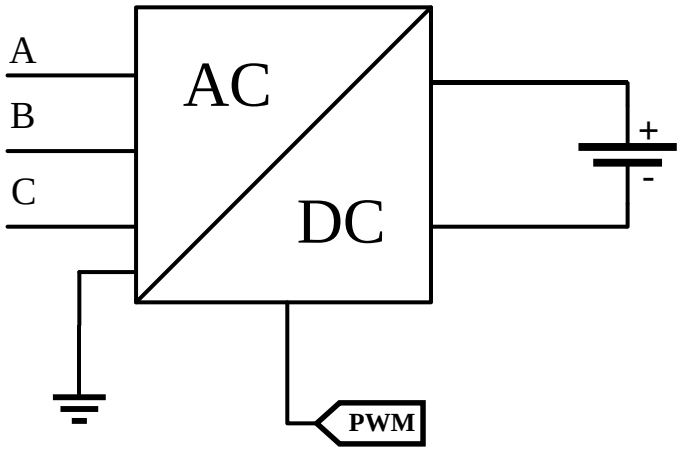

***Figure 1.1**: Black box of the inverter*

Internally, the DC side features the voltage source wires connected to a pair of capacitors with a ground in between. This ground works as a 4th wire connection allowing to generate three phase unbalanced systems with a homopolar or zero sequence component.

The AC side features a pair of IGBT transistors per phase coordinated by a PWM signal at their gates (Figure 1.2).

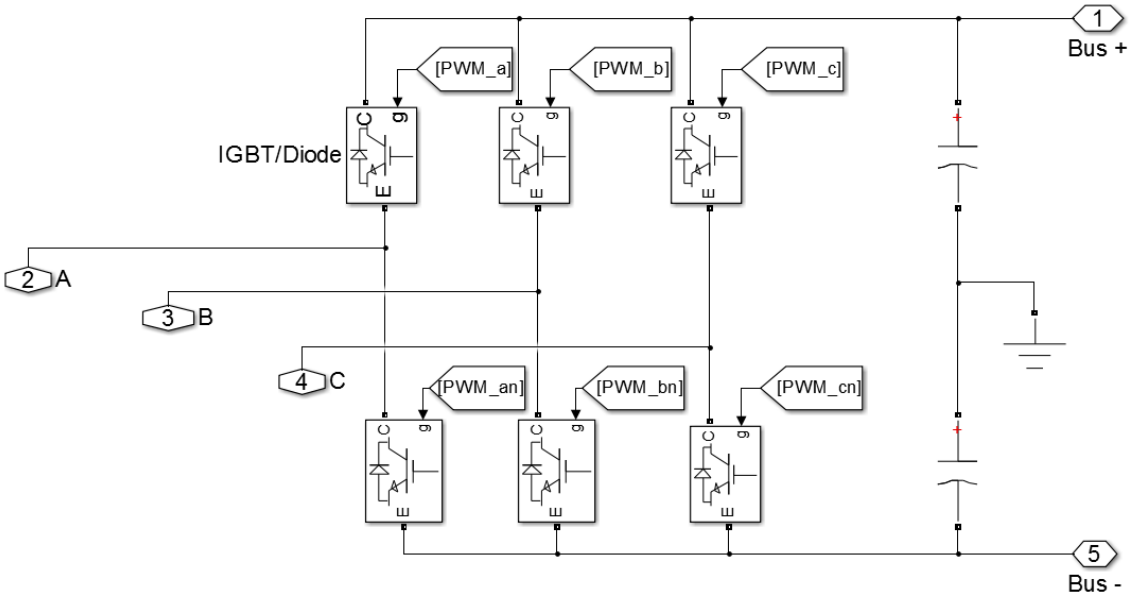

***Figure 1.2**: Inverter internal electronics*

1.2. Commutated model

To fully understand the control loops of the converter we will first study the commutated transistor based model.

Initially, the desired voltage output will be synthesized. As the DC voltage source is only able to energize at a high and low voltage, to get any voltage in between, a Pulse Width Modulation method will be used.

In this case, the desired signal is a sinus of 325 peak voltage and 50 Hz frequency. However, in order to create the PWM, the signal has to be pre-processed.

As can be seen in Figure 1.3 the desired signal is divided by the DC Voltage, then it's scaled by 0.5 and added 0.5 units to move it to the positive domain. The saturation block works as a safety precaution ensuring we are not able to demand more voltage than the DC voltage source can provide.

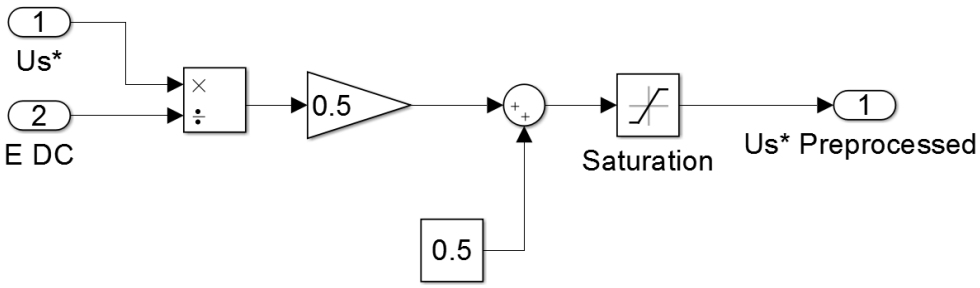

***Figure 1.3**: Desired signal pre-processor*

To implement the PWM a simple greater than logic between our desired pre-processed function and a high frequency triangular function will be used (Figure 1.4). The output voltage duty cycle PWM is synthesized for each of the AC branches.

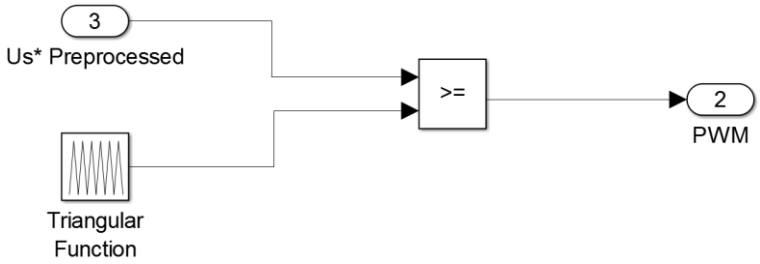

***Figure 1.4**: PWM logic*

For illustrative purposes, a 1 kHz triangular function is used to create the PWM in the (Figure 1.5).

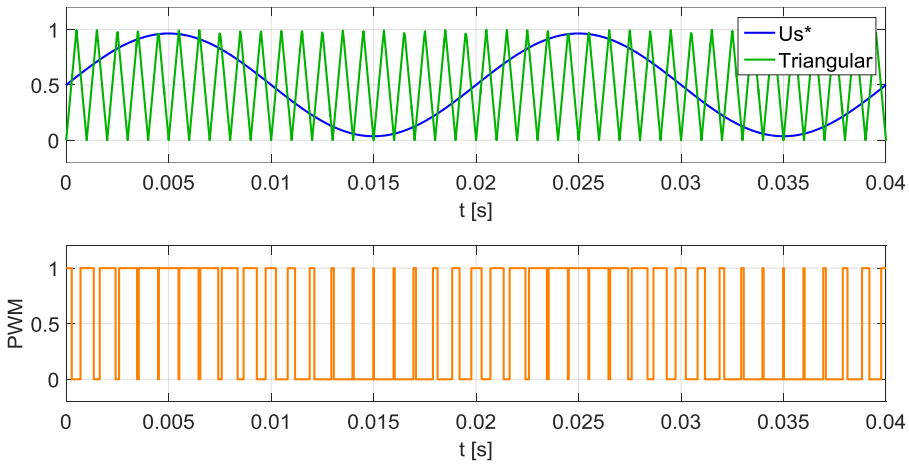

***Figure 1.5**: PWM from desired and triangular function*

The PWM implemented works at 8 kHz frequency. It will activate one of the IGBT gates while deactivating the other, obtaining a highly similar squared signal at the transistors output voltage. The current can be obtained from equation (1.1).

$$I_L = \frac{1}{L}\int U_L(t)dt \qquad (1.1)$$

The commutation time is so short that the current behaviour can be approximated by a straight line, thus the triangular shape (Figure 1.6). Current ripple is proportional to the voltage and L.

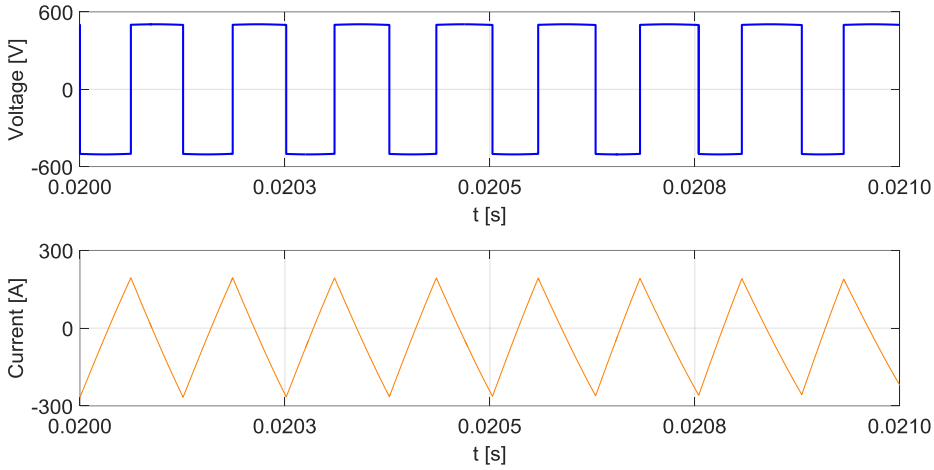

***Figure 1.6**: PWM ripple*

1.3. Averaged model

The PWM triangular function operates at a very high frequency to reproduce the sine wave correctly. From a simulation point of view, the quickly change of state of the transistors leads to a major computational load that makes anti islanding simulations too long.

As far as this project goes, we are not interested in studying the dynamics of the high frequency commutating transistors. For that reason an ideal averaging converter will be used. The averaged model can be created by simply including three AC voltage sources that consume the power generated from the DC voltage source.

Acknowledging this model won't feature transistors, the duty cycle used will be directly the desired output voltage pre-processed.

This way by simply including the inverse block inside the converter we will regenerate the output voltage desired and command the controlled AC voltage source (Figure 1.7).

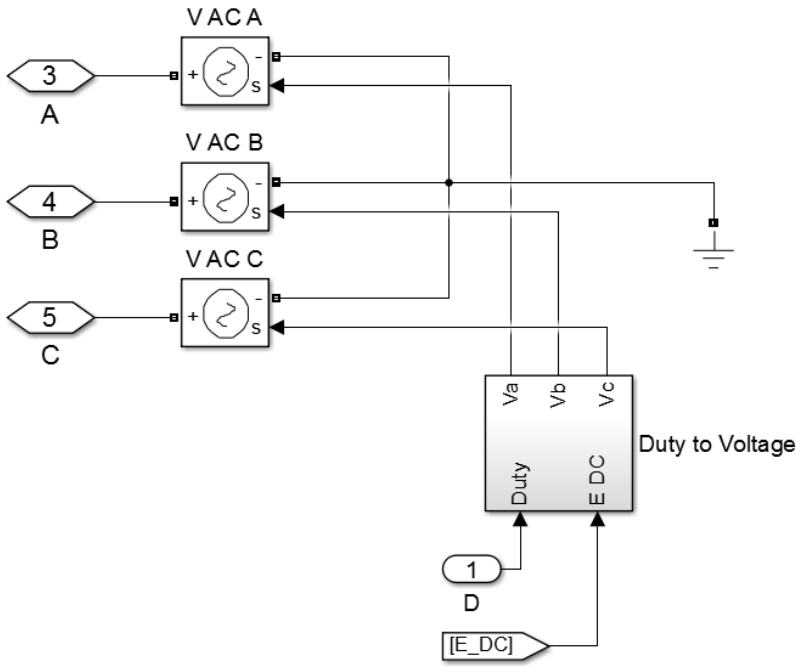

***Figure 1.7**: Averaged model duty to voltage*

As an ideal converter all the energy given equals the generated. This principle can be implemented by calculating the power consumed in the AC branches and then dividing it by the DC Voltage to obtain the DC current (Figure 1.8).

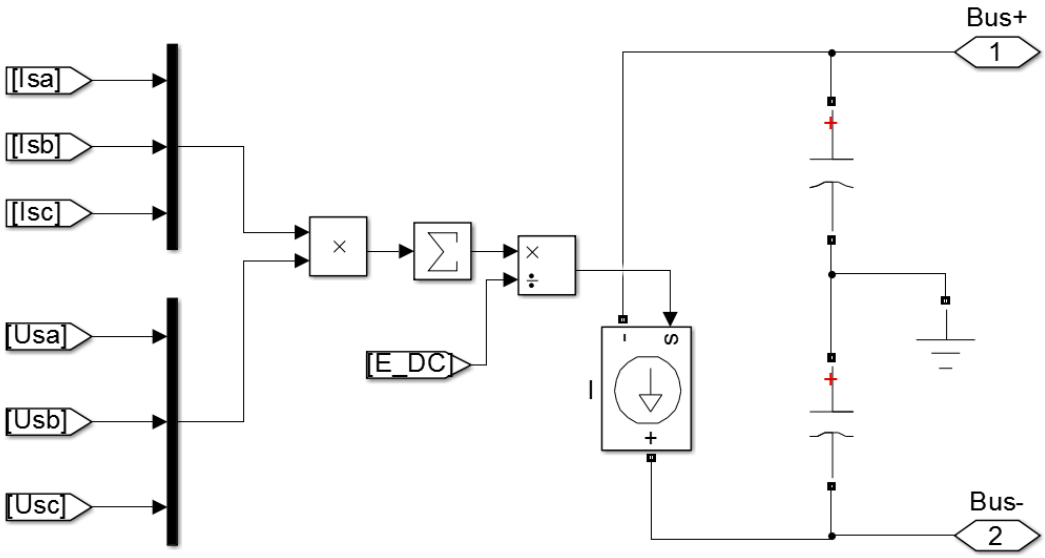

***Figure 1.8**: Averaged model DC current*

With this simple energy algorithm the computing load is greatly reduced and we can perform simulations of the model within a reasonable time. Voltage and current ripple and transistor based issues no longer exist.

1.4. Voltage and current filtering

The averaged model synthesizes the desired voltage by using an AC source directly.

However, in a real life scenario, output signals of the inverter present a squared nature due to due to the PWM duty (Figures 1.2.3 and 1.2.4). For that reason, the output signal of the PWM must be filtered to obtain the function desired.

The filter implemented at the inverter output is a LC impedance (250e-6 Henry 350e-6 Faraday).

The L inductance filters the ripple of the current by integrating the voltage output of the inverter (Equation 1.1). The use of this inductance allows the first control loop.

The C capacitor filters the ripple of the voltage by integrating the current filtered by the L inductance (Equation 1.2). The use of this capacitor allows the second control loop.

$$V_C = \frac{1}{C}\int I_C(t)dt \qquad (1.2)$$

1.5. Simulink model

To test the control and the anti-islanding algorithm a functioning model is created. The general scheme can be seen in Figure 1.9.

The DC side of the model it's implemented with a DC source connected to the inverter.

The AC side features the characteristic impedances, a set of inductors and capacitors working as filters, the load and the grid.

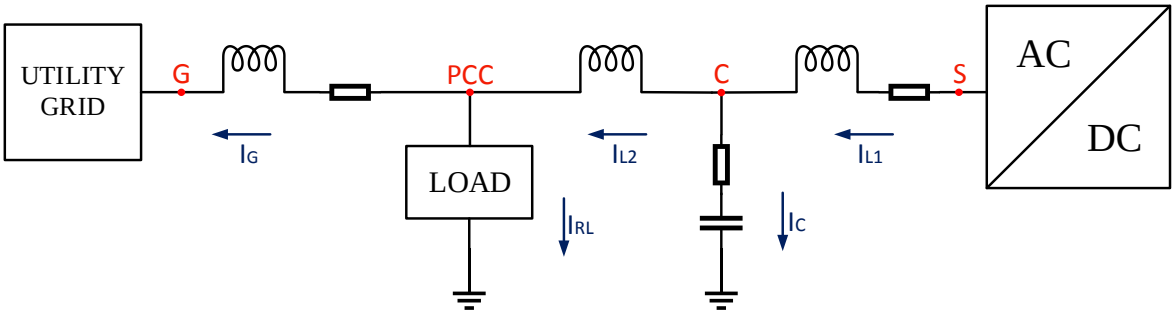

***Figure 1.9**: General scheme*

As can be seen in Figure 1.10 the load is composed of three parallel branches of RLC (More information at Chapter 3.4).

$R = 1.763\,\Omega \;\; L = 0.0028\,H \;\; C = 0.0036\,F$

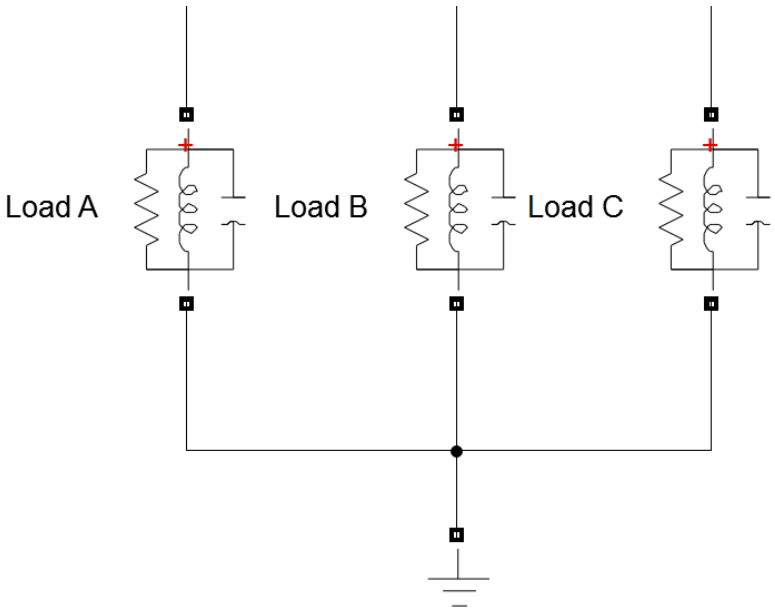

***Figure 1.10**: RLC Load*

The utility grid is implemented by 3 AC controlled voltage sources in series with a RL. Ideal switches allow simulating a grid disconnection (Figure 1.11).

$R = 0.005\,\Omega \;\; L = 0.00003\,H$

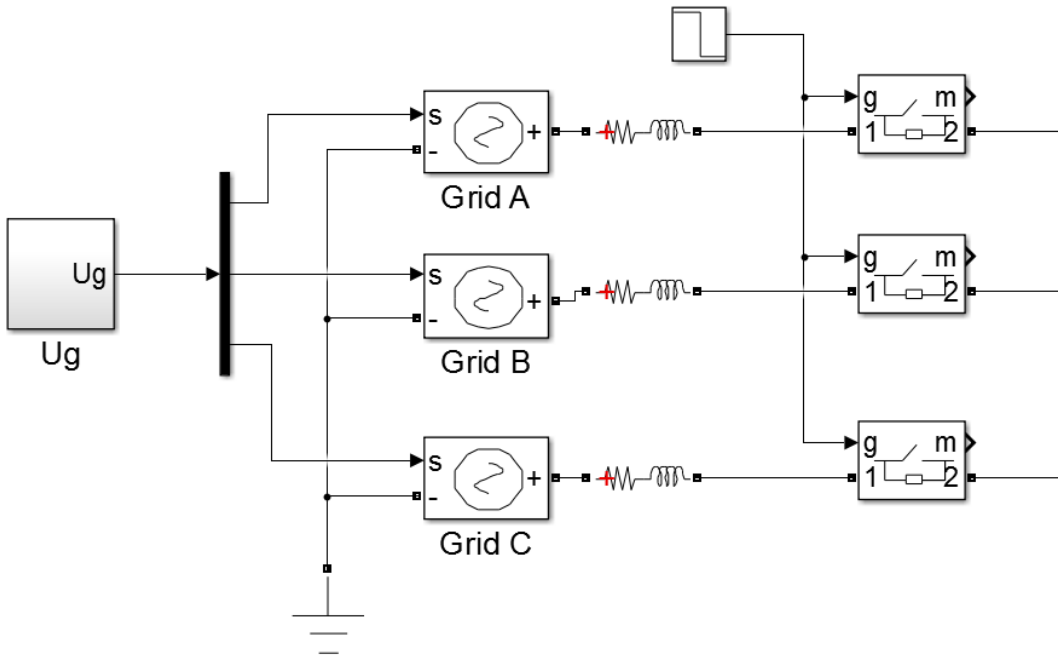

***Figure 1.11**: Utility grid*

2. CONTROL LOOPS

During this chapter the control loops for both CC-VSC and VC-VSC are explained, this aims to give the lector an idea about cascaded control loops design and control of alternating variables with resonant controllers. This chapter also covers the main differences in design and nature of both kinds of converters.

2.1. Resonant controller

PI controllers present an infinite gain at $\omega = 0$. However at higher frequencies gain diminishes resulting in an increasing steady state error. This becomes a problem when following a 50 Hz sinusoidal reference.

$$G_{PI}(s) = K_P + \frac{K_I}{s} \qquad (2.1)$$

Figure 2.1 shows the bode diagram of an integral controller. Conclusions drawn are valid for PI controllers as well.

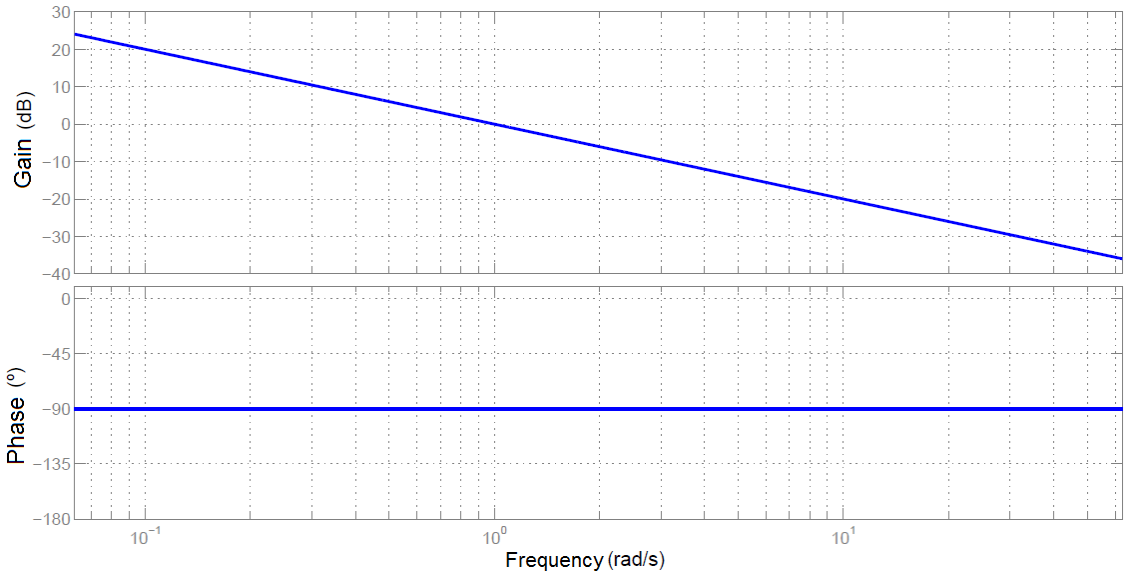

***Figure 2.1**: Bode plot of an integrator [3]*

Resonant controllers solve these shortcomings by a filter type design that only grants a theoretical infinite gain at a particular frequency (Figure 2.2).

$$G_{PR}(s) = K_P + K_I \cdot \frac{s}{s^2+\omega_0^2} \qquad (2.2)$$

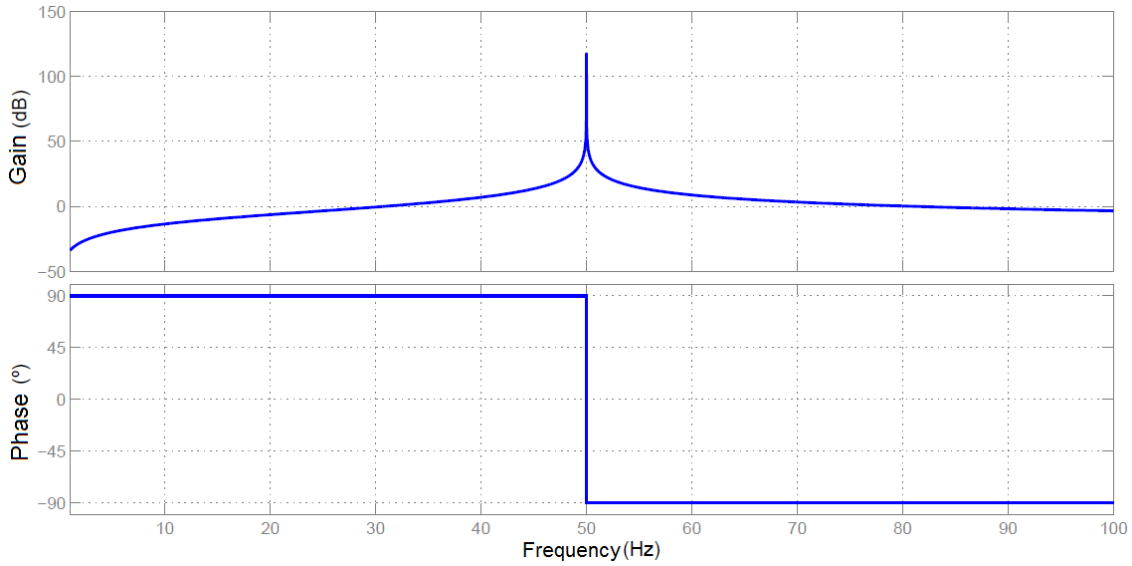

***Figure 2.2**: Bode plot resonant controller [3]*

Also multiple controllers can be set in cascade to control multiple frequencies simultaneously (Figure 2.3).

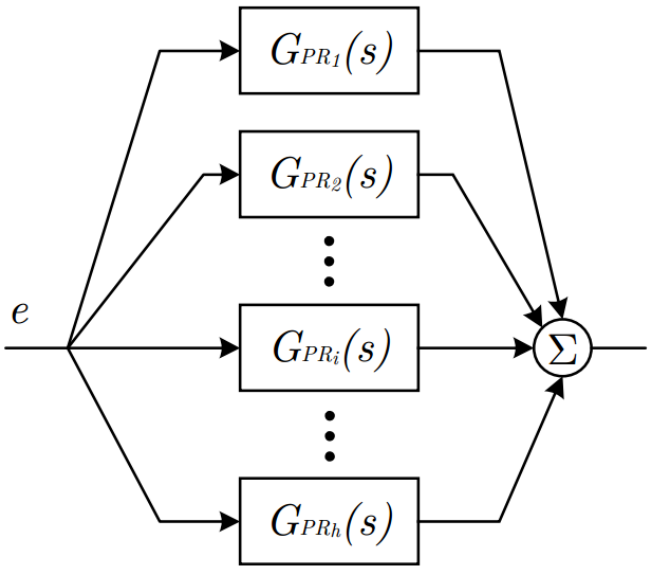

***Figure 2.3**: Cascaded resonant controllers to control multiple frequencies [3]*

Figure 2.4 shows the implementation of the resonant controller in simulink.

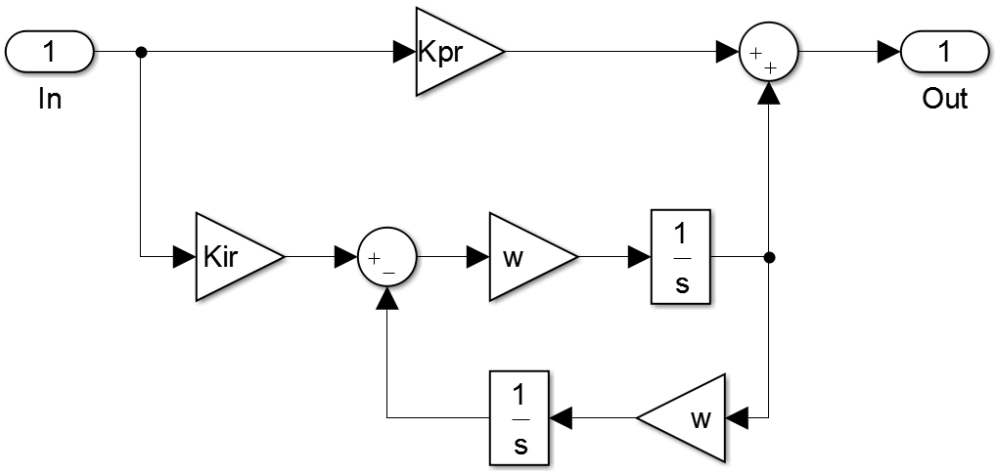

***Figure 2.4**: Resonant controller implemented in simulink*

2.2. CC VSC control

Current Controlled Voltage Source Converters (CC-VSC) are the most widely used converters in AC drive systems. Current controlled converters provide a high dynamic response with a relatively easy control (Figure 2.5).

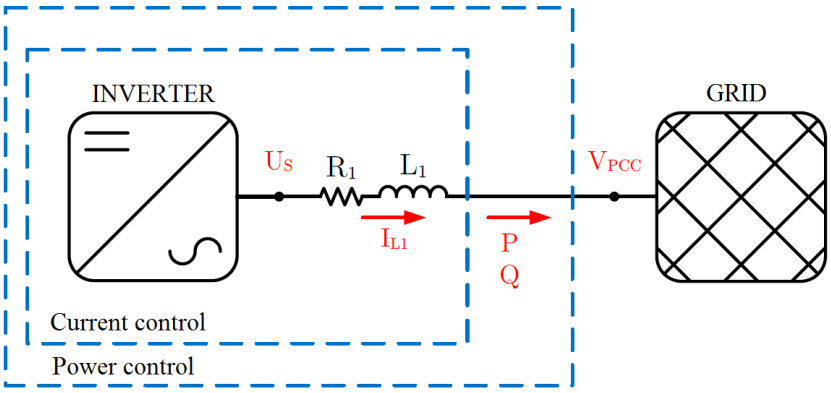

***Figure 2.5**: CC VSC [1]*

As the name suggests, power control is achieved by controlling the output current of the converter (More information about current control on Chapter 2.3.1). As we can see in Figure 2.6, current and output voltage are directly related to the RL resistance at the phase output. A resonant controller will be used for the inverse non-causal relation.

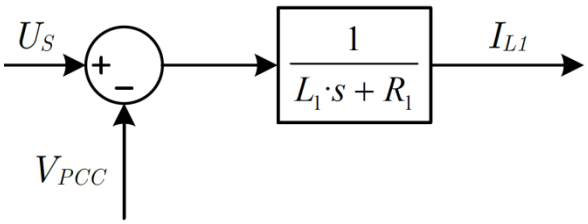

***Figure 2.6**: Output current from voltage transfer function [1]*

The functioning base of the converter is the constant V_{PCC} voltage fixed by the grid. With this reference, active and reactive power control becomes proportional to the output current of the converter (Both phase and module).

Setting V_{PCC} as the reference.

$$V_{PCC} = |V_{PCC}|\lfloor 0° \quad (2.3)$$

$$I_S = |I_S|\lfloor \theta° \quad (2.4)$$

Active and reactive power can be computed as:

$$P = |I_S| \cdot |V_{PCC}| \cdot cos\,\theta° \quad (2.5)$$

$$Q = |I_S| \cdot |V_{PCC}| \cdot sin\,\theta° \quad (2.6)$$

However, current controlled converters are not able to control the V_{PCC} voltage and thus not able to work as an island when the grid disconnects (unless it's connected to a Voltage Controlled Voltage Source Converter). In an islanding situation, the previously fixed V_{PCC} becomes unstable and the power given is no longer proportional to current which leads to uncontrolled voltages and currents that may damage the micro grid.

As we will see later, this instability of V_{PCC} is the working base of some active methods for CC VSC inverters (Active methods for CC VSC at chapter 3.5.1).

2.3. VC VSC control

Voltage Controlled Voltage Source Converters (VC-VSC) present a more complex control and implementation than its CC counterpart. For that reason, VC VSC haven't been as far developed and don't have a strong presence in the market.

However, the capability to work as an island opens up a multitude of possibilities. VC VSC converters may find use as a security measure, an uninterruptible power source or to manage isolated grids for rural settlements.

As we can see in Figure 2.7 power control is achieved by controlling the voltage of the point of common coupling. The control loop will be implemented sequentially starting from the voltage output of the converter up to the power given.

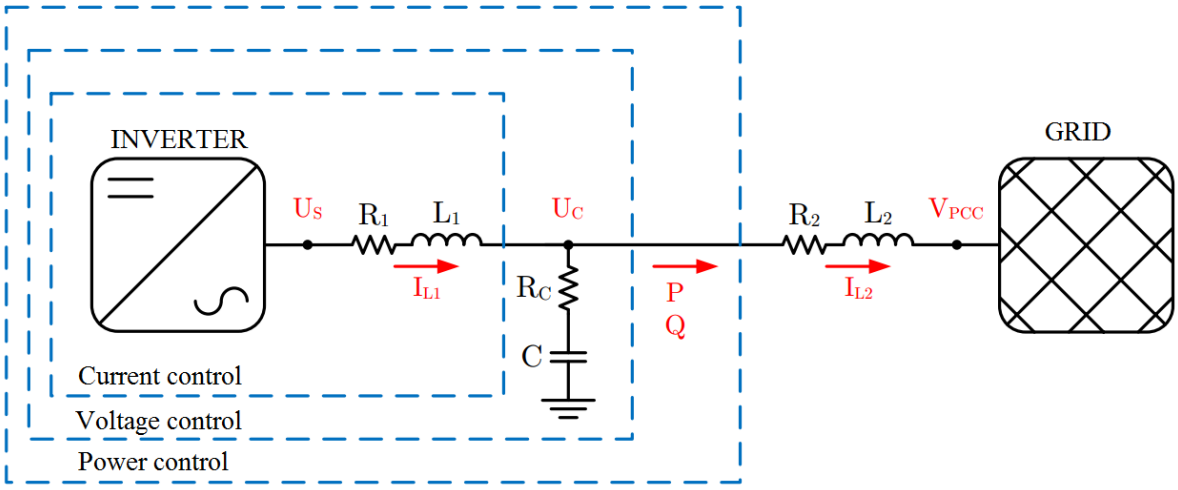

***Figure 2.7**: VC VSC [1]*

In order to understand the entire power loop control of the converter we first need to understand each internal loop individually. For that reason, the control of the converter will be built and explained sequentially.

2.3.1. Current control

First electrical variable controlled by the VC-VSC is the output current of the converter. To design the control loop the desired output voltage U_{SG}^{*} must be created from the desired output current I_{L1}^{*}.

To understand the control process is recommended to first understand the physical transformation of U_S to I_{L1} (Figure 2.8). The control loop reverses this transformation by including a PR controller instead of a non-causal relation to achieve control through error.

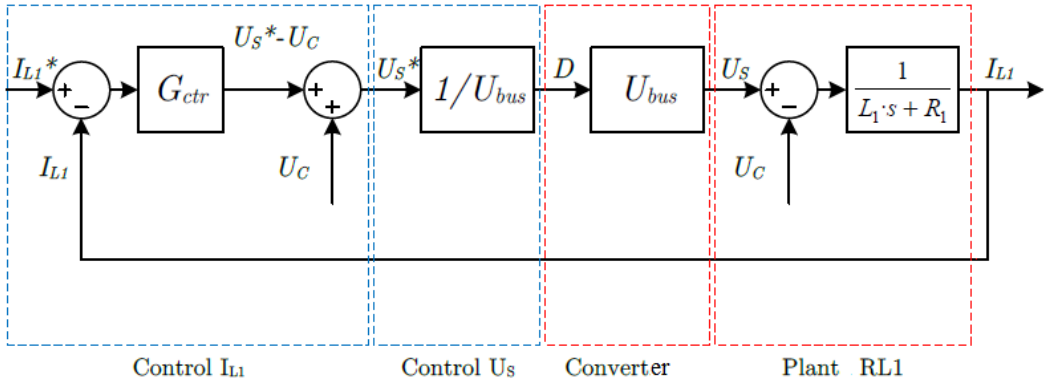

***Figure 2.8**: Block diagram for output current control [1]*

Figure 2.9 aims to illustrate the electrical variables involved in this control loop.

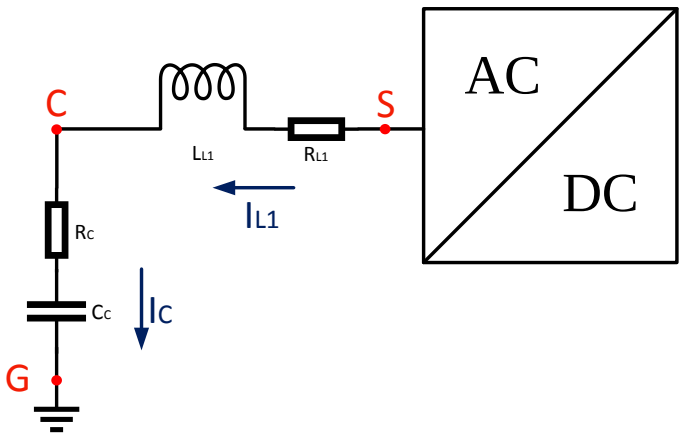

***Figure 2.9**: Output current scheme*

As we can see in the previous image, the voltage drop between the capacitors and the output of the inverter can be seen as the output voltage minus the capacitors voltage.

$$U_{SC} = U_{SG} - U_{CG} = (R_{L1} + sL_{L1}) \cdot I_{L1} \qquad (2.7)$$

Considering that as for now U_{CG} is an uncontrolled but measurable variable U_{SC}^* can be expressed as

$$U_{SC}^* = U_{SG}^* - U_{CG} = R_{L1} \cdot I_{L1} + L_{L1} \frac{dI_{L1}}{dt} \qquad (2.8)$$

As we know, inductance sets a non-causal linear relation for a current dependent voltage. For that reason, a resonant PR controller is implemented ($K_P = 1.4 \quad K_I = 1.352$) so the desired U_{SC}^* can be seen as a linear combination of the output current error $I_{S\,Error}$ and the controller transfer function.

$$U_{SC}^* = I_{L1\,Error} \cdot G_{CTR} \qquad (2.9)$$

$$I_{L1\,Error} \cdot G_{CTR} = U_{SG}^* - U_{CG} \qquad (2.10)$$

As it's demonstrated in the previous equation, the desired output voltage U_{SG}^* can be generated from the output current error $I_{L1\,Error}$. Running a simulation with a desired output current of 2 amperes per phase we obtain Figure 2.10.

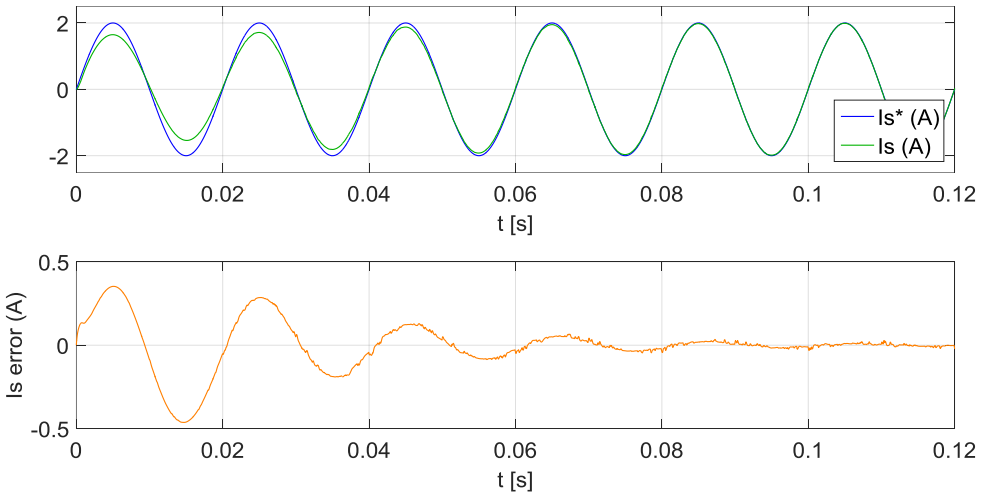

***Figure 2.10**: Output current simulations*

To generate the output voltage quicker from the current control loop a positive feed forward of the capacitors voltage is implemented.

$$I_{L1\,Error} \cdot G_{CTR} = U_{SG}^* - U_{CG} + U_{CG} = U_{SG}^* \qquad (2.11)$$

This cancels the U_C perturbation improving the whole loop speed (Figure 2.11).

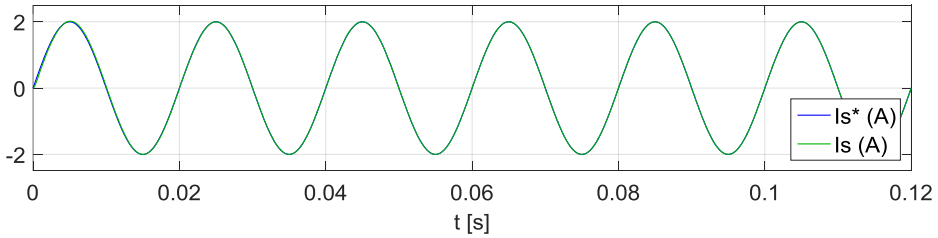

***Figure 2.11**: Output current simulations with feed forward*

The current output loop implemented in simulink in Figure 2.12:

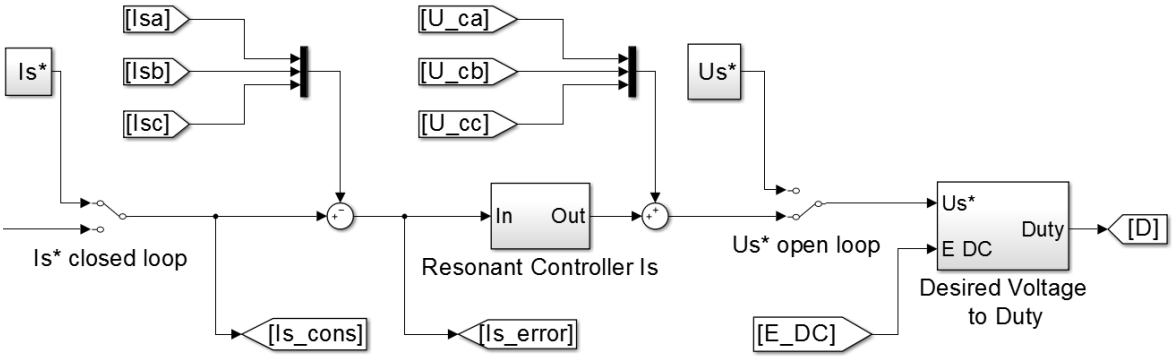

***Figure 2.12**: Output current control loop Simulink*

2.3.2. Capacitors voltage control

Second electrical variable controlled by the VC-VSC is the capacitors voltage. To design the control loop the desired output current I_{L1}^* must be created from the desired capacitors voltage U_C^*.

To understand the control process is recommended to first understand the physical transformation of I_{L1} to U_C (Figure 2.13). The control loop reverses this transformation by including a PR controller instead a non-causal relation to achieve control through error.

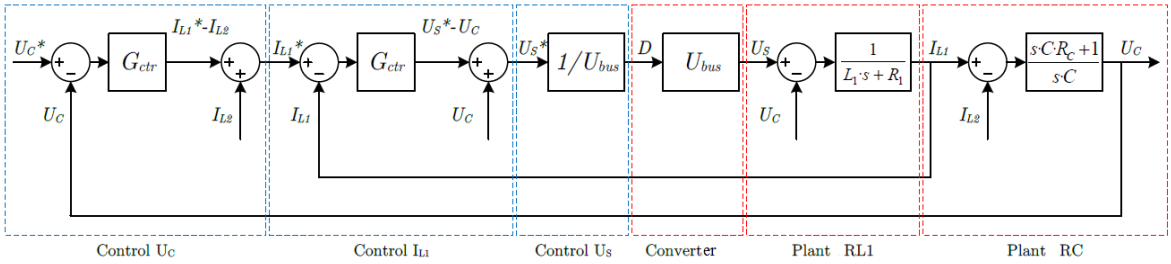

***Figure 2.13**: Block diagram for capacitors voltage control [1]*

Figure 2.14 aims to illustrate the electrical variables involved in this control loop.

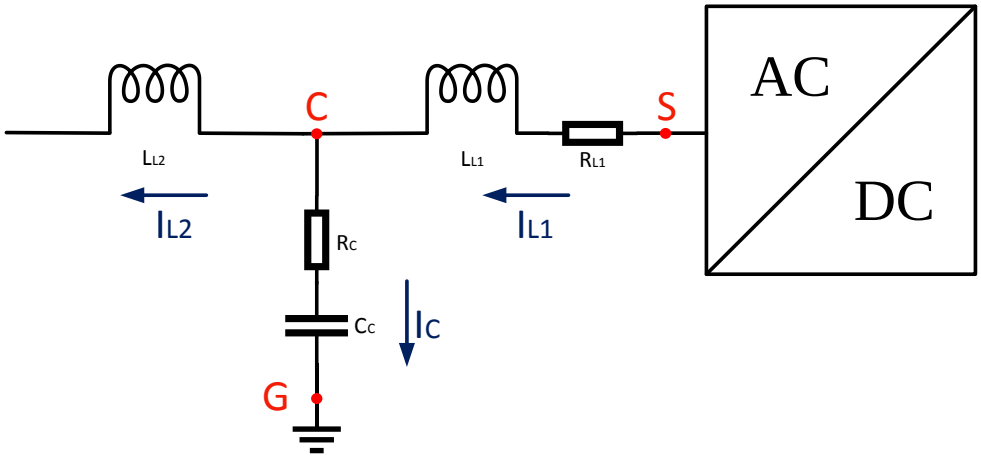

***Figure 2.14**: Capacitors voltage scheme*

As we can see in the previous figure, the capacitors current can be seen as the load and grid current minus the output converter current.

$$I_C = I_{L1} - I_{L2} = \frac{sC_c}{sC_cR_C+1} \cdot U_{CG} \qquad (2.12)$$

Considering that as for now I_{L2} is an uncontrolled but measurable variable I_C^* can be expressed as

$$I_C^* = I_{L1}^* - I_{L2} \qquad (2.13)$$

As we know, capacitors set a non-causal relation for a voltage dependent current. For that reason, a resonant PI controller is implemented ($K_P = 0.2664 \quad K_I = 0.276$) so the desired I_C^* can be seen as a linear combination of the capacitors voltage error $U_{C\,Error}$ and the controller transfer function.

$$I_C^* = U_{C\,Error} \cdot G_{CTR} \qquad (2.14)$$

$$U_{C\,Error} \cdot G_{CTR} = I_{L1}^* - I_{L2} \qquad (2.15)$$

As it's demonstrated in the previous equation, output current I_{L1}^{*}can be generated from the capacitors voltage error $U_{C\ Error}$. To generate the output current quicker from the capacitors voltage control loop, a positive feed forward of the load and grid current I_{L2} is implemented.

$$U_{C\ Error} \cdot G_{CTR} = I_{L1}^{*} - I_{L2} + I_{L2} = I_{L1}^{*} \qquad (2.16)$$

This cancels the I_{L2} perturbation improving the whole loop speed.

Running a simulation with a desired capacitors voltage of 230 V_{RMS} per phase (Figure 2.15).

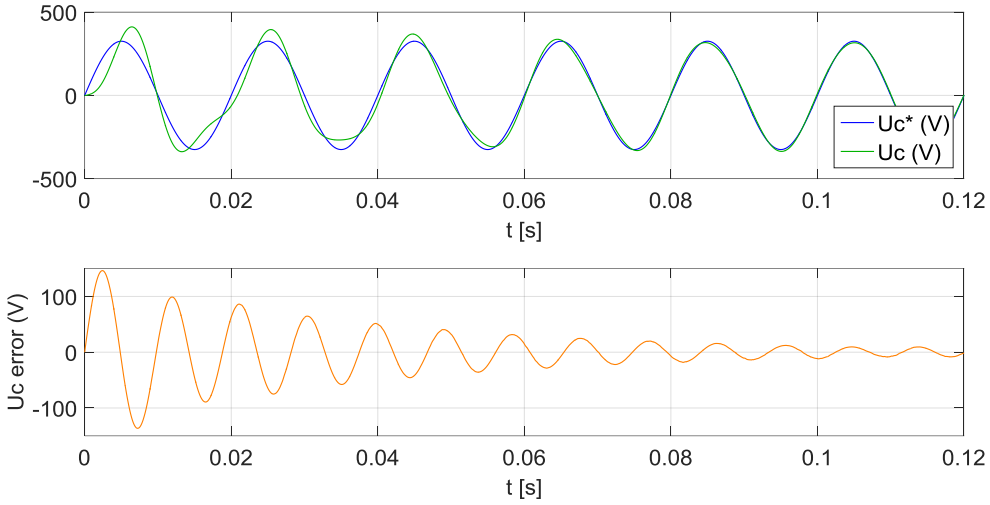

***Figure 2.15**: Capacitors voltage simulations*

The capacitors voltage loop implemented in simulink in Figure 2.16.

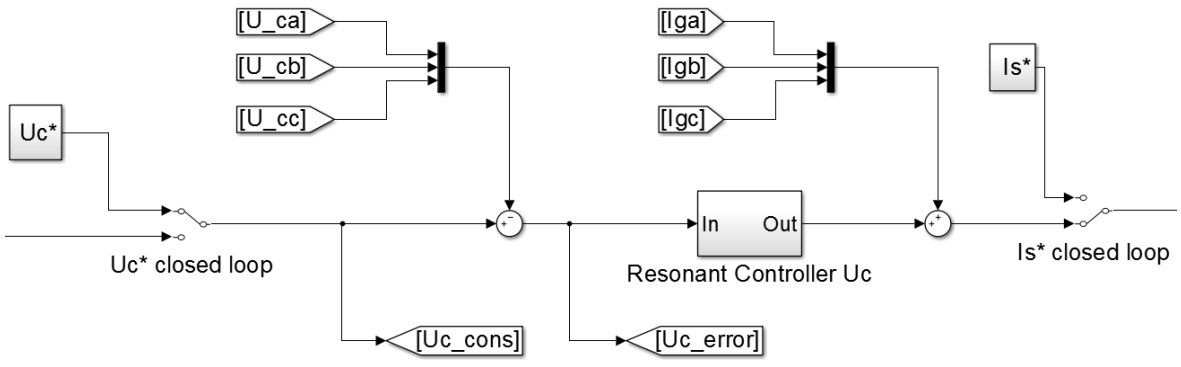

***Figure 2.16:** Capacitors voltage control loop simulink*

2.3.3. Apparent power control

Final electrical variable controlled by the VC-VSC is the output apparent power.

As can be seen in Figure 2.17 the apparent power can be calculated as the product of the voltage drop by the impedance in between.

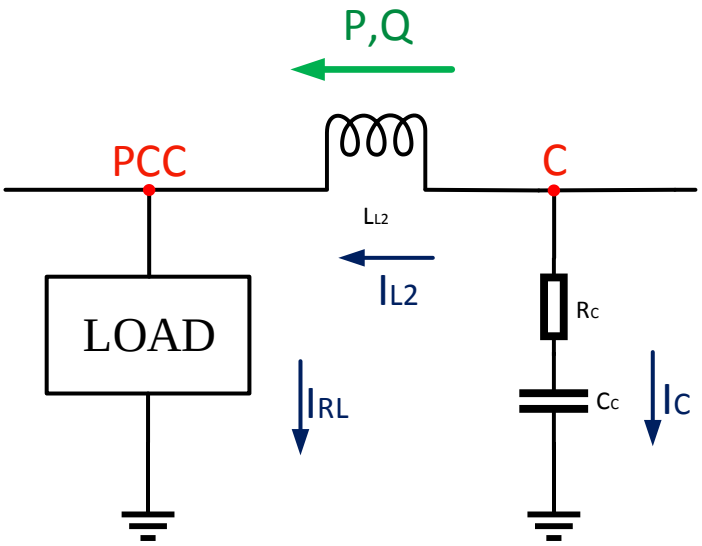

***Figure 2.17**: Output power scheme*

$$\vec{S} = \vec{V}_{PCC} \cdot \vec{I}_{L2} \qquad (2.17)$$

Apparent power can be divided into active and reactive power following the next equations [1].

$$P = \frac{(U_C \cdot V_{PCC} - V_{PCC}^2) \cdot R_2}{R_2^2 + \omega^2 L_2^2} + \frac{(U_C \cdot V_{PCC} \cdot \delta) \cdot \omega L_2}{R_2^2 + \omega^2 L_2^2} \qquad (2.18)$$

$$Q = \frac{(U_C \cdot V_{PCC} - V_{PCC}^2) \cdot \omega L_2}{R_2^2 + \omega^2 L_2^2} - \frac{(U_C \cdot V_{PCC} \cdot \delta) \cdot R_2}{R_2^2 + \omega^2 L_2^2} \qquad (2.19)$$

The impedance used in the model is mostly inductive, this simplifies and decouples the active and reactive power equations ($\omega L_2 \gg R_2 \rightarrow R_2 \approx 0$):

$$P \approx \frac{U_C^2 \cdot \omega L_2}{(R_2 + s \cdot L_2)^2 + (\omega L_2)^2} \cdot (\theta_{U_C} - \theta_{V_{PCC}}) \quad (2.20)$$

$$Q \approx \frac{U_C \cdot \omega L_2}{(R_2 + s \cdot L_2)^2 + (\omega L_2)^2} \cdot (U_C - V_{PCC}) \quad (2.21)$$

In order to control both active and reactive power two independent variables are needed. In this case, active power is attributed to the capacitors voltage and PCC phase and reactive power to the capacitors voltage and PCC module.

Active power is directly dependent on the difference between U_C and V_{PCC} phase δ, however its inverse is noncausal.

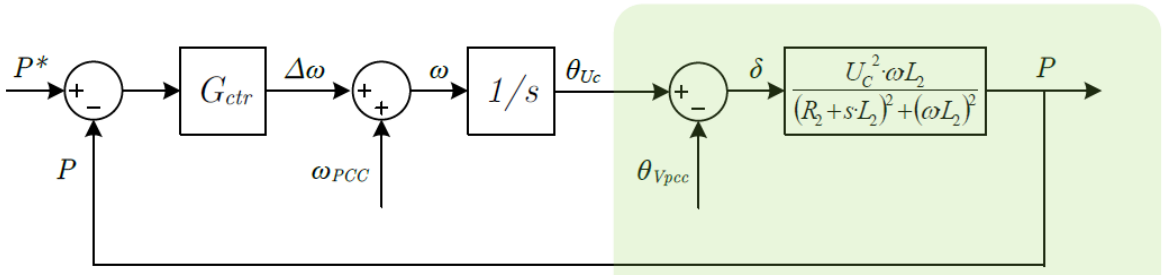

***Figure 2.18**: Block diagram active power [1]*

To understand the control process is recommended to read the figure backwards from the delta variable from the physical plant (Figure 2.18). The operations are inverted.

$$\left[\left(\delta + \theta_{V_{PCC}}\right) \cdot s\right] - \omega_{PCC} = \Delta\omega \quad (2.22)$$

The integrator is implemented to use angular speed as the control variable. Angular speed is a more robust and steady variable than phase, allowing an easier control. This way, with only a proportional controller, the control of the capacitors voltage phase is achieved ($K_P = 0.000003$).

As the working frequency is expected to be 50 Hz, the ω_{PCC} feed forward could be implemented with a constant value.

Figure 2.19 shows the control loop implemented in simulink.

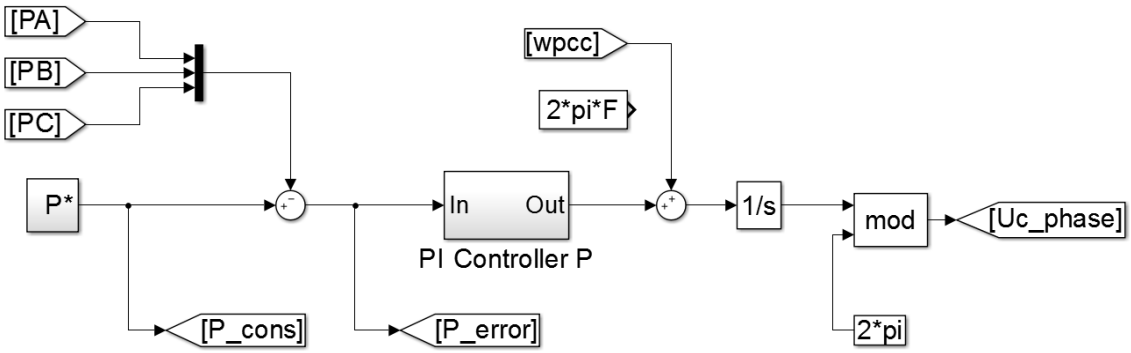

***Figure 2.19**: Active power control loop Simulink*

Reactive power is directly dependent on the difference between U_C and V_{PCC} module, however it's inverse is non-causal.

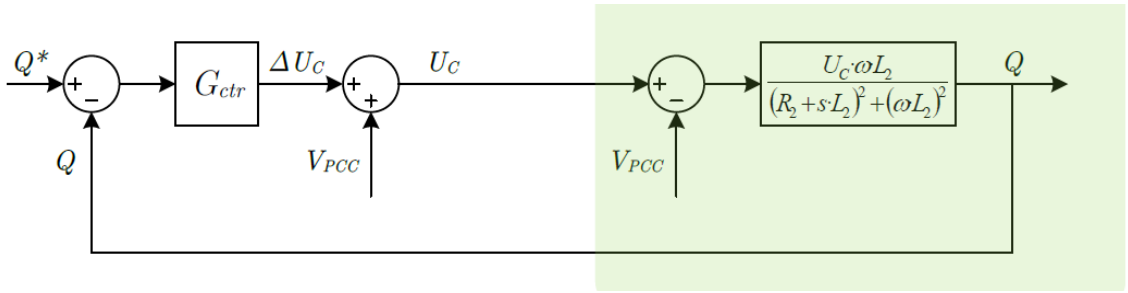

***Figure 2.20**: Block diagram reactive power [1]*

To understand the control process is recommended to read the figure backwards from the module difference variable from the physical plant (Figure 2.20). The control loop simply includes a feed forward of the V_{PCC} module.

This way, with a PI controller, the control of the capacitors voltage module can be achieved ($K_P = 0.000004\ K_I = 0.0009$).

Figure 2.19 shows the control loop implemented in simulink.

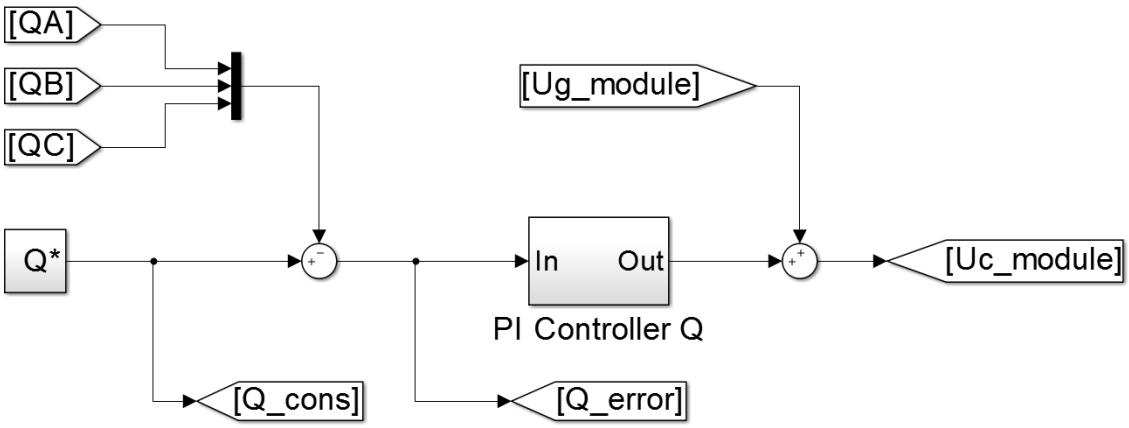

***Figure 2.21**: Reactive power control loop simulink*

With this approach the capacitors voltage can be synthesized from the apparent power desired (Figure 2.22).

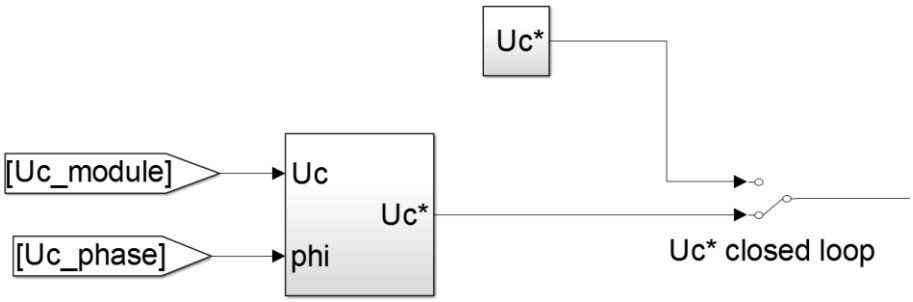

***Figure 2.22**: Capacitors voltage from apparent power*

3. ANTI ISLANDING ALGORITHMS

Anti-islanding algorithms can be divided in two main categories depending on if we send probe signals (active) or not (passive) at our system.

Most passive methods rely on voltage and frequency measurements to detect islanding.

Usually this works just fine but in the particular case where the load of the micro grid absorbs all the power generated, voltage and frequency remain the same after the disconnection.

This condition known as load resonance results in a Non Detection Zone for passive methods. In order to address this we will study active methods which are able to detect islanding based on other electrical variables.

3.1. Islanding

Islanding occurs when the utility grid disconnects and the micro grid keeps powering the point of common coupling.

As it was explained before, this is a dangerous and undesirable situation. For that reason, anti-islanding methods aim to detect disconnection quickly and reliably.

3.2. Point of Common Coupling behaviour

In a general situation, both, the utility grid and the inverter exchange power (Figure 3.1). A sudden disconnection from the utility grid creates a power unbalance that results in a transitory state. Mathematically the steady-state equations that govern the model change, leading to a shift of the electrical variables.

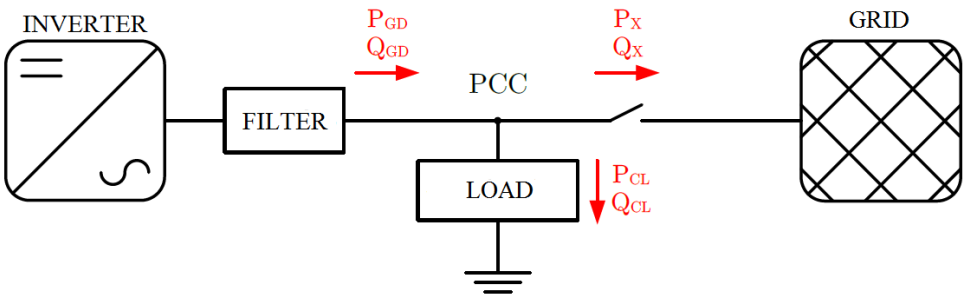

***Figure 3.1**: Power scheme connected grid [1]*

Assuming the power flux from the utility grid is not null, the voltage and frequency of the point of common coupling vary in a disconnection. This is the principle on which passive methods are designed.

3.3. Passive methods

Passive methods rely on the voltage and frequency of the PCC and only work if the utility grid exchanges power with the utility grid.

3.3.1. Voltage and Frequency detection

When the utility grid disconnects, the voltage and frequency of the PCC shift from the expected nominal values. The method can be implemented by simply defining the threshold values on which we may assume disconnection. However, as it's evidenced in Figure 3.2, this creates a non-detection zone were islanding remains undetectable.

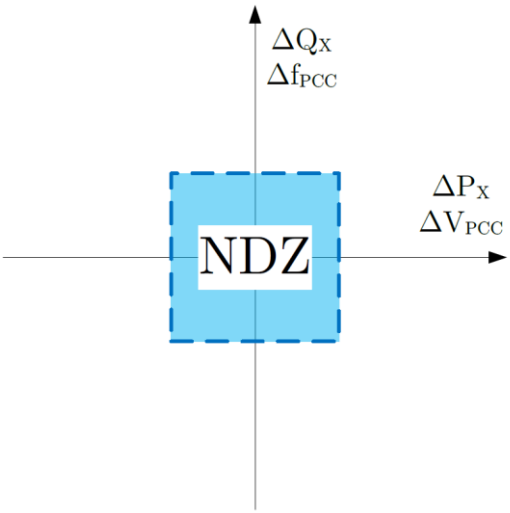

***Figure 3.2**: Non Detection Zone window [1]*

3.3.2. Phase Jump Detection

This method relies on a phase jump of the voltage of the PCC to detect islanding.

As long as the grid is connected it will impose its nominal values over the micro grid. However, when it disconnects, the phase of the PCC will be mostly determined by the load, resulting in a possible variation (Figure 3.3).

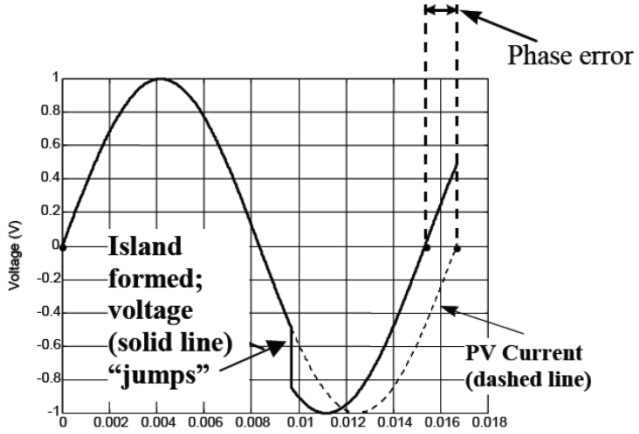

***Figure 3.3**: Effect on voltage wave from grid disconnection [4]*

This method won't be able to detect islanding if the phase of the load and the utility grid match, which is not a strange situation, because inverters usually aim to dump active power to the utility grid and most loads are designed to absorb active power as well.

For that reason the NDZ may be too big to consider this an effective method.

3.3.3. Harmonics detection

Inevitably, as a consequence of converting DC to AC the inverter generates current harmonics. The strong nature of the utility grid causes the impedance of the PCC to stay low. Due to the low impedance as a direct consequence of Ohm's law, voltage harmonics remain unnoticeable.

However when the grid disconnects the PCC impedance rises abruptly, causing voltage harmonics to be more noticeable.

This method doesn't present a NDZ but is highly susceptible to perturbations and it's not as effective in presence of a weak utility grid or high end inverters which minimize harmonics.

3.4. Resonant load

As it has been explained, passive methods offer a robust and relatively easy way to detect islanding. Nonetheless these methods only work when the utility grid is exchanging power with the load or the inverter.

In the particular situation where all the power given by the inverter is absorbed by the load (Figure 3.4), when the grid disconnects voltage and frequency of the PCC remain the same, making passive methods useless.

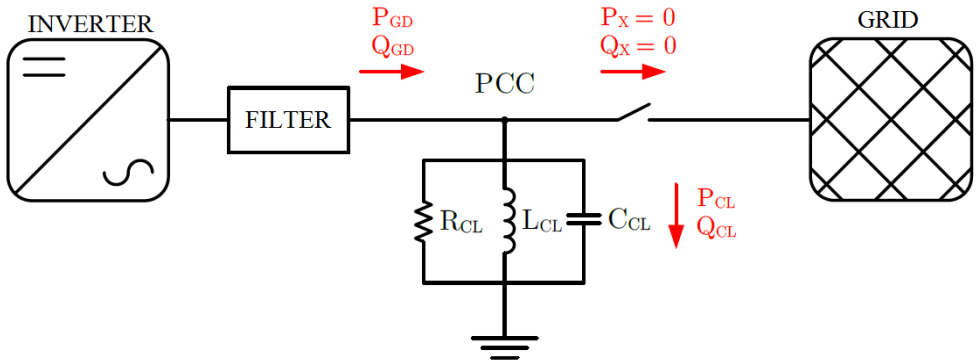

***Figure 3.4**: Power scheme disconnected grid [1]*

For a certain P and Q given by the inverter at a particular frequency, by adjusting the R, L and C components a resonant state can be achieved.

The utility grid has an effective voltage of 230 V and a fundamental frequency of 50 Hz. Connected to the grid, the load absorbs 30 kW of active power and 0 var of reactive power. The resonant load can be determined by imposing all the power absorbed by the load is given by the inverter at the same exact tension and frequency.

Active power condition [1]

$$P_{CL} = \Re e\left\{\frac{|V_{PCC}|^2}{\vec{Z}_{CL}^*}\right\} = \Re e\left\{|V_{PCC}|^2 \cdot \vec{Y}_{CL}^*\right\} = {V_{PCC}}^2 \cdot \frac{1}{R_{CL}} \qquad (3.1)$$

$$V_{PCC} = \sqrt{R_{CL} \cdot P_{CL}} \qquad (3.2)$$

Reactive power condition [1]

$$Q_{CL} = \Im \mathfrak{m}\left\{\frac{|V_{PCC}|^2}{\vec{Z}_{CL}^*}\right\} = \Im \mathfrak{m}\left\{|V_{PCC}|^2 \cdot \vec{Y}_{CL}^*\right\} \qquad (3.3)$$

$$Q_{CL} = {V_{PCC}}^2 \cdot \left(\frac{1}{\omega \cdot L_{CL}} - \omega \cdot C_{CL}\right) \qquad (3.4)$$

$$\omega = -\frac{Q_{CL}}{2 \cdot C_{CL} \cdot {V_{PCC}}^2} \pm \sqrt{\left(\frac{Q_{CL}}{2 \cdot C_{CL} \cdot {V_{PCC}}^2}\right)^2 + \frac{1}{L_{CL} \cdot C_{CL}}} \qquad (3.5)$$

Understanding that the load RLC features 3 free variables and only 2 are needed to achieve resonance, it's clear that another condition must be defined. The condition used during this project is the quality factor.

Quality factor states the relation between the reactive power of the inductance and the capacitor over the active power of the resistance.

$$q = -\frac{\sqrt{|Q_{CL}| \cdot |Q_C|}}{P} = R \cdot \sqrt{\frac{C}{L}} \qquad (3.6)$$

Imposing a quality factor of 2 the resonant load is perfectly defined.

3.5. Active methods

Active methods seek to solve the NDZ of passive methods in presence of a resonant load.

These methods are known as active because some kind of probe signal is used. Considering that active methods only make sense when passive methods do not work, it's assumed the load used is resonant.

3.5.1. Positive feedback methods

In order to understand the nature of these methods it's highly recommended to check out the control loop of the CC VSC.

As it was explained earlier, to work properly CC VSC needs the V_{PCC} reference set by the utility grid. In an islanding situation where such reference no longer exists the PCC voltage and frequency are left floating inside the NDZ.

These methods rely on positive depending variables to set an unstable feedback loop that drives voltage or frequency out of the NDZ.

3.5.1.1. Sandia Voltage Shift

Considering an island situation the active power consumed by the load can be expressed as the following:

$$P_{GD} = P_{CL} = \frac{{V_{PCC}}^2}{R_{CL}} \qquad (3.7)$$

The active power is directly proportional to the PCC Voltage, this property is the base on which the unstable loop is built. Setting a reference, an approximated linear model can be implemented as can be seen in Figure 3.5.

$$P_{SVS^*} = K_{SVS} \cdot (V_{PCC} - V_{ref}) \quad (3.8)$$

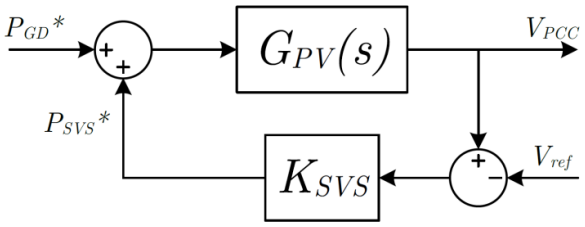

***Figure 3.5**: Conceptual block diagram SVS [1]*

If V_{PCC} increases so does the active power which tends to increase V_{PCC} as well. Same happens the opposite way if V_{PCC} decreases. This feedback instability moves Voltage out of the NDZ so a V_{PCC} passive method is able to detect the disconnection.

3.5.1.2. Sandia Frequency Shift

Considering an island situation the reactive power consumed by the load can be expressed as the following:

$$Q_{GD} = Q_{CL} = {V_{PCC}}^2 \cdot \left(\frac{1}{\omega \cdot L_{CL}} - \omega \cdot C_{CL}\right) \quad (3.9)$$

The reactive power is inversely proportional to the PCC frequency, this property is the base on which the unstable loop is built. Setting a reference, an approximated linear model can be implemented (Figure 3.6).

$$Q_{SFS^*} = -K_{SFS} \cdot (\omega - \omega_{ref}) \quad (3.10)$$

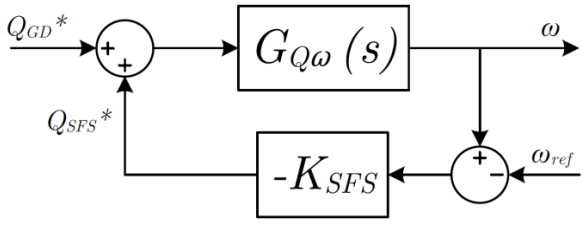

***Figure 3.6**: Conceptual block diagram SVS [1]*

If ω_{PCC} increases the reactive power decreases which tends to increase ω_{PCC}. Same happens the opposite way if ω_{PCC} decreases. This feedback instability moves PCC frequency out of the NDZ so a PCC frequency passive method is able to detect the disconnection.

3.5.1.3. Active Frequency Drift

This method uses the utility grid electric inertia to detect disconnection.

The output current is commanded at a higher frequency than the utility grid and at the pass by zero is set to wait up until the utility grid current passes by zero (Figure 3.7).

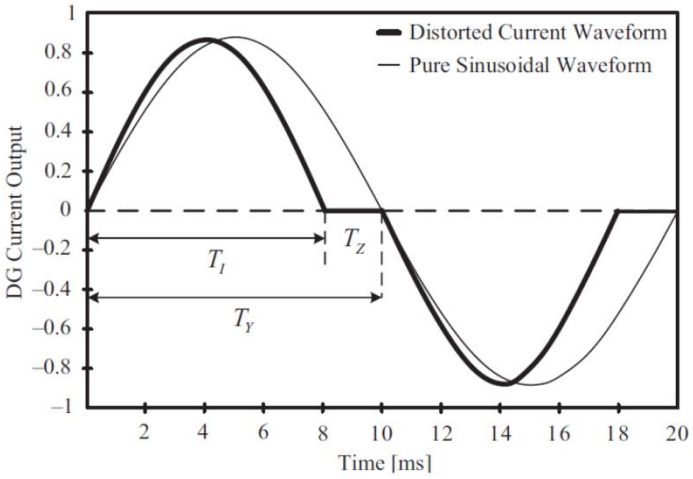

***Figure 3.7**: Deformed current from AFD [5]*

As long as it's connected, the utility grid forces it's frequency over the inverter, however in an islanding situation it increases up to the commanded frequency triggering the detection.

3.5.1.4. Slip-Mode Frequency Shift

SMS sets an unstable equilibrium point at the grid frequency and two stable points above and under. As long as the grid is connected it will impose its frequency. However, under disconnection, PCC frequency tends to one of the stable points triggering anti-islanding.

3.5.2. Impedance measuring of the PCC

Impedance measuring methods rely on the sudden variation of impedance of the PCC when the grid disconnects in order to detect islanding.

Understanding the model as a superposition of models at different frequencies, assuming that grid voltage only possesses a fundamental component at 50 Hz, for any frequency ≠ 50 Hz the model of Figure 3.8 is correct.

Outside nominal frequency, impedance of the PCC can be computed under Ohm's law as:

$$\vec{Z}_{PCC} = \frac{\vec{V}_{PCC}}{\vec{I}_{L2}} \qquad (3.11)$$

As it can be seen in Figure 3.8, the equivalent impedance of the PCC varies depending if the grid is connected or not.

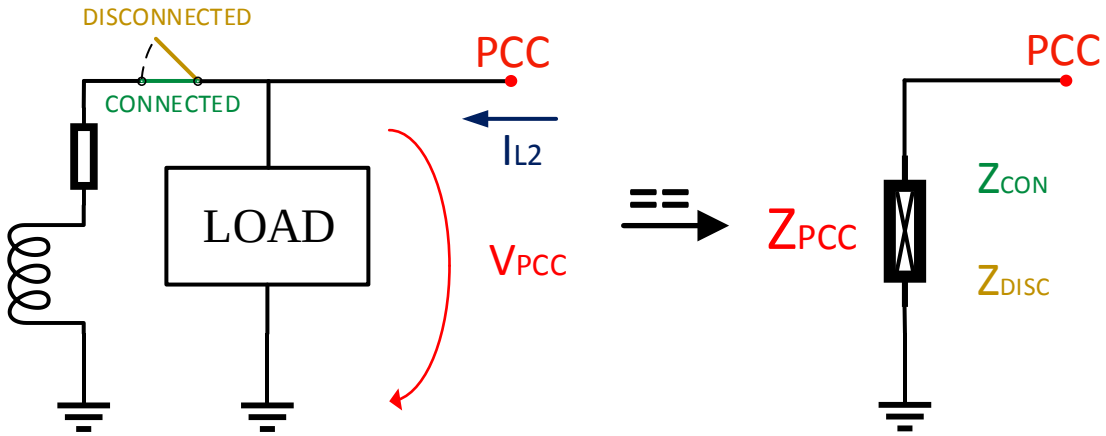

***Figure 3.8**: Equivalent impedance of the PCC*

Assuming the change is noticeable, which will be widely discussed later on, this method proves effective even with resonant loads.

3.5.3. Harmonic Injection

Harmonic injection is a method used to read the impedance of the PCC to later apply an impedance measurement algorithm for detection.

In order to read the equivalent impedance of the PCC at a frequency higher than nominal a voltage perturbation of the PCC at that frequency must be set (Figure 3.9). This way voltage and current would be noticeable by the sensors and the impedance could be computed at that frequency.

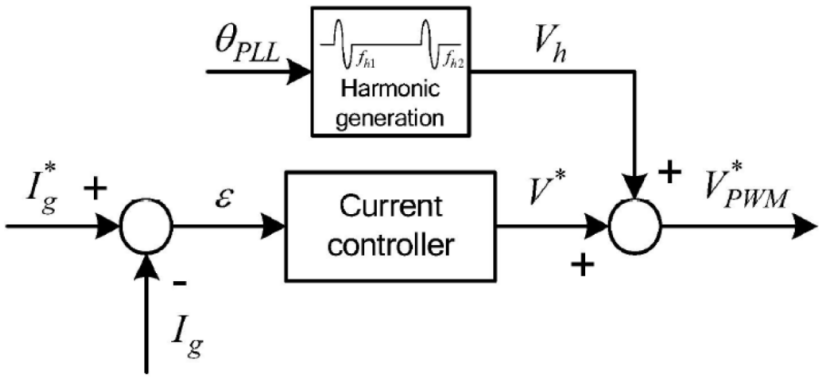

***Figure 3.9**: Block diagram of harmonic injection [6]*

To keep the total harmonic distortion as low as possible, only one period is injected at the pass by zero (Figure 3.10). It's important to keep in mind possible resonance when choosing the frequency.

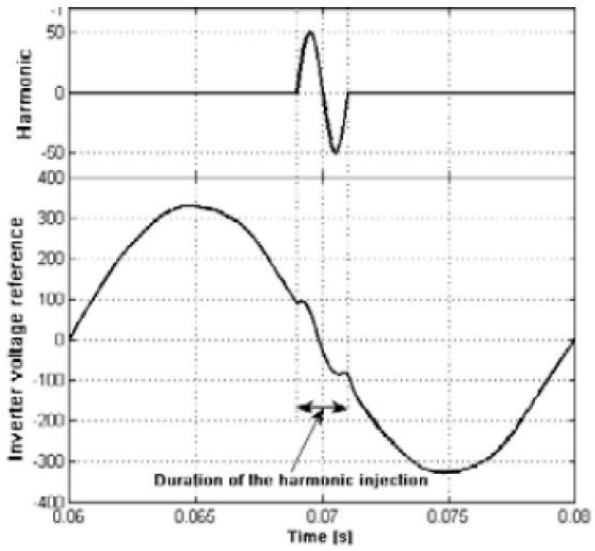

***Figure 3.10**: Harmonic injection at pass by zero [6]*

Finally, the discrete Fourier transformation is applied to the voltage and current of the PCC to read the equivalent impedance at that frequency (Figure 3.11).

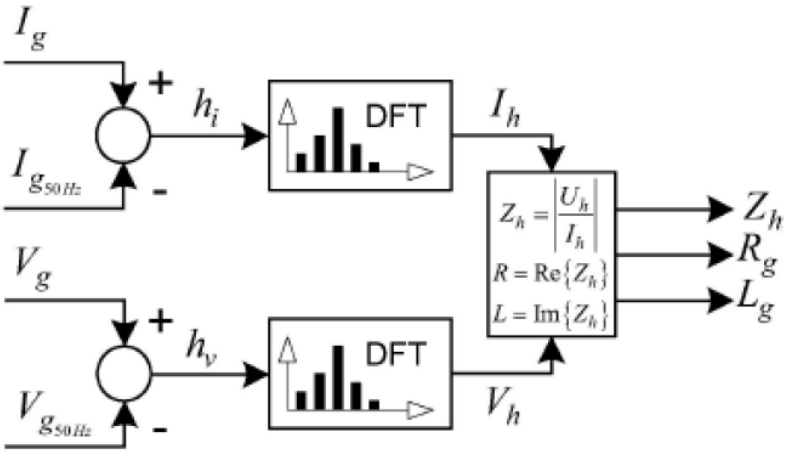

***Figure 3.11**: Impedance estimation algorithm [6]*

3.5.4. Other methods

Grid detection

This method would be implemented from the utility grid. By simply connecting a load at the PCC after disconnection passive methods would be able to detect the sudden change of frequency or voltage.

Grid inverter communication method

Grid disconnection can be detected by establishing a communications protocol between an emitter related to the grid status and a receiver connected to the inverter.

The communication could be achieved through the PCC as a carrier current or an external communication interface.

4. DETECTION AND SIMULATIONS

During this chapter the basics of the algorithm are explained without entering in too many details to get a global concept of its working principle.

Later on each of the algorithm variables will be analysed and a study will be conducted to determine its optimal values.

4.1. Harmonic injection

To reduce the total harmonic distortion only one period is injected during the pass by zero. This signal is generated by injecting the harmonic signal only when the phase of the fundamental frequency is between two values. These values are calculated using the fundamental and harmonic frequency and the Injection Starting Period (ISP) and Injection Ending Period (IEP) of the harmonic. The implementation in simulink can be seen at Figure 4.1.

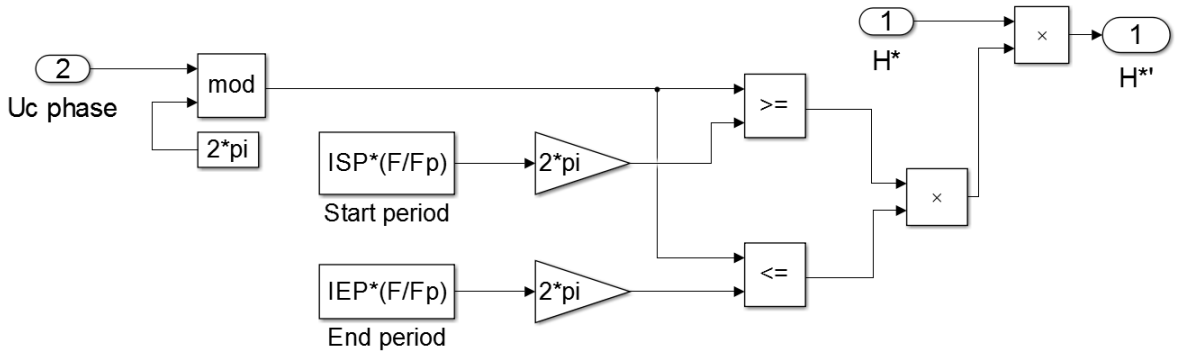

***Figure 4.1**: Harmonic injection periods selector algorithm*

For illustrative purposes the harmonic sinus has a voltage peak of 40 volts and a frequency of 450 Hz and it's injected within the capacitors voltage loop. An additional resonant controller should be set at harmonic frequency to avoid filtering and get the perturbation at the capacitors voltage. The implementation in simulink can be seen in Figure 4.1.

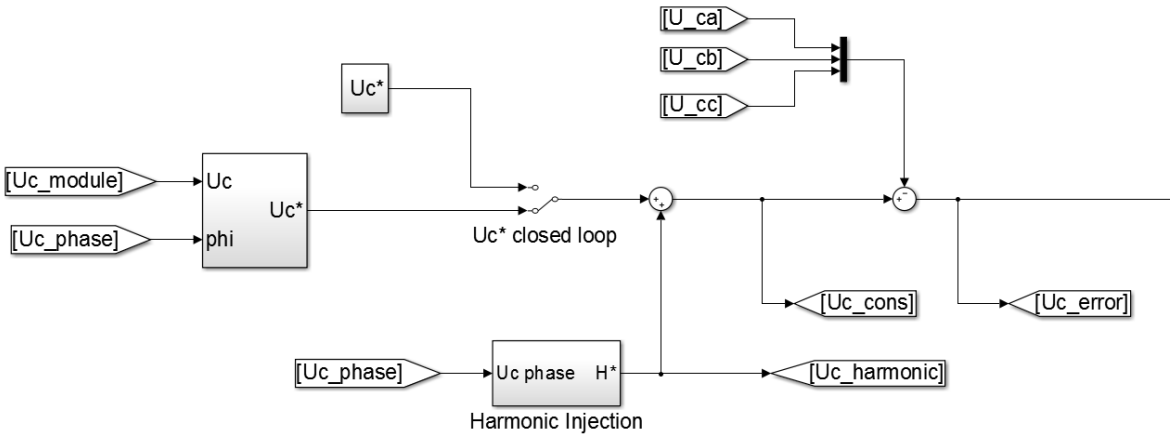

***Figure 4.2**: Harmonic injection within capacitors control loop in simulink*

Figure 4.3 shows the results of the simulation of the harmonic injection.

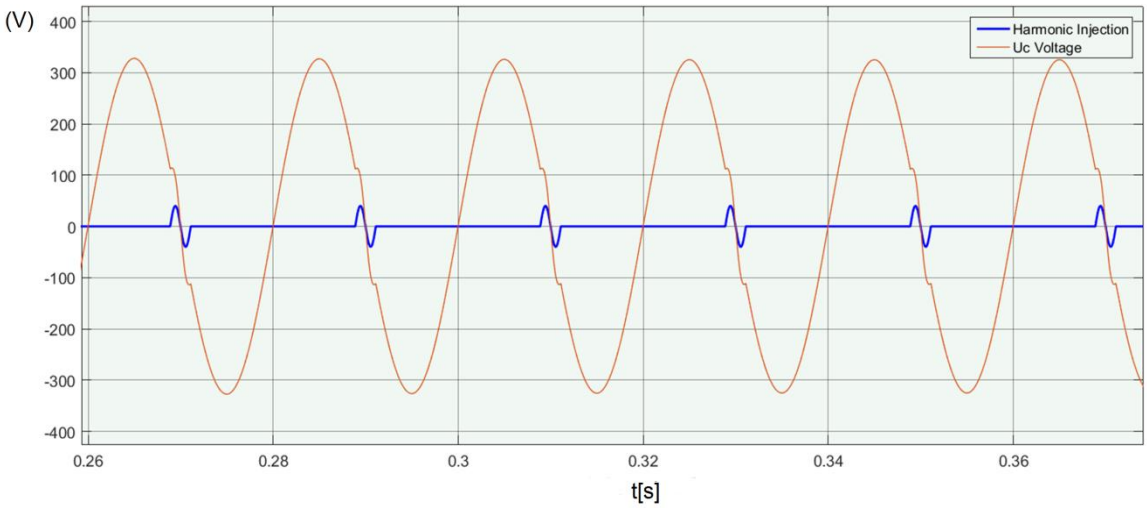

***Figure 4.3**: Harmonic injection at pass by zero effect on capacitors voltage*

4.2. Impedance measurement

Harmonic injection functions as an amplifier to read voltage and current at that particular frequency.

In this model, a bandwidth filter is tuned at fundamental frequency to eliminate the fundamental component on both voltage and current. Then a Fourier analysis is performed at the harmonic frequency to obtain the magnitude and the phase to finally compute the impedance of the PCC (Figure 4.4).

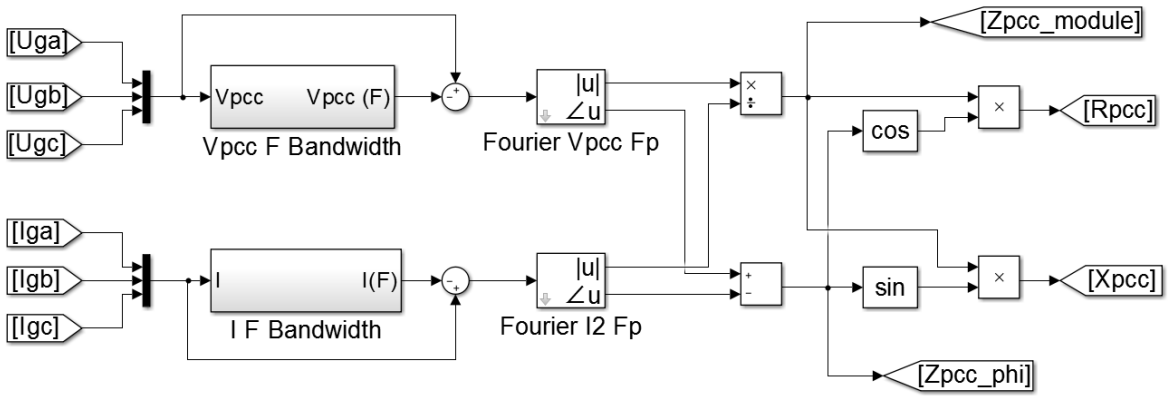

***Figure 4.4**: Impedance estimation simulink*

To illustrate the usefulness of impedance measurement and active methods a simulation is performed with a resonant load (Figure 4.5). The grid disconnects at 0.7 seconds through the simulation. The impedance magnitude at harmonic frequency is implemented with a 1st order filter to avoid ripple.

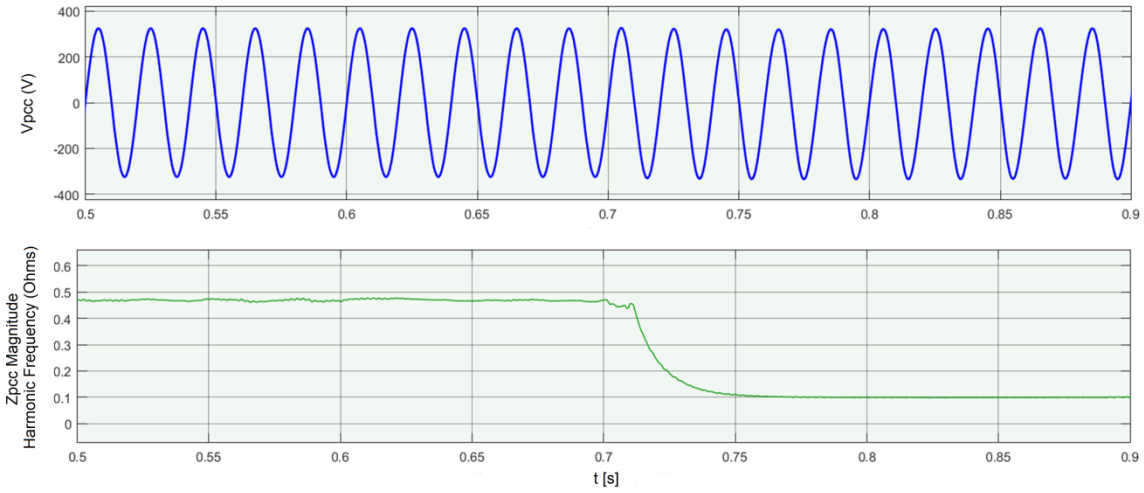

***Figure 4.5**: Grid disconnection effects with a resonant load*

Watching the graph is impossible to distinguish grid disconnection based on the PCC voltage. However, impedance magnitude at harmonic frequency suffers a clear change due to the disconnection.

.

4.3. Detection algorithm

The impedance magnitude of the PCC at harmonic frequency is filtered with a first and second order filter.

The first order filter is considerably faster with a time constant of 0.01 s.

$$t_s(95\%) = 3\tau = 0.03\ s \qquad (4.1)$$

The second order filter presents a slower response with a natural frequency of 10 rad/s and an ξ factor of 1.

$$t_s(95\%) = \frac{-ln(0.05)}{\xi\omega_n} = 0.33\ s \qquad (4.2)$$

The difference between both filters is the variable used to measure the absolute change of the impedance magnitude over time. This signal referred as δ provides the tools to avoid islanding (Figure 4.6).

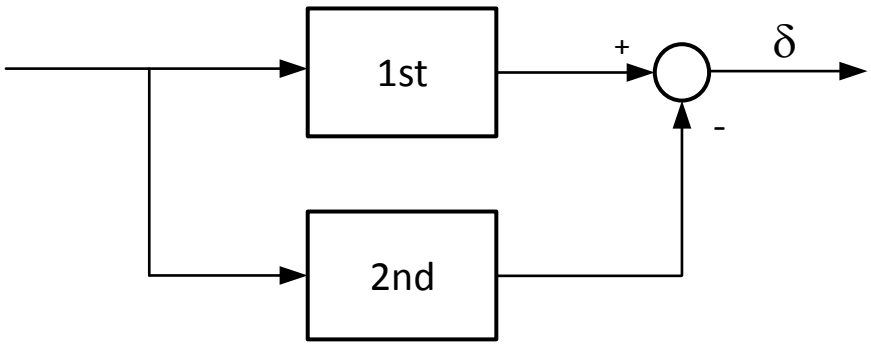

***Figure 4.6**: Block diagram of δ*

In this case, disconnection is set at 1.22 seconds. Figure 4.7 shows both filters and δ during the simulation.

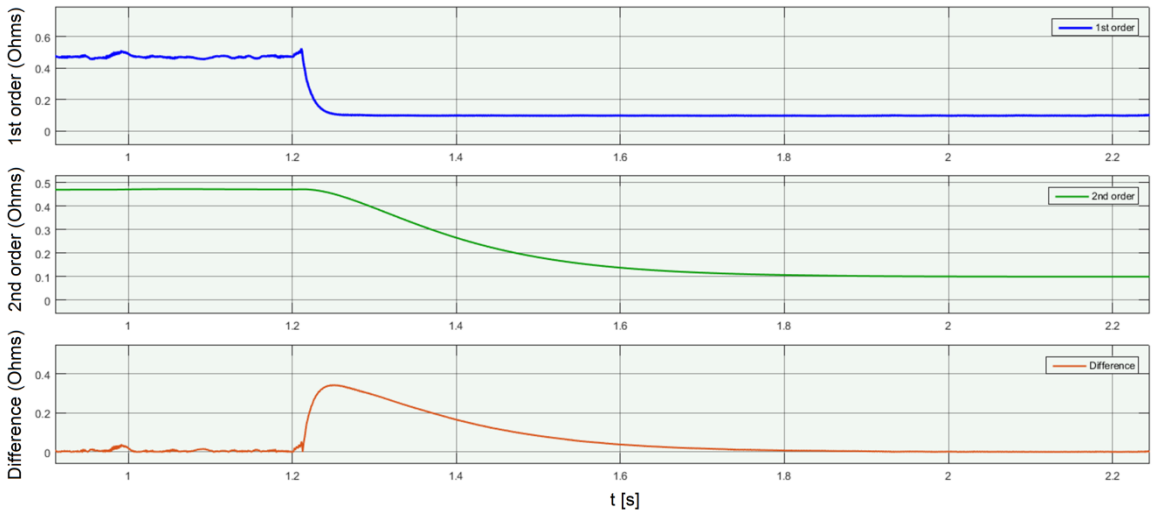

***Figure 4.7**: 1st order filter, 2nd order filter and difference variables*

In order to detect islanding, δ (difference) has to be over a determined value for a certain period of time.

The minimal impedance magnitude change to start counting time is referred as $\delta_{ref} = \delta_{lim} = 0.1\ \Omega$.

The time limit to trigger islanding detection is referred as $t_{ref} = 0.4\ s$.

To implement the algorithm in simulink both filters are first applied and then δ is computed (Figure 4.8).

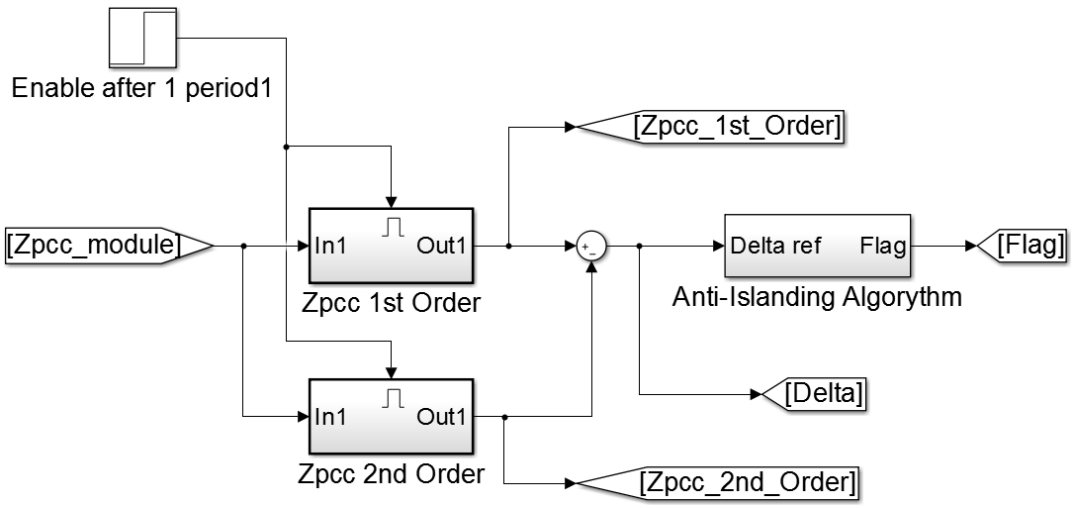

***Figure 4.8**: Anti-Islanding algorithm in simulink*

Then δ is compared to δ_{ref}.

-If it's over, a counter starts counting with an integrator.

-If it's under, it resets the counter.

If the counter reaches the reference time, the anti-islanding flag is activated (Figure 4.9).

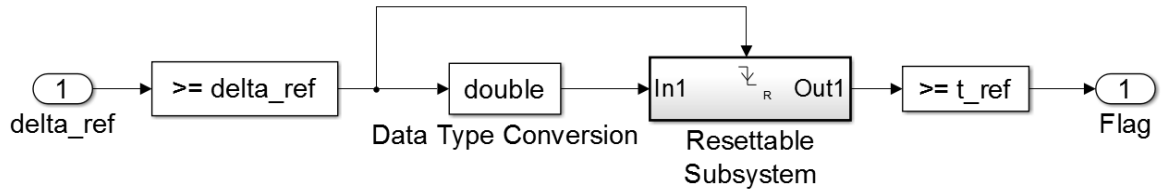

***Figure 4.9**: Detection algorithm in simulink*

Figure 4.10 shows a block diagram to illustrate the logic process.

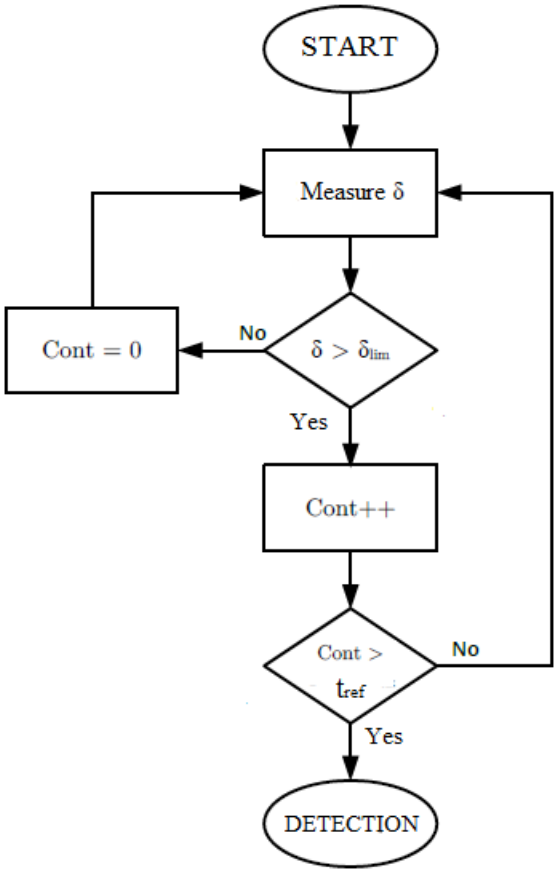

***Figure 4.10**: Conceptual Anti-Islanding algorithm block diagram [1]*

The model used during this project contemplates a static load of constant impedance and a static strong grid (obtained from an unofficial source) .However, depending on the frequency, the impedance magnitude of the PCC may present considerably different values.

Figure 4.11 shows the impedance magnitude Bode diagram of the PCC with the grid connected.

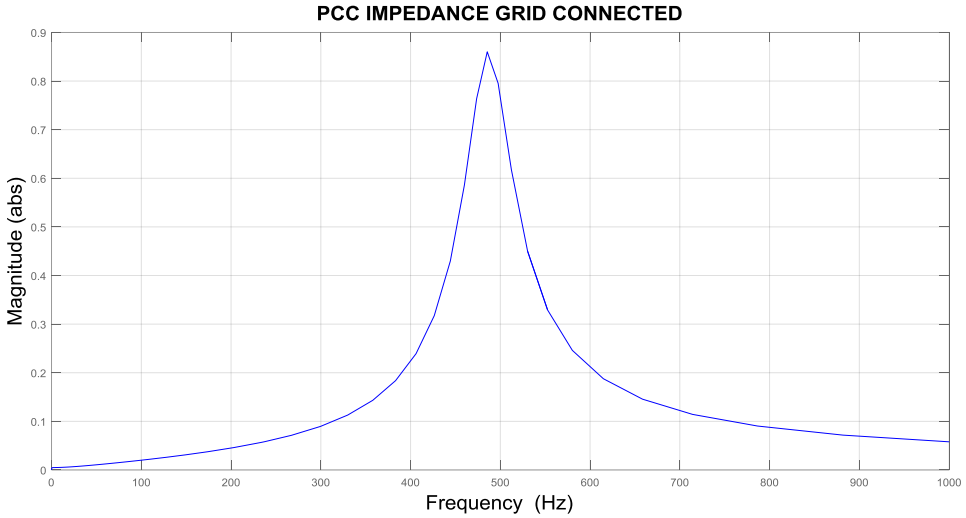

***Figure 4.11**: Bode diagram of the PCC impedance magnitude with the grid connected*

Figure 4.12 shows the impedance magnitude Bode diagram of the PCC with the grid disconnected.

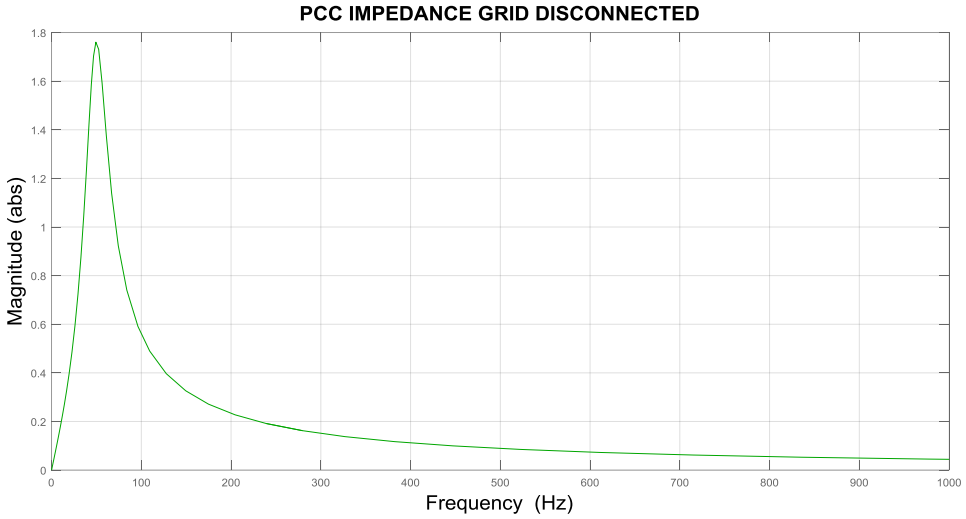

***Figure 4.12**: Bode diagram of the PCC impedance magnitude with the grid disconnected*

The signal used to detect islanding depends directly on the impedance difference of the PCC with a connected or disconnected grid.

Figure 4.13 illustrates the variability of such difference depending on the frequency.

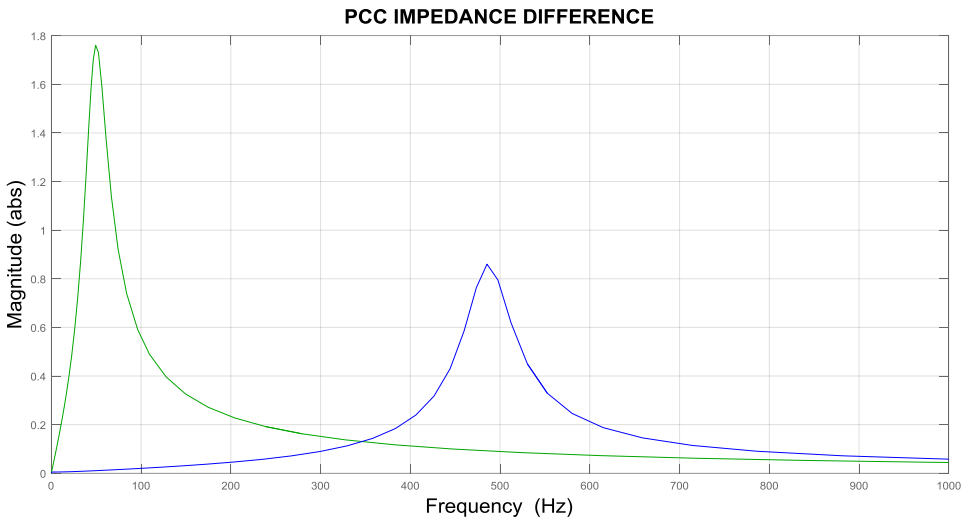

***Figure 4.13**: Bode diagram of the PCC impedance magnitude with and without grid*

Simulating the algorithm at 300 Hz, the impedance raises around 0.06 ohm after disconnection (Figure 4.14).

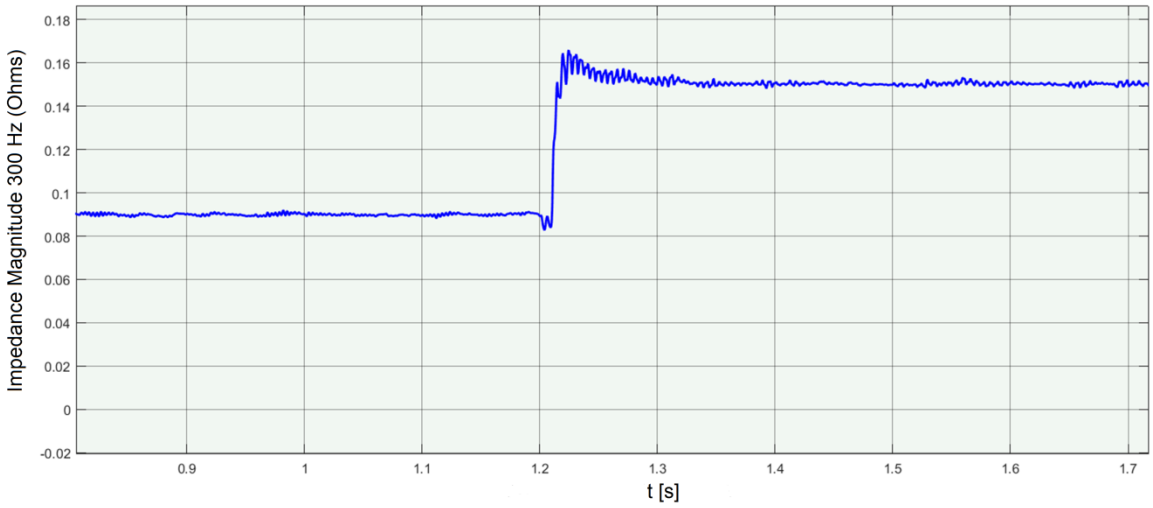

***Figure 4.14**: PCC impedance magnitude variation after disconnection at 300 Hz*

At 500 Hz, impedance magnitude drops around 0.6 ohm after disconnection (Figure 4.15).

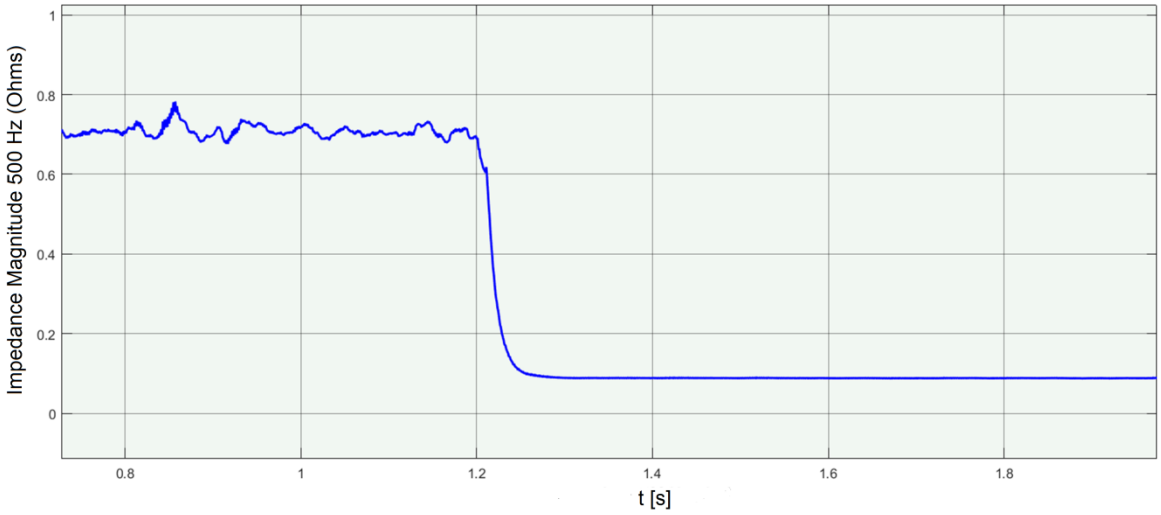

***Figure 4.15**: PCC impedance magnitude variation after disconnection at 500 Hz*

At 350 Hz, it almost remains the same (Figure 4.16).

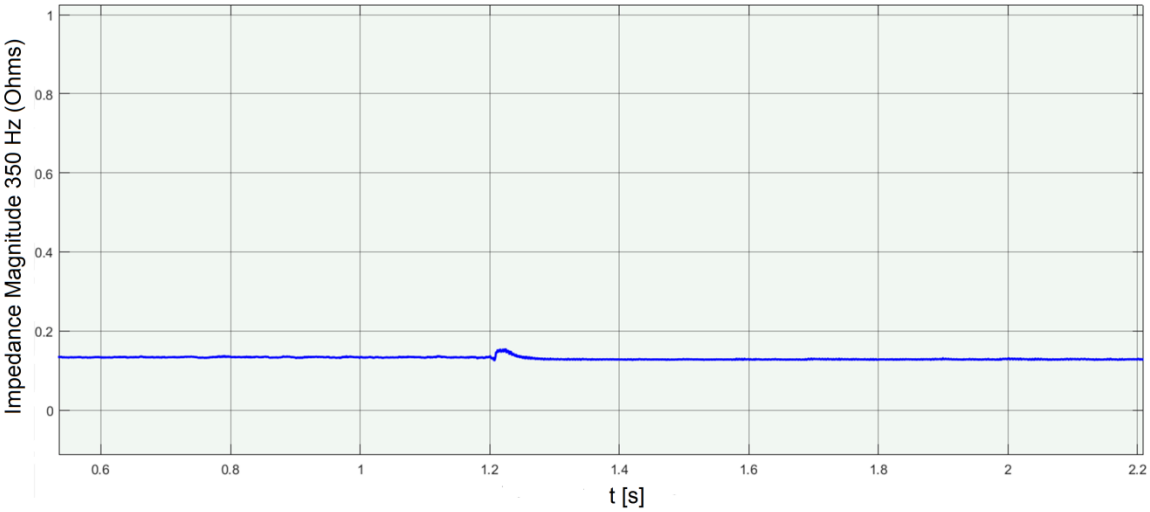

***Figure 4.16**: PCC impedance magnitude variation after disconnection at 350 Hz*

This demonstrates the importance of selecting the adequate frequency. If not done correctly, the algorithm may turn useless.

4.4. Algorithm tuning

Harmonic injection has been tested and proved, however it still has some undetermined variables that must be studied.

4.4.1. Peak voltage

As it was explained before, in order to read the equivalent impedance at a given frequency first the voltage and current at that given frequency must be read.

Harmonic injection peak voltage functions as an amplifier to read PCC impedance. Its value should be big enough so voltage and current are clear and readable over real life perturbations but small enough to generate as less THD as possible. As it depends on the sensor sensibility and real life noise and perturbations, we are unable to define its value. For the purposes of the simulated model, 40 V work well.

4.4.2. 1st 2nd Order filters time constant

First order filter must follow impedance as quick as possible while being stable and filtering high frequency noise. For the purpose of the simulated model, 0.01 s time constant works well.

Second order filter must be considerably slower to generate a noticeable difference from the 1st order filter in case of sudden change but fast enough to follow a continuous slower change over time. It can be seen as a cascade of two first order filters. For the purpose of the simulated model, a natural frequency of 10 rad/s and an ξ factor of 1 works well.

4.4.3. δ_{ref}

δ_{ref} value must discriminate a grid disconnection from noise, perturbations and sudden load variations. For the purpose of the simulated model, at the optimal harmonic frequency, 0.4 Ohms work well.

4.4.4. $\mathbf{t_{ref}}$

Time reference must discriminate unexpected short peaks and singularities from grid disconnection. For the purpose of the simulated model, 0.1 s work well.

4.4.5. Harmonic frequency

To determine the optimal harmonic frequency we first need to study the frequency response of the PCC impedance magnitude.

4.5. PCC Impedance frequency response

Harmonic injection main objective is to make impedance magnitude readable at a certain frequency. However, deciding which frequency should be set is not an easy task.
For that purpose, the frequency response of the impedances involved in the method will be studied.

To quickly analyse the upcoming bode diagrams a colour criteria is established.
Green stands for only load dependant, blue when a strong grid it's involved and red when a weak grid it's involved.

The resonant load considered is defined by the by most European regulations related to anti-islanding safety measures. For that reason, it will be considered a fixed value. Below are represented the expression of the parallel RLC of the load, the transfer function (Figure 4.17) and the values used.

$$\vec{Z}_{RL} = \frac{1}{\frac{1}{R_{RL}} + \frac{1}{j\omega L_{RL}} + j\omega C_{RL}} \qquad (4.3)$$

$$G_{RL} = \frac{s}{s^2 C_{RL} + \frac{s}{R_{RL}} + \frac{1}{L_{RL}}} \qquad (4.4)$$

$$R_{RL} = 1.763\,\Omega \quad L_{RL} = 2.8\,mH \quad C_{RL} = 3.6\,mF$$

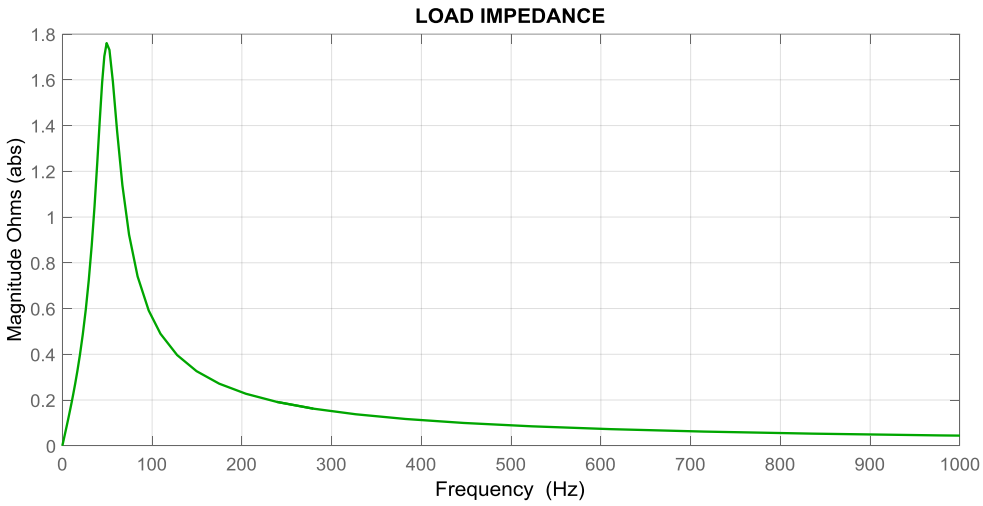

Figure 4.17: *Bode diagram of the load impedance magnitude*

To study the grid impedance behaviour 2 limit cases are considered, a strong and a weak grid (obtained from an unofficial source). Below, the expression of the equivalent grid impedance outside nominal frequency, the transfer function and the values used (Figure 4.18).

$$\vec{Z}_G = R_G + j\omega L_G \qquad (4.5)$$

$$G_G = sL_G + R_G \qquad (4.6)$$

$$R_{GS} = 0.005\,\Omega \quad L_{GS} = 0.03\,mH$$

$$R_{GW} = 0.05\,\Omega \quad L_{GW} = 0.3\,mH$$

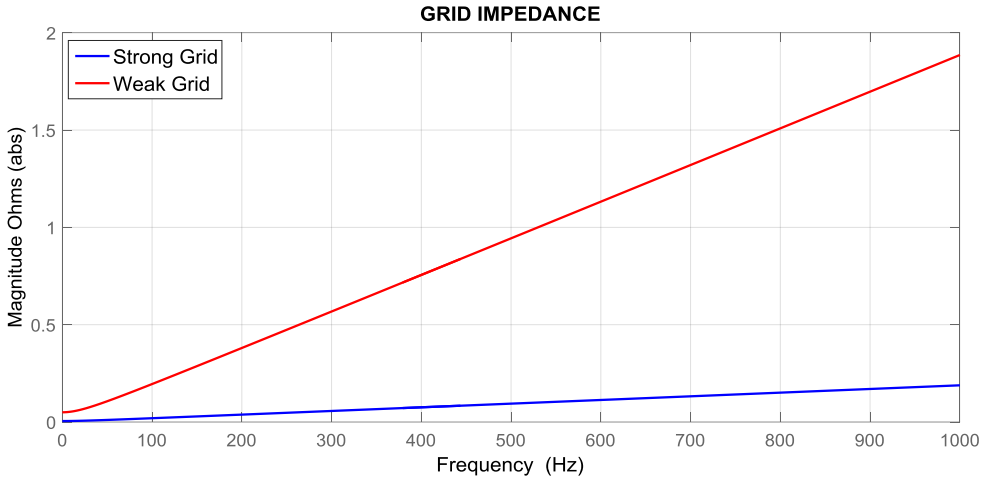

***Figure 4.18**: Bode diagram of the impedance magnitude of a strong and weak grid*

As it can be seen in Figure 4.19 as long as the grid is connected the equivalent impedance magnitude of the PCC is equal to the parallel of the load and the grid. Figure 4.20 shows the Bode diagram for both cases.

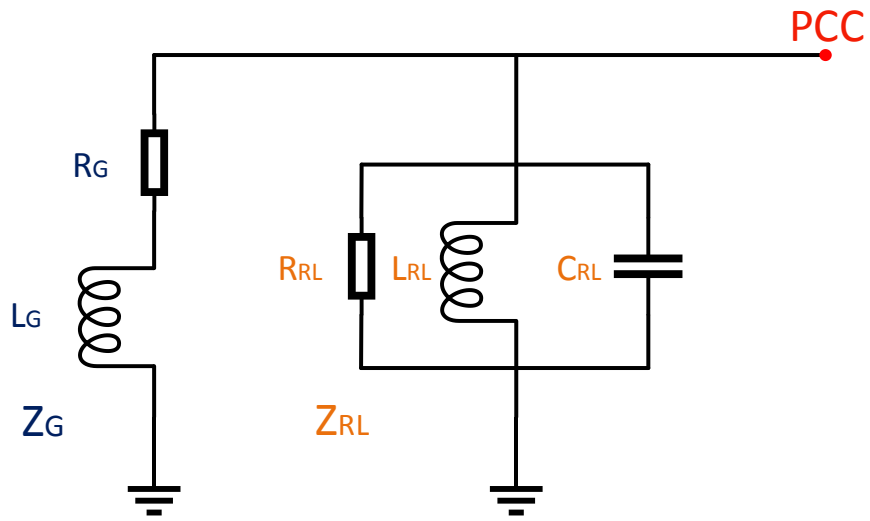

***Figure 4.19**: Scheme of the PCC impedance with the grid connected*

$$\vec{Z}_{PCC\ C} = \frac{\vec{Z}_{RL} \cdot \vec{Z}_G}{\vec{Z}_{RL} + \vec{Z}_G} \qquad (4.7)$$

$$G_{PCC\ C} = \frac{G_{RL} \cdot G_G}{G_{RL} + G_G} \qquad (4.8)$$

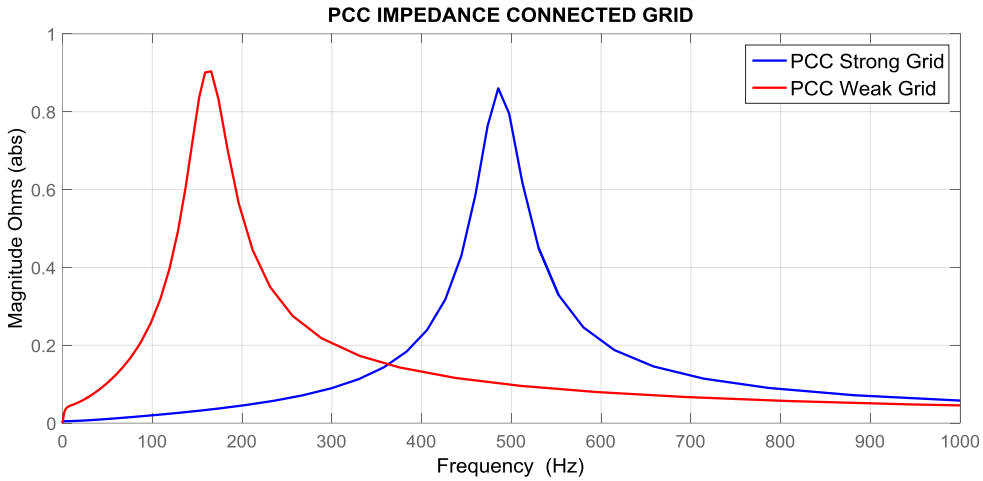

***Figure 4.20**: Bode diagram of the PCC impedance with a weak and strong grid connected*

However, when the grid disconnects, the equivalent impedance magnitude of the PCC becomes equal to the load (Figure 4.21).

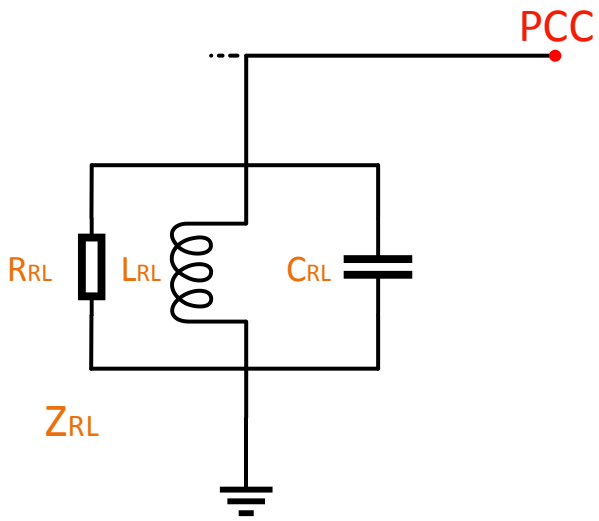

***Figure 4.21**: Scheme of the PCC impedance with the grid disconnected*

$$\vec{Z}_{PCC\ DC} = \vec{Z}_{RL} \qquad (4.9)$$

$$G_{PCC\ DC} = G_{RL} \qquad (4.10)$$

To detect an islanding situation the PCC impedance magnitude must change considerably when the grid disconnects. This is the main criteria to choose the harmonic frequency.

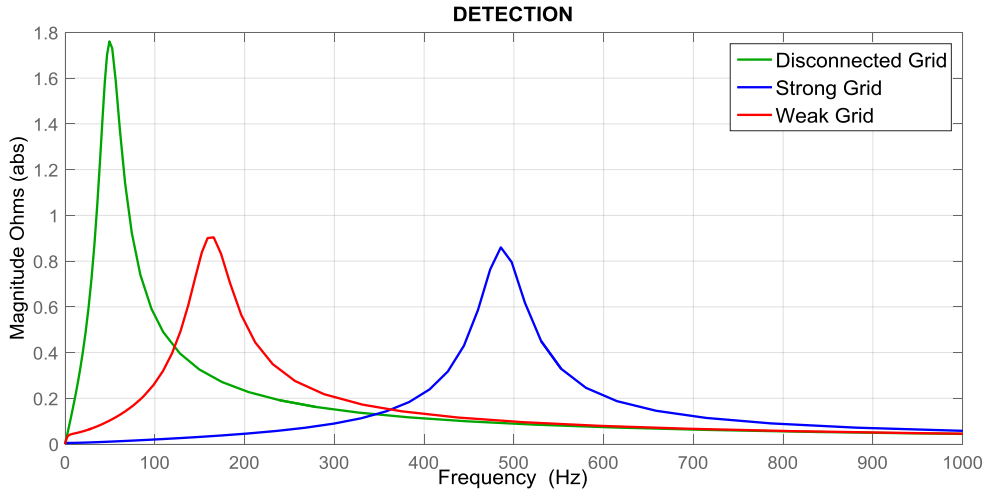

***Figure 4.22**: Bode diagram of the PCC impedance magnitude for all possible cases*

As it can be seen in Figure 4.22, results change drastically depending on the grid.

To clarify this further in the following figure the absolute difference of impedance magnitude when the grid disconnects is represented.

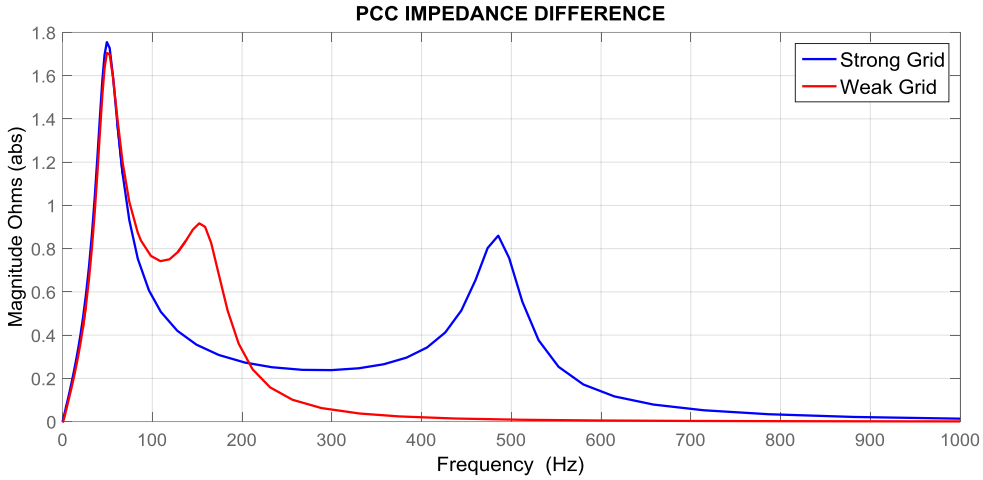

***Figure 4.23**: Bode diagram of the PCC impedance magnitude difference for a strong and weak grid*

For a weak grid the optimal frequency revolves around 150 Hz. However, for a strong grid the optimal frequency goes up to 500 Hz.

In conclusion, due to the variable nature of this method, it's imperative to implement some kind of dynamic control to adjust the frequency at its optimal value.

4.6. Harmonic frequency control

With all the previous analysis we are now prepared to define the boundaries and conditions surrounding harmonic frequency to find a solution.

Load related false detections

A load disconnection or sudden change may modify PCC impedance to the point it could trigger a false detection. The δ_{ref} value should be big enough to cover any sudden change of load impedance while assuring islanding detection.

Recognize the NDZ

Even though this method seeks to cover all possible situations and provide a reliable method to detect islanding we must be aware of a possible NDZ.

A clear case would be if the delta (detection amplitude) is smaller than the maximum impedance difference we can achieve. In this situation the algorithm should warn the user of the NDZ.

Maximize the difference in impedance magnitude

The variable that leads to detection is the difference in impedance magnitude. To get an accurate and fast detection we need to find the optimal harmonic frequency that grants the most difference. As it was explained early, this method presents too much variability to allow a pre-determined fixed frequency. For that reason, we need a dynamic algorithm that provides a tailor-made solution.

Set a lower limit of 100 Hz

Frequency should never get as low as 50 Hz. At 50 Hz grid voltage possesses a fundamental component so PCC impedance cannot be calculated as it was intended. Also, injecting only one period at 50 Hz would mean a continuous signal injection. As the method studied was intended for higher frequencies the consequences and considerations revolving this case are not within the project extent.

4.7. Optimal harmonic frequency seeking algorithm

To find a possible solution for all the conditions mentioned above a simplified program to seek the optimal frequency was developed to illustrate the logic behind.

Previous to installation a formed operator should turn up at the selected micro grid to conduct a study to define its optimal frequency. For that matter, the operator should connect the resonant load defined and let the algorithm run for some time. Then, the anti-islanding device could be tuned in assuring it's the optimal harmonic frequency for that particular grid.

As it can be seen in Figure 4.24 impedance difference magnitude presents two local peaks. It's crucial to only seek for the high frequency peak over the 50 Hz. The designed algorithm gets stuck in the first local optimal it finds, for that reason the harmonic frequency variable must be initialized towards high frequencies.

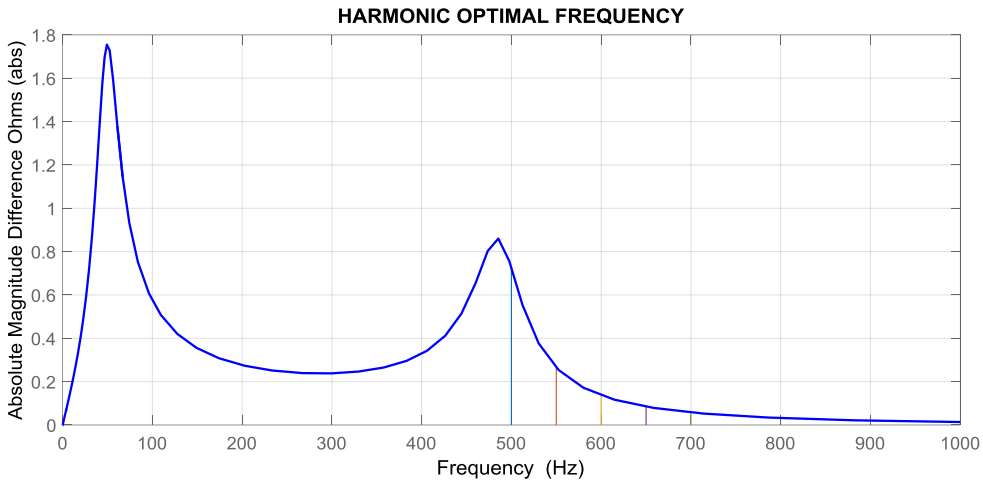

***Figure 4.24**: Optimal harmonic frequency seeking algorithm representation*

First off, some subroutines must be programmed to provide some crucial variables for the main routine. We won't provide any detail on how it computes the variables; it's assumed it functions correctly and regularly.

-A float variable called *z* that represents the difference in impedance magnitude between the connected and disconnected states. The related function is PCC_impedance_difference.

The following list intends to give the reader an idea of how the program works.

1-Supposing the variables are correctly declared it proceeds to the main loop and initialize the ones needed.

2-The algorithm is presented as an interruption service, for that reason the timer is set for 10 seconds.

3-Save the current impedance difference in a variable.

4-Check if the impedance difference is greater than δ_{ref}, if it isn't, a warning is sent.

5-A binary variable referred as n is negated. This variable functions as a pointer towards higher or lower frequencies to seek the optimal.

6-The new harmonic frequency is computed.

7-If the new harmonic frequency is lesser than the lower limit it resets at 700 Hz, a warning is sent and it exits the interruption.

8-A delay is set for this interruption so meanwhile the impedance difference at the new harmonic frequency can be computed.

9-The current value is compared to the value before the delay, if it's greater, we keep the new harmonic frequency, if not, we recover the previous one.

10-If the new frequency is more optimal n is negated again so the next time it enters the

interruption it points towards the same direction. Also, it breaks of the interruption without clearing the flag to seek for the optimal right away.

11-The flag is cleared and it exits the interruption.

```
# DECLARED VARIABLES  1

void main(void)

{
        # INITIALIZE VARIABLES

        ff = 50; # fundamental frequency
        fh = 700; # harmonic frequency injected
        n = 1; # pointer binary  variable
        zs = 0; # impedance magnitude difference static
        OpenTimer0(10000ms) # trigger interruption for each 10 seconds for Timer0 2
        INTCONbits.GIEH = 1; # enable interrupts


        while(1); # main loop
        {
        }
}
void InterruptHandlerHigh()  # Interruption service of the function
{
    if(INTCONbits.TMR0IF)  #  Has Timer0 overflow causing an interrupt?
                        {
                                zs = z; # z = impedance difference in real time / zs     = '' static   3
                                if (z0< δ ) # disconnection unnoticeable?  4
                                        NDZ_warning(void);  # Send a warning
                                n =~ n; # 1 -> -1 -> 1 ...  5
                                fh = fh + f·n; # Try new closest frequency multiple of the fundamental  6
                                if(fh < 100) # Lesser than lower limit?  7
                                        {
                                        Low_fh_warning(void) # Send a warning
                                        fh = 700; # Reset harmonic frequency
                                        INTCONbits.TMR0IF = 0;     # Clear Interrupt Flag
                                        break  # Exit interruption
                                        }
                                delay(60ms); # Wait so z updates its value  8
                                if (|z|>|z0|) # If new frequency is better stay  9
                                        n =~ n; # Keep the pointer in the same direction  10
                                        break # break without clearing the flag to enter the interruption right away
                                else # If not return to the previous value
                                        fh = fh - f·n;

        INTCONbits.TMR0IF = 0;     # Clear Interrupt Flag  11
                        }
}

# SUBRUTINES

void PCC_impedance(fh) # Computes z for a certain fh
{
...
z = X;
...
}
```

The block diagram in Figure 4.25 illustrates the logic behind the algorithm.

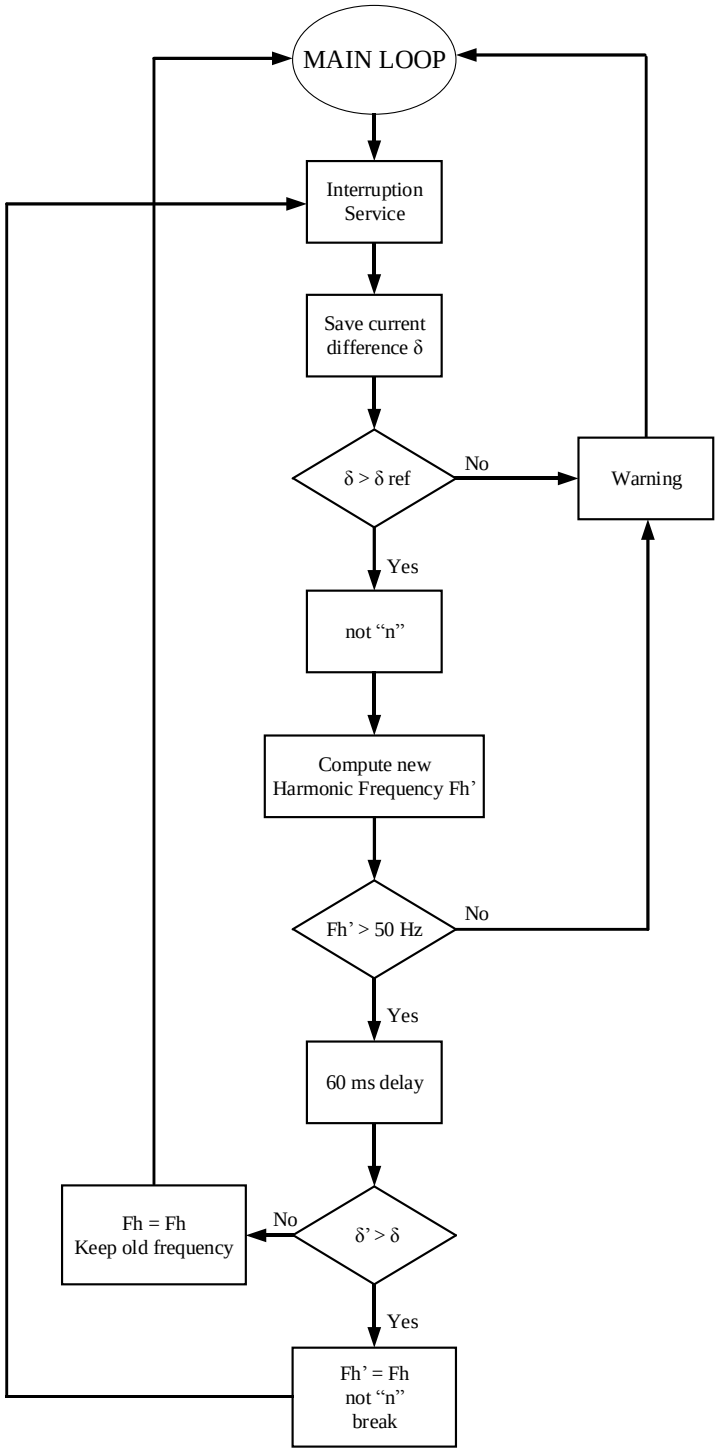

***Figure 4.25**: Block diagram optimal harmonic frequency seeking algorithm*

Conclusions

Completed tasks

During the first stage of the project I studied the working principles of the commutated inverter. Then I implemented a duty generator using a PWM method to synthesize the voltage output. I also covered the current ripple and filters at the inverter output to later introduce an ideal averaged model based on energy conservation. Also I implemented the source, the load, the grid and the electric lines in between.

In the second stage I studied the implementation of resonant controllers over PI controllers. Then I covered the control of CC-VSC, highlighting the differences over VC-VSC to pave the way for anti-islanding algorithms. Finally, I explained the control loops of the VC-VSC controller sequentially (U_S, I_S, U_C, P, Q).

During the third stage I analysed anti-islanding methods for both CC-VSC and VC-VSC.I started covering passive methods, to later explain the resonant load situation. Afterwards, I introduced active methods based on positive feedback and finally impedance measurement methods which are the only viable algorithms for VC-VSC.

In the fourth and final stage, I briefly explained impedance measurement based on harmonic injection to give a general idea of its working principle. Then I conducted a study over the decisive factors of the method and the functionality of each variable to finally come up with an optimal seeking algorithm and protocol to assure the method is optimal.

Conclusion

The main goal of this project was to corroborate the influence of the harmonic frequency of the perturbation for impedance measurement methods and develop a strategy to determine its values.

This was accomplished by analysing the functionality of each variable, designing an optimal seeking algorithm and establishing a protocol to tune the anti-islanding device.

Future work lines

- Study the influence of the local grid in depth and how it may vary over time.
- Find the optimal relation of the peak voltage and relative time of injection per period for multiple frequencies
- Test the viability of low frequency injection
- Implement the transition from grid to islanding of the converter.
- Implement the method studied in real life.

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I would like to thank Marc Llonch for teaching me through all this project, guiding me over the difficulties and dedicating me more time anyone has dedicated in my years of study. He has showed me through his experience how a real engineer thinks and proceeds allowing me to carry on a project that would've been simply impossible without him.

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