

An Alternative Characterization Method of pFET Sub-threshold Slope under NBTI Stress

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Abstract— The effects of negative bias temperature instability (NBTI) on the sub-threshold performance of a pFET have been investigated by means of experimental methods. Specifically, the sub-threshold slope under static and dynamic NBTI stress has been characterized for different NBTI stress conditions. In order to perform the characterization, a proposal based on an alternative measurement technique to obtain the sub-threshold slope is presented. Our first results indicate that similar sub-threshold slope is obtained in all stress conditions.

I. INTRODUCTION

The impact of Negative Bias Temperature Instability (NBTI) on MOS devices and circuits has been flagged as the foremost reliability problem for present CMOS technology which can limit the IC dimensions reduction [1]. It is mainly accepted that NBTI is ascribed to the formation of Si/SiO₂ interface states and the oxide positive charge [2]. Regarding this problem, the work has been focused on evaluating the pFET conduction behavior. These works have been concluded that NBTI provoke a threshold voltage shift (ΔV_{th}) [3, 4]. Due to the NBTI recovery, careful characterization and stress techniques must be used in order to determine the impact of this reliability problem [5]. These techniques suppose that sub-threshold slope (SS) is not affected by NBTI. However, recently some works have claimed that SS is affected by NBTI [6, 7]. These contradictions, together with the fact that nowadays, a lot of CMOS circuits operate at sub-threshold area [8], consistent data over different stress conditions are needed.

In this paper, we have measured the sub-threshold slope under different NBTI stress conditions. In order to do that, an alternative characterization method based on two measurement points is presented.

II. EXPERIMENTAL

The samples under test are pFET with aspect ratio $2\mu\text{m}/0.13\mu\text{m}$, with SiON gate dielectrics with $EOT = 1.4$

nm, provided by IMEC. These devices have been tested with a standard 4156C semiconductor analyzer at 125°C. The standard measurement method [9] is based on a stress-measurement-stress sequence with exponentially increasing periods of time (Fig.1a). The standard characterization method start with a completed I_D - V_G measurement and the pFET constant current voltage threshold (V_{thcc}) and sub-threshold slope (SS) are obtained. Once the initial V_{thcc0} and SS_0 are measured, the stress is applied to the devices. After each stress period, the drain current for one value of V_G is measured ($I_{D\text{stress}}$) and assuming that SS is not affected by NBTI the V_{thcc} shift (ΔV_{thcc}) is obtained by equation (1). Therefore, with the standard characterization method the sub-threshold slope cannot be obtained.

$$\Delta V_{thcc} = \frac{\log\left(\frac{I_{D0}}{I_{D\text{stress}}}\right)}{SS_0} \quad (1)$$

Fig.1b depicts the proposed characterization method to obtain the SS. The method is a trade off between measurement time and recovery effect. In the standard stress measurement stress sequence only one drain current value is obtained. In the proposed method the drain current is measured at two different values of V_G in the sub-threshold area, which is faster than measuring the full I_D - V_G . Therefore, the recovery effects are reduced. From these measured points, the SS is calculated by equation (2), where sub-index 1 and 2 denote the measured points.

$$SS = \frac{V_{G2} - V_{G1}}{\log\left(\frac{I_{D2}}{I_{D1}}\right)} \quad (2)$$

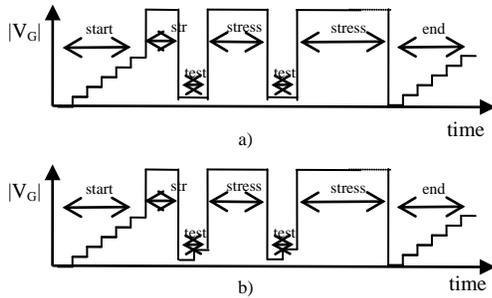


Fig.1 a) standard fast NBTI stress sequence b) alternative proposed method.

III. RESULTS

In Fig.2 the I_D - V_G curve of a fresh and stressed pFET is plotted. As expected, after stress the I_D - V_G curve is shifted and therefore, $|VT|$ increases. However, in order to observe the impact on sub-threshold behavior the $\log I_D$ - V_G , which is shown in Fig.3, should be analyzed. In this graph, a shift in this characteristic is observed due to NBTI stress and a clear impact on SS is not observed. The required measurement time for this curve is too high. Consequently, the recovery effect can mask the real impact of NBTI on SS. Fig. 4 represents SS as a function of the stress time of pFETs subjected to DC and AC NBTI stress obtained by means of the proposal method. The graph shows that SS is independent of stress time, with an average value of 122mV/dec for all samples and stress time. For instance, before stress the SS is 123mV/dec with standard deviation between samples of 1.28mV/de whereas after 1000s stress (125°C and -1.8V) SS is 122mV/dec with standard deviation of 3.16mV/dec. The impact of stress voltage on SS has been also analyzed. In Fig.5 the SS against stress voltage after 400s stress at 125°C is plotted. In this case, again, at most weak stress voltage dependence is observed in the SS.

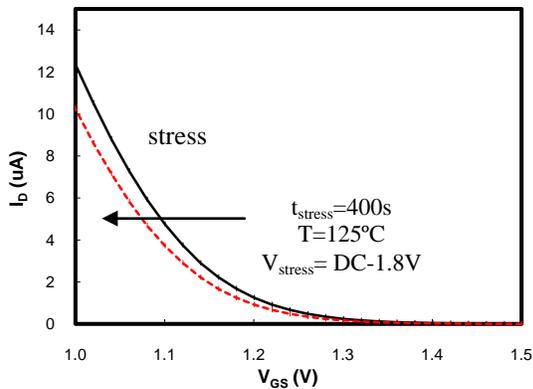


Fig. 2 Measured V_{TH} for fresh an after DC.

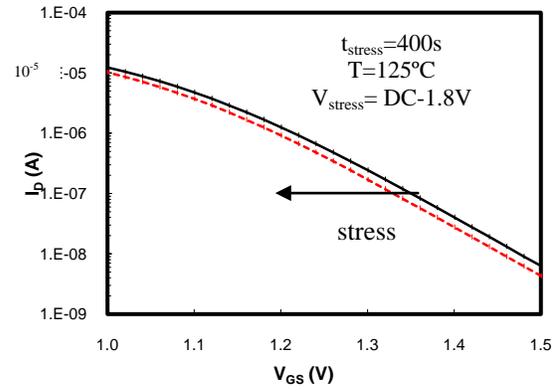


Fig. 3. Measured sub-threshold V_{TH} for fresh an after DC stress.

Finally, the SS again stress frequency up to 2GHz has been also analyzed on dedicated on-chip circuit [10]. Fig.6 shows the SS frequency dependence after a 400s at -2V and 125°C, once again, a clear impact of NBTI on SS is not observed.

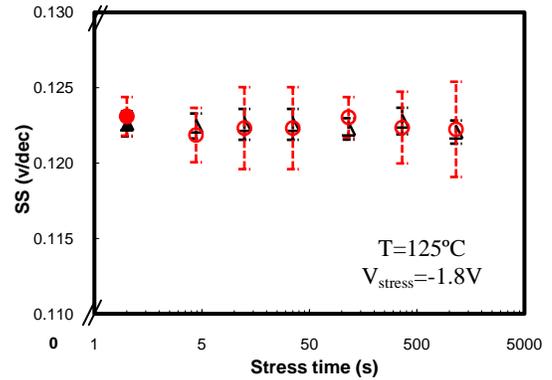


Fig. 4. Measured sub-threshold slope against stress time for AC (black) and DC (red) NBTI stress -1.8V, 125°C.

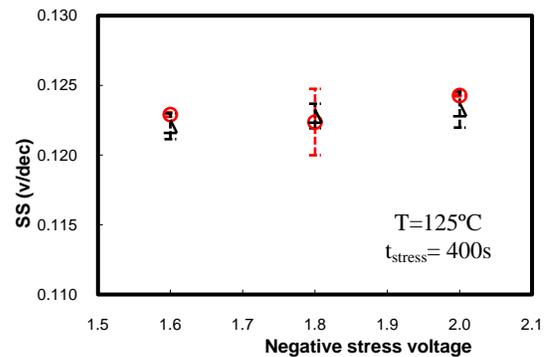


Fig. 5. Measured sub-threshold slope against AC (black) and DC (red) stress.

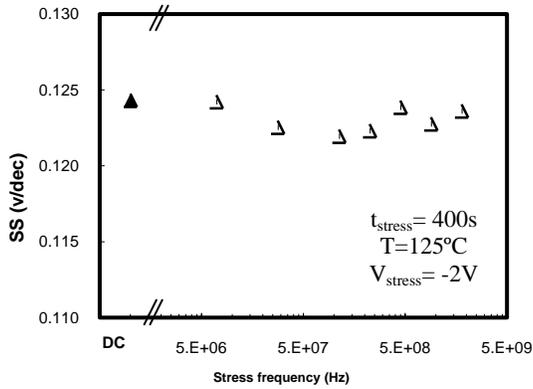


Fig. 6. Frequency response of SS after NBTI stress.

IV. CONCLUSIONS

In this paper, the impact of NBTI on pFET sub-threshold behaviour has been experimentally analyzed. A characterization method based on two measurement points has been proposed. In our experiment, the results point out that there is not a strong impact of NBTI stress on the sub-threshold slope. This would imply that, to the first approximation, NBTI effects on CMOS circuit can be predicted in SPICE simulator just shifting the V_{TH} parameter of pFET. Further, more extensive characterization and comparison with other techniques are ongoing.

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