Development and implementation of a LabVIEW based SCADA system for a meshed multi-terminal VSC-HVDC grid scaled platform

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Content

Summary

This project is oriented to the development of a Supervisory, Control and Data Acquisition (SCADA) software to control and supervise electrical variables from a scaled platform that represents a meshed HVDC grid employing National Instruments hardware and LabVIEW logic environment. The objective is to obtain real time visualization of DC and AC electrical variables and a lossless data stream acquisition.

The acquisition system hardware elements have been configured, tested and installed on the grid platform. The system is composed of three chassis, each inside of a VSC terminal cabinet, with integrated Field-Programmable Gate Arrays (FPGAs), one of them connected via PCI bus to a local processor and the rest too via Ethernet through a switch. Analogical acquisition modules were A/D conversion takes place are inserted into the chassis. A personal computer is used as host, screen terminal and storing space.

There are two main access modes to the FPGAs through the real time system. It has been implemented a Scan mode VI to monitor all the grid DC signals and a faster FPGA access mode VI to monitor one converter AC and DC values. The FPGA application consists of two tasks running at different rates and a FIFO has been implemented to communicate between them without data loss.

Multiple structures have been tested on the grid platform and evaluated, ensuring the compliance of previously established specifications, such as sampling and scanning rate, screen refreshment or possible data loss.

Additionally a turbine emulator was implemented and tested in Labview for further testing.

Glossary

P_t	Mechanical power
C_p	Power coefficient
P_v	Wind power
ρ	Air density
A	Blades delimited area
v_v	Average wind speed
R	Blades radius
ρ	Air density
w_{nom}	Nominal speed
ϑ	Pitch angle
$c1$	Adjusting coefficient 1
$c2$	Adjusting coefficient 2
$c3$	Adjusting coefficient 3
$c4$	Adjusting coefficient 4
$c5$	Adjusting coefficient 5
$c6$	Adjusting coefficient 6
$c7$	Adjusting coefficient 7
$c8$	Adjusting coefficient 8
$c9$	Adjusting coefficient 9
P_{DC}	Active power
P_{DC*}	Active power control signal
K_d	Droop constant
E_{DC}	VSC DC voltage
E_{DC*}	VSC DC voltage control signal
P_{DCadd*}	Additional active power control signal
λ	Tip-speed-ratio
λ_{opt}	Optimum Tip-speed-ratio
Cp_{opt}	Optimum power coefficent
Iq	Active power current control signal
Idc	Direct current from AC to DC
Pdc	Power transferred from AC to DC
Van,bn,cn	Three-phase phase to neutral voltages
Ia,b,c	Line currents
ωt	Rotor speed

Acronyms

AC	Alternating Current
DC	Direct Current
FPGA	Field Programmable Gate Array
HVAC	High Voltage Alternating Current
M-HVDC	Multi-Terminal High Voltage Direct Current
NI	National Instruments
PCI	Peripheral Components Interconnection
RSE	Referenced Single-Ended
SCADA	Supervisory Control And Data Acquisition
VI	Virtual Instrument

VSC   Voltage Source Converters

1 Introduction

The required measurements from the scaled meshed HVDC grid are DC current and voltage of each of the converters as well as AC current and voltage. With these measures powers will also be calculated together with frequencies, averages and RMS values.

The acquisition modules can be accessed through an interface Scan engine or personalized sampling system programmed with LabVIEW FPGA[1].

The user friendly programming interface provided on Scan mode was tested and a SCADA application for DC signals of all the grid was implemented.

On second try, it was decided to tackle FPGA programming to implement a SCADA application to monitor DC and AC signals of one of the converters. With LabVIEW FPGA programming is possible to attain personalized sampling, data transfer and synchronization of the FPGA task and the real time host task.

1.1 Initial goals

- To learn about HVDC grid scaled platform components and its functions.
- To define which measures are important for VSC-HVDC grid control.
- To configure, test, and install the software and hardware.
- To implement and test a SCADA system for the whole grid DC signals monitoring in Labview.
- To implement and test a SCADA system for a converter DC and AC signals monitoring in Labview FPGA, attain an 700 us sampling period optimised system.
- To implement and test a wind turbine emulator for the platform.

1.2 Reach

The designed SCADA system has been put to test with a meshed multi-terminal VSC-HVDC grid scaled platform. The program has been optimized using multiple operation rates task separation, a personalized sampling and adapting the FIFO transmission channels to the generated amount of data.

A comparison of the different computational resource locations and the available communication interfaces between the PC host, FPGA and cRIO processor has been made and thus an appropriate choose amongst the available solutions for the system design.

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[1] *http://www.ni.com/white-paper/7338/es/#toc5*

Once established the optimal resource location and data communication methods, the program itself has been defined which is composed by the following parallel multi-rate tasks: data acquisition, FIFO transmission, processing of deducted measurements, logging and user interface for control and visualization.

Two functional and safe applications have been developed:

- A Scan mode based DC signals monitoring and data logging system hosted on the PC, which due its FPGA access mode configuration time limitations cannot keep track of AC signals.
- A FPGA mode based AC signals monitoring hosted on the cRIO that deterministically ensures 700 us sampling to individually monitor one of the VSCs.

Lastly, a wind turbine simulator has been designed to emulate the power injection into the grid by wind turbines under different wind conditions and tested with the Scan mode AC monitoring SCADA.

2 HVDC transmission

In the twentieth century, HIgh Voltage Direct Current (HVDC) was demonstrated to be the best solution for many specific application areas and the rise of the number of installations per year has been rising at the beginning of the twenty-first century [1].

2.1 Long distance bulk power transmission

Power transmission from point to point through large distances employing requires less cable laying (two instead of the three necessary lines for three-phase system). Furthermore, in DC current transmission, the cable inductance and capacitance only affects during the transient state, but not during the permanent regime.

When considering to choose between HVDC or High Voltage Alternating Current (HVAC) it is important to consider the break-even distance concept. It is the transmission distance from which HVDC becomes economically preferable over HVAC. This distance takes place when the AC transmission power loss costs become superior to the installation of the HVDC converters. For terrestrial transfer this distance is typically over 500 km. The NordNed submarine HVDC between Norway and the Netherlands, for example, reaches a 580 km distance [1].

2.2 Submarine transmission

Break-even distance for submarine transmission is considerably lower than the terrestrial, from over 50 km, since the existence of parasitical capacitances forces to charge and discharge the capacitors periodically which derives in the augment of reactive power and power loss.

2.3 AC asynchronous connections and different frequency systems connections

HVDC can be employed to connect AC asynchronous systems and act as electrical insulation to prevent grid perturbation propagation, such as the 150 MW, ±42 kW McNeill back to back HVDC link between Alberta and Saskatchewan [1].

An example of different frequency systems connection is the Melo HVDC between Uruguay and Brazil, which run at 50 and 60 Hz respectively [1].

3 Meshed multi-terminal VSC-HVDC grid scaled platform.

A meshed multi-terminal VSC-HVDC grid scaled platform designed to test and verify VSC control scheme performance. The experimental platform emulates the temporal behaviour of a real scale system . It is composed by three VSCs terminals connected on the DC side through a meshed grid and on the ac side to the AC supply grid. An emulation of a wind farm can be achieved by injecting an amount of active power equivalent to the wind power collected at the farm through one of the converters.
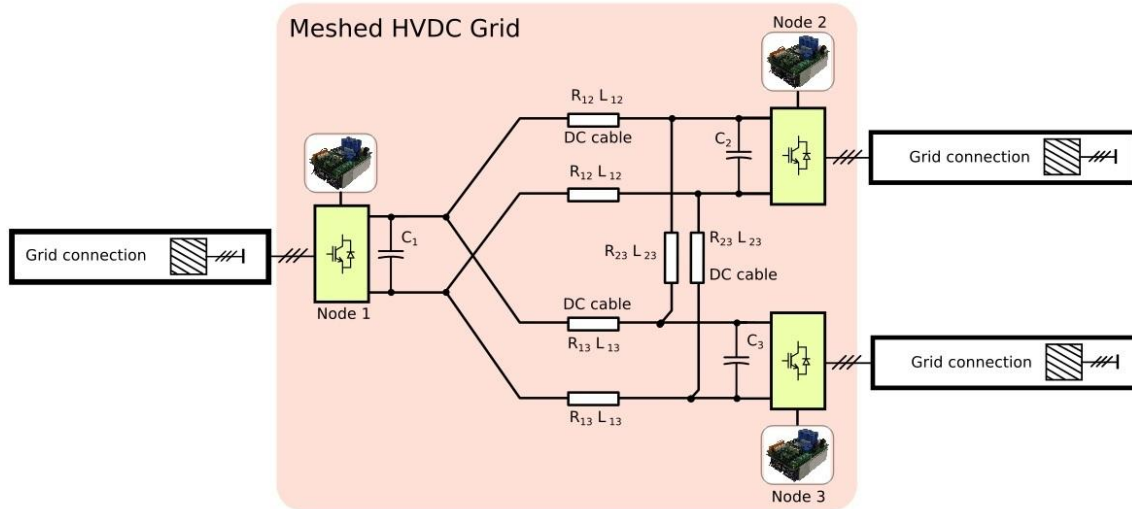

Figure 1. Meshed multi-terminal VSC-HVDC grid scaled platform scheme

Figure 2. The three cabinates containing the M-HVDC VSCs

The line inductances and resistors between converters have scaled values chosen according to the methodology exposed in [5].

Each converter (Figure 3) is composed of a power board and a control board based on a Digital Signal Processor (DSP) of Texas Instruments (TI), the DC and AC measures required for the SCADA system are provided by additional measuring boards, which provide six electrical measures: dc line current and voltage and ac current and voltage from two ac lines. Three numerated cabinets contain each of the VSC terminals .
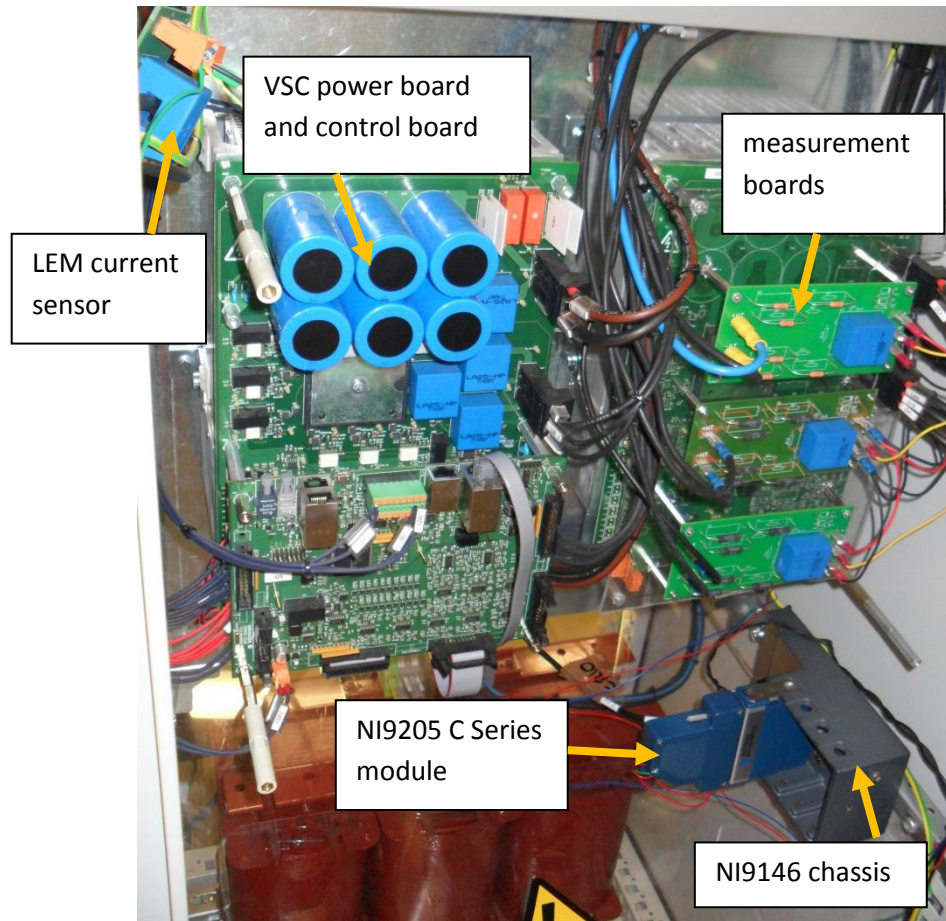
Figure 3. VSC terminal cabinet number 3.

Nominal values			
DC		**AC**	
Enom	500V	Vf-f rms	230 V
Inom	11.4 A	If rms	14.3 A
Pnom	5700 W	Pnom	5700 W

Table 1. Meshed multi-terminal VSC-HVDC grid scaled platform nominal values.

4 Hardware employed to implement the SCADA system

The Figure 4. NI hardware employed for the SCADA system implementation exposes the interconnected elements of the acquisition system: chassis, series C acquisition modules, cRIO, and host PC. The hardware employed belongs to National Instruments.
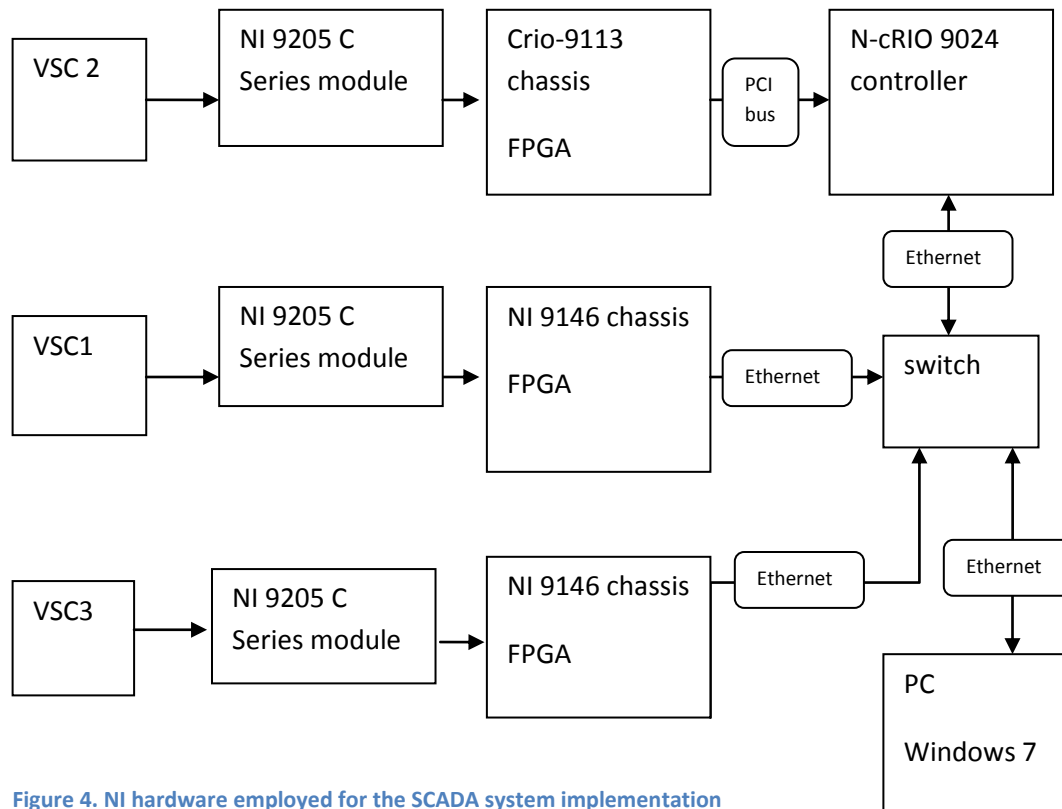

Figure 4. NI hardware employed for the SCADA system implementation

4.1 cRIO-9113 chassis

The CompactRIO chassis contains reconfigurable I/O. The reconfigurable FPGA core i individually connected to each I/O module and can be programmed with I/O functions to read or write signal information to each module. Since each module has an independent bus from the RIO FPGA, the I/O operations in each module can be precisely synchronized with a 25 ns resolution.

The RIO core can locally process integer-based or fixed-point and decision and send signals directly from one module to another. It is connected to the CompactRIO real-time controller through a local PCI bus [2]. The real-time controller can collect data from any control or indicator included on the front panel of a RIO FPGA by means of a scanning interface or write/read FPGA functions. The FPGA RIO can generate interruption requests to synchronize the real-time

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[2] PCIs directly connect peripheral devices to the motherboard and allow dynamic configuration of the device.

program to the FPGA. The real-time controller is used to perform waveform analysis, data logging, Ethernet and serial communication. The reconfigurable chassis, the real-time controller and the I/O modules are combined to create a integrated autonomous system.

The cRIO-9113 chassis is provided of four slots to install the input or output signal modules and the Xilinx Virtex-5 programmable FPGA with configurable I/O's. It supports LabVIEW Real-Time and LabVIEW FPGA logic support which provides predetermined virtual instruments (vi's) to facilitate FPGA programming.

4.2 NI9146 chassis

The NI 9146 is a 4 slots expansion chassis that can be used to easily add I/O C Series modules to a Ethernet 10/100 standard net. It can be accessed either from LabVIEW on Windows, or as a remote extension on LabVIEW Real-Time systems such as CompactRIO and it does not require the Real-Time module to access it.

For low level access, LabVIEW FPGA can be used to program the integrated Spartan-6 LX45 FPGA which provides reliable high speed, personalized timing and processing algorithms.

4.3 NI 9205 data acquisition module and LEM sensors

The NI 920 Series C module is provided of 32 analogical single-reference inputs or 16 differential channels of 16 bits resolution and a maximum sampling rate of 250 kS/s [3]. Each channel's input voltage can be separately configured. It includes an up to 60 V protection against overvoltages between input channels and COM channel (ground). Its equipped with a double isolation barrier from channels to ground for major protection.

The channels have been configured in Referenced Single-Ended (RSE) terminal mode in which all channels are referenced to the COM channel, connected to the ground. The voltage range has been settled to ±10 V. It is recommended connecting all unused channels to ground to obtain neutral lectures, otherwise noise signals appear which could be confused with signals.

Regarding analogical signal collection; the voltages will be obtained from the measure boards, which provide a proportional voltage between ±10 V and the LEM sensors will provide a proportional current that the mearure board will process and return as a proportional voltage between ±10 V.

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[3] If you would like to know how fast you can get a reading from every channel then you take the kS/s number and divide by the number of channels you wish to scan. This will tell you how many samples you can get for EACH channel per second.

4.4 NI-cRIO9024

The integrated real-time controller cRIO-9204 is part of the programmable automation platform CompactRIO. Its equipped with a 800 Hz industrial processor *Freescale* for deterministic and reliable real-time applications, and contains 512 MB of RAM DDR and 4 GB of non volatile storing to preserve programs and registered data.

It is designed for low power consumption with double supply inputs of 9 to 35 VDC.

The controller is provided of two Ethernet ports which have been employed to communicate with the chassis on the other two VSC terminals.

For additional higher storing capacity built-in logging applications it is equipped with a Hi-Speed USB port to connect USB based storage units.

4.5 Host PC

The program development has been conducted in a personal laptop with Windows 7 Home Premium operative system, which has been configured with the necessary Labview logical support. The PC is also used as a screen terminal for the SCADA applications.

5 Logic support.

5.1 Real-Time Operating System (RTOS)

Generally, an operating system manages computer hardware resources and lodges the application to run. A RTOS does the sake task, but is specially designed to run applications with a high precision and reliability synchronisation to attain deterministic applications.

To be considered "real-time", an operative system needs to have a determined maximum time for each critical operation performed (or at least being able to ensure said maximum most of the time). The OS able to completely ensure a maximum time for said operations is usually referred as "hard real-time", whilst OS's which can only partially guarantee it are referred as "soft-real time".

The hard real-time systems are necessary in those instances when for security or control requirements the system designer requires to have guarantee that none of the operations will exceed the indicated temporal specifications. On the other hand, if the occasional data loss does not constitute a problem a soft real-time OS suffices.

The most important feature of a RTOS is its ability to ensure a really consistent execution synchronization. This is achieved providing the programmer with high control over the prioritization of tasks.

Comparing to RTOS, general use OS are designed to be more responsive whilst multiple services are run at once, while RTOS are designed to ensure reliable and precise execution of a few critical applications. Real-time systems were designed to solve two general class instances: event response and closed loop control.

5.1.A Determinism and jitter

Determinism is the characteristic of a system that describes how consistently the system responds to external events or performs operations within a given time limit. Jitter is a measure of the extent to which execution timing fails to meet deterministic expectations. Most real-time applications require timing behaviour to consistently execute within a small window of acceptable jitter.

For example, in this project FPGA application acquisition task, six channels signals must be A/D converted, and stored into the FIFO in no more that 700 us whilst a few other control operators take place in parallel, such as reading from indicators and writing into controls.

5.2 Employed software packages

The CompactRIO has been configured with software modules for correct communication, synchronous time management and common network resources. The *Measurement & Automation Explorer de National Instruments* (*NI MAX*) machinery management platform was uses was used. The following list contains a description of the drivers installed on the CompactRIO.

- LabVIEW 2015

  Base software.

- LabVIEW FPGA

  Provides the tools to program on FPGA targets and communicate with them from host.

- API VISA

  Automatically selects the adequate drivers for a resource, for a variety of instrument kinds: GPIB, serial, USB, Ethernet, PXI, or VXI or Ethernet.

- Labview Real Time

  Configuration management and synchronization with the RT target (the cRIO)

- Scanning Engine

  Provides access to the I/O with LabVIEW real-time an host applications without FPGA programming. Provides a coherent access to the I/O variables, which are stored in a global memory and are synchronously actualized with the configurable Scanning Period.

- Network Variable Engine

  Negotiates between different data structure protocols employed by different system applications or networked elements and provides the Networked variables, which are common to every system element, configurable and easily accessible.

5.3 Programming interfaces configurations

To adjust to the requirements and complexity of a project and available development time, LabVIEW offers two main different access modes and programming configurations.

5.3.A Scanning mode

Te Scanning mode allows the acquisition of calibrated data without employing FPGA programming. It is assisted by LabVIEW Real-Time environment and composed of two

elements: firstly, the Scanning Engine, which actualizes the I/O variables value at a specified rate, including the analogical lecture modules and abstract user defined variables. Secondly, the Scanning Interface, a set of software packages responsible of the I/O modules detection, temporization, synchronization and communication. Said interface is executed in a hardware temporized scan cycle actualizing the physical I/O values.

There a local and networked defined variables and their maximum refreshment rate is limited to 1KHz and 100 Hz respectively.

Using the Scanning mode it is not necessary to employ LabVIEW FPGA or define the communications between the FPGA and the host vi. Neither there is need to compile the program before deploying it and running it. On Scanning mode, LabVIEW programs the FPGA on the CompactRIO to work with the scanning variables.

5.3.B FPGA mode

LabVIEW FPGA mode allows to access the C Series modules, in our case analogical modules, from the FPGA target VI's. The modules appear under the FPGA target on the exploration windows and the I/O channels can be accessed.

FPGA mode allows FPGA programming and therefore more flexibility, personalization and determinist synchronization of the tasks. There is a 8 us minimum time between conversions from Analogical to Digital (A/D) signal. The minimum time can be reduced affecting, though, conversion quality.

FPGA programs require to be compiled before execution and the program developing time becomes much more slow.
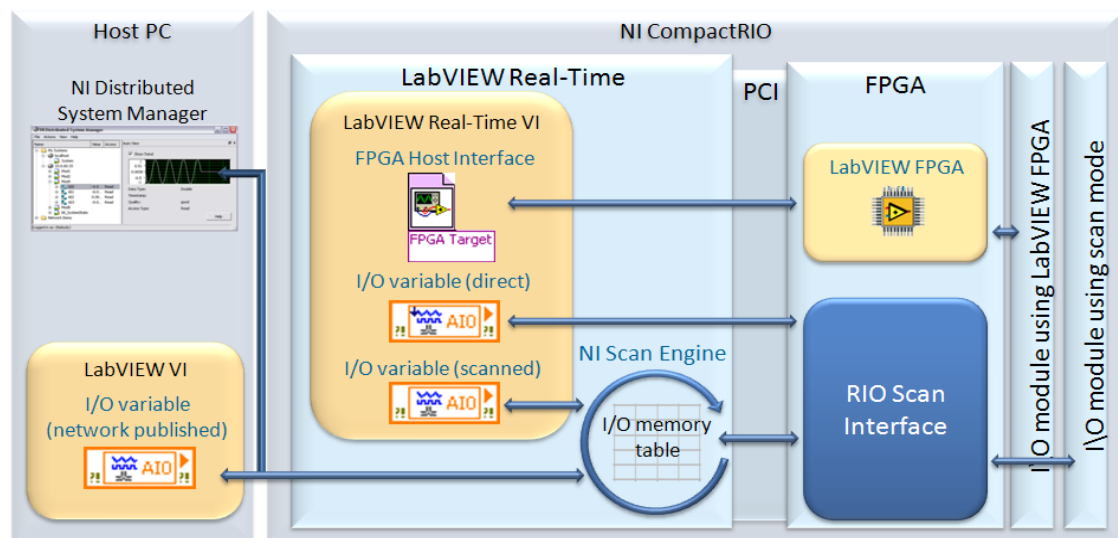

Figure 5. Labvies Scan mode and FPGA mode communication methods.[4]

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[4] NI tutorial image; *http://www.ni.com/white-paper/7338/es/#toc5*

6 Scan mode DC current SCADA system for the whole grid

6.1 VSC-MHVDC interest indicators and controls

The following tables show the control and indicators implemented on The Scan mode an FPGA mode application.

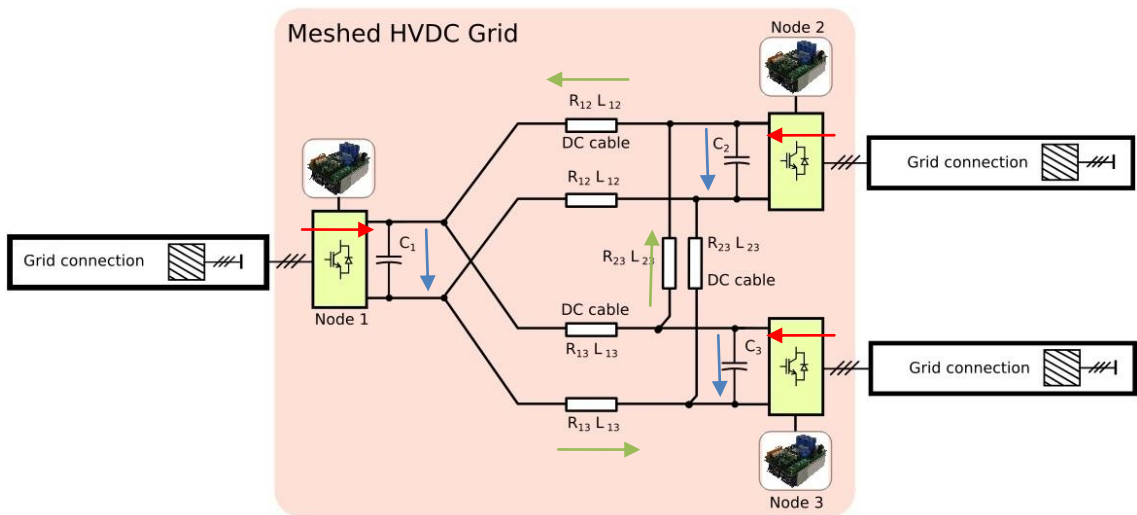The figure below portraits the DC grid and VSC terminal nodes and shows the measured signals.

Figure 6. Meshed HVDC grid and its measurements.

Indicator	Glossary	Units	Indicator type	Figure 5 legend
VSC DC voltage	*Edc1, Edc2, Edc3*	V	Waveform graph	Blue arrows
VSC DC current	*Idc1, Idc2, Idc3*	A	Waveform graph	Red arrows
VSC DC Power	*Pdc1, Pdc2, Pdc3*	W	Waveform graph	-
DC Line current	*Idc21, Idc13, Idc32*	A	Waveform graph	Green arrows
Number of iterations	*Iteration*	[u]	Single value	-
Recording state	*Recording*	-	Boolean	-
Control	***Glossary***	**Units**	**Control type**	
Stop application	*Stop*	-	Boolean	-
Start/Stop recording	*Recording*	-	Boolean	-

Table 2. Scan mode DC current SCADA system indicators and controls

6.2 Data logging

The data logging application must ensure to attain a lossless, uninterrupted, and accurately timed data stream from the grids electrical signals and the signals generated by the wind turbine emulator.

6.3 Post processing and monitoring

The screen must show a stable image of the waveform that can be attained by performing periodical sweeping, and refresh fast enough to be able to monitor the signal changes without lag. There is a minimum scan period restricted to 20ms by the loop execution and the network variables maximum actualization rate of 100 Hz.

Led indicators must respond fast enough to allow a control response on time.

6.3.A Shared variables with RT FIFO configuration

The Scan mode application shares information between parallel loops and tasks to optimise the execution rate. The data communication is preformed through the scan engine and scan interface, the variables are defined

The Scan mode allows to implement applications that require synchronous actualizations of I/O and internal communication variables at a maximum rate of 1 kHz. It does not perform with the most optimum resource use, such as FPGA programming would allow, but the interface is intuitive and facilitates a lot the access to the I/O ports and its treatment avoiding the kind of errors derived of bad synchronization between applications tasks, as seen further on when programming the FPGA. On the other hand, it is quiet restricted compared to FPGA programming.

6.3.B Error treatment and warning system

The application must stop in case of an error sprouting in any of the involved tasks, since the data stream must be ensured to be uninterrupted. The employed tool blocks generate error information which must be transmitted between blocks and iterations following the established data flow, at the end of every important subset the Boolean error status is read and its logic transmitted to the stop function that will halt the application if necessary.

6.4 SCADA application structure and performing

The data visualization interface consists on a tab structure to easily access the measurements at the different VSC and a start and stop control
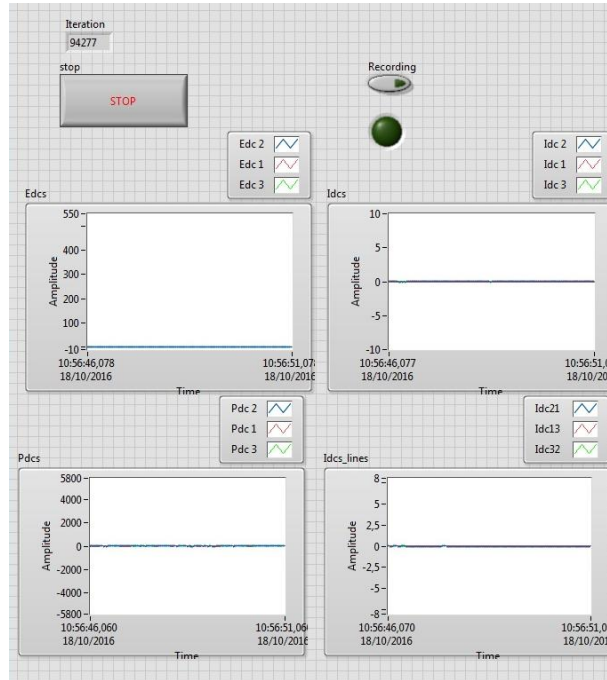

Figure 7. DC SCADA system user interface.

This SCADA system is composed of a PC VI where logging takes places and a cRIO VI where acquisition and electrical measurements and display take place in two independent loops

Amongst the different structures that could be implemented with graphical code it has been chosen a flat structure, which sequentially runs the program initializations, executing and closing frames. In the execution frame two parallel loops run with different priorities to optimise the execution time.

The first loop rate is synchronized with the data acquisition rate and is the highest priority loop. It only includes the calculation of the necessary deducted measures for control and supervision. This way it is ensured that the acquired and calculated data and control response is the most recent and faster to obtain.

The second loop includes the post processing, such as visualization and logging of the different acquired and calculated data, it is a lower priority loop with lower execution rate.

The communication between loops and tasks is performed through network or local variables, whose refreshing time is configured to be the same and has a predefined maximum (10 ms and 1 ms respectively). They can be associated to physical I/O and employ FIFOs which store elements in arrival order and then provides access to them using the first-in, first-out protocol.

The correct operation of the acquisition system has been tested on the VSC-MHVDC grid platform. There was no problem when applying low frequency voltages, but at the desired 50 Hz frequency, the amplitude and frequency variations on the visualization screen were lagged due to an insufficient refreshment rate.

In conclusion, it can be used to track DC signals but not AC ones. Additionally, since the acquisition module has to be configured on either the real-time scan mode system or the FPGA target, it cannot be used simultaneously with the later on developed FPGA acquisition VI, that solves the AC monitoring problem.

7 FPGA mode AC current SCADA system for a converter

7.1 Interest indicators and controls

Grid indicator	Glossary	Units	Indicator type
VSC DC voltage	Edc1, Edc2, Edc3	V	Waveform graph
VSC DC current	Idc1, Idc2, Idc3	A	Waveform graph
VSC three-phase phase to neutral voltages	Van, Vbn, Vcn	V	Waveform graph
VSC three-phase currents	Ia, Ib, Ic	A	Waveform graph
VSC AC power	P_{AC}	W	Waveform graph
Edc average	Edc average	V	Single value
Idc average	Idc average	A	Single value
Pdc average	Pdc average	W	Single value
I_{AC} signals RMS	Ia RMS, Ib RMS, Ic RMS	A	Single value
V_{AC} signals RMS	Van RMS, Vbn RMS, Vcn RMS	V	Single value
I_{AC} and V_{AC} signals frequency	f Ia, f Ib, f Ic, f Van, f Vbn, f Vcn	Hz	Single value
Application indicator	**Glossary**	**Units**	**Indicator type**
Host scan period	Tloop	ms	Chart graph
Sampling rate	Ts	us	Chart graph
Scanned samples array size	Size(s)		Single value
Error	error out	-	Boolean status Error code Description text
FIFO indicator	**Glossary**	**Units**	**Indicator type**
Buffer overflow	Buffer overflow	-	Boolean
Timed out	Timed out	-	Boolean
Underflow	Underflow	-	Boolean
Elements remaining to be read	Elements remaining	[u]	Single value
Number of elements to write	Number of elements to write	[u]	Single Value

Table 3. FPGA mode DC and AC current SCADA system indicators and controls

7.2 Sampling and minimum time between conversions

For the sampling to be valid it must, according to Shannon theorem, the sampling rate must be at less the double of the oscillation period.

$$Ts \leq 2 \cdot Tgrid$$

[1]

In this case the system is designed to sample a 50 Hz grid, thus the minimum sampling rate is of 100 Hz (Ts=0.01s). The sampling period has been decided to be of 700 us.

Thanks to the deterministic FPGA clock, we can ensure that all

Every chassis reads six signal measurements, samples and stores them in a FIFO from the FPGA side, so the PC host or controller host program can request and read the data arrays to processes higher amounts of data at a lower rate without data loss and ensuring a deterministic timing of the data sampling.

7.3 Multi-rate tasks communication

7.3.A FIFO configuration and management

Steps to set the right buffer size:

- Configure FIFO data structure with just the necessary precision bits.
- Set right size buffer depth: too small overflow, too large waste of resources
- Scanning rate underflow and timeout if attempting to read more values than available
- Prevent stale data from accumulating.

There are two methods to calculate the number of elements requested by the host each iteration:

$$Requested\ elements = WaitTimer\ Value * Ts * decimating\ factor$$

- Constant value

$$Requested\ elements = Elements\ remaining - Remainder\left\{\frac{Elements\ remaining}{decimating\ factor}\right\}$$

- Non constant value
- More robust

The second method was chosen since it can respond better to possible host lags and easily attains FPGA and host coordination

7.3.A1 Data interleaving and array decimation

It must be considered that in this application there is data interleaving to transfer six signals through a single FIFO. Since the data arrays read from the host will be decimated it is important that every iteration the host request a number of samples multiple of the decimating factor (which is six in this case)

7.3.A2 Timing and synchronization

The synchronisation is correct and the host can be requested to access more or less samples per host scan iteration, whilst the number of samples is not bigger that the buffer size.

The host cannot scan a single oscillation, it requires a minimum of 40 ms (two oscillations) to execute.

7.4 FPGA application scheme

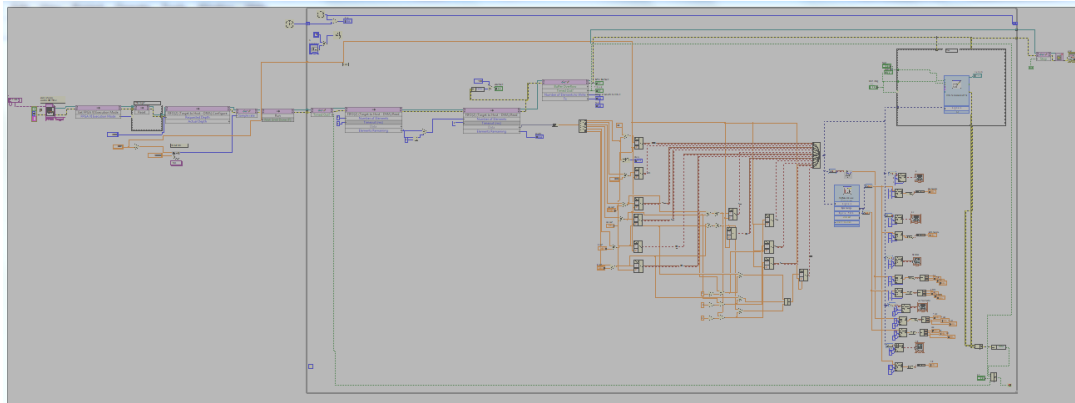This SCADA applications is composed of the PC visualization terminal, a FPGA acquisition VI and a cRIO processing VI.
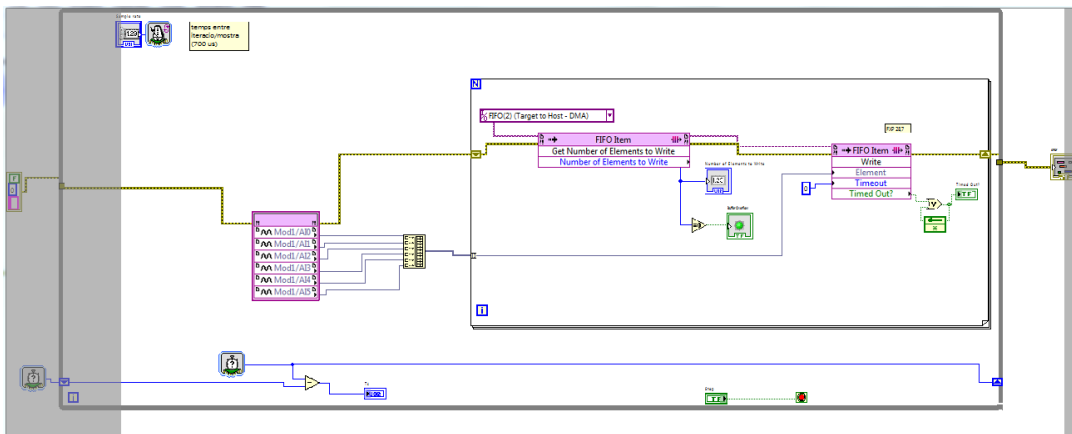

Figure 8. cRIO host VI.

Figure 9. FPGA acquisition VI.

8 Wind turbine emulator

This emulator was designed on first term as a complement to get acquainted with the program. It allows to recreate and visualize a step or ramp wind signal, define its maximum speed and duration and choose de turbine parameters. Running the simulation, it returns the mechanical power obtained at the engine shaft and, disregarding the transmission gears and converter losses, it provides the electrical power a wind turbine would provide to the grid under different wind conditions.
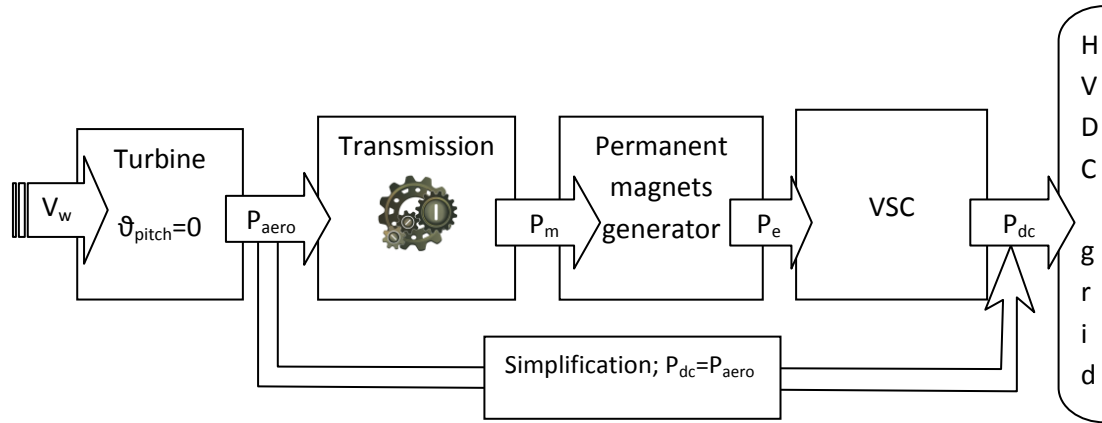
Figure 10. Wind turbine model

Thus, the VSC can be used to emulate dc power injection by a wind turbine, this signal is sent to an analogical output module which generates a ±10 V signal taht is sent to the VSC control board. There is no implemented pitch control and the pitch angle ϑ_{pitch} is maintained at zero.

8.1 Turbine model and employed parameters

The mechanical power collected by the turbine *Pt* can be expressed as the wind power flowing through the blades area *Pv* multiplied to an dimensionless coefficient called power coefficient *Cp*. Obtaining the following expression:

$$P_t = C_p P_v = \frac{1}{2} C_p \rho A v_v^3$$

(2)

ρ air densisty

A blades delimited area

v_v average wind speed

The *Cp* can be interpreted as the turbine aerodynamic efficiency. It depends on turbine characteristics, wind velocity, rotation speed and pitch angle. The 0.593 maximum value is

known as Betz limit. It is common to make use of the following expressions [3] depending on the turbine characteristics parameters:

$$Cp(\lambda, \vartheta) = c_1 \left(c_2 \frac{1}{\Lambda} - c_3 \vartheta - c4\vartheta^{c_5} - c_6 \right) e^{-c_7 \frac{1}{\Lambda}} \tag{3}$$

$$\frac{1}{\Lambda} = \frac{1}{\lambda + c_8 \vartheta} - \frac{c_9}{1 + \vartheta_3} \tag{4}$$

When the Cp is to reach negative values it is considered it saturates and a zero value is imposed.

The Tip-speed ratio λ parameter is defined as the relation between the turbine rotation speed and the average wind speed.

$$\lambda = \frac{w_t R}{v_v} \tag{5}$$

8.1.A Maximum power extraction algorithm

The simulation imitates a constant Tip-speed ratio PM generator control, which works on the premise that for a specific wind speed and pitch angle exists a rotation speed regim that maximises the power extraction. An optimum λ_{opt} is determined from de derivate of Cp as a function of λ. For a null pitch angle we obtain:

$$\lambda_{opt} = \frac{c_2 c_7}{c_2 c_7 c_9 + c_6 c_7 + c_2} \tag{6}$$

Then the optimum Tip-speed ratio is substituted on the Cp expression and we obtain the Cp_{opt} to calculate the power extracted in optimum operation.

$$Cp_{opt} = \frac{c_1 c_2 e^{-\frac{c_6 c_7 + c_2}{c_2}}}{c_7} \tag{7}$$

The turbine base power is 5.3 MW and saturates when reaching this value. In the following table the employed turbine and PMG parameters are indicated.

Parameters	Notation	Numeric value	Units
Blades radius	R	58	[m]
Air density	ρ	1.18	[kg/m³]
Nominal speed	w_{nom}	14.8	[min⁻¹]
Pitch angle	ϑ	0	[°]
Adjusting coefficient 1	c1	0.5	
Adjusting coefficient 2	c2	116	
Adjusting coefficient 3	c3	0.4	

Parameters	Notation	Numeric value	
Adjusting coefficient 4	c4	0	
Adjusting coefficient 5	c5	0	
Adjusting coefficient 6	c6	5	
Adjusting coefficient 7	c7	21	
Adjusting coefficient 8	c8	0.08	
Adjusting coefficient 9	c9	0.035	

Table 4. Wind turbine parameters

Parameters	Notation	Numeric value	Units
Base power	Pnom	5.3	[MW]

Table 5. PMG parameters

The screen caption below shows the user interface.
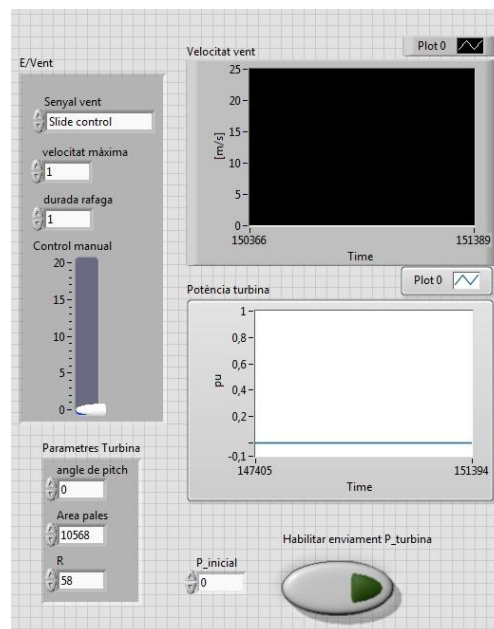
Figure 11. Wind turbine emulator user interface

The employed Labview environment is the most simple, the synchronising clock is that of the PC. The employed turbine model and parameters were drawn from the project referenced at the bibliography. The program is organized in substructures to facilitate the interpretation.

The following captures (Figure 12, Figure 13 and Figure 14) show the simulation program.
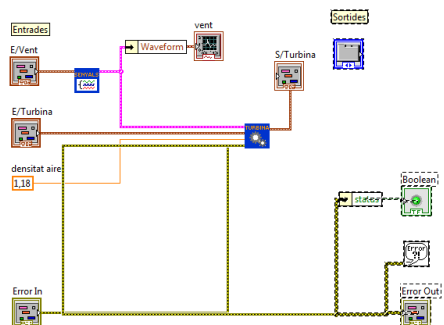
Figure 12. *Aerogenerator VI*

Figure 14. *Turbina* **subVI**
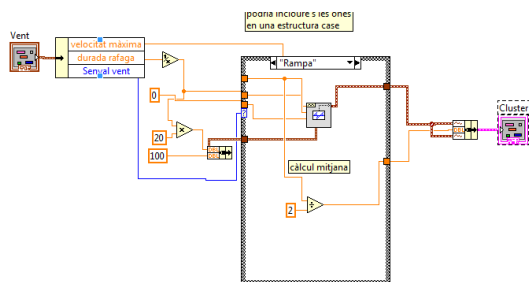
Figure 13. **Wind signal SubVI**
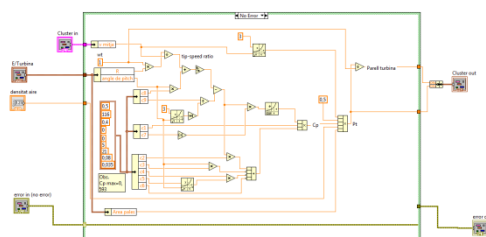
9 SCADA systems testing.

To ensure the SCADA applications functionality testing with the M-HVDC grid platform were performed.

9.1 VSC control scheme

To control the injected power distribution through the DC grid, a voltage droop control that was already implemented on the controllers (Figure 15) was applied to each VSC terminal.

Said control calculates the power flow through the converter proportionally to the $E_{DC}*$ error, being the proportionality constant K_d or constant drop.

$$P_{DC} = K_d(E_{DC} - E_{DC} *)$$ [8]

Additionally a power supply consign can be applied to further control power injection. Finally the necessary current flow is calculated through a PI. The converters control is based on classic vector control [7].

As a result, one of the VSC acts as the grid power supplier and the other two balance its distribution depending on their droop constant.
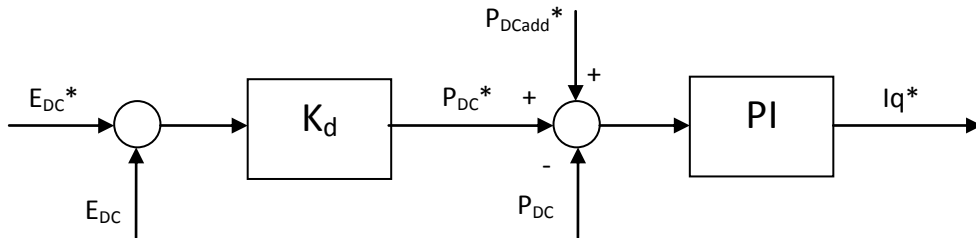
Figure 15. Voltage dropp control

Drop control advantages are the shared power balance and resources distribution and the preservation of the DC grid voltage in case of one of the converters being disconnected. On the other hand, unlike voltage and power controls, there is always a little voltage and power error.

9.2 Scan mode DC current SCADA system and turbine emulator

After setting the converters to 500 V and the voltage droop control, the turbine emulator (tied to the 2nd VSC) was employed to generate wind signals power injection response and the DC SCADA system to monitor the DC grid response. The Figure 16 shows the two user interfaces.

A ramp and step wind speed signals were generated, and the turbine power, equal to the VSC2 power injection is coherent to what would be expected of the configured turbine and DC system response (Figure 19 and Figure 22) adjust to a drop control type we can conclude that the emulator and SCADA work correctly.
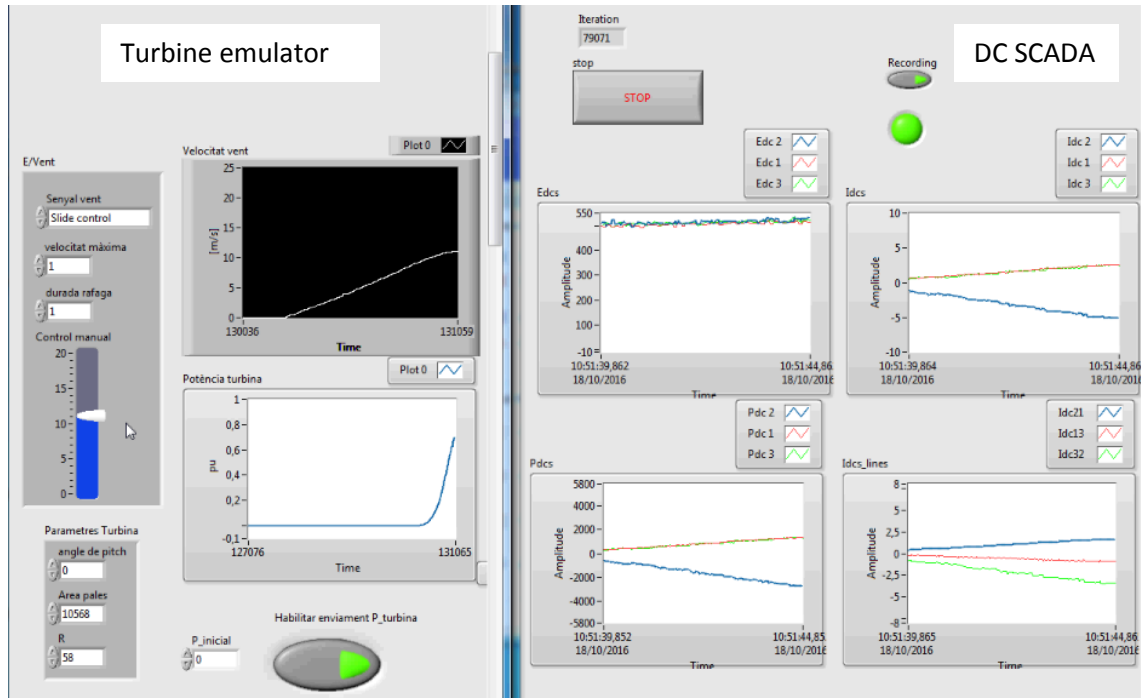

Figure 16. Turbine emulator and DC SCADA user interfaces.

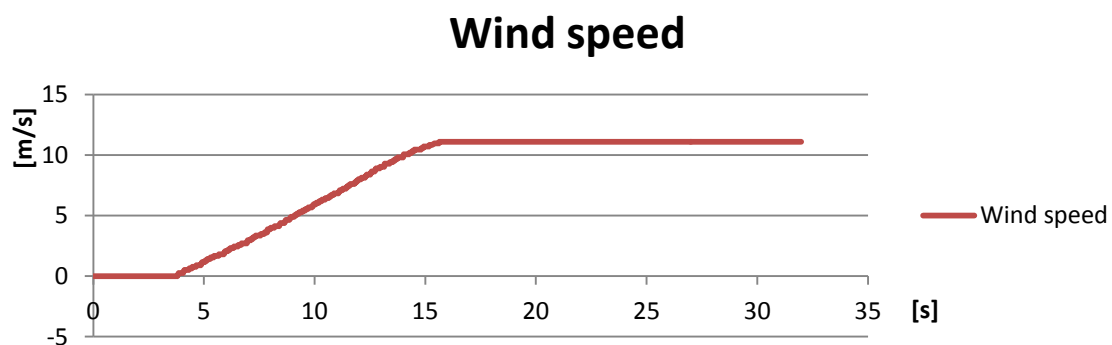System response to a ramp wind signal (Figure 13) is portrayed on the graphics on Figure 19:

- Wind speed signal and rotor speed.

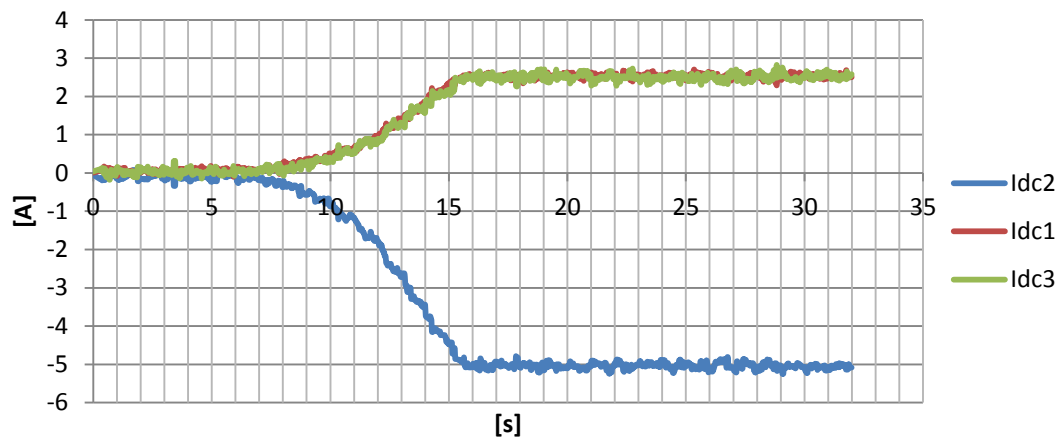Figure 17. Wind speed ramp control signal.

Rotational speed wt
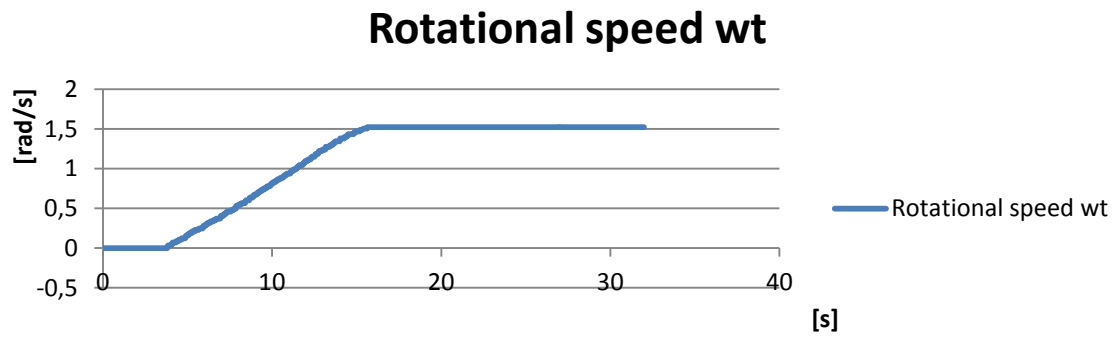
Figure 18. Wind turbine emulator response to a ramp wind signal.
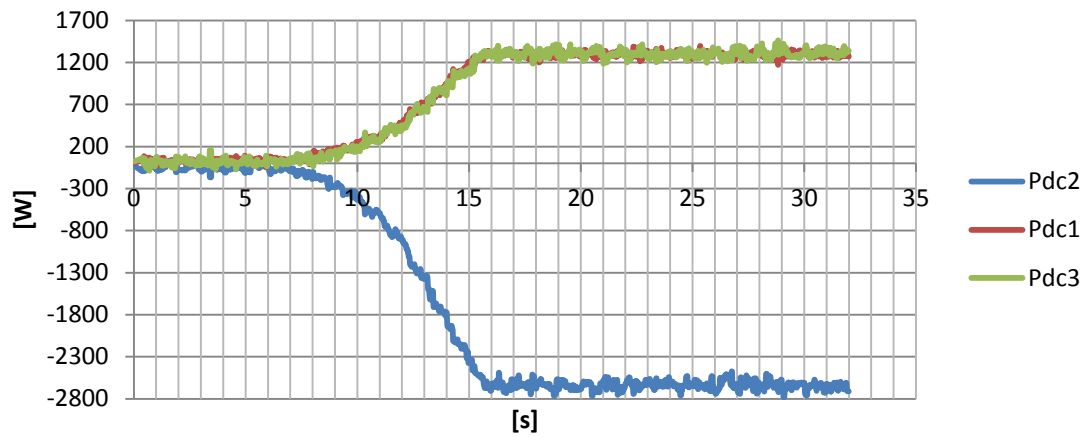
- Edc voltage averaged every 30 samples.
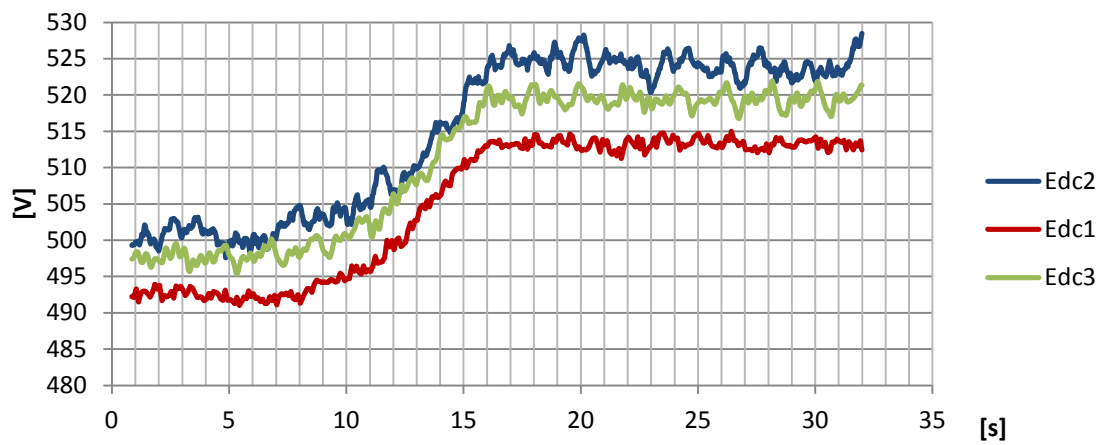
- Current injected from DC to AC side.

- Power injection from DC to AC side.
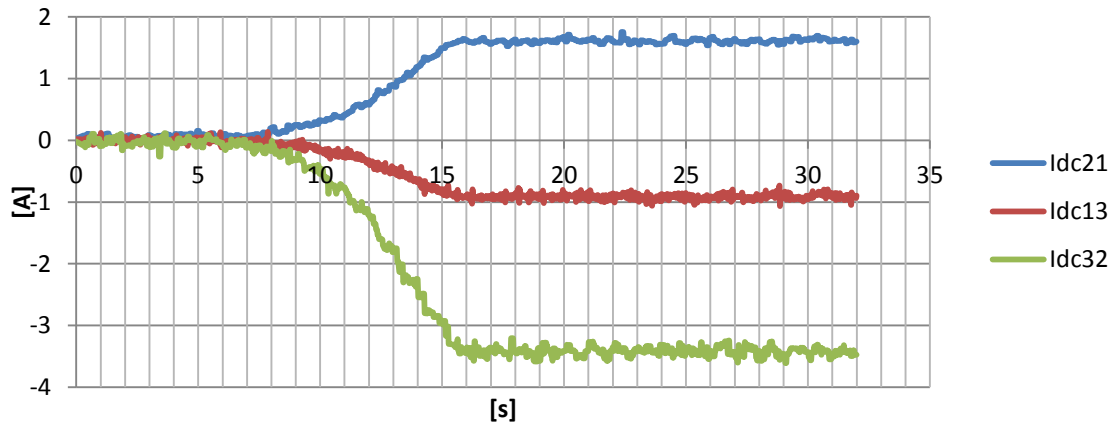

- Line currents. [A]/[s]

Figure 19. DC system response measurements to a wind speed ramp control signal.

System response to a wind speed step signal (Figure 20) is shown in Figure 22.

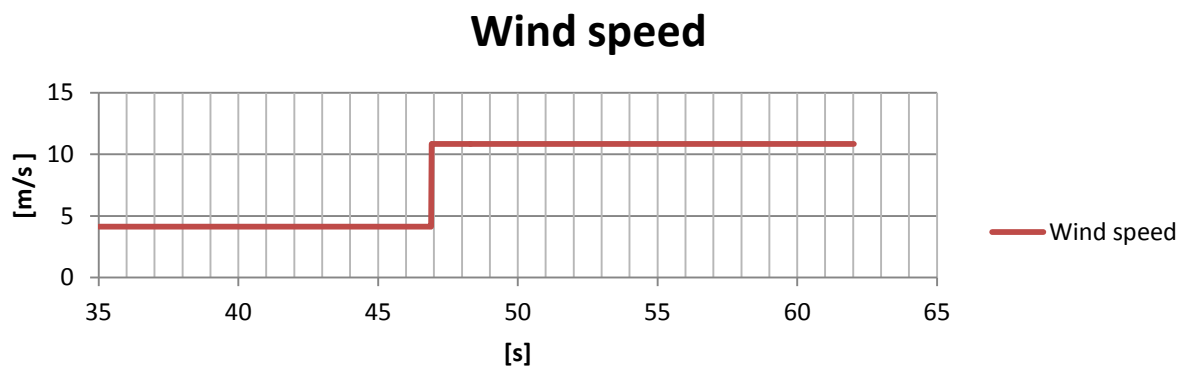- Wind speed step signal and rotor speed. time scale axis in seconds.

Wind speed

Figure 20. Wind speed step control signal.
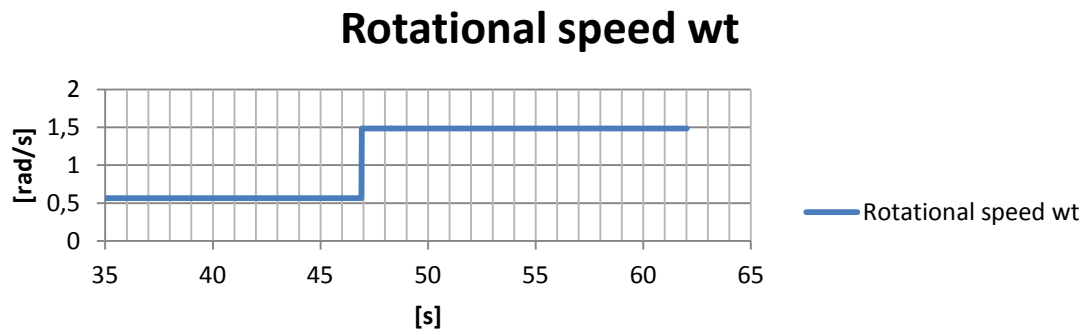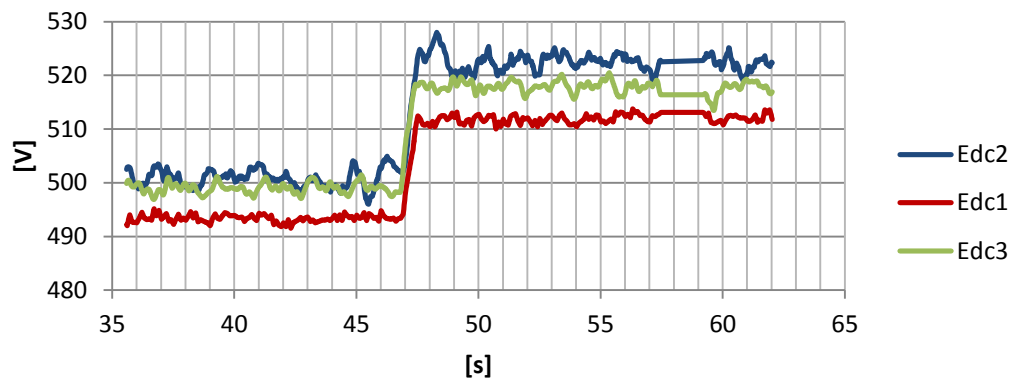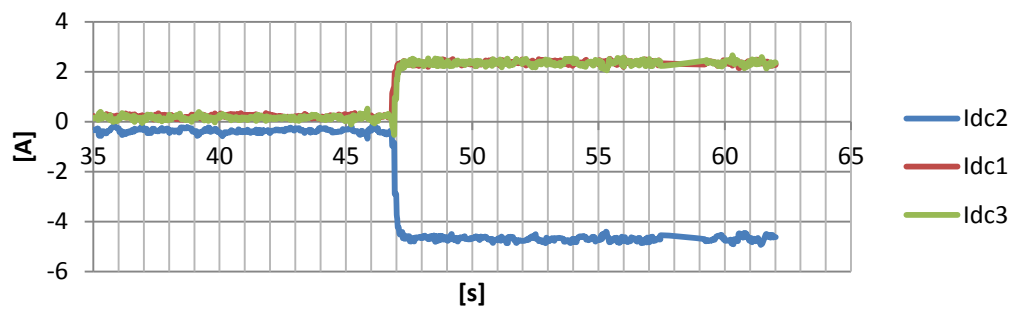
Rotational speed wt

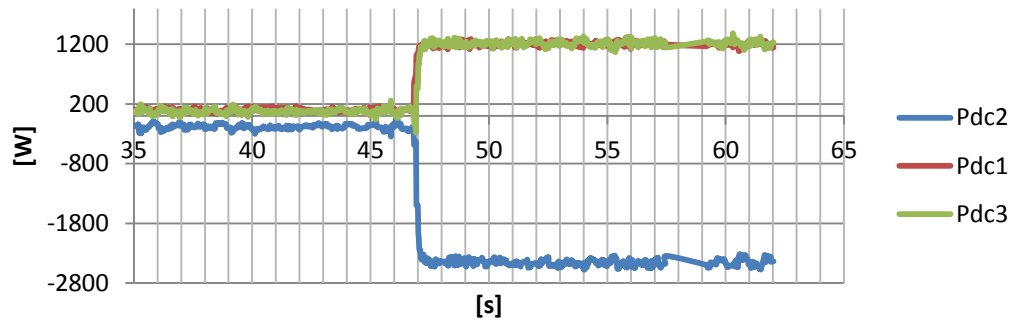**Figure 21. Wind turbine emulator response.**

- Edc voltage averaged every 30 samples

- Current injected from DC to AC side.

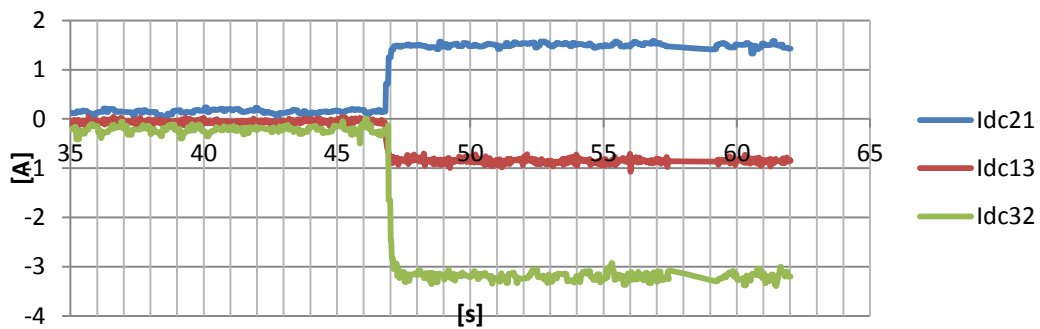- Power injection from DC to AC side.

- Line currents.

Figure 22. DC system response to a wind speed step control signal.

9.3 FPGA mode AC current SCADA system

In this case the whole grid is in operation but only the second cabinet VSC response has been monitored, directly requesting to its control to inject three different active power values: 2000, 350 and 5000 W. The screen visualization is uninterrupted and without noticeable lags.

The FIFO indicators stay off, there is no overflow of data, thus the acquired data stream is continuous and could be transferred to a logging task.
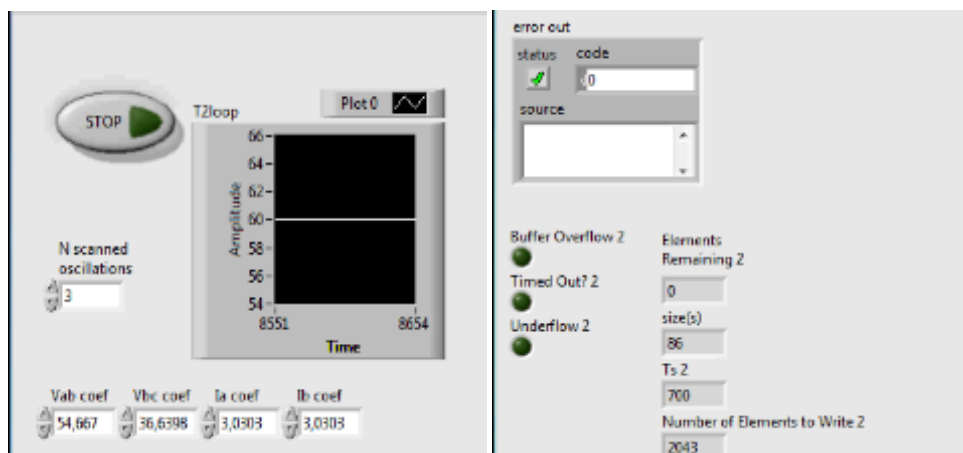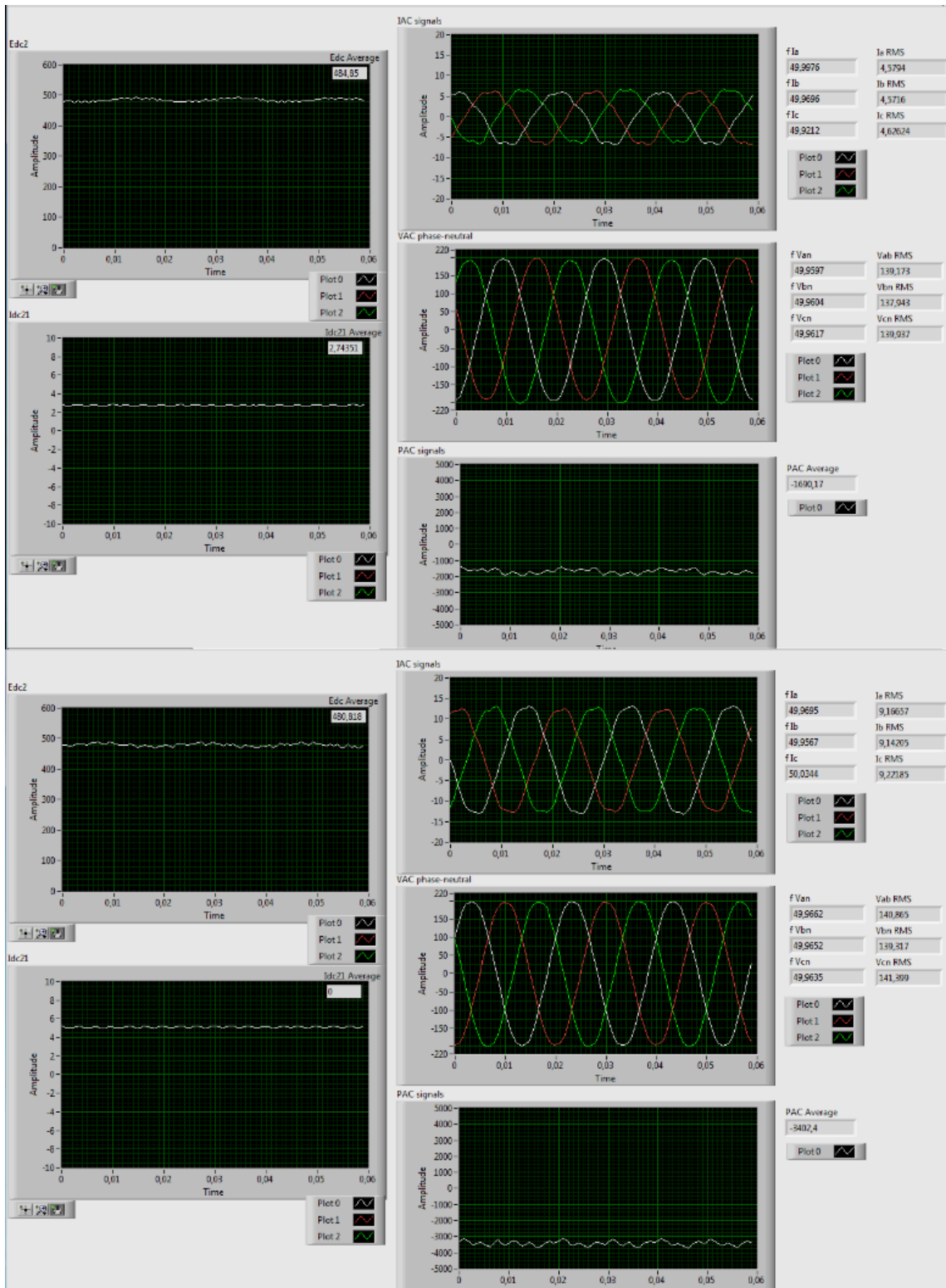

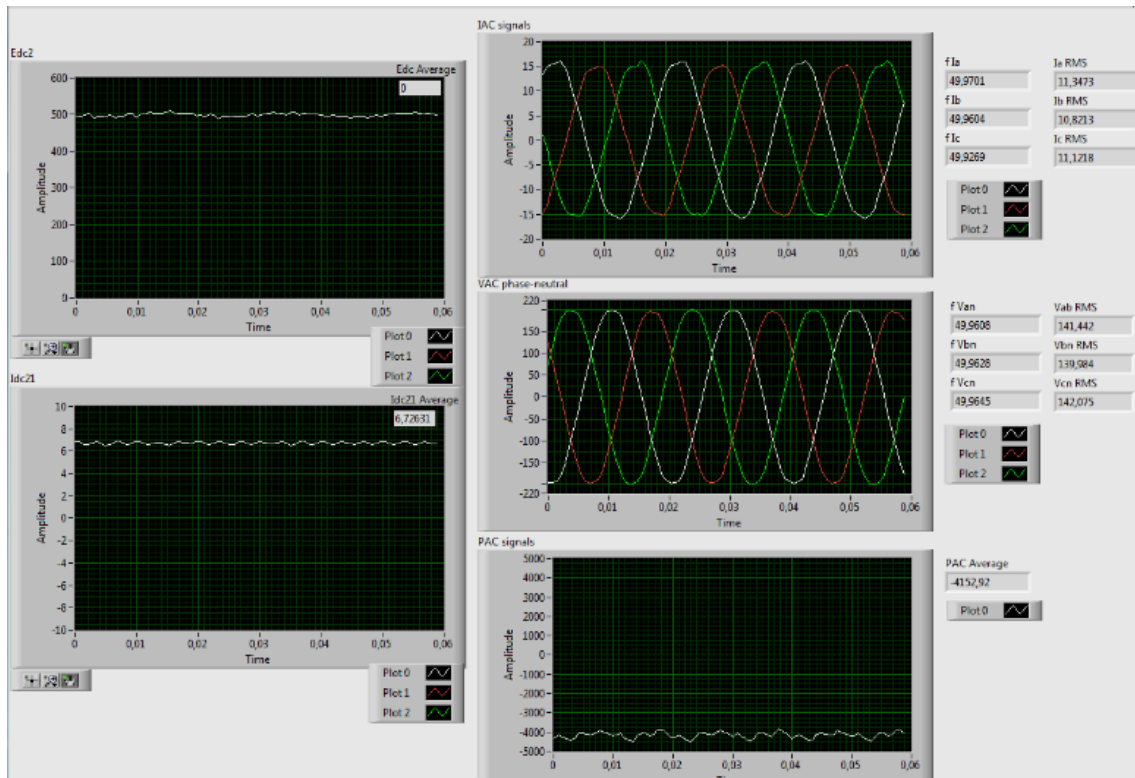**Figure 23. User control (left) and error interface (right)**

Figure 24. Monitoring screen response to a 2000, 3500 and 5000 W power injection request from the 2nd VSC.

Conclusions

In this project, two SCADA applications have implemented in LabVIEW and tested in a meshed multi-terminal VSC-HVDC grid scaled platform. One of them, employing LabVIEW Scan engine and Interface to access the FPGA, monitor and log data from the whole grid DC signals and the other, employing LabVIEW FPGA programming access to monitor one of the converters DC and AC signals when the whole grid is also operating.

A wind turbine emulator was also implemented and tested on one of the converters whilst evaluating the Scan mode SCADA application.

The applications behaviour was as expected the sampling correctly timed ensuring a lossless data stream acquisition.

Further work would be directed to the whole grid AC signals monitoring. Since the access mode is different hey cannot function together. With further work time, to solve the FPGA reference conflict an application that executed the host scanning loop access to the FPGA targets sequentially instead of parallel access could be tested. Once solved the conflict, the DC

monitoring could be merged and function together. Secondly, additional FIFO communication would have been implemented between the cRIO hosted FPGA application to with the PC host, which would allow AC data logging.

Agraïments

Per tota la paciència i alegria, gràcies. A la meva família, amics i al Joan i la resta de companys d'equip.

A. Budget

For the budget three main budget lines have been considered: the hardware, software and human resources budgets. The necessary items cost to develop the project has been accounted.

The project has had an approximate duration of six month, so the amortization has been considered during this period for the human resources, on the other hand, the hardware and software amortization time is considered of five years. The interest rates considered are 4% annual rate and 2% monthly rate.

NI academic price discounts are applied on the unit cost.

Hardware budget

Concept	Unit cost [€]	Units	Amortized cost [€]
NI cRIO-9113	651.9	1	583.46
NI 9205	738.90	3	1 983.97
cRIO-9204	1 325.10	1	1 185.98
NI 9146	638.10	2	1 142.21
Total cost [€]			**4 895.62 €**

Table 6. Hardware budget

Software Budget

Concept	Unit cost [€]	Units	Amortized cost [€]
NI LabVIEW Professional	1 423	1	1 273.6
Total cost [€]			**1 273.6 €**

Table 7. Software budget

Human resources budget

Concept	Monthly cost [€]	Time weighing	6 months cost [€]
Study and design	1 800	0.4	4 320
Programming and installation setting	1 800	0.4	4 320
Testing	1 700	0.15	1 530
Drafting	1 500	0.05	450
Total cost [€]			**10 620 €**

Table 8. Human resources budget

Total budget

In Table 9 all the lines budgets are added and the corresponding IVA is applied.

Concept	Cost [€]
Hardware	4 895.62
Software	1 273.6
Human resources	10 620
TOTAL	16 789.22
IVA (21%)	
TOTAL	**20 314.9562 €**

Table 9. Total budget with IVA

B Environmental impact

In this section the environmental impact of different elements related to a possible M-HVDC grid, an offshore wind farm and a HVDC submarine line, are analyzed. The analysis exposes the main problems aroused in the project development and precaution measurements to take into account [8].

B.1 Environmental impact of a offshore wind farm and HVDC submarine line.

B.1.2 Sea bed habitat loos or disturbance

On first term, The wind farm sea bed foundation for the wind turbine and platforms installation greatly affect the soil and the life in it.

Secondly, To install submarine HVDC lines, ditches must be dug in the sea bed. A boat with a towing a hook like tool used to withdraw the soil. Then, the cable is installed and the ditch covered with the same extracted soil.

Precaution measurements for Sea bed habitat loos or disturbance

- Analyse soil composition and present life and make an estimation of the damages in order to trace new distributions if there is risk of endangering local life.

B.1.3 Sea life disturbance

Mammals
The primary risk to marine mammals arises from underwater noise arising from construction activities, most notably pile-driving. The magnitude of such noise is likely to be great enough to cause disturbance, and in close proximity to the works even injury or death to individuals or populations of marine mammals.

Fish
Fish are especially vulnerable to loud noises. Risking deafnes or even death caused by ruptures of their swim bladers

Birds
The main risks for birds to be considered are: direct loss of habitat, displacement, collision risk or avoidance behaviour due to the wind farm installation.

Precaution measurementsfor sea life disturbance

- Assessment of use of the site and regional populations.

- Prediction of source noise level and temporal ranges.
- Monitoring the populations and their migration routes.

B.1.4 Human traffic disturbance

The placement of an elevated number of wind turbines can negatively alter both aerial an maritime navigation, changing traffic routes or even causing accidents in case of bad visibility.

The wind farm installation precludes fishing industry

Precaution measurements for Human activity traffic disturbance
- Previously study the local fishing industry and traffic routes context .
- Luminous signalization to prevent accidents.

B.1.5 Carbon footprint

The construction and installation and dismantling stages of wind farms an HVDC lines imply heavy machinery which can mean elevated carbon dioxide emissions.

On the other hand wind turbines operation does not produce CO_2 emission and can substitute power produced by coal plants.

It must also be considered reached given transmission distance, HVDC transmission implies lower power loss than AC . In this study [9] different transmission systems and distances power loss is compared and VSC HVDC becomes more efficient than HVAC when the transmission distance surpasses 150 km.

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