# Mismatch and Dynamic Modeling of Current Sources in Current-Steering CMOS D/A Converters: An Extended Design Procedure

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***Abstract*—This paper presents an improved modeling of the effect of random mismatch and current source transient switching behavior on the performance of current-steering CMOS digital-to-analog converters (DACs). The work considers two current source cell topologies, namely a simple cell and a cascoded cell, obtaining the relation of transistors design parameters to the static and dynamic models. On the one hand, a mismatching statistical analysis is applied to all the transistors of the current source circuit, which allows to define design expressions relating the circuit parameters to the DAC specifications without the need of arbitrary design margins or Monte Carlo simulations. On the other hand, improved analysis of the current source switching characteristics provides a more realistic modeling of the relation between transistors sizes and output current settling time. By including these two improved models into the usual design procedure, circuit sizing for optimum settling time and proper static behavior can be obtained analytically, reverting in smaller current source area, and, hence, in an overall DAC area reduction.**

***Index Terms*—CMOS integrated circuits, current-steering D/A converters, digital–analog conversion, matching, mixed analog–digital integrated circuits, transient analysis.**

## I. Introduction

MODERN broad-band communication integrated circuits require as fundamental subcircuits digital-to-analog converters (DACs) exhibiting both high speed and high resolution [1]. Wide bit-count DACs working at sampling clock frequencies in the range of hundreds of megahertz will continue to be required, hence dictating Nyquist-rate data conversion, as for instance to convert digital bitstreams into continuous-time signals prior to up-conversion mixers preceding RF transmitters in wireless systems or to drive digital cable communications modems. The development of future mobile communication systems (including both third–generation (3G) terminals and basestations) as well as the prospective use of ubiquitous communication systems will continue the trust toward high-performance DAC conversion stages.

A CMOS current-steering DAC is the usual choice for this type of application since that topology best suits the aforementioned requirements. Fig. 1 shows a typical block diagram of an $n$-bit current-steering DAC. The input word is segmented into the $b$ least significant bits (LSBs) that switch a binary weighted array and the $m = n - b$ most significant bits (MSBs) that control the switching of a unary current source array. The $m$ input bits are thermometer decoded to individually switch each of the $2^m - 1$ unary sources. A dummy decoder is placed in the binary weighted input path to equalize the delay. A latch is placed just before the switch transistors of each current source to minimize timing errors. Latches and switches are grouped in a separated array placed between the decoders and the current source arrays in order to isolate these noisy digital circuits from the sensitive analog circuits that generate precise currents.

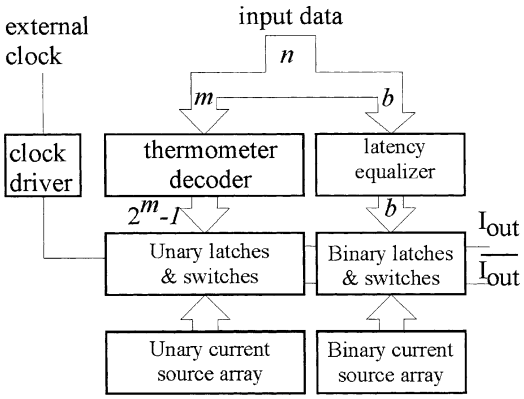


Fig. 1. Current-steering DAC architecture.

Since all current sources have the same circuit topology, only the sizes of their transistors are scaled from a basic current cell circuit (usually the LSB current source) according to their weights. Fig. 2 shows the two most usual topologies for the current source cell circuit. The basic circuit includes the current source transistor CS and two complementary switch transistors (SW and $\overline{\text{SW}}$), as shown in Fig. 2(a). Some cases require an additional cascode transistor (CAS) in series with the CS transistor to increase the cell output impedance and improve node isolation, as shown in Fig. 2(b). Bias voltages for transistors CS and CAS are common to all current sources. Complementary control signals for SW transistors of both current sources are generated by the corresponding latch and output driver circuits. The HIGH level of these signals is adjusted in such a way that the SW transistor in the ON state is actually operating as a first cascode transistor. If the CAS transistor is used, it operates as a second cascode transistor that further increases the output impedance of

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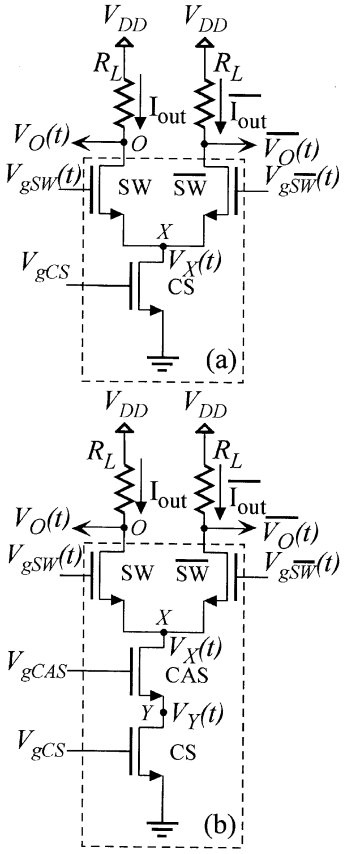


Fig. 2. Current source cell topologies. (a) Basic unary current source. (b) Cascoded unary current source.

the current source. This impedance boosting is needed in order to fulfil requirements for high-resolution high-bandwidth current-steering DACs [2].

DAC performance is specified both through static parameters, namely integral nonlinearity (INL), differential nonlinearity (DNL), and parametric yield, as well as dynamic parameters, namely glitch energy, settling time, and spurious-free dynamic range (SFDR) [3]. Static performance is mainly dominated by systematic and random mismatch errors. Systematic errors caused by process, temperature, and electrical slow variation gradients are almost cancelled by proper layout techniques [4]. Random errors are determined solely by random mismatch due to fast process variation gradients.

The design of a DAC is carried out at three levels: architecture design, circuit design, and physical design. In the usual design procedure, the degree of segmentation ($m$ over $n$) is decided at the architecture level by combining static and dynamic specifications and overall minimum area requirements [5]–[7]. Subsequently, the basic current cell circuit (usually the LSB current source) is designed by determining the sizes and bias voltages for the different transistors and the voltage levels required for the switches' control signals. Most of the DAC static and dynamic performance is determined by the performance of the basic current source cell. The circuit design of the rest of the components within the DAC architecture is mainly influenced by speed requirements. The digital binary-to-thermometer decoder must be fast enough so that the converter speed is solely limited by the current sources settling time. Latches should also be designed to be fast enough whilst their output driver should be sized to generate the desired levels for the switches' control signals, which are determined during the current cell circuit design procedure. The timing of these control signals is also of utmost relevance to minimize the glitches at the DAC output by avoiding both complementary SW transistors to be switched OFF simultaneously during the output transition [8]. Finally, special layout techniques [4], [9] are applied to floorplan the different DAC architecture components, especially the current source arrays, so as to compensate for systematic mismatch errors and isolate the sensitive analog section from the digital section.

This work focuses on the current cell design procedure. Two main contributions are presented. The first one, presented in Section II, is an extended modeling of random mismatch effects which considers statistical variations in all the transistors of the current source circuit and studies how they impinge upon the overall DAC static performance. The second contribution of the work, presented in Section III, addresses the dynamic modeling of current source switching transient behavior, extending the previous work of [11]. The model presented in this section allows us to properly describe the dynamic performance of the DAC and calculate a realistic settling time. In Section IV, those models are embedded within a complete design procedure for the optimum sizing of the current source cell of high-speed high-accuracy current-steering DACs. Finally, Section V provides the conclusions of the work.

## II. Static Performance

Static and dynamic performances of current-steering DACs are mostly determined by the current sources accuracy, noninfinite output impedance, and switching time. In the following, the dependencies of the DAC static performance on the current sources' accuracy and output impedance constrained by the transistors' operating region are presented. Afterwards, the implications of those static and statistical constraints in the sizing design procedure of the current cell circuit are presented and compared with other previously published approaches.

### A. Current Source Accuracy

The transistor CS of Fig. 2 sets the cell's current. Based on the statistical mismatch model of [12], a relation exists between the CS transistor area, its overdrive voltage, and its relative accuracy (we will refer in the following to the LSB current source)

$$\frac{\sigma_{I^2_{\rm LSB}}}{I^2_{\rm LSB}} = \frac{1}{2W_{\rm CS}L_{\rm CS}}\left(A^2_\beta + \frac{4A^2_{\rm VT}}{V^{\rm CS^2}_{\rm OD}}\right) \tag{1}$$

where $I_{\rm LSB}$ is the cell's current, $W_{\rm CS}$ and $L_{\rm CS}$ are the CS transistor width and length, respectively, $A_\beta$ and $A_{\rm VT}$ are mismatch process constants for the transistor large signal gain and threshold voltage, respectively, $V^{\rm CS}_{\rm OD}$ is the CS overdrive voltage, i.e., $(V_{\rm gs} - V_T)$, where $V_{\rm gs}$ is the CS gate-to-source voltage and $V_T$ is the threshold voltage, and $\sigma^2_{I_{\rm LSB}}$ is the variance of the current source value due to random mismatch.

The aspect ratio of the CS transistors is determined by the drain current and the overdrive voltage according to the MOSFET saturation drain current expression

$$I_{\mathrm{LSB}} = \frac{K'}{2} \cdot \frac{W_{\mathrm{CS}}}{L_{\mathrm{CS}}} \cdot V_{\mathrm{OD}}^{\mathrm{CS}^2}. \tag{2}$$

The CS transistor dimensions are univocally determined once the overdrive voltage is chosen and vice versa, according to (1) and (2). The INL of a set of theoretically equal manufactured DACs is a statistical process that depends on process variations. Systematic mismatch is addressed at the physical design phase. If only random mismatch is considered, the worst case INL, free of offset and gain errors, is found at the mid code in the DAC static transfer function. In this case, the INL error for an $N$-bit DAC is due to the combination of $2^N - 1$ LSB current sources (independently of the DAC segmentation[1]). The LSB current source minimum relative accuracy required to achieve a certain INL upper bound with a given statistical yield, as a function of the DAC resolution, is [10], [13]

$$\frac{\sigma_{I_{\mathrm{LSB}}^2}}{I_{\mathrm{LSB}}^2} < \frac{\mathrm{INL}_{\mathrm{upper\_bound}}}{\mathrm{inv\_normal}(0.5 + \frac{\mathrm{yield}}{2}) \cdot \sqrt{2^{\mathrm{N}-1}}} \tag{3}$$

where $\mathrm{inv-norm}$ is the inverse cumulative normal distribution, and $\mathrm{yield}$ is the percentage of manufactured DACs with an INL smaller or equal than the upper bound $\mathrm{INL}_{\mathrm{upper\_bound}}$.

### *B. Current Source Output Impedance*

The small-signal output impedance $R_{\mathrm{out}}$ for the $\mathrm{CS} + \mathrm{SW}$ current source topology of Fig. 2(a) is given by

$$R_{\mathrm{out}}^{\mathrm{SW+CS}} \approx g_{m\mathrm{SW}} \cdot r_{\mathrm{dsSW}} \cdot r_{\mathrm{dsCS}} \tag{4}$$

where $g_m$ is the small-signal transconductance and $r_{\mathrm{ds}}$ is the drain-to-source small-signal resistance. The labels $\mathrm{SW}$, $\mathrm{CS}$, and $\mathrm{CAS}$ are used here and in the rest of the paper as accompanying subscripts or superscripts to indicate the transistor to which the parameters, voltages, or other expressions refer.

For the $\mathrm{CS} + \mathrm{CAS} + \mathrm{SW}$ topology of Fig. 2(b), the output impedance is given by

$$R_{\mathrm{out}}^{\mathrm{casc}} \approx g_{m\mathrm{SW}} \cdot g_{m\mathrm{CAS}} \cdot r_{\mathrm{dsSW}} \cdot r_{\mathrm{dsCAS}} \cdot r_{\mathrm{dsCS}}. \tag{5}$$

Since the drain current is a value fixed by the DAC specifications, the only degree of freedom available to design the transconductances is either the overdrive voltage or the aspect ratio

$$g_m = \frac{2 \cdot I}{V_{\mathrm{OD}}} = \sqrt{2 \cdot I \cdot K' \cdot \left(\frac{W}{L}\right)}. \tag{6}$$

[1]This is due to the fact that a source of value $k$ LSBs is actually obtained by combining $k$ sources of LSB value in parallel, instead of a single source with transistors $k$ times wider than the LSB source transistors.

The drain-to-source impedance, considering channel length modulation, is expressed by

$$r_{\mathrm{ds}} = \frac{1}{\lambda \cdot I_{\mathrm{sat}}}, \text{ with } \lambda = \frac{K_{\mathrm{ds}}}{2 \cdot L \cdot \sqrt{V_{\mathrm{DS}} - V_{\mathrm{OD}} + \phi_o}} \tag{7}$$

where $\lambda$ is the channel length modulation parameter, $I_{\mathrm{sat}}$ the drain-to-source saturation current, $K_{\mathrm{ds}}$ is a technology constant [14], $V_{\mathrm{DS}}$ is the drain-to-source voltage, and $\phi_o$ is the built-in junction potential, which is also a technology constant.

Combining (4), (5), and (7) and expressing the drain-to-source voltages as function of node voltages (SW and CAS gate bias voltage, and the output node minimum voltage $V_o^{\min}$, which is the worst case for output impedance) yields

$$\begin{aligned} R_{\mathrm{out}}^{\mathrm{CS+SW}} = {} & g_{m\mathrm{SW}} \frac{4 L_{\mathrm{CS}} L_{\mathrm{SW}}}{K_{\mathrm{ds}}^2 I_{\mathrm{sat}}^2} \\ & \cdot \sqrt{V_{g\mathrm{SW}} - (V_{\mathrm{OD}}^{\mathrm{SW}} + V_T^{\mathrm{SW}}) - V_{\mathrm{OD}}^{\mathrm{CS}} + \phi_o} \\ & \cdot \sqrt{V_o^{\min} - (V_{g\mathrm{SW}} - V_T^{\mathrm{SW}}) + \phi_o} \end{aligned} \tag{8}$$

for the $\mathrm{CS} + \mathrm{SW}$ topology and

$$\begin{aligned} R_{\mathrm{out}}^{\mathrm{casc}} = {} & g_{m\mathrm{SW}} g_{m\mathrm{CAS}} \frac{8 L_{\mathrm{CS}} L_{\mathrm{CAS}} L_{\mathrm{SW}}}{K_{\mathrm{ds}}^3 I_{sat}^3} \\ & \cdot \sqrt{V_{g\mathrm{CAS}} - (V_{\mathrm{OD}}^{\mathrm{CAS}} + V_T^{\mathrm{CAS}}) - V_{\mathrm{OD}}^{\mathrm{CS}} + \phi_o} \\ & \cdot \sqrt{V_{g\mathrm{SW}} - (V_{\mathrm{OD}}^{\mathrm{SW}} + V_T^{\mathrm{SW}}) - V_{g\mathrm{CAS}} + V_T^{\mathrm{CAS}} + \phi_o} \\ & \cdot \sqrt{V_o^{\min} - (V_{g\mathrm{SW}} - V_T^{\mathrm{SW}}) + \phi_o} \end{aligned} \tag{9}$$

for the $\mathrm{CS} + \mathrm{CAS} + \mathrm{SW}$ topology.

The optimum SW and CAS gate bias voltages concerning the output impedance are found by differentiating (8) and (9) with respect to $V_{g\mathrm{SW}}$ and $V_{g\mathrm{CAS}}$. For the $\mathrm{CS}+\mathrm{SW}$ topology, the SW gate bias voltage that maximizes output impedance is found as

$$V_{g\mathrm{SW}}^{\mathrm{opt}} = V_T^{\mathrm{SW}} + \frac{1}{2}(V_o^{\min} + V_{\mathrm{OD}}^{\mathrm{CS}} + V_{\mathrm{OD}}^{\mathrm{SW}}) \tag{10}$$

whereas for the $\mathrm{CS} + \mathrm{CAS} + \mathrm{SW}$ topology the SW and CAS gate bias voltages that maximize output impedance are

$$\begin{aligned} V_{g\mathrm{CAS}}^{\mathrm{opt}} &= V_T^{\mathrm{CAS}} + \frac{1}{3}(V_o^{\min} + 2V_{\mathrm{OD}}^{\mathrm{CS}} + 2V_{\mathrm{OD}}^{\mathrm{CAS}} - V_{\mathrm{OD}}^{\mathrm{SW}}) \\ V_{g\mathrm{SW}}^{\mathrm{opt}} &= V_T^{\mathrm{SW}} + \frac{1}{3}(2V_o^{\min} + V_{\mathrm{OD}}^{\mathrm{CS}} + V_{\mathrm{OD}}^{\mathrm{CAS}} + V_{\mathrm{OD}}^{\mathrm{SW}}). \end{aligned} \tag{11}$$

### *C. Analysis of the Current Source Circuit Transistors Operating Region*

Despite the fact that the overdrive voltage $V_{\mathrm{OD}}^{\mathrm{CS}}$ in (1) should be maximized to minimize the CS area, it should be small enough to allow the other transistors (SW and CAS if present) to work in saturation (the region in which higher output impedance is obtained) in any situation.

*1) Simple Current Cell* $(\mathrm{CS+SW})$*:* Applying the MOSFET saturation condition $(V_{\mathrm{DS}} > V_{\mathrm{OD}} = V_{\mathrm{GS}} - V_T)$ to all transistors in the current source of Fig. 2(a) leads to the definition of a

voltage range in which the SW gate bias voltage must be kept in order to allow both CS and SW transistors to work in saturation

$$\underbrace{V_{\mathrm{OD}}^{\mathrm{CS}}+V_{\mathrm{OD}}^{\mathrm{SW}}+V_T^{SW}}_{V_{g\mathrm{SW}}^{\min}}<V_{g\mathrm{SW}}<\underbrace{V_o^{\max}+V_T^{\mathrm{SW}}}_{V_{g\mathrm{SW}}^{\min}}. \tag{12}$$

A solution exists for (12) if and only if the difference between the upper and lower bounds is positive (i.e., the lower bound for the SW gate voltage $(V_{g\mathrm{SW}}^{\min})$ is smaller than the upper bound $(V_{g\mathrm{SW}}^{\max})$. This determines an upper bound for the addition of the two transistors' overdrive voltages

$$V_{\mathrm{OD}}^{\mathrm{CS}}+V_{\mathrm{OD}}^{\mathrm{SW}}\leq V_o^{\min}. \tag{13}$$

Resuming the saturation constraint of (12), note that the midpoint between the upper and lower bounds for the SW gate bias voltage corresponds to the optimum voltage that maximizes the dc output impedance found in Section II-B

$$V_{g\mathrm{SW}}^{\mathrm{opt}}=\frac{V_{g\mathrm{SW}}^{\min}+V_{g\mathrm{SW}}^{\max}}{2}=V_T^{\mathrm{SW}}+\frac{1}{2}\left(V_o^{\min}+V_{\mathrm{OD}}^{\mathrm{CS}}+V_{\mathrm{OD}}^{\mathrm{SW}}\right). \tag{14}$$

This is not a coincidence, since this optimum SW gate voltage places the operating point of both SW and CS transistors at the same voltage *distance* from the triode region.

If there are no other criteria for choosing the overdrive voltages, such as dynamic output impedance, settling time, etc., it would be interesting to choose the combination of overdrive voltages that leads to the minimum area solution. This usually corresponds to an SW transistor with minimum length and width, from which the SW overdrive voltage is derived, and the maximum CS overdrive voltage that verifies (13), provided that the corresponding CS transistor width and length obtained from (1) and (2) satisfy the technology minimum size constraint. By doing this, the operating points of both transistors are found just at the limit between the triode and the saturation regions.

In the previously published current source sizing procedure [10], which is representative of the usual design process for this type of DAC, only the mismatch error of the current source transistor is considered. Hence, an arbitrary safety margin $\Delta V_{\mathrm{safe}}$ is introduced as follows in the saturation constraint (13) to prevent the transistors to enter triode region due to process variations:

$$V_{\mathrm{OD}}^{\mathrm{CS}}+V_{\mathrm{OD}}^{\mathrm{SW}}\leq V_o^{\min}-\Delta V_{\mathrm{safe}}. \tag{15}$$

If not only the mismatch errors of the CS transistor, but also the switches and additional cascode transistors mismatch errors are taken into account, the overall basic current cell circuit can be optimized without introducing that arbitrary safety margin. Alternatively, this safety margin can be found by performing parametric Monte Carlo simulations. The model that will be presented in the following avoids either the arbitrary design margin or the time-consuming Monte Carlo simulations.

In order to include the effects of process variations in the saturation condition of (12), the statistical variation of the two bounds for the SW gate bias voltage is modeled by means of a normal distribution. The variance of the upper and lower bounds is found, first by expressing these bounds as a function of the random variables of the circuit that appear when mismatching effects are taking into account:

$$V_{g\mathrm{SW}}^{\max}=\underbrace{V_{DD}-(2^N-1)\cdot I_{\mathrm{LSB}}\cdot R_L}_{V_o^{\min}}+V_T^{\mathrm{SW}}$$

$$V_{g\mathrm{SW}}^{\min}=\underbrace{V_{g\mathrm{CS}}-V_T^{\mathrm{CS}}}_{V_{\mathrm{OD}}^{\mathrm{CS}}}+\underbrace{\sqrt{\frac{2\cdot I}{K'_{\mathrm{SW}}\cdot\left(\frac{W_{\mathrm{SW}}}{L_{\mathrm{SW}}}\right)}}}_{V_{\mathrm{OD}}^{\mathrm{SW}}}+V_T^{\mathrm{SW}} \tag{16}$$

and subsequently by calculating the partial derivatives of these expressions with respect to each one of the random variables (that are considered independent). In this way, the variance of the upper bound for the SW gate voltage that guarantees saturation when random mismatch effects are taken into account is found as

$$\begin{aligned}\sigma^2_{V_{g\mathrm{SW}}^{\max}}&\approx\left(\frac{\partial V_{g\mathrm{SW}}^{\max}}{\partial I}\right)\sigma_I^2+\left(\frac{\partial V_{g\mathrm{SW}}^{\max}}{\partial V_T^{\mathrm{SW}}}\right)\sigma^2_{V_T^{\mathrm{SW}}}\\&\quad+\left(\frac{\partial V_{g\mathrm{SW}}^{\max}}{\partial R_L}\right)\sigma^2_{R_L}\\&=\frac{A^2_{\mathrm{VT}}}{W_{\mathrm{SW}}L_{\mathrm{SW}}}+\Delta V_o^{\max^2}\left(\frac{\sigma_I^2}{I^2}+\frac{\sigma^2_{R_L}}{R_L}\right).\end{aligned} \tag{17}$$

Similarly, the variance of the lower bound yields

$$\begin{aligned}\sigma^2_{V_{g\mathrm{SW}}^{\min}}&\approx\frac{A^2_{\mathrm{VT}}}{W_{\mathrm{CS}}L_{\mathrm{CS}}}+\frac{A^2_{\mathrm{VT}}}{W_{\mathrm{SW}}L_{\mathrm{SW}}}\\&\quad+\frac{V_{\mathrm{OD}}^{\mathrm{SW}^2}}{4}\left(\frac{\sigma_I^2}{I^2}+\frac{A^2_\beta}{W_{\mathrm{SW}}L_{\mathrm{SW}}K'^2}\right).\end{aligned} \tag{18}$$

In (17) and (18), only node voltages (except biasing gate voltages), current values, and load impedance have been considered as being random variables affected by mismatching. In order to take into account also die-to-die process variations, the worst case process parameter values (min or max) should be used instead of the typical ones. In the case of $V_{g\mathrm{SW}}^{\max}$, the only parameter affected by die-to-die process variations is the SW threshold voltage ($V_o^{\min}$ is always the same assuming that the full-scale DAC output value is adjusted to eliminate offset and gain errors). Therefore, the minimum SW threshold voltage should be used. In the case of $V_{g\mathrm{SW}}^{\min}$, the variation of the SW and CS threshold voltage compensate for each other, as they appear in (16) with opposite sign. Therefore, only the die-to-die variation of the $K'_{\mathrm{SW}}$ affects the lower bound and the worst case is the minimum $K'_{\mathrm{SW}}$ value for that process.

To find an appropriate value for the SW gate voltage, the upper bound must be larger than the lower bound in a given percentage of the cases expressed by yield_SW. Fig. 3 illustrates this tradeoff. To accomplish that the saturation constraint is fulfilled with a given probability yield_SW, the optimum of the SW gate voltage found in (10), which is now the mean value of a random variable, has to verify that

$$\begin{aligned}&P\left(\left[V_{g\mathrm{SW}}^{\max}-\overline{V_{g\mathrm{SW}}^{\mathrm{opt}}}\right]>0\right)\geq\mathrm{yield\_SW}\ \text{and}\\&P\left(\left[\overline{V_{g\mathrm{SW}}^{\mathrm{opt}}}-V_{g\mathrm{SW}}^{\min}\right]>0\right)\geq\mathrm{yield\_SW}\end{aligned} \tag{19}$$

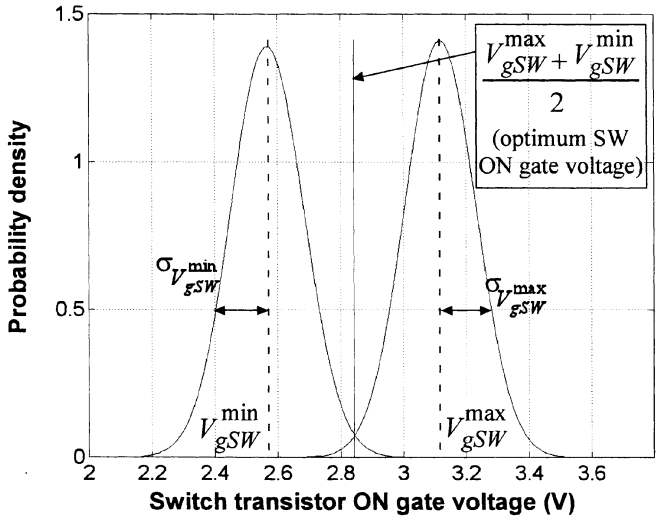


Fig. 3. Graphical representation of the constraint (19).

which can be expressed also by the following equation:

$$\frac{V_{g\mathrm{SW}}^{\max}-V_{g\mathrm{SW}}^{\min}}{2}\geq S\max\left[\sigma_{V_{g\mathrm{SW}}^{\max}},\sigma_{V_{g\mathrm{SW}}^{\min}}\right] \tag{20}$$

which is the same as

$$V_{\mathrm{OD}}^{\mathrm{CS}}+V_{\mathrm{OD}}^{\mathrm{SW}}\leq V_o^{\min}-2S\max\left[\sigma_{V_{g\mathrm{SW}}^{\max}},\sigma_{V_{g\mathrm{SW}}^{\min}}\right]. \tag{21}$$

Here, since only one half of the normal distribution has to be considered, $S=\mathrm{inv\_norm}(\mathrm{yield\_SW})$, where yield_SW is related to the previously defined INLyield by

$$\mathrm{yield}=\mathrm{yield\_SW}^4 \tag{22}$$

because the worst case of the bounds variance for the several current sources of the DAC is found in the LSB current source (since its area is the smallest of all the current sources), and its two complementary SW transistors must be inside both of the bounds with the same probability.

The expression of (21) represents a saturation constraint more realistically than (15) for the CS and SW current cell circuit, where an arbitrary safety margin was included. The safety margin appearing in (21) is not arbitrary nor needs to be found using parametric Monte Carlo simulation. It can be related to other circuit parameters and mismatch process parameters using (17) and (18), which enables us to include (21) in an analytical optimization process.

*2) Cascoded Current Cell* (CS+CAS+SW)*:* Applying the MOSFET saturation condition ($V_{\mathrm{DS}}>V_{\mathrm{OD}}=V_{\mathrm{GS}}-V_T$) to all transistors in the current source of Fig. 2(b) leads to the definition of two voltage ranges, one for the SW gate bias voltage, and another for the CAS gate bias voltage as shown in (23) at the bottom of the page.

The mid-points of the above voltage ranges also correspond to the optimum SW and CAS gate voltages, respectively, that maximize the current source output impedance found in Section II-B for this topology. Each range has two bounds, and these four bounds can also be expressed as a function of the random variables of the design when random mismatch errors are considered. The variance of the bounds can be estimated in the same way as that in Section II-C1. Using the same criteria as in the CS + SW topology case, we have

$$\begin{aligned}
\sigma^2_{V_{g\mathrm{SW}}^{\max}} &\approx \frac{A_{\mathrm{VT}}^2}{W_{\mathrm{SW}}L_{\mathrm{SW}}}+\Delta V_o^{\max^2}\left(\frac{\sigma_I^2}{I^2}+\frac{\sigma_{R_L}^2}{R_L}\right)\\
\sigma^2_{V_{g\mathrm{SW}}^{\min}} &\approx \frac{A_{\mathrm{VT}}^2}{W_{\mathrm{SW}}L_{\mathrm{SW}}}+\frac{A_{\mathrm{VT}}^2}{W_{\mathrm{CAS}}L_{\mathrm{CAS}}}+\frac{V_{\mathrm{OD}}^{\mathrm{SW}^2}}{4}\\
&\quad\times\left(\frac{\sigma_I^2}{I^2}+\frac{A_\beta^2}{W_{\mathrm{SW}}L_{\mathrm{SW}}K'^2}\right)\\
\sigma^2_{V_{g\mathrm{CAS}}^{\max}} &\approx \frac{A_{\mathrm{VT}}^2}{W_{\mathrm{SW}}L_{\mathrm{SW}}}+\frac{A_{\mathrm{VT}}^2}{W_{\mathrm{CAS}}L_{\mathrm{CAS}}}+\frac{V_{\mathrm{OD}}^{\mathrm{SW}^2}}{4}\\
&\quad\times\left(\frac{\sigma_I^2}{I^2}+\frac{A_\beta^2}{W_{\mathrm{SW}}L_{\mathrm{SW}}K'^2}\right)\\
\sigma^2_{V_{g\mathrm{CAS}}^{\min}} &\approx \frac{A_{\mathrm{VT}}^2}{W_{\mathrm{CS}}L_{\mathrm{CS}}}+\frac{A_{\mathrm{VT}}^2}{W_{\mathrm{CAS}}L_{\mathrm{CAS}}}+\frac{V_{\mathrm{OD}}^{\mathrm{CAS}^2}}{4}\\
&\quad\times\left(\frac{\sigma_I^2}{I^2}+\frac{A_\beta^2}{W_{\mathrm{CAS}}L_{\mathrm{CAS}}K'^2}\right)
\end{aligned} \tag{24}$$

which in this case of the CS + CAS + SW topology lead to two saturation conditions

$$\begin{aligned}
\frac{V_{g\mathrm{SW}}^{\max}-V_{g\mathrm{SW}}^{\min}}{2} &\geq S\max\left[\sigma_{V_{g\mathrm{SW}}^{\max}},\sigma_{V_{g\mathrm{SW}}^{\min}}\right]\\
\frac{V_{g\mathrm{CAS}}^{\max}-V_{g\mathrm{CAS}}^{\min}}{2} &\geq S\max\left[\sigma_{V_{g\mathrm{CAS}}^{\max}},\sigma_{V_{g\mathrm{CAS}}^{\min}}\right].
\end{aligned} \tag{25}$$

The equations in (25) are analytical expressions that depend on circuit and mismatch parameters. They will be used in the

$$\begin{aligned}
&\overbrace{V_o^{\min}+V_T^{\mathrm{SW}}}^{V_{g\mathrm{SW}}^{\max}} > V_{g\mathrm{SW}} > \overbrace{V_{g\mathrm{CAS}}-V_T^{\mathrm{CAS}}+\left(V_{\mathrm{OD}}^{\mathrm{SW}}+V_T^{\mathrm{SW}}\right)}^{V_{g\mathrm{SW}}^{\min}} \underbrace{V_{g\mathrm{SW}}-\left(V_{\mathrm{OD}}^{\mathrm{SW}}+V_T^{\mathrm{SW}}\right)+V_T^{\mathrm{CAS}}}_{V_{g\mathrm{CAS}}^{\max}}\\
&> V_{g\mathrm{CAS}} > \underbrace{V_{\mathrm{OD}}^{\mathrm{CS}}+\left(V_{\mathrm{OD}}^{\mathrm{CAS}}+V_T^{\mathrm{CAS}}\right)}_{V_{g\mathrm{CAS}}^{\min}}.
\end{aligned} \tag{23}$$

design procedure of Section IV for the optimum sizing of the CS + CAS + SW current cell topology.

### *D. Implications of the Extended Static Performance Constraints in the Design Procedure*

In this subsection, the extended modeling of the mismatch effects presented in Sections II-A–C (including the optimum output impedance biasing) are related to the circuit sizing for the two topologies. The occupied area saving that is obtained in the design by using the proposed extended modeling is contrasted with previous design approaches.

*1) Simple Current Cell* (CS+SW)*:* In the case of the CS+ SW topology, (1) and (2) leave only one degree of freedom for the CS transistor, namely the overdrive voltage (which univocally determines the CS gate bias voltage). The SW transistor then introduces four more design variables: $W_{\rm SW}$, $L_{\rm SW}$, overdrive voltage, and gate bias voltage. For the SW transistor the overdrive voltage and the width to length ratio $(W_{\rm SW}/L_{\rm SW})$ are also related by the current value, so only two of them are really free parameters. The optimum SW gate bias voltage (i.e., the ON gate voltage for the switch transistors) can be calculated using (10) as a function of the overdrive voltages, so only two degrees of freedom are left: the SW area and its overdrive voltage. The three degrees of freedom left for the overall circuit are constrained by the saturation condition of (21). They can be used to optimize other criteria, as for example the dynamic performance, as will be shown in Section III.

In order to compare the proposed saturation statistical model with the literature, a usual assumption is made which is that the minimum area current cell is a prior target (which corresponds to the worst case mismatch). In this sense, minimum area CS and SW transistor are chosen, and only the SW transistor overdrive voltage is left as a variable. By doing this, the SW transistor must have either minimum length or minimum width, depending on its overdrive voltage. The maximum CS overdrive voltage (its minimum area) is found as a function of the SW overdrive voltage using (21). Therefore, the SW overdrive voltage is the only degree of freedom left. Fig. 4 compares the saturation conditions of (15) and (21) for a 12-b DAC designed in a standard 0.35-$\mu$m process with a specifications similar to [10] and other smaller safety margins. Fig. 4(a) depicts the maximum CS overdrive voltage and Fig. 4(b) shows the minimum CS and overall current cell area. Both graphs are represented against the SW overdrive voltage assuming a minimum current cell area requirement. The smallest area achieved by applying the extended modeling and the saturation constraint of (21) is almost a 70% of the smallest area that will be obtained if the arbitrary safety margin of 500 mV used in [10] is considered, this indicating that the latter approach is notably pessimistic concerning process variations effects. The use of smaller safety margins leads to a reduction in the smallest area obtained, as shown in Fig. 4(b). However, even for a safety margin as small as 150 mV, the extended modeling approach yields a better result.

*2) Cascoded Current Cell* (CS + CAS + SW)*:* In the case of the CS + SW + CAS topology, the CS has also one degree of freedom left. The four degrees of freedom of each one of the two other transistors (SW and CAS) are reduced to two degrees of freedom for each one, using the current value expression and optimum gate bias voltage expressions of (11). The saturation conditions of (25) constrain the available design space in a similar way as (21) for the basic current cell. If minimum current cell area is imposed, the maximum CS overdrive voltage and CS minimum area can be represented against CS and CAS overdrive voltages as discussed in [15].

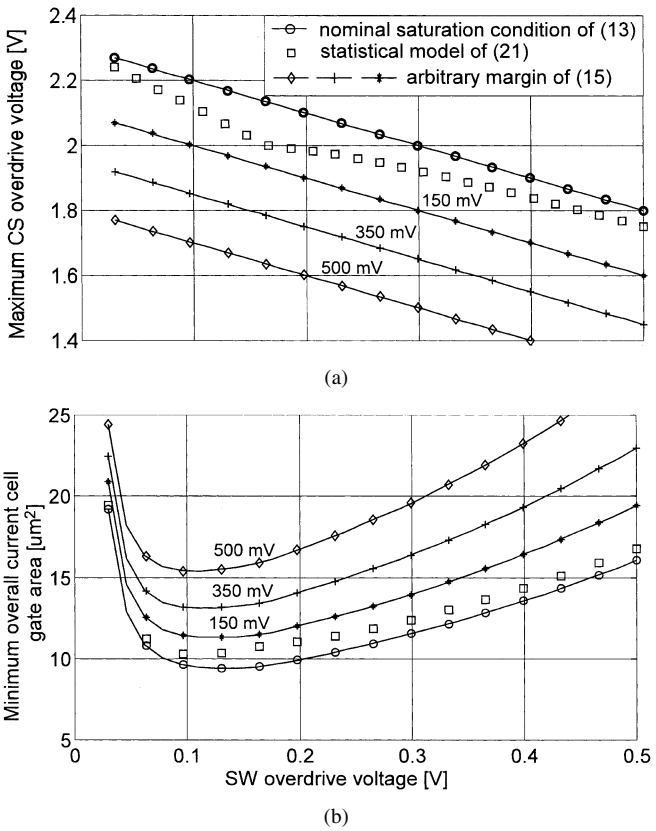


Fig. 4. Comparison between sizing results using (a) the proposed extended modeling and (b) previous sizing approaches with safety margins.

## III. Dynamic Performance

The dynamic performance of a segment current steering (SCS) DAC is mainly dependent on two characteristics of the current sources: settling time and dynamic output impedance. Another contribution that will also be included in the design procedure of Section IV is clock-feedthrough to the outputs, which is an important contribution to glitch energy. In this section, however, we will concentrate in the analysis of the settling time for switched current sources, by extending the work presented in [11] to find the relation of this settling time to the current cell circuit parameters. Next the dynamic output impedance modeling is reviewed.

### *A. Settling Time Modeling*

Following the same approach as in Section II, first the simple topology of Fig. 2(a) will be analyzed, followed by an analysis of the cascoded topology of Fig. 2(b).

*1) Simple Current Cell* (CS + SW)*:* During the switching process of a steered current source, two phases may be distinguished, as discussed in [11]. During the first phase, the two

complementary control signals drive one of the switch transistors from OFF to saturation whilst its complementary is driven in the opposite direction. This first phase of the switching process ends when both of the control signals attain their final value. During the second phase, only the voltages at the switch transistors drains (node $O$ in Fig. 2(a) and the common source (node $X$ in Fig. 2(a) vary until they achieve their steady state values. If the complementary control signals slopes are fast enough compared to the dynamic response of the current source nodes almost all the complementary output nodes transient takes place in the second phase of the current sources switching process, which is analyzed in the following.

The switching output voltage waveform is obtained by applying an incremental small-signal analysis around the steady state $X$ and $O$ node voltages at the end of the second phase ($V_{O0}$ and $V_{X0}$) and output current ($I_0$). This analysis uses the following small-signal $X$ and $O$ node voltage initial conditions:

$$\begin{aligned} v_{(0)} &= v_{(Oi)} = V_o(0) - V_{O0} \\ v_X(0) &= v_{Xi} = V_X(0) - V_{X0}. \end{aligned} \tag{26}$$

The small-signal output voltage waveform $v_O(t) = V_O(t) - V_{O0}$ found by the analysis is [11]

$$\begin{aligned} v_o(t) &= v_{ot} \cdot \exp(-P_o t) \\ &\times \left(1 + \frac{\gamma_X}{\frac{P_O}{P_X} - 1} \cdot \left(\exp\left(-\left(\frac{P_X}{P_O} - 1\right) P_o t\right) - 1\right)\right) \end{aligned} \tag{27}$$

where $P_o$ is the pole associated with the output node $O$, $P_X$ the pole associated with the internal node $X$, and $\gamma_X$ is the ratio between the small-signal initial charge at the internal node $X$ and at the output node $O$ at the beginning of phase 2. In the derivation of (27), the following simplifications have been performed: $g_{m\mathrm{SW}} \gg 1/r_{\mathrm{ds\_SW}} + 1/r_{\mathrm{ds\_CS}}$; $R_L \ll r_{\mathrm{ds\_SW}}$. The poles and initial charge ratio are related to the circuit parameters and initial conditions through

$$P_O = \frac{1}{R_L \cdot C_o}$$
$$P_X = \frac{g_{m\mathrm{SW}}}{C_X}$$

and

$$\gamma_X = \frac{v_{Xi} \cdot C_X}{v_{Oi} \cdot C_O} = \frac{q_{Xi}}{q_{Oi}} \tag{28}$$

where $C_O$ and $C_X$ are the parasitic capacitances at nodes $O$ and $X$, respectively, and $g_{m\mathrm{SW}}$ is the SW transistor small-signal transconductance. It should be noted that $v_o(\infty) = 0$.

Fig. 5 represents the current source output node transient waveforms obtained with (27) for a given value of $P_{X/O} = P_X/P_o$ and different values of $\gamma_X$, where $v_o(t)$ has been normalized to $v_{oi}$, and the time $t$ has been normalized to $1/P_o$. This waveforms have been obtained for a 12-b current-steering DAC using standard 0.35-$\mu$m process parameters. Considering that the settling time is the time needed by the output voltage to reach its final steady state value within an accuracy of $\pm M$ volts, it is concluded from Fig. 5 that there

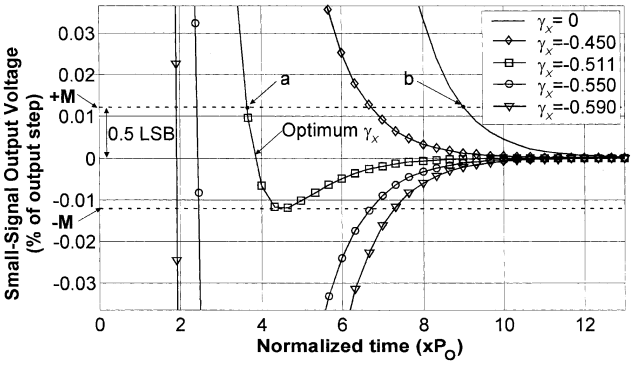


Fig. 5. Current source switching transient waveforms for the CS + SW topology.

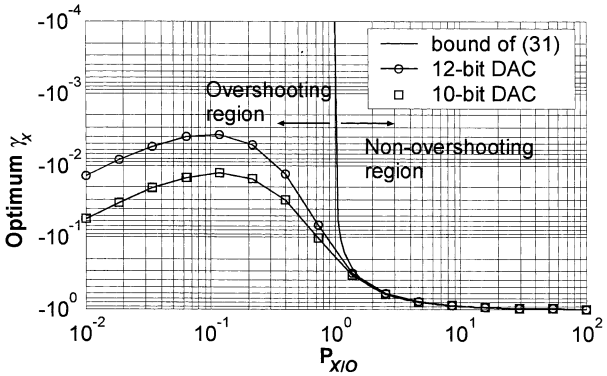


Fig. 6. Optimum $\gamma_X$ as a function of poles quotient for a 12- and 10-b DAC.

exists an optimum value for $\gamma_X$ that minimizes the settling time, for a given $M$ and $P_{X/O}$. In the figure, $M$ has been set to 0.5 LSB.

Two important conclusions are extracted from the previous analysis.

1) There exists an optimum value of $\gamma_X$ for every $P_{X/O}$ ratio that minimizes the settling time. This optimum is achieved through the appropriate design of the latch and its output driver circuit. The traditional design practice has been hitherto to design this control signals with a crossing point in which one of the transistors enters in saturation just when the other enters OFF state [8]. However, this is not necessarily the optimum case, because a small overshoot will help to speed-up the output settling time of the D/A converter, as has been shown above. For the illustrative 12-b DAC used to plot Fig. 5, and provided that the usual criterion of minimizing the overshoot ($\gamma_X = 0$) is used, the time needed for the output voltage to settle (point b) is almost 6 times larger than when the optimum $\gamma_X$ is used (point a).
2) The model of (27) allows the quantitative estimation of the settling time. It is a more accurate model than previous ones [10], which consider the settling time to depend just on the minimum of the two poles, $P_O$ or $P_X$, without coupling.

The optimum $\gamma_X$ waveform presents a negative overshooting that is equal to $-M$ (note that in Fig. 5 $M$ has been also normalized to $v_{Oi}$). No closed-form analytical expression exists for $\gamma_X$, but it is relatively easy to solve it numerically with the use of

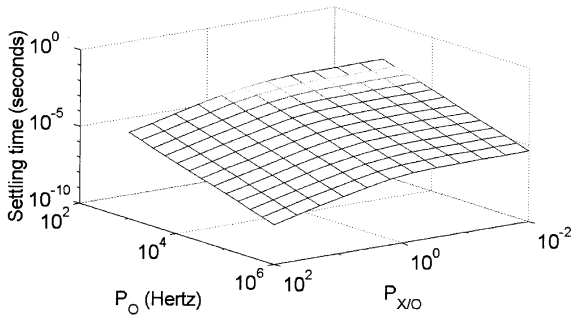


Fig. 7. Optimum settling-time for the CS + SW topology.

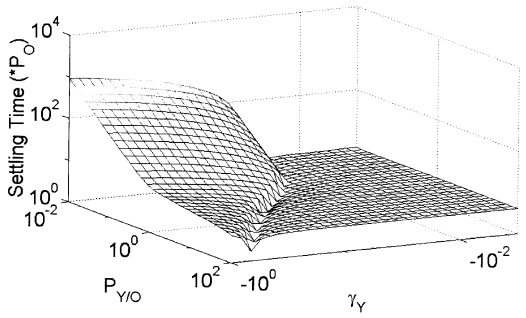


Fig. 8. Effects of the $Y$ node in the optimum settling time for the CS + CAS + SW topology.

differentiation, and considering that the optimum is found when $v_O(t)$ equals $-M$ at the instant for which (27) is minimum:

$$-M = v_{Oi}\gamma_X P_{X/O} \times \exp\left(\frac{P_{X/O}}{1-P_{X/O}}\ln\left(\frac{1}{P_{X/O}}\cdot\left(1-\frac{1-P_{X/O}}{\gamma_X P_{X/O}}\right)\right)\right). \quad (29)$$

Fig. 6 shows the optimum value of $\gamma_X$ as a function of $P_{X/O}$ for $M = 1/2^{13}$ and $M = 1/2^{11}$ (12- and 10-b DAC, respectively). The figure also depicts the following boundary condition that $\gamma_X$ must verify for overshooting to exist [11]:

$$P_X \le P_O \Rightarrow \gamma_X < 0 \quad P_X > P_O \Rightarrow \gamma_X < P_{X/O} - 1. \quad (30)$$

Fig. 7 shows the optimum settling time against $P_O$ and P_{X/O} obtained for 12-bits DAC and typical 0.35-CMOS technology parameters, assuming that the optimum $\gamma_X$ is used.

*2) Cascoded Current Cell* (CS + CAS + SW)*:* In this case, the circuit model used to estimate the output transient response is shown in Fig. 2(b). An analysis equivalent to that done for the CS + SW topology leads to the following result in the Laplace domain:

$$V_O(s) = \underbrace{v_{Oi}\cdot\frac{s+P_X\cdot(1+\gamma_X)}{(s+P_O)\cdot(s+P_X)}}_{V_O^{\text{no\_casc}}(s)} + \underbrace{v_{Oi}\cdot\frac{\gamma_Y\cdot P_Y\cdot P_X}{(s+P_O)\cdot(s+P_X)\cdot(s+P_Y)}}_{V'_O(s)} \quad (31)$$

where $P_Y = g_{m\text{CAS}}/C_Y$ and $\gamma_Y = v_Y i\cdot C_Y/(v_{Oi}\cdot C_O) = q_{Yi}/q_{Oi}$ are the additional pole and initial conditions coefficients due to the additional internal node $Y$ in Fig. 2(b). In the time domain, the small-signal output voltage waveform derived from (30) corresponds to

$$v_o(t) = v_O^{no\_casc}(t) + v'_O(t) \quad (32)$$

with

$$v'_O(t) = v_{Oi}\cdot\frac{P_X\cdot P_Y}{P_O^2}\cdot\gamma_Y \cdot\left(\frac{\exp(-P_O t)}{(P_{X/O}-1)(P_{Y/O}-1)} + \frac{\exp(-P_X t)}{(P_{X/O}-1)(P_{X/O}-P_{Y/O})} - \frac{\exp(-P_Y t)}{(P_{Y/O}-1)(P_{X/O}-P_{Y/O})}\right) \quad (33)$$

where an additional pole ratio $P_{Y/O} = P_Y/P_O$ is defined.

In this case, an additional component exists on the transient response, which satisfies $v'_O(0) = v'_O(\infty) = 0$.

The additional component $v'_O(t)$ effect is difficult to evaluate either analytically or graphically since considering it together with $\gamma_X$ and $P_{X/O}$ implies too many degrees of freedom. Fig. 8 shows the influence of the additional component on the estimated settling time as a function of $P_{Y/O}$ and $\gamma_Y$, for a reasonable value of $P_{X/O} = 2.6$ and optimum $\gamma_X$, extracted from an actual 12-b SCS DAC designed on a 0.35-$\mu$m CMOS technology [16].

### *B. Dynamic Output Impedance Modeling*

The current-steering DAC SFDR performance is strongly determined by the output impedance of the current sources [1], [2], as expressed by the following expression:

$$\text{SFDR} = \left[\frac{1+\rho\cdot k_{\text{dc}}}{\rho\cdot k_{\text{ac}}} + \sqrt{\left(\frac{1+\rho\cdot k_{\text{dc}}}{\rho\cdot k_{\text{ac}}}\right)-1}\right]^2 \quad (34)$$

where $\rho = R_L/R_{\text{out}}$ is the output load ($R_L$) to LSB current source output impedance ($R_{\text{out}}$) ratio, $k_{\text{dc}}$ and $k_{\text{ac}}$ are the dc component and ac amplitude, respectively, of the sinusoidal ($k_{\text{dc}} \ge k_{\text{ac}} > 0$ and $k_{\text{dc}} + k_{\text{ac}} \le 2^N - 1$). For proper spectral performance, the SFDR has to be greater than the signal-to-quantization-noise ratio, which is 86 dB for a 14-b DAC or 74 dB for a 12-b DAC. This implies a minimum output impedance requirement. Output impedance SFDR requirements are easily fulfilled for low-frequency signals, but when signal frequency is deep in the megahertz band parasitic capacitances of the current source strongly degrade its output impedance and, consequently, the SFDR performance of the DAC is worsened.

In Section II-B, it was mentioned that the current source output impedance could be estimated using (4) and (5), for the simple and cascoded current cell, respectively. This is true for slow variations of the output voltage. In [2], it is shown that in the case of the simple current cell topology the effect of the nondesired capacitances may be modeled by adding a pole and a zero to (4) and two poles and two zeros to (5) in the case of the

cascoded current cell. This yields to the frequency-dependent output impedances of (35) and (36), shown at the bottom of the page. In the frequency band of interest (up to Nyquist), the zeros do not affect dynamic output impedance because $g_m \gg 1/r_{ds}$ for reasonable transistor sizes.

### *C. Implications of the Settling Time and Dynamic Output Impedance in the Design Procedure*

In this subsection, the settling time and dynamic output impedance dependencies on circuit poles and initial conditions are related to the transistors sizes and other circuit parameters.

*1) Simple Current Cell* (CS + SW)*:* Fig. 7 depicts the estimated optimum settling time as a function of $P_O$ and $P_{X/O}$, assuming that the optimum $\gamma_X$ is obtained by the proper synchronization of the switches' control signals. From Fig. 7, the intuitive rule that maximizing both poles leads to lower settling time is quantitatively confirmed. In order to maximize $P_X$, a minimum-length SW transistor should be used. The SW transconductance increases as the square root of the SW transistor width, but gate-to-source capacitance increases linearly, thus a minimum-width SW transistor also maximizes $P_X$. On the other hand, a minimum-width CS transistor minimizes the CS drain capacitance, therefore minimizing $C_X$. A minimum width for the CS implies that it must have the maximum CS overdrive voltage that guarantees saturation for all transistors (Section II-C). In most cases, however, the influence of the SW and CS transistors' width on $C_X$ can be neglected. This capacitance is dominated by the interconnect capacitance between the CS and SW transistors in actual circuits, as each transistor is placed in a different array and their interconnections usually are large enough to dominate the $X$ node parasitic capacitance. Furthermore, a minimum-width SW transistor also maximizes $P_O$ by minimizing its drain and overlap capacitances. This is specially significant for high segmentation ratios, where a great number of switch drains are connected together at the output node. Apart from the benefits to the settling time, the clock-feedthrough is reduced if the SW gate and drain overlap capacitances are lowered, which occurs when the SW width is minimum.

The main design implication extracted from the previous discussion is that a minimum-length and -width SW transistor and minimum-width CS transistor (maximum overdrive voltage) is the optimum choice for settling time. However, the effect of SW and CS width should be evaluated for every particular case, especially when node $X$ and $O$ parasitic capacitances are not dominated by the SW capacitances. In this latter case, increasing the SW width will increase its transconductance without significantly affecting $C_X$ and $C_O$, although the clock-feedthrough will be compromised.

The previous analysis applies to the OFF–ON switching branch of the current source. If the same criterion is considered in the analysis of the complementary ON–OFF switching branch, the conclusion is that during the second switching phase the time response of the complementary output node exclusively depends on $P_O$.

Concerning the dynamic output impedance requirement, in the case of the simple current cell (SW + CS), a minimum-length SW transistor allows minimizing $C_X$. Even if interconnect capacitance dominates, it is not worth increasing the SW transistor length to attempt to decrease the output impedance zero down to the pole frequency, as this compromises settling time and dramatically increases the current cell area and, consequently, the overall DAC area. Choosing the minimum area for the CS transistor allows to minimize CS array area and, thus, the interconnect capacitance. Furthermore, a minimum CS width will also reduce node $X$ capacitance.

*2) Cascoded Current Cell* (CS + CAS + SW)*:* The same conclusions of Section III-A1 and design implications of Section III-C1 are applicable to $v_O^{\text{no-casc}}$ with respect to $\gamma_X$ and $P_{X/O}$. A minimum-length and -width SW transistor and minimum-width CAS transistor (instead of CS) are optimum for the settling time. This is especially true if it is taken into account that a small interconnect capacitance exists between SW and CAS transistors in actual circuits. In this sense, the CAS transistor not only increases current cell dc output impedance, but also improves settling time performance. Concerning the influence of the additional node $Y$, as discussed in Section III-A2 and from Fig. 8, it is clear that only when $P_Y$ is low enough and $\gamma_Y$ is high is the settling time compromised. This situation is not common, since the smaller $P_Y$ is, the smaller $\gamma_Y$ will be, as $C_Y$ opposes voltage variations at node $Y$. In general, for reasonable values of $P_O$, $P_X$, and $P_Y$, and reasonable voltage variations at the internal nodes, pole $P_Y$ does not effectively affect the settling time.

As far the dynamic output impedance is concerned, the same argument than in Section III-C1 may be applied to the SW and CAS transistors length. Also, minimum CS area is the best choice for output impedance bandwidth. Finally, minimum CAS width leads to better performance, as it minimizes nodes $X$ and $Y$ capacitance. Minimum transistor dimensions produce maximum bandwidth for output impedance and SFDR performance, apart from minimizing DAC area. Note that if the dominant pole is $1/(2\pi r_{\text{dsCS}} C_Y)$, adding one or more extra

$$|Z_{\text{out}}^{\text{CS+SW}}(f)| \approx R_{\text{out}}^{\text{CS+SW}} \sqrt{\frac{\left(1+\left(\frac{s2\pi C_X f}{g_{m\text{SW}}}\right)^2\right)}{(1+(2\pi r_{\text{dsCS}} C_X f)^2)}} \tag{35}$$

$$|Z_{\text{out}}^{\text{cascoded}}(f)| \approx R_{\text{out}}^{\text{cascoded}} \sqrt{\frac{\left(1+\left(\frac{2\pi C_s f}{g_{m\text{SW}}}\right)^2\right)\left(1+\left(\frac{2\pi C_y f}{g_{m\text{CAS}}}\right)^2\right)}{(1+(2\pi r_{\text{dsCAS}} C_x f)^2)(1+2\pi r_{\text{dsCAS}} C_y f)^2}} \tag{36}$$

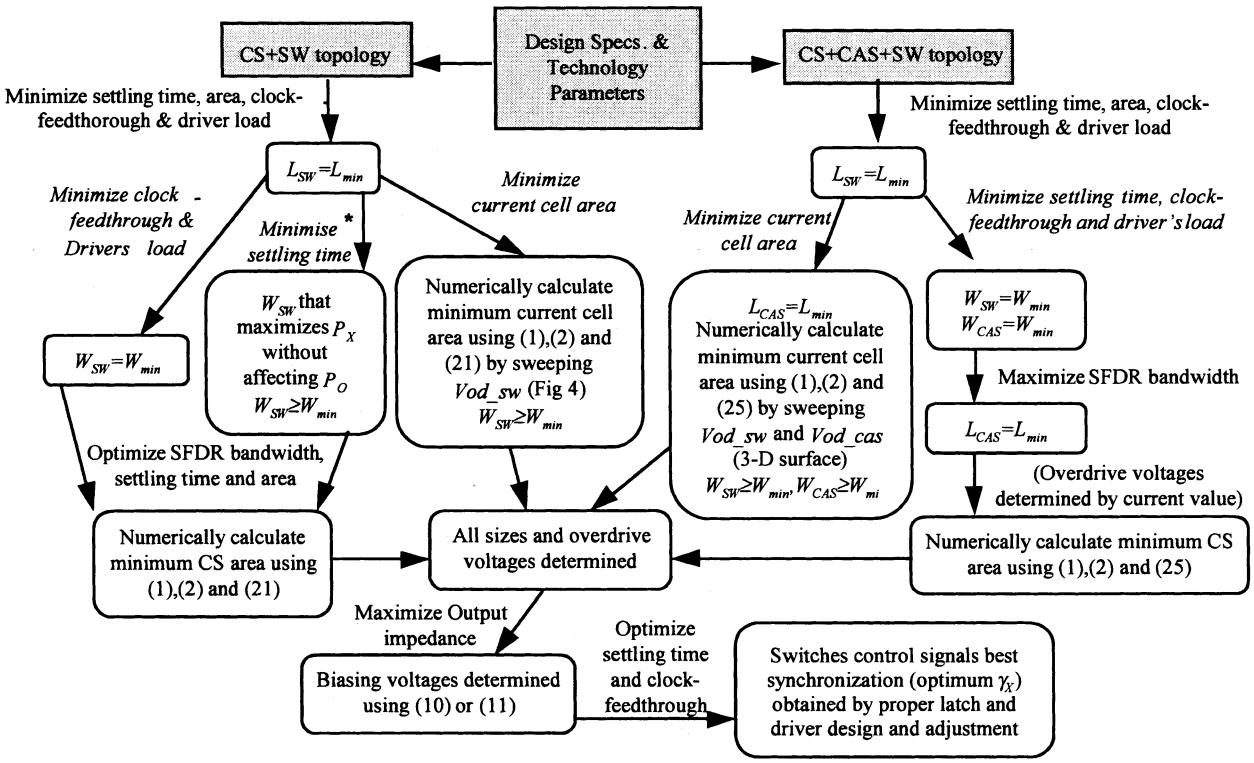


Fig. 9. Current sources design procedure flow for current-steering DACs.

cascode transistors between CAS and SW may improve SFDR bandwidth performance without compromising settling time, although the overall DAC area is increased (especially if we take into account that a lower CS overdrive voltage will need to be chosen).

## IV. Design Procedure

In Sections II and III, the DAC current sources' static, dynamic, area, and statistical models have been presented. Performance requirements are related to the DAC design specifications, such as number of bits, linearity (INL and DNL), sampling frequency, spectral performance, yield, area, and technology [1].

On the basis of the models presented in Sections II and III, a current cell design procedure can be derived for both the simple (CS+SW) and cascoded (CS+CAS+SW) current cell topologies.

Fig. 9 shows the design procedures for the two topologies. The starting point includes design specifications and technology parameters. For the two topologies there are basically two targets driving the optimization process (indicated with italics in the figure), namely minimize current cell area and minimize settling time. Note that in the cascoded topology the minimum settling time target is coincident with the optimum clock feedthrough and driver's load target, whereas for the simple current source topology (left part of the figure) the settling time optimization has some negative impact on the clock-feedthrough (because of the required increase in the SW transistor width). Hence, two alternatives are shown in this case depending on whether glitch energy or sampling frequency is priorized. Intermediate results of the design procedure are enclosed within the boxes. The design criteria used to derive the intermediate results are shown by the arrows. Note that, in general, the design procedures do not require the segmentation ratio to be chosen previously, at least not until the driver and latches are designed. The only exception is the case in which the output node capacitance needs to be estimated with precision (this design path is indicated in Fig. 9 with an asterisk). The proposed design procedure is closed and provides as a final result the complete sizing of the DAC current source circuits.

## V. Conclusion

This work provides an extended design procedure for current-steering DACs through the static and dynamic study of two usually considered current source circuit cells. On the one hand, an extended mismatch statistical study which takes into account random variations in all the transistors of the current source cells yields an improved analytical static model. This refined model permits us to tighten the required biasing margins without resorting to arbitrary margins, which, given the design space of the DAC, results in notable area reductions. Conditions for optimum gate bias voltages concerning output resistance are obtained as well. On the other hand, an extension of the switching transient behavior is discussed, and its relation to transistor parameters is discussed. As a consequence of the extended static and dynamic modeling, an improved DAC design procedure is presented. By applying the design method to a particular technology and DAC specifications, comparisons with previous design approaches clearly indicate that the improved modeling of mismatching and dynamics effects presented in this work allow to reduce the area and improve the settling time of the DAC. The results of this paper may ease the automatization of the

circuit design of future current-steering DACs with improved performance.

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