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TCMOS: Low noise power supply technique for digital ICs

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Indexing terms: Power supply circuits, Digital integrated circuits

Mixed signal circuits have become an important trend in IC design. In these circuits, the effect of digital noise on the analogue part of the circuit is one of the most important performance constraints. The authors present a new technique for providing power to conventional CMOS circuits which minimises the noise in the power buses.

Introduction: The switching noise generated in a conventional CMOS digital circuit can be transmitted to the analogue part in several ways. The most important mechanisms are: coupling through the common substrate, parasitic capacitances and direct injection through the power supply lines [1 – 3]. The noise present in power lines is mainly caused by the large current peaks drawn from or supplied to these lines by the MOS circuits at the switching times, for charging or discharging the output capacitances. Any serial impedance in the power lines transforms the current spikes in voltage noise. The main serial impedances along the power supply path are the inductance and resistance of the pins and the lead frame of the package. These noisy power lines were once the main source of noise to the analogue part of the circuit because the power lines are used to bias the common substrate and are routed across all of the IC surface. Some approaches have already been presented for minimising the current peaks generated by the logic gates [4, 5]. They have the characteristic of constant power consumption and the disadvantages of not being conventional CMOS complementary logics and having larger area requirements than conventional logic. The approach presented in this Letter (called the tankCMOS or TCMOS technique) is compatible with conventional CMOS logic because it only affects the way the power to the whole digital part of the circuit is provided. Additionally, the TCMOS approach has a similar power consumption to the conventional CMOS approach.

Description: In the TCMOS approach, power is provided to the conventional CMOS logic (CCL) through a controlled current injector (CCI) stage (see Fig. 1). This stage has the ability to isolate the main power supply bus (V_{dd}) from the current noisy power lines of the CCL. To achieve this goal, a tank capacitor (C_T) connected directly to the CCL circuit is used. This capacitor stores enough energy to provide power to the CCL for a certain period of time with a controlled drop of voltage. Initially the CCL is isolated from the V_{dd} power bus and the voltage of C_T (V_2 in Fig. 1) falls following the CCL switching activity. When V_2 falls to a given minimum voltage (V_{2_min} in Fig. 2) the capacitor C_T is recharged, by the CCI stage, using a constant current of value I_r, until V_2 reaches a maximum value (V_{2_max}). The CCI stage then turns off again. This technique avoids the presence of noise in the V_{dd} power bus in two ways: first, during the recharge phase, the current is forced to be a constant, and secondly, during the rest of the CCI duty cycle the V_{dd} power bus is isolated from the CCL current noisy power lines.

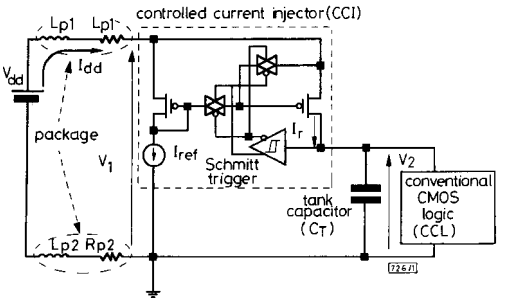

Fig. 1 *TCMOS structure*

V_1: on-chip power bus voltage, V_2: CCL power line voltage
V_{dd} and I_{dd}: main power supply voltage and current, respectively

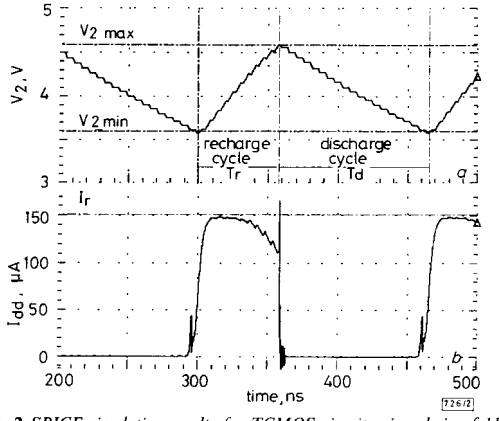

Fig. 2 *SPICE simulation results for TCMOS circuit using chain of 11 CMOS inverters with input clock of frequency = 90.9MHz*

a Voltage at C_T (V_2) used to supply CCL
b Current supplied by main V_{dd} power source

For the technique to function properly, the injected current (I_r) must be greater than the current drawn by the CCL during the charging period. That is

$$I_r > \frac{P_D}{V_{dd}}$$

where P_D is the CCL power consumption using V_{dd} as the constant supply voltage for the CCL. The recharging (T_r) and discharging (T_d) duration cycles are given by

$$T_r = C_T \frac{V_{2\_max} - V_{2\_min}}{I_r - P_D/V_{dd}} \qquad T_d = C_T \frac{V_{2\_max} - V_{2\_min}}{P_D/V_{dd}}$$

where $V_{dd} > V_{2\_max} > V_{2\_min}$. These time values are pessimistic approximations, fixing a worst case duty cycle of the TCMOS.

In the two phases of the CCI duty cycle (recharge/isolation), the CCL sees a slow increase/decrease of V_2 between V_{2_min} and V_{2_max}. If these two limits are properly fixed, the noise margins of the CMOS make the logic functionality almost insensitive to CCL power supply voltage fluctuations.

Results: In Fig. 2, the results of SPICE simulations of a CCL consisting of a chain of 11 CMOS inverters with power provided by the TCMOS approach, are presented. Fig. 2*a* shows the voltage V_2 during several periods of the input clock. Fig. 2*b* shows the current (I_{dd}) supplied by the V_{dd} source. The I_{dd} waveform does not show current noise except at the turn-on/turn-off events of the CCI. During the recharge cycle, the current is approximately constant and equal to I_r = 150 μA. In the isolated cycle, I_{dd} = 0. In Fig. 3, the voltage noise in the on-chip power buses (V_1) of three different techniques of providing power to the same CCL of Fig. 2 are presented. In the first (conventional) approach the power is directly provided to the CCL from the main power supply buses. The inductance and resistance of the package considered in the analysis are typical values for a 24 pin DIL [6]: $L_{p1} = L_{p2}$ = 20nH, $R_{p1} = R_{p2}$ = 0.1Ω. In the second approach, we use a low noise folded source-coupled logic (FSCL) from [4], to implement the chain of 11 inverters. This FSCL digital block is directly connected to the main power buses as in the first approach. The third approach is the TCMOS approach. In this example, we use C_T = 5pF, V_{2_min} = 3.6V and V_{2_max} = 4.6V. A reduction of noise obtained by the TCMOS approach is clearly shown in the third graph of Fig. 3. Comparing the three approaches of Fig. 3, the TCMOS approach has the best power to noise ratio (see Table 1).

Table 1: Power consumption and RMS noise voltage in power buses for chain of 11 inverters for three strategies of Fig. 3

	Conventional CMOS	FSCL from [4]	TCMOS
Noise [mV, RMS]	12.24	1.51	1.26
PD [mW]	0.310	1.891	0.256

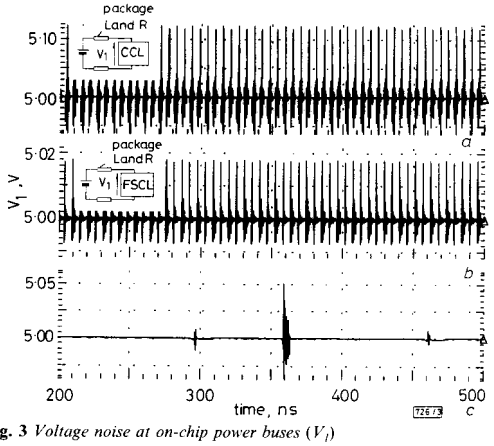

Fig. 3 *Voltage noise at on-chip power buses (V_1)*

a Conventional CMOS logic
b FSCL logic
c Conventional CMOS with power provided using TCMOS approach

Conclusions: We have presented the TCMOS supply technique, which clearly reduces the on-chip power bus noise produced by the digital parts of a mixed signal IC. The TCMOS technique has a power consumption similar to that of conventional CMOS logic, rather than the constant current consumption required for other low noise logics such as in [4, 5]. TCMOS is straightforward to implement using CMOS technology for the CCI stage and a capacitor in the cavity [7] for the tank capacitor, or using MCM techniques to put together the IC, tank capacitor and CCI logic. TCMOS can be adjusted to a wide range of situations by simply adjusting the injection current and the tank capacitor value, fixing the desired TCMOS duty cycle for the given application.

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1.3μm waveguided electroabsorption modulators with strain-compensated InAsP/InGaP MQW structures

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Indexing terms: Electroabsorption modulators, Semiconductor quantum wells

High-quality multiquantum well (MQW) structures with 1.5% compressive strain in InAsP wells and 0.8% tensile strain in InGaP barriers have been grown by gas-source molecular beam epitaxy on InP substrates. High-speed (3dB bandwidth over 10GHz) and low driving voltage (lower than 2V for 20dB on/off ratio) operation using these structures is demonstrated. These characteristics are the first reported for MQW modulators operating at 1.3μm.

Optical modulators using InP as a transparent substrate and operating at wavelength regions of reduced fibre loss, 1.3 and 1.55μm, are expected to be used in high bit rate and long haul optical fibre transmission systems because of their low chirping characteristics. In particular, multiquantum well (MQW) electroabsorption (EA) modulators have advantages such as low driving voltage and high-speed operation [1, 2]. To achieve operation at 1.3μm, GaInAsP/InP quaternary quantum wells have been used to provide continuous tunability in both composition and thickness [3, 4]. Strained InAsP/InP MQW structures are alternative material systems to quaternary layers [5, 6]. This is particularly useful for short wavelengths without resorting to ultra-thin well thickness, because a small well width suffers from reduced energy shift with applied field and results in reduced electroabsorption or quantum confined Stark effect (QCSE).

The introduction of compressive strain into the quantum well has been reported for increasing conduction band offset and making the escape of photogenerated holes easier under high input power for EA modulators [7 – 9]. Gas-source molecular beam epitaxy or chemical beam epitaxy (CBE) has been shown to provide high-quality epi-layers with low unintentional background and high strain because of their low growth temperature. Strain compensation also increases the critical layer thickness and enlarges the QCSE.

In this Letter, we report strained-compensated InAsP/InGaP MQW structures grown by CBE and demonstrate excellent electroabsorption modulator characteristics. High-speed operation with a 3dB bandwidth of over 10GHz and very low driving voltage less than 2V for a 20dB on/off ratio have been achieved. These device characteristics are the first reported for modulators operating at 1.3μm wavelength.