**Departament de Teoria del Senyal i Comunicacions**

UNIVERSITAT POLITÈCNICA DE CATALUNYA

Ph.D. Thesis

# Multi Look-Up Table Digital Predistortion for RF Power Amplifier Linearization

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# Chapter 7

# Conclusion and Future Work

## 7.1 Conclusion

As it has been shown along this thesis, the PA is a key device for the overall RF transmitter efficiency and linearity performance. On the one hand, power efficiency is an important figure of merit taken into account by designers and manufacturers. On the other hand, linear amplification is a must and certain levels of signal fidelity at the transmitted antenna are specified by communication standards. The PA inherent nonlinear behavior has been confronted from two different approaches: an accurate circuit level design aiming at obtaining highly linear PAs and when necessary, making use of linearization solutions at device level; and system level linearization, a broad approach that considers the PA as a nonlinear black-box to be linearized.

In this thesis, an overview on the most common system level solutions to face the problem of PA linearization has been presented, focusing the attention in revived solutions thanks to new current DSP capabilities. The tendency of avoiding hardware limitations (losses, maladjustments) by using SDR systems together with the increasing speed that can be achieved in digital processing, makes designers reconsider the use of digital linearization solutions such as EE&R, outphasing techniques (LINC, CALLUM) and digital predistortion.

The main contribution of this thesis has been focused in presenting a new predictive DPD based in a NARMA architecture capable of taking into account PA dynamics and therefore compensate for PA memory effects. For that reason, in a first approach, the basic principles of digital predistortion have been introduced emphasizing the need to find PA behavioral models able to reproduce not only PA nonlinear behavior, but also its dynamics. Later, and aiming at a final implementation, this PA models have to be extracted attending the trade-off between complexity and accuracy. Therefore, techniques to reduce the order of the models, such as the use of heuristic search algorithms, are of significant importance to guarantee certain fidelity without introducing an excessive computational complexity.

The NARMA-based PA behavioral model, with a recursive structure aimed at relaxing the number of coefficients to reproduce PA nonlinear memory effects, has been described in detail. Within this thesis, stability issues related to the NARMA recursive nature have been discussed, providing a method that permits monitoring and thus avoiding possible unstable configurations of the NARMA structure. Moreover, the principles of the extraction of the NARMA-based DPD function by means of the predictive predistortion approach have been described, as well as its later derivation into a set of LUTs for its FPGA implementation.

In order to validate theories, a Matlab simulator that emulates the multi-LUT implementation in an FPGA of the proposed adaptive DPD has been developed. This simulator offers the possibility to choose among different scenarios and configurations to validate our predictive NARMA-based DPD. It is possible to choose among a set of PA models with different nonlinear behaviors taking into account memory effects, different single carrier and multicarrier modulation schemes or even among different adaptation algorithms to perform LUT updates. Some of the results obtained with this simulator have been presented in this thesis to show the linearization performance achieved with the adaptive DPD.

To provide a more realistic view of the capabilities of our NARMA-based DPD, it has been experimentally validated by implementing it in a reconfigurable FPGA board. For debugging purposes, the LUT update process has been performed in an external host PC running Matlab. Experimental results have shown the linearization capabilities of the proposed NARMA based DPD, over a wide range of signal bandwidths and independently of the modulated signal used; highlighting the potential of the proposed recursive DPD architecture over the more usual non recursive DPD approaches.

Besides, practical design issues and real-time DPD hardware implementation topics have been also tackled. Among them, we have proposed the concept of scalable FPGA DPD implementation by replication of BPCs, as well as an iterative adaptation process for signals with high PAPR and limited data recording capabilities. Indeed, it has been shown how the training of the DPD with a spectrally rich wideband signal provides stability and reliability despite the specific signal to be predistorted during regular operation.

This thesis has also focused on the power consumption of the DPD implementation, concluding that the DPD contribution to the overall efficiency may be negligible in front of the PA consumption and that of the devices deployed for adaptation purposes.

Finally, considering that the inclusion of the DPD is necessary to provide transmitted signal fidelity against memory effects, we have explored the possibility of biasing the PA in a power efficient quiescent point, showing how the added non-linearity resulting from that power efficient polarization can be compensated by the DPD, therefore improving the overall efficiency at no extra cost.

## 7.2  Future Work

As it has been advanced, the possibility to include real-time adaptation in the same FPGA responsible for the predistortion represents an advance to reduce size and power consumption of the whole DPD structure since no additional power consuming DSPs are required. Moreover it avoids uncertainties related to polynomial identification since LUT updates are performed directly (one gain value of each LUT at every iteration step), taking advantage of the FPGA parallel processing capabilities and without the need to derive LUT gains from a polynomial function. Therefore, next step towards the improvement of our predictive NARMA-based DPD will be focused in the development of the real-time (LMS based) adaptation process in the FPGA.

Finally, taking advantage of the experience acquired applying digital solutions to system level linearization we might explore the possibility to use alternative digital linearization approaches, such the EE&R or Envelope Tranking techniques, to linearize current highly efficient but extremely nonlinear switched PAs. Furthermore, it will be interesting to reuse digital resources, yet deployed for predistortion purposes, to enhance the PA efficiency by controlling the dynamic supply of the PA. Therefore, our research will be focused in combining digital linearization techniques with the development of strategies for driving very efficient, but limited in bandwidth, switched DC/DC converters for the dynamic supply of the PA in wideband communication systems [Ces06].