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Ph.D. Thesis

Multi Look-Up Table Digital Predistortion for RF Power Amplifier Linearization

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to my family,

The true delight is in the finding out rather than in the knowing.

Isaac Asimov

Abstract

This Ph.D. thesis addresses the design of a new Digital Predistortion (DPD) linearizer capable to compensate the unwanted nonlinear and dynamic behavior of power amplifiers (PAs). The distinctive characteristic of this new adaptive DPD is its deduction from a Nonlinear Auto Regressive Moving Average (NARMA) PA behavioral model and its particular multi look-up table (LUT) architecture that allows its implementation in a Field Programmable Gate Array (FPGA) device.

The DPD linearizer presented in this thesis operates at baseband, thus becoming independent on the final RF frequency band and making it suitable for multiband or reconfigurable scenarios. Moreover, the proposed DPD takes into account PA memory effects compensation which represents an step forward in overcoming classical limitations of memoryless predistorters. Compared to more computational complex DPDs with dynamic compensation, such Time-Delayed Neural Networks (TDNN), this new DPD takes advantage of the recursive nature of the NARMA structure to relax the number of LUTs required to compensate memory effects in PAs. Furthermore, its parallel multi-LUT architecture is scalable, that is, permits enabling or disabling the contribution of specific LUTs depending on the dynamics presented by a particular PA.

In a first approach, it is necessary to identify a NARMA PA behavioral model. The extraction of PA behavioral models for DPD linearization purposes is carried out by means of input and output complex envelope signal observations. One of the major advantages of the NARMA structure regards its capacity to deal with the existing trade-off between computational complexity and accuracy in PA behavioral modeling. To reinforce this compromise, heuristic search algorithms such the Simulated Annealing or Genetic Algorithms are utilized to find the best sparse delays that permit accurately reproducing the PA nonlinear dynamic behavior. However, due to the recursive nature of the NARMA model, an stability test becomes a previous requisite before advancing towards DPD linearization.

Once the PA model is identified and its stability verified, the DPD function is extracted applying a predictive predistortion method. This identification method relies just on the PA NARMA model and consists in adaptively forcing the PA to behave as a linear device. Focusing in the DPD implementation, it is possible to map the predistortion function in a FPGA, but to fulfill this objective it is first necessary to express the predistortion function as a combined set of LUTs.

In order to store the DPD function into a FPGA, it has to be stated in terms of parallel and cascade Basic Predistortion Cells (BPCs), which are the fundamental building blocks of the NARMA based DPD. A BPC is formed by a complex multiplier, a dual port RAM memory block acting as LUT and an address calculator. The LUT contents are filled following an uniform spacing procedure and its indexing is performed with the amplitude (modulus) of the signal's

envelope.

Finally, the DPD adaptation consists in monitoring the input-output data and performing frequent updates of the LUT contents that conform the BPCs. This adaptation process can be carried out in the same FPGA in charge of performing the DPD function, or alternatively can be performed by an external device (i.e. a DSP device) in a different time-scale than real-time operation.

To support all the theoretical design and to prove the linearization performance achieved by this new DPD, simulation and experimental results are provided. Moreover, some issues derived from practical experimentation, such as power consumption and efficiency, are also reported and discussed within this thesis.

Resum

Aquesta Tesi Doctoral se centra en el disseny d'un nou linealitzador de Predistorsió Digital (*Digital Predistortion* - DPD) capaç de compensar la dinàmica i els efectes no lineals introduïts pels Amplificadors de Potència (*Power Amplifiers* - PAs). Un dels trets més rellevants d'aquest nou predistorsionador digital i adaptatiu consisteix en ser deduïble a partir d'un model de PA anomenat *Nonlinear Auto-Regressive Moving Average* (NARMA). A més, la seva arquitectura multi-*Look-Up Table* (LUT) permet la implementació en un dispositiu *Field Programmable Gate Array* (FPGA).

La funció de predistorsió es realitza en banda base, per tant, és independent de la banda freqüencial on es durà a terme l'amplificació del senyal de RF, el que pot resultar útil si tenim en compte escenaris multibanda o reconfigurables. D'altra banda, el fet que aquest DPD tingui en compte els efectes de memòria introduïts pel PA, representa una clara millora de les prestacions aconseguides per un simple DPD sense memòria. En comparació amb d'altres DPDs basats en models més computacionalment complexos, com és el cas de les xarxes neuronals amb memòria (*Time-Delayed Neural Networks* - TDNN), la estructura recursiva del DPD proposat permet reduir el nombre de LUTs necessàries per compensar els efectes de memòria del PA. A més, la seva estructura multi-LUT permet l'escalabilitat, és a dir, activar or desactivar les LUTs que formen el DPD en funció de la dinàmica que presenti el PA.

En una primera aproximació al disseny del DPD, és necessari identificar el model NARMA del PA. L'extracció del model comportament del PA es duu a terme a partir de mostres d'entrada i sortida de l'envoltant complexa del senyal. Un dels majors avantatges que presenta el model NARMA és la seva capacitat per trobar un compromís entre la fidelitat en l'estimació del PA i la complexitat computacional introduïda. Per reforçar aquest compromís, l' ús d'algoritmes heurístics de cerca, com són el Simulated Annealing o els Genetic Algorithms, s'utilitzen per trobar els retards que millor caracteritzen la memòria del PA i per tant, permeten la reducció del nombre de coeficients necessaris per caracteritzar-la. Tot i així, la naturalesa recursiva del model NARMA comporta que, de cara a garantir l'estabilitat final del DPD, cal dur a terme un estudi previ sobre l'estabilitat del model.

Una vegada s'ha obtingut el model NARMA del PA i s'ha verificat l'estabilitat d'aquest, es procedeix a l'obtenció de la funció de predistorsió a través del mètode d'identificació predictiu. Aquest mètode es basa en la continua identificació del model NARMA del PA i posteriorment, a partir del model obtingut, es força al PA perquè es comporti de manera lineal. Per poder implementar la funció de predistorsió en la FPGA, cal primer expressar-la en forma de combinacions en paral·lel i cascada de les anomenades *Cel·les Bàsiques de Predistorsió* (BPCs), que són les unitats fonamentals que composen el DPD. Una BPC està formada per un multiplicador complex, un port RAM dual que actua com a LUT (taula de registres) i un calculador d'adreces. Les

LUTs s'omplen tenint en compte una distribució uniforme dels continguts i l'indexat d'aquestes es duu a terme mitjançant el mòdul de l'envoltant del senyal.

Finalment, l'adaptació del DPD consisteix en monitoritzar els senyals d'entrada i sortida del PA i anar duent a terme actualitzacions periòdiques del contingut de les LUTs que formen les BPCs. El procés d'adaptació del contingut de les LUTs es pot dur a terme en la mateixa FPGA encarregada de fer la funció de predistorsió, o de manera alternativa, pot ser duta a terme per un dispositiu extern (com per exemple un DSP - *Digital Signal Processor*) en una escala de temps més relaxada.

Per validar l'exposició teòrica i provar el bon funcionalment del DPD proposat en aquesta Tesi, es proporcionen resultats tant de simulació com experimentals que reflecteixen els objectius assolits en la linealització del PA. A més, certes qüestions derivades de la implementació pràctica, tals com el consum de potència o la eficiència del PA, són també tractades amb detall.

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Pere Ll. Gilabert Pinal

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Contents

Acronyms

ABC & S	Always Best Connected and Served.
ACLR	Adjacent Channel Leakage power Ratio.
ACEPR	Adjacent Channel Error Power Ratio.
ACPR	Adjacent Channel Power Ratio.
AM/AM	Amplitude Modulation to Amplitude Modulation conversion.
AM/PM	Amplitude Modulation to Phase Modulation conversion.
ANN	Artificial Neural Network.
AWGN	Additive White Gaussian Noise.
BB	Baseband.
BER	Bit Error Rate.
BO	Back-off.
BPC	Basic Predistorter Cell (or Basic Predistortion Cell).
BPSK	Binary Phase Shift Keying.
CALLUM	Combined Analog-Locked Loop Universal Modulator.
cdf	cumulative density function.
CDMA	Code Division Multiple Access.
CFB	Cartesian Feedback.
CFB-RM	Cartesian Feedback with Reference Model.
cte	constant.
DPD	Digital Predistortion (or Digital Predistorter).
DSP	Digital Signal Processor (or Digital Signal Processing).
DVB	Terrestrial Digital Video Broadcasting.
etc.	etcetera.
EE&R	Envelope Elimination and Restoration.
ETSI	European Telecommunications Standards Institute.
EVM	Error Vector Magnitude.
FET	Field-Effect Transistor.
FFT	Fast Fourier Transform.

FIR Finite Impulse Response.
FOM Figure Of Merit.
FPGA Field-Programmable Gate Array.
GA Genetic Algorithm.
GS Gradient Search.
GSM Global System for Mobile communications.
HD Harmonic Distortion.
I In-phase.
IBO Input Back-off.
IEEE Institute of Electrical and Electronics Engineers.
IF Intermediate Frequency.
IFFT Inverse Fast Fourier Transform.
IIR Infinite Impulse Response.
IMD Intermodulation Distortion.
IMP Intermodulation Products.
ISI Inter-Symbol-Interference.
LINC LInear amplification using Nonlinear Components.
LMS Least Mean Squares.
LO Local Oscillator.
LS Least Squares.
LTI Linear Time-Invariant.
LUT Look-Up Table.
MLP Multilayer Perceptron.
MMC Metropolis Monte Carlo.
MOSFET Metal Oxide Semiconductor Field-Effect Transistor.
MSE Mean Square Error.
NARMA Nonlinear Auto-Regressive Moving Average.
NMA Nonlinear Moving Average.
NMSE Normalized Mean Square Error.
NN Neural Network.
OBO Output Back-off.
OFDM Orthogonal Frequency Division Multiplexing.
PA Power Amplifier.
PAE Power Added Efficiency.
PAPR Peak-to-Average Power Ratio.
PD Predistortion.

pdf	probability density function.
PHY	Physical layer.
PSA	Performance Spectrum Analyzer.
PSK	Phase Shift Keying.
Q	Quadrature.
QAM	Quadrature Amplitude Modulation.
QoS	Quality of Service.
QPSK	Quadrature Phase Shift Keying.
RF	Radio Frequency.
rms	root mean square.
RRC	Root Raised Cosine.
Rx.	Receiver.
SA	Simulated Annealing.
SC	Single Carrier.
SDR	Software-Defined Radio.
SER	Symbol Error Rate.
SISO	Single-Input-Single-Output.
SNR	Signal to Noise Ratio.
SVD	Singular Value Decomposition.
SSPA	Solid State Power Amplifier.
TDNN	Time-Delayed Neural Network.
Tx.	Transmitter.
TWTA	Traveling Wave Tube Amplifiers .
UMTS	Universal Mobile Telecommunications System.
VCO	Voltage-Controlled Oscillator.
vs.	versus.
VSA	Vector Signal Analyzer.
W-CDMA	Wideband Code Division Multiple Access
WiMAX	Worldwide Interoperability for Microwave Access.
WLAN	Wireless Local Area Network.