# REFERENCES


[ABC+94] A. Aziz, F. Balarin, S.T. Cheng, R. Hojati, T. Kam, S.C. Krishnan, R.K. Ranjan, T.R. Shiple, V. Singhal, S. Taşiran, H.Y. Wang, R.K. Brayton, and A.L. Sangiovanni-Vincentelli. HSIS: A BDD-based environment for formal verification. In *Proceedings ACM/IEEE Design Automation Conference*, pages 454–459, 1994.

[ABH+97] R. Alur, R.K. Brayton, T.A. Henzinger, S. Qadeer, and S. Rajamani. Partial-order reduction in symbolic state space exploration. In *Proceedings International Workshop on Computer Aided Verification*, volume 1254 of *LNCS*, pages 340–351. Springer-Verlag, 1997.

[ACD90] R. Alur, C. Courcoubetis, and D.L. Dill. Model-checking for real-time systems. In *Proceedings of the 5th annual IEEE Symposium on Logic in Computer Science*, pages 414–425. IEEE Computer Society Press, 1990.

[ACD+92] R. Alur, C. Courcoubetis, D.L. Dill, N. Halbwachs, and H. Wong-Toi. An implementation of three algorithms for timing verification based on automata emptiness. In *Real-Time Systems Symposioum*, pages 157–166, 1992.

[ACD93] R. Alur, C. Courcoubetis, and D.L. Dill. Model-checking in dense real-time. *Information and Computation*, 104(1):2–34, 1993.

[AD90] R. Alur and D.L. Dill. Automata for modeling real-time systems. In *Automata, Languages and Programming: Proceedings of the 17th ICALP*, volume 443 of *LNCS*, pages 322–335. Springer-Verlag, 1990.

[AD94] R. Alur and D.L. Dill. A Theory of Timed Automata. *Theoretical Computer Science*, 126:183–235, 1994.

[AD96] R. Alur and D.L. Dill. Automata-theoretic verification of real-time systems. In *Formal Methods for Real-Time Computing*, Trends in Software Series, pages 55–82. John Wiley & Sons, 1996.

[AFH91] R. Alur, T. Feder, and T.A. Henzinger. The benefits of relaxing punctuality. In *Symposium on Principles of Distributed Computing*, pages 139–152, 1991.

[AH89] R. Alur and T.A. Henzinger. A really temporal logic. In *IEEE Symposium on Foundations of Computer Science*, pages 164–169, 1989.

[AH90] R. Alur and T.A. Henzinger. Real-Time Logics: Complexity and Expressiveness. In *Fifth Annual IEEE Symposium on Logic in Computer Science*, pages 390–401. IEEE Computer Society Press, 1990.

[AH97] R. Alur and T.A. Henzinger. Modularity for timed and hybrid systems. In *International Conference on Concurrency Theory*, volume 1243 of *LNCS*, pages 74–88. Springer-Verlag, 1997.

[AH99] T. Amon and H. Hulgaard. Symbolic time separation of events. In *Proceedings International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 83–93, April 1999.

[AHBB93] T. Amon, H. Hulgaard, S.M. Burns, and G. Borriello. An algorithm for exact bounds on the time separation of events in concurrent systems. In *Proceedings of the IEEE International Conference on Computer Design*, pages 166–173, 1993.

[AHM+98] R. Alur, T.A. Henzinger, F.Y.C. Mang, S. Qadeer, S.K. Rajamani, and S. Taşiran. MOCHA: Modularity in model checking. In *Proceedings International Workshop on Computer Aided Verification*, LNCS, pages 521–525. Springer-Verlag, 1998.

[AIKY92] R. Alur, A. Itai, R.P. Kurshan, and M. Yannakakis. Timing verification by successive approximations. In *Proceedings International Workshop on Computer Aided Verification*, volume 663 of *LNCS*, pages 137–150. Springer-Verlag, 1992.

[AK83] S. Aggarwal and R.P. Kurshan. Modeling elapsed time in protocol specification. In H. Rudin and C.H. West, editors, *Protocol Specification, Testing, and Verification*, volume III, pages 51–62. North-Holland, 1983.

[AK95] R. Alur and R.P. Kurshan. Timing Analysis in COSPAN. In *Hybrid Systems III: Verification and Control*, volume 1066, pages 220–231. Springer-Verlag, October 1995.

[AK96] R. Alur and R.P. Kurshan. Timing analysis in COSPAN. In *Hybrid Systems III: Control an Verification*, number 1066 in LNCS, pages 220–231. Springer-Verlag, 1996.

[Alu98] R. Alur. Timed automata, 1998. In NATO ASI Summer School on Verification of Digital and Hybrid Systems. Available at http://www.cis.upenn.edu/∼alur/Nato97.ps.gz.

[Arn94] A. Arnold. *Finite Transition Systems.* Prentice-Hall, 1994.

[BAPM81] M. Ben-Ari, A. Pnueli, and Z. Manna. The temporal logic of branching time. In *Eighth Annual Symposium on Principles of Programming Languages*, pages 164–176. ACM Press, 1981.

[BBF+01] B. Bérard, M. Bidoit, A. Finkel, F. Laroussinie, A. Petit, L. Petrucci, Ph. Schnoebelen, and P. McKenzie. *Systems and Software Verification: Model-Checking Techniques and Tools.* Springer-Verlag, 2001.

[BCM+92] J.R. Burch, E.M. Clarke, K.L. McMillan, D.L. Dill, and L.J. Hwang. Symbolic model checking: $10^{20}$ states and beyond. *Information and Computation*, 98(2):142–170, 1992.

[BD91] B. Berthomieu and M. Diaz. Modeling and verification of time dependent systems using time Petri nets. *IEEE Transactions on Software Engineering*, 17(3):259–273, 1991.

[BDM+98] M. Bozga, C. Daws, O. Maler, A. Olivero, S. Tripakis, and S. Yovine. Kronos: a model-checking tool for real-time systems. In *Proceedings International Workshop on Computer Aided Verification*, volume 1427 of *LNCS*, pages 546–550. Springer-Verlag, 1998.

[BJLY98] J. Bengtsson, B. Jonsson, J. Lilius, and W. Yi. Partial order reductions for timed systems. In *International Conference on Concurrency Theory*, pages 485–500, 1998.

[BJMY02] M. Bozga, H. Jianmin, O. Maler, and S. Yovine. Verification of asynchronous circuits using timed automata. In *Workshop on Theory and Practice of Timed Systems*, 2002.

[BLL+95] J. Bengtsson, K. Larsen, F. Larsson, P. Pettersson, and W. Yi. UPAAL – a tool suite for automatic verification of real-time systems. In *Proccedings of the 4th DIMACS Workshop on Verification and Control of Hybrid Systems*, LNCS. Springer-Verlag, 1995.

[BM92] P. Beerel and T.H.-Y. Meng. Automatic gate-level synthesis of speed-independent circuits. In *Proceedings of the IEEE/ACM International Conference on Computer Aided Design*, pages 581–587. IEEE Computer Society Press, November 1992.

[BM97] W. Belluomini and C.J. Myers. Timed event-level structures. In *Proc. International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)*, 1997.

[BM00] O. Bournez and O. Maler. On the representation of timed polyhedra. In *Proceedings International Conference on Automata, Languages and Programming (ICALP)*, volume 1853 of *LNCS*, pages 793–807. Springer-Verlag, 2000.

[BMH99] W. Belluomini, C.J. Myers, and H.P. Hofstee. Verification of delayed-reset domino circuits using ATACS. In *Proceedings International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 3–12, 1999.

[BMH01] W. Belluomini, C.J. Myers, and H.P. Hofstee. Timed circuit verification using tel structures. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 20(1):129–146, January 2001.

[BMPY97] M. Bozga, O. Maler, A. Pnueli, and S. Yovine. Some progress in the symbolic verification of timed automata. In O. Grumberg, editor, *Proceedings International Workshop on Computer Aided Verification*, volume 1254 of *LNCS*, pages 179–190. Springer-Verlag, 1997.

[Bro90] F.M. Brown. *Boolean Reasoning: The Logic of Boolean Equations.* Kluwer Academic Publishers, 1990.

[Bry86] R.E. Bryant. Graph-based algorithms for boolean function manipulation. *IEEE Transactions on Computers*, C-35(8):677–691, August 1986.

[BS91] J. Brzozowski and C. Seger. Advances in asynchronous circuit theory part ii: Bounded inertial delay models, mos circuits, design techniques. *Bulletin of the European Association for Computer Science*, 43(3):199–263, 1991.

[BSV94] F. Balarin and A.L. Sangiovanni-Vincentelli. On the automatic computation of network invariants. In *Proceedings International Workshop on Computer Aided Verification*, volume 818 of *LNCS*, pages 234–246. Springer-Verlag, 1994.

[BSV95] F. Balarin and A.L. Sangiovanni-Vincentelli. An iterative approach to verification of real-time systems. *Formal Methods in System Design*, 6:67–95, January 1995.

[Bur89] J.R. Burch. Combining CTL, trace theory and timing models. In *Proceedings of the First Workshop on Automatic Verication Methods for Finite State Systems*, volume 407, pages 197–212. LNCS, 1989.

[Bur92] J.R. Burch. Delay models for verifying speed-dependent asynchronous circuits. In *International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, March 1992.

[Bur96] S.M. Burns. General condition for the decomposition of state holding elements. In *Proceedings International Symposium on Advanced Research in Asynchronous Circuits and Systems*, March 1996.

[BW90] J.C.M. Baeten and W.P. Weijland. *Process Algebra*. Cambridge University Press, 1990.

[CDS93] B. COates, A. Davis, and K. Stevens. The post office experience: Designing a large asynchronous chip. *Integration, the VLSI journal*, 15(3):341–366, October 1993.

[CDY99] S. Chakraborty, D.L. Dill, and K.Y. Yun. Min-max timing analysis and an application to asynchronous circuits. *Proceedings of the IEEE*, 87(2):332–346, February 1999.

[CE81] E.M. Clarke and E.A. Emerson. Synthesis of Synchronization Skeletons for Branching Time Temporal Logic. In *Logics of Programs: Workshop*, volume 131 of *LNCS*. Springer-Verlag, 1981.

[CES86] E.M. Clarke, E.A. Emerson, and A.P. Sistla. Automatic verification of finite-state concurrent systems using temporal logic specifications. *ACM Transactions on Programming Languages and Systems*, 8(2):244–263, 1986.

[CGL92] E.M. Clarke, O. Grumberg, and D.E. Long. Model checking and abstraction. *ACM Transactions on Programming Languages*, 16(5):1512–1542, 1992.

[CGP00] E.M. Clarke, O. Grumberg, and D.A. Peled. *Model Checking*. The MIT Press, 2000.

[Chu87] T.-A. Chu. *Synthesis of Self-timed VLSI Circuits from Graph-theoretic Specifications*. PhD thesis, MIT, June 1987.

[CJEF96] E.M. Clarke, S. Jha, R. Enders, and T. Filkorn. Exploiting symmetry in temporal logic model checking. *Formal Methods in System Design*, 9(1/2):77–104, 1996.

[CKK+97] J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, and A. Yakovlev. Petrify: a tool for manipulating concurrent specifications and synthesis of asynchronous controllers. *IEICE Transactions on Information and Systems*, E80-D(3):315–325, 1997.

[CKK+98] J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, and A. Yakovlev. Lazy transition systems: application to timing optimization of asynchronous circuits. In *Proceedings of the IEEE/ACM International Conference on Computer Aided Design*, November 1998.

[CKK+02] J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, and A. Yakovlev. *Logic Synthesis for Asynchronous Controllers and Interfaces*. Springer-Verlag, 2002.

[CKLY98] J. Cortadella, M. Kishinevsky, L. Lavagno, and A. Yakovlev. Deriving Petri nets from finite transition systems. *IEEE Transactions on Computers*, 47(8):859–882, 1998.

[CLM89] E. Clarke, D.E. Long, and K.L. McMillan. Compositional model checking. In *Proceedings of the Fourth Annual IEEE Symposium on Logic in Computer Science*, June 1989.

[CPS93] R. Cleaveland, J. Parrow, and B. Steffen. The Concurrency Workbench: A Semantics-Based Tool for the Verification of Concurrent Systems. *ACM Transactions on Programming Languages and Systems*, 15(1):36–72, January 1993.

[CW96] E.M. Clarke and J.M. Wing. Formal Methods: State of the Art and Future Directions. *ACM Computing Surveys*, 28(4):626–643, December 1996.

[CY91] C. Courcoubetis and M. Yannakakis. Minimum and maximum delay problems in real-time systems. In *Proceedings International Workshop on Computer Aided Verification*, volume 575 of *LNCS*, pages 399–409. Springer-Verlag, 1991.

[DGG97] D. Dams, R. Gerth, and O. Grumberg. Abstract interpretation of reactive systems. *ACM Transactions on Programming Languages and Systems*, 19(2):253–291, March 1997.

[DHWT91] D.L. Dill, A.J. Hu, and H. Wong-Toi. Checking for language inclusion using simulation relations. In *Proceedings International Workshop on Computer Aided Verification*, volume 575 of *LNCS*, pages 255–265. Springer-Verlag, 1991.

[Dil89a] David L. Dill. *Trace Theory for Automatic Hierarchical Verification of Speed-Independent Circuits*. ACM Distinguished Dissertations. MIT Press, 1989.

[Dil89b] D.L. Dill. Timing assumptions and verification of finite-state concurrent systems. In *Automatic Verification Methods for Finite State Systems*, volume 407 of *LNCS*, pages 197–212. Springer-Verlag, 1989.

[DKMW92] S. Devadas, K. Keutzer, S. Malik, and A. Wang. Verification of asynchronous interface circuits with bounded wire delays. In *Proceedings of the IEEE/ACM International Conference on Computer Aided Design*, pages 188–195, November 1992.

[EC82] E.A. Emerson and E.M. Clarke. Using branching time temporal logic to synthesize synchronization skeletons. *Science of Computer Programming*, 2(3):241–266, 1982.

[EH86] E.A. Emerson and J.Y. Halpern. "Sometimes" and "Not Never" revisited: On branching versus linear time temporal logic. *Journal of the ACM*, 33(1):151–178, 1986.

[Eme90] E.A. Emerson. Temporal and modal logic. In J. van Leuven, editor, *Handbook of Theoretical Computer Science*, volume B, pages 995–1072. Elsevier Science Publishers, 1990.

[EMSS90] E.A. Emerson, A.K. Mok, A.P. Sistla, and J. Srinivasan. Quantitative temporal reasoning. In *Proceedings International Workshop on Computer Aided Verification*, volume 531 of *LNCS*, pages 136–145. Springer-Verlag, 1990.

[EN94] J. Esparza and M. Nielsen. Decidability issues for petri nets - a survey. *Bulletin of the European Association for Theoretical Computer Science*, 52:245–262, 1994.

[ES96] E.A. Emerson and A.P. Sistla. Symmetry and model checking. *Formal Methods in System Design (Special Issue on Symmetry in Automatic Verification)*, 9, 1996.

[GA98] M.K. Ganai and A. Aziz. Efficient coverage directed state space search. In *Proceedings International Workshop on Logic Synthesis*, 1998.

[GL94] O. Grumberg and D.E. Long. Model checking and modular verification. *ACM Transactions on Programming Languages*, 16:843–872, 1994.

[GM93] M.J.C. Gordon and T.F. Melham. *Introduction to HOL: A Theorem Proving Environment for Higher-Order Logic*. Cambridge University Press, 1993.

[GMW79] M.J.C. Gordon, R. Milner, and C.P. Wadsworth. *Edinburgh LCF: a mechanised logic of computation*, volume 78. Springer-Verlag, New York, NY, USA, 1979.

[Gor89] M.J.C. Gordon. Lectures on the Specification and Verification of Hardware. Course Notes, University of Cambridge, 1989.

[Gun93] J. Gunawardena. Timing analysis of digital circuits and the theory of min-max functions. In *Int. Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, 1993.

[Gup92] A. Gupta. Formal Hardware Verification Methods: A Survey. *Formal Methods in System Design*, 1:151–238, 1992.

[GW91] P. Godefroid and P. Wolper. A partial approach to model checking. In *Sixth Annual Symposium on Logic in Computer Science*, pages 406–415. IEEE Computer Society Press, 1991.

[HB94] H. Hulgaard and S.M. Burns. Bounded delay timing analysis of a class of CSP programs with choice. In *Proceedings International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 2–11, November 1994.

[Hen90] T.A. Henzinger. Half-Order Modal Logic: How to Prove Real-Time Properties. In *Proceedings of the 9th Annual Symposium on Principles of Distributed Computing*, pages 281–296. ACM Press, 1990.

[Hen98] T.A. Henzinger. It's about time: Real-time logics reviewed. In *International Conference on Concurrency Theory*, volume 1466 of *LNCS*, pages 439–454. Springer-Verlag, 1998.

[HHWT97] T.A. Henzinger, P. H. Ho, and H. Wong-Toi. HYTECH: A Model Checker for Hybrid Systems. *International Journal on Software Tools for Technology Transfer*, 1(1-2):110–122, 1997.

[HLP90] E. Harel, O. Lichtenstein, and A. Pnueli. Explicit Clock Temporal Logic. In *Proceedings of the Fifth Annual IEEE Symposium on Logic in Computer Science*, pages 402–413. IEEE Computer Society Press, 1990.

[HMP91] T.A. Henzinger, Z. Manna, and A. Pnueli. Temporal proof methodologies for real-time systems. In *Proceedings of the 18th ACM Symposium on Principles of Programming Languages*, pages 353–366, 1991.

[HMP92a] T.A. Henzinger, Z. Manna, and A. Pnueli. Timed transition systems. In *REX Workshop. Real-Time: Theory in Practice*, volume 600 of *LNCS*, pages 226–251. Springer-Verlag, 1992.

[HMP92b] T.A. Henzinger, Z. Manna, and A. Pnueli. What good are digital clocks? In *Proceedings International Conference on Automata, Languages and Programming (ICALP)*, volume 623 of *LNCS*, pages 545–558. Springer-Verlag, 1992.

[HNSY92] T.A. Henzinger, X. Nicollin, J. Sifakis, and S. Yovine. Symbolic Model Checking for Real-Time Systems. In *7th. Symposium of Logics in Computer Science*, pages 394–406. IEEE Computer Scienty Press, 1992.

[Hoa85] C.A.R. Hoare. *Communicating Sequential Processes.* Prentice-Hall, 1985.

[Hol97] G. Holzmann. The model checker SPIN. *IEEE Transactions on Software Engineering*, 23:279–295, 1997.

[HPR97] N. Halbwachs, Y.E. Proy, and P. Roumanoff. Verification of real-time systems using linear relation analysis. *Formal Methods in System Design*, 11(2):157–185, 1997.

[HRS98] T.A. Henzinger, J.F Raskin, and P.Y. Schobbens. The regular real-time languages. In *Automata, Languages and Programming*, pages 580–591, 1998.

[Huf54] D.A. Huffman. The synthesis of sequential switching circuits. *J.Franklin Institute*, 257:161–190,275–303, March 1954.

[Hul95] H. Hulgaard. *Timing Analysis and Verification of Timed Asynchronous Circuits.* PhD thesis, Department of Computer Science, University of Washington, 1995.

[ISO89] ISO. ISO/IEC: Information Processing Systems – Open Systems Interconnection – LOTOS, A formal description technique based on the temporal ordering of observational behaviour, ISO 8807, February 1989.

[Jen92] K. Jensen. *Coloured Petri Nets 1: Basic Concepts, Analysis Methods and Practical Use.* Springer-Verlag, 1992.

[JM86] F. Jahanian and A.K. Mok. Safety analysis of timing properties in real-time systems. *IEEE Transaction on Software Engineering*, 12(9):890–904, 1986.

[JR91] K. Jensen and G. Rozenberg, editors. *High-Level Petri Nets — Theory and Application.* Springer-Verlag, 1991.

[KBS02] H. Kim, P.A. Beerel, and K. Stevens. Relative timing based verification of timed circuits and systems. In *Proceedings International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 115–124, April 2002.

[KCKL99] A. Kondratyev, J. Cortadella, M. Kishinevsky, and L. Lavagno. Logic decomposition of speed-independent circuits. *Proceedings of the IEEE*, 87(2):347–362, February 1999.

[KE96] A. Kovalyov and J. Esparza. A polynomial algorithm to compute the concurrency relation of free-choice signal transition graphs. In *Proceedings of the International Workshop on Discrete Event Systems*, pages 1–6, August 1996.

[KN02] R. Kaivola and N. Narasimhan. Formal verification of the Pentium 4 Floating-Point Multiplier. In *Proceedings Design, Automation and Test in Europe*, pages 20–27, Paris, France, March 2002.

[Koy90] R. Koymans. Specifying real-time properties with metric temporal logic. In *LNCS*, volume 443, pages 255–299. Springer-Verlag, 1990.

[KP88] S. Katz and D.A. Peled. An Efficient Verification Method for Parallel and Distributed Programs. In *Workshop on Linear Time, Branching Time and Partial Order in Logics and Models for Concurrency*, volume 354 of *LNCS*, pages 489–507. Springer-Verlag, 1988.

[Kro99] T. Kropf. *Introduction to Formal Hardware Verification.* Springer-Verlag, 1999.

[KT94] A. Kondratyev and A. Taubin. Verification of speed-independent circuits by STG unfoldings. In *Proceedings International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 64–75, November 1994.

[Kur94] R.P. Kurshan. *Computer–Aided Verification of Coordinated Processes – An Automata Theoretic Approach.* Princeton University Press, 1994.

[LG95] C. Leung and M. Greenstreet. A simple proof checker for timing verification. In *ACM International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, pages 294–305, November 1995.

[Lio96] J.L. Lions. Ariane 5: Flight 501 failure. *ESA: Report by the Inquiry Board*, July 1996. Available at http://www.esa.int/export/esaCP/Pr_33_1996_p_EN.html.

[Lon93] D.E. Long. *Model Checking, Abstraction and Compositional Verification.* PhD thesis, Carnegie Mellon University, July 1993.

[LP85] O. Lichtenstein and A. Pnueli. Checking that finite state concurrent programs satisfy their linear specification. In *12th annual Symposium on Principles of Programming Languages*, pages 97–107. ACM Press, 1985.

[LPY95] K.G. Larsen, P. Pettersson, and W. Yi. Compositional and symbolic model-checking of real-time systems. In *IEEE Real-Time Systems Symposium*, pages 76–89, 1995.

[Maz88] A. Mazurkiewicz. Basic notions of trace theory. In J. W. Baker, W. P. de Roever, and G. Rozenberg, editors, *Linear Time, Branching Time, and Partial Order in Logics and Models for Concurrency*, volume 354 of *LNCS*, pages 285–363. Springer-Verlag, 1988.

[MB59] D. E. Muller and W. S. Bartky. A theory of asynchronous circuits. In *Proceedings of an International Symposium on the Theory of Switching*, pages 204–243. Harvard University Press, April 1959.

[McM92] K. McMillan. Using unfoldings to avoid the state explosion problem in the verification of asynchronous circuits. In *Proceedings International Workshop on Computer Aided Verification*, volume 663 of *LNCS*, pages 164–177. Springer-Verlag, 1992.

[McM93] K.L. McMillan. *Symbolic Model Checking.* Kluwer Academic Publishers, 1993.

[McM97] K.L. McMillan. A compositional rule for hardware design refinement. In *Proceedings International Workshop on Computer Aided Verification*, volume 1254 of *LNCS*, pages 24–35. Springer-Verlag, 1997.

[MD92] K.L. McMillan and D.L. Dill. Algorithms for interface verification. In *Proceedings of the IEEE International Conference on Computer Design*, October 1992.

[Mel88] T.F. Melham. Abstraction mechanisms for hardware verification. In *VLSI Specification, Verification and Synthesis*, pages 129–157. Kluwer Academic Publishers, 1988.

[MF76] P. Merlin and D.J. Faber. Recoverability of communication protocols. *IEEE Transactions on Communications*, 24(9):1036–1043, September 1976.

[Mil89] R. Milner. *Communication and Concurrency.* Prentice-Hall, 1989.

[MM93] C.J. Myers and T.H.-Y. Meng. Synthesis of timed asynchronous circuits. *IEEE Transaction on VLSI Systems*, 1(2):106–119, June 1993.

[MP95] O. Maler and A. Pnueli. Timing analysis of asynchronous circuits using timed automata. In P.E. Camurati and H. Eveking, editors, *Proceedings of CHARME'95*, volume 987 of *LNCS*, pages 189–205. Springer-Verlag, 1995.

[MP96] Z. Manna and A. Pnueli. Clocked transition systems. Technical Report STAN-CS-TR-96-1566, Computer Science Department, Stanford University, April 1996.

[MRM99] C.J. Myers, T.G. Rokicki, and T.H.-Y. Meng. POSET timing and its application to the synthesis and verification of gate-level timed circuits. *IEEE Transactions on Computer-Aided Design*, 18(6):769–786, 1999.

[Mur89] T. Murata. Petri nets: Properties, analysis and applications. *Proceedings of the IEEE*, 77(4):541–574, April 1989.

[Mye01] C.J. Myers. *Asynchronous Circuit Design*. John Wiley & Sons, July 2001.

[Neu] P.G. Neumann. The Risks Digest. Forum on Risks to the Public in Computers and Related Systems. ACM Commitee on Computers and Public Policy. Available at http://www.infowar.com/iwftp/risks/all_risks_index.shtml.

[NK94] C.D. Nielsen and M. Kishinevsky. Performance analysis based on timing simulation. In *Proceedings ACM/IEEE Design Automation Conference*, pages 70–76, June 1994.

[Now93] S.M. Nowick. *Automatic synthesis of burst-mode asynchronous controllers*. PhD thesis, Stanford University, 1993.

[NPW81] M. Nielsen, G. Plotkin, and G. Winskel. Petri Nets, Event Structures and Domains. *Theoretical Computer Science*, 13:85–108, 1981.

[NRT92] M. Nielsen, G. Rozenberg, and P. S. Thiagarajan. Elementary transition systems. *Theoretical Computer Science*, 96(1):3–33, 1992.

[OL82] S. Owicki and L. Lamport. Proving liveness properties of concurrent programs. *ACM Transactions on Programming Languages and Systems*, 4(3):455–495, 1982.

[ORSS94] S. Owre, J.M. Rushby, N. Shankar, and M.K. Srivas. A Tutorial on Using PVS for Hardware Verification. In T. Kropf and R. Kumar, editors, *Proceedings of the 2nd International Conference on Theorem Provers in Circuit Design (TPCD94)*, volume 901 of *LNCS*, pages 258–279, Bad Herrenalb, Germany, 1994. Springer-Verlag.

[Ost90] J.S. Ostroff. *Temporal Logic for Real-Time Systems*. Research Studies Press / Wiley, 1990.

[PCKP00] M.A. Peña, J. Cortadella, A. Kondratyev, and E. Pastor. Formal verification of safety properties in timed circuits. In *Proceedings International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 2–11, Eilat, Israel, April 2000.

[PCP99] E. Pastor, J. Cortadella, and M.A. Peña. Structural methods to improve the symbolic analysis of petri nets. In *International Conference on Application and Theory of Petri Nets*, volume 1639 of *LNCS*, pages 26–45. Springer-Verlag, June 1999.

[PCSP02] M.A. Peña, J. Cortadella, A. Smirnov, and E. Pastor. A case study for the verification of complex timed circuits: IPCMOS. In *Proceedings Design, Automation and Test in Europe*, pages 44–51, Paris, France, March 2002.

[Pel96] D.A. Peled. Combining Partial Order Reductions with on-the-fly Model-Checking. *Formal Methods in System Design*, 8(1):39–64, 1996.

[Pet62] C.A. Petri. *Kommunikation mit Automaten*. PhD thesis, Bonn, Institut für Instrumentelle Mathematik, Schriften des IIM Nr. 3, 1962. English translation, "Communication with Automata", Griffiss Air Force Base, Technical Report RADC-TR-65-377, vol. 1, Suppl. 1, 1966.

[Pet81] J.L. Peterson. *Petri Net Theory and the Modeling of Systems*. Prentice-Hall, 1981.

[Pet97] I. Peterson. Pentium bug revisited. *The Mathematical Association of America: MAA Online*, May 1997. Available at http://www.maa.org/mathland/mathland_5_12.html.

[PH88] A. Pnueli and E. Harel. Applications of Temporal Logic to the Specification of Real Time Systems. In M. Joseph, editor, *Formal Techniques in Real Time and Fault Tolerant Systems*, volume 331 of *LNCS*, pages 84–98. Springer-Verlag, 1988.

[Pnu77] A. Pnueli. The temporal logic of programs. In *Proceedings of the 18th Annual Symposium on the Foundations of Computer Science*, pages 46–57. IEEE Computer Society Press, 1977.

[Pnu81] A. Pnueli. The temporal logic of concurrent programs. *Theoretical Computer Science*, 13:45–60, 1981.

[Pnu84] A. Pnueli. In transition for global to modular temporal reasoning about programs. In *Logics and Models of Concurrent Systems*, volume 13 of *NATO ASI Series*. Springer-Verlag, 1984.

[PPa] E. Pastor and M.A. Peña. Transition System Interchange Format, TSIF. Soon available at http://research.ac.upc.es/VLSI/transyt/transyt.html.

[PPb] E. Pastor and M.A. Peña. TRANSYT user's manual. Soon available at http://research.ac.upc.es/VLSI/transyt/transyt.html.

[PP03] E. Pastor and M.A. Peña. Efficient hybrid reachability analysis for asynchronous concurrent systems. Technical Report UPC-DAC-2003-6, Department of Computer Architecture, Technical University of Catalonia, January 2003.

[PRCB94] E. Pastor, O. Roig, J. Cortadella, and R. M. Badia. Petri net analysis using boolean manipulation. In *15th International Conference on Application and Theory of Petri Nets*, volume 815 of *LNCS*, pages 416–435. Springer-Verlag, June 1994.

[QS81] J. Queille and J. Sifakis. Specification and Verification of Concurrent Systems in CÆSAR. In *In Proceedings of the 5th International Symposium on Programming*, volume 137 of *LNCS*, pages 337–351. Springer-Verlag, 1981.

[Ram74] C. Ramchandani. *Analysis of Asynchronous Concurrent Systems by Timed Petri Nets*. PhD thesis, MIT, February 1974.

[RCP95] O. Roig, J. Cortadella, and E. Pastor. Hierarchical gate-level verification of speed-independent circuits. In *Asynchronous Design Methodologies*, pages 129–137. IEEE Computer Society Press, May 1995.

[RE88] G. Rozenberg and J. Engelfriet. Elementary net systems. In W. Reisig and G. Rozenberg, editors, *Lectures on Petri Nets I: Basic Models. Advances in Petri Nets 1988*, volume 1491 of *LNCS*, pages 12–121, 1988.

[Rei85] W. Reisig. *Petri Nets: An Introduction*. Springer-Verlag, 1985.

[RM94] T.G. Rokicki and C.J. Myers. Automatic verification of timed circuits. In David L. Dill, editor, *Proceedings International Workshop on Computer Aided Verification*, volume 818 of *LNCS*, pages 468–480. Springer-Verlag, 1994.

[Rok93] T. Rokicki. *Representing and Modeling Digital Circuits.* PhD thesis, Stanford University, December 1993.

[Ros94] A.W. Roscoe. Model-Checking CSP. In A.W. Roscoe, editor, *A Classical Mind: Essays in Honour of C.A.R. Hoare*, pages 353–378. Prentice-Hall, 1994.

[RSG+99] S. Rotem, K. Stevens, R. Ginosar, P. Beerel, C. Myers, K. Yun, R. Kol, C. Dike, M. Roncken, and B. Agapiev. RAPPID: An asynchronous instruction length decoder. In *Proceedings International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 60–70, April 1999.

[Rus93] J. Rushby. Formal Methods and Digital Systems Validation for Airborne Systems. Technical Report SRI-CSL-93-7, Computer Science Laboratory, SRI International, December 1993. Also available as NASA Contractor Report 4551.

[RY85] L. Rosenblum and A. Yakovlev. Signal graphs: From self-timed to timed ones. In *International Workshop on Timed Petri Nets*, pages 199–206, July 1985.

[SB97] R.H. Sloan and U. Buy. Stubborn sets for real-time Petri nets. *Formal Methods in System Design*, 11(1):23–40, July 1997.

[Sei80] C.L. Seitz. System timing. In *Introduction to VLSI Systems*, chapter 7. Mead & Conway, Addison-Wesley, 1980.

[SF01] J Sparsø and S. Furber, editors. *Principles of Asynchronous Circuit Design. A Systems Perspective.* European Low-Power Initiative for Electronic System Design. Kluwer Academic Publishers, 2001.

[SGR99] K. Stevens, R. Ginosar, and S. Rotem. Relative timing. In *Proceedings International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 208–218, April 1999.

[Spi88] J. Spivey. *Understanding Z: A Specification Language and its Formal Semantics.* Cambridge University Press, 1988.

[SRC+00] S. Schuster, W. Reohr, P. Cook, D. Heidel, M. Immediato, and K. Jenkins. Asynchronous Interlocked Pipelined CMOS Circuits Operating at $3.3 - 4.5$GHz. In *IEEE International Solid-State Circuits Conference (ISSCC)*, pages 292–293, February 2000.

[SSL+92] E.M. Sentovich, K.J. Singh, L. Lavagno, C. Moon, R. Murgai, A. Saldanha, H. Savoj, P.R. Stephan, R.K. Brayton, and A. Sangiovanni-Vincentelli. SIS: A System for Sequential Circuits Synthesis. Technical Report M92/41, UCB/ERL, May 1992.

[Ste02] K. Stevens. Private communication, December 2002.

[Sut89] I.E. Sutherland. Micropipelines. *Communications of the ACM*, June 1989. Turing Award Lecture.

[SY96] A. Semenov and A. Yakovlev. Verification of asynchronous circuits using time Petri-net unfolding. In *Proceedings ACM/IEEE Design Automation Conference*, 1996.

[TAKB96] S. Taşıran, R. Alur, R.P. Kurshan, and R.K. Brayton. Verifying abstractions of timed systems. In *International Conference on Concurrency Theory*, volume 1119 of *LNCS*, pages 546–562. Springer-Verlag, 1996.

[Tho81] W. Thomas. A combinatorial approach to the theory of $\omega$-automata. *Information and Computation*, 48:261–283, 1981.

[TKY+98] S. Taşiran, S. Khatri, S. Yovine, R.K. Brayton, and A. Sangiovanni-Vincentelli. A timed-automaton-based method for accurate computation of circuit delay in the presence of cross-talk. In *Proceedings of Formal Methods in Computer-Aided Design*, LNCS. Springer-Verlag, 1998.

[VdJL96] E. Verlind, G. de Jong, and B. Lin. Efficient partial enumeration for timing analysis of asynchronous systems. In *Proceedings ACM/IEEE Design Automation Conference*, 1996.

[VGM92] P. Vanbekbergen, G. Goossens, and H. De Man. Specification and analysis of timing constraints in signal transition graphs. In *Proceedings Design, Automation and Test in Europe*, pages 302–306, March 1992.

[VK98] A. Valmari and I. Kokkarinen. Unbounded verification results by finite-state compositional techniques: $10^{\text{any}}$ states and beyond. In *IEEE International Conference on Application of Concurrency to System Design (CSD)*, pages 75–85, March 1998.

[Wal95] E.A. Walkup. *Optimization of Linear Max-Plus Systems with Application to Timing Analysis*. PhD thesis, Department of Computer Science and Engineering, University of Washington, 1995.

[YD98] C. Han Yang and D.L. Dill. Validation with guided search of the state space. In *Proceedings ACM/IEEE Design Automation Conference*, pages 599–604, 1998.

[Yov97] S. Yovine. KRONOS: A verification tool for real-time systems. *International Journal on Software Tools for Technology Transfer*, 1(1-2):123–133, 1997.

[YSSC93] T. Yoneda, A. Shibayama, B. Schlingloff, and E.M. Clarke. Efficient verification of parallel real-time systems. In *Proceedings International Workshop on Computer Aided Verification*, LNCS, pages 321–332. Springer-Verlag, 1993.