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Current Sharing Control Strategy for IGBTs Connected in Parallel

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Abstract

This work focuses on current sharing between punch-through insulated gate bipolar transistors (IGBTs) connected in parallel and evaluates the mechanisms that allow overall current balancing. Two different control strategies are presented. These strategies are based on the modification of transistor gate-emitter control voltage V_{GE} by using an active gate driver circuit. The first strategy relies on the calculation of the average value of the current flowing through all parallel-connected IGBTs. The second strategy is proposed by the authors on the basis of a current cross reference control scheme. Finally, the simulation and experimental results of the application of the two current sharing control algorithms are presented.

Key words: Current imbalance, Current sharing, IGBT parallel operation

I. INTRODUCTION

In power converters operating at high current ranges, the ratings of insulated gate bipolar transistors (IGBTs) currently available exceed standard values. As a consequence, multiple IGBTs can be connected in parallel to provide the required current. For converters involving currents of a few kA, IGBT modules are typically used; however, multiple IGBT modules must be connected in parallel in applications exceeding tens of kA. By contrast, in applications influenced by switch costs, the use of parallel switch configurations based on discrete IGBTs is suggested (instead of using one IGBT module) because it improves the cost-per-ampere ratio [1]-[3].

One important drawback of the parallel connection of IGBTs is related to the unbalanced current sharing between transistors. In this regard, activities that deal with this issue are focused on two different areas. One area deals with issues related to the combination of multiple IGBT chips (or IGBT dies) in parallel inside an IGBT module and their sharing of the same substrate [4]-[7]. The second area of activity focuses on issues related to the parallel interconnection of IGBTs integrated in different substrates, as in the case of the interconnections of IGBT modules [8], [9] and discrete IGBTs [10]. The problem of the inhomogeneous sharing of currents between IGBTs connected in parallel can be addressed in two ways: static current sharing and dynamic current sharing. This two-way approach is necessary because the influential parameters in both cases are different. Hence, manufacturers of IGBT modules and many researchers have introduced several techniques to ensure homogenous current sharing within parallel-connected IGBTs.

IGBT manufacturers suggest the use of passive technical measures based on the following:

- IGBTs with the same saturation voltage ranges for parallel interconnection should be used.
- Parallel-connected IGBTs should either be thermally coupled or not be thermally coupled depending on their temperature coefficient (TC). When TC is negative, the devices should be mounted on the same heat sink and near each other to maintain uniform temperatures between paralleled devices. When TC is positive, the thermal decoupling of IGBTs is suggested [11].
- The power circuit and gate driver circuit layout and connections with and between IGBTs in parallel must

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feature low inductance and symmetric layout.

- The same gate driver circuit must be used for all paralleled devices to avoid different time delays. Nevertheless, the use of one gate resistor for each IGBT to reduce the possibility of oscillations between parallel-connected devices and reduce turn-on delays caused by the Miller–Plateau effect is strongly recommended. However, some manufacturers (such as CONCEPT) develop gate driver circuits that are specially tailored to this application; these gate driver circuits feature very small signal propagation delays and narrow tolerances [12].
- A total derating current factor should be applied as a function of the number of devices connected in parallel.

Several manufacturers of IGBTs, such as IXYS [3], ABB [13], Infineon [14], Fuji Electric [15], Semikron [16], and Mitsubishi Electric [17], publish interesting application notes related to these subjects.

The problem in the inhomogeneous sharing of currents between parallel-connected IGBTs has been addressed in the literature [18], and most studies point to strategies based on active gate driver circuits to avoid this issue. Regarding the dynamic current sharing problem, the strategies proposed are based on electronically adjustable gate resistors [19]-[21] or on the delay of the turning ON and OFF of IGBT signals [22]-[24]. By contrast, the strategies devoted to static current balancing (using active gate driver circuits) are based on the control of the gate-emitter voltages of IGBTs [19], [22], [23], [25]. Techniques based on the high frequency modulation of gate-emitter pulse voltages were reported in [26].

In accordance with the previous discussion, the present work discusses and compares two control strategies for improving the static current sharing between IGBTs connected in parallel. The first strategy [18], [27] is based on the determination of the average value of the current in all parallel-connected IGBTs. The second strategy, which is proposed by the authors, utilizes a scheme involving the cross references of current values based on a daisy chain structure (similar to the structure proposed in [28]). The two control strategies are implemented in the same active gate driver circuit according to the control of the gate-emitter voltages of IGBTs to compare their performances.

A brief research on the characteristics that affect the balance of the current in IGBTs connected in parallel is presented in Section II. With the aim of equalizing the static current sharing between transistors, a comparison of the current sharing control strategies is performed in Section III. Some authors propose a current sharing control scheme based on the determined average value of the total current as a reference for each IGBT connected in parallel [18], [27]. The error introduced in the determination of this average value shows the limitation of the method. The proposed control method is based on a current cross reference algorithm to avoid controller saturation, which occurs when the average current method is applied. The simulation results, gate driver circuit implementation, and experimental results of the control strategies are presented in Sections IV, V, and VI, respectively.

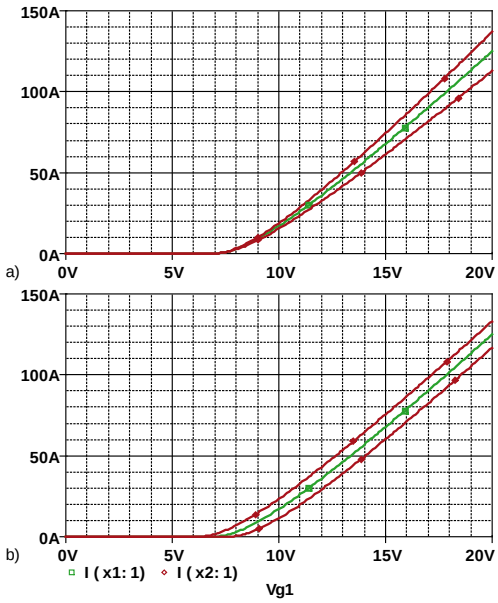

Fig. 1. Relation of V_{GE} and I_C in an IGBT. (a) Modifying ±10% of the K_P nominal value. (b) Modifying ±10% of the V_{GEth} nominal value.

II. CURRENT SHARING

The parameters transconductance (g_{fs}) and gate-emitter threshold voltage (V_{GEth}) have the highest effect on current balancing in IGBTs connected in parallel, as can be deduced from Eq. (1). Fig. 1 shows the relationship between the collector current (I_C) and these two parameters.

$$I_C = \frac{g_{fs}}{2}\left(V_{GE} - V_{GEth}\right) \tag{1}$$

$$V_{GE} = V_{driver} - V_{Rg} - v_{Le} = V_{driver} - V_{Rg} - L_e \frac{dI_C(t)}{dt} \tag{2}$$

The gate-emitter voltage (V_{GE}) is imposed by the gate driver circuit (V_{driver}). To ensure the saturation of the transistor, a voltage value greater than V_{GEth} must be applied. Nevertheless, the values of the parasitic inductor (L_e) and gate resistor (R_g) of the transistor emitter are important in current sharing, as stated in Eq. (2).

The values of L_e and R_g modify the switching transient, which in turn affects the dynamic current sharing between IGBTs. This effect is related to the collector current variation when the switch is closed (from OFF to ON), which causes high voltage values in L_e and leads to the modification of the total gate-source control voltage.

Fig. 1(a) shows how a ±10% variation in the nominal value of the IGBT transconductance (K_P) modifies the I_C-V_{GE} ratio.

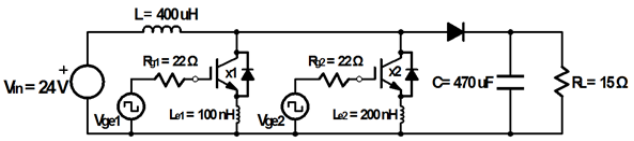

Fig. 2. Boost converter with a power switch based on two IGBT transistors connected in parallel.

TABLE I
SIMULATION PARAMETERS

Symbol	Description	Value
x_1, x_2	IGBT: STGP7NC60HD [1]	
V_{GEth1} V_{GEth2}	Gate-emitter threshold voltage [1]	6.9550 V 6.2595 V
K_{P1} K_{P2}	MOS Transconductance [1]	7.4778 A/V^2 6.7980 A/V^2
R_{g1}, R_{g2}	Gate resistor in IGBT x_1 and x_2	22 Ω
L_{e1} L_{e2}	Parasitic emitter inductance	100 nH 200 nH
L	Boost inductor	400 µH
C	Boost output capacitor	470 µF
R_L	Load resistor	15 Ω
V_{in}	Boost input voltage	24 V
DC	Boost duty cycle	42%

[1] Parameters extracted from the SPICE simulation model provided by ST Microelectronics

In the same way, Fig. 1(b) shows how a ±10% variation in V_{GEth} modifies the I_C-V_{GE} characteristic. The tolerances to the values of these technological parameters result in an unbalanced current sharing in IGBTs connected in parallel. Eq. (3) shows that parameter K_P is part of the forward transconductance used in Eq. (1).

$$g_{fs} = K_P \frac{1}{1-\alpha_{PNP}} \frac{W}{L}(V_{GE} - V_{GEth}) \tag{3}$$

To expose this behavior, a power switch based on two parallel-connected IGBTs operating in a boost converter is simulated. The simulation circuit is shown in Fig. 2, and the simulation conditions are summarized in Table I.

Fig. 3 shows the collector current through IGBTs (I_{x1} and I_{x2}) and boost inductor current (I_L). Two different situations can be observed from the simulation results.

Fig. 3(a) shows the current flowing through the two IGBTs when only two different values of the emitter parasitic inductor are considered (L_{e1} = 100 nH and L_{e2} = 200 nH). An accurate current sharing is observed in this case.

Fig. 3(b) shows the simulation results of the modification of the transistor transconductance (K_P) and gate-emitter threshold voltage (V_{GEth}), as defined in Table I (K_{P1} = 7.4778 A/V^2, V_{GEth1} = 6.9550 V; and K_{P2} = 6.7980 A/V^2, V_{GEth2} = 6.2595 V). In this case, the obtained waveforms show an unbalanced current sharing between the two IGBTs.

To reduce the observed current unbalance, the effect in the collector current (I_C) of each transistor is analyzed by modifying the values of the gate resistor (R_g) and the applied

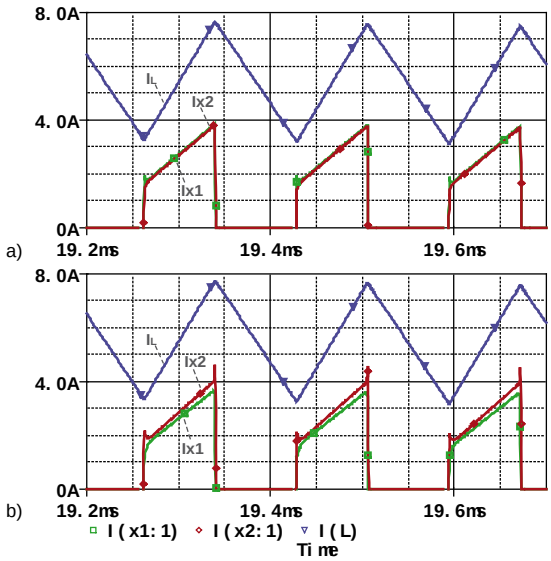

Fig. 3. Collector current of transistors x_1 and x_2 (a) with the same V_{GEth} and K_P parameters and (b) with the parameters modified, as shown in Table I.

gate-emitter control (V_{GE}) voltage. These new simulations and the obtained results are described and shown in the following paragraphs.

A. Effect of Gate Resistor Values

Different gate resistor (R_g) values imply changes in the charge and discharge time constants of the gate stray capacitances of IGBTs. The use of different gate resistor (R_g) values is a method that is usually applied in transistor driver circuits to reduce switching losses; such method improves the I_C transient conditions in switching operation [29]. Fig. 4 shows the effect obtained for the collector current (I_C) by modifying the gate resistor value. These results imply that the variation of the gate resistor value modifies the response of the switching process and improves the behavior of the transient response when the transistor is turned ON; however, this method does not improve the static current balancing between the IGBTs connected in parallel.

B. Variation of Gate Voltage Values

Different gate-emitter voltage values are applied to transistor control to analyze the effect on the collector current. Fig. 5 shows how this change improves the current balancing in IGBT transistors connected in parallel.

The next section is devoted to the analysis of two different current sharing control strategies. According to the previous discussion, these two strategies are based on the variations of gate voltage values to improve static current balancing between IGBTs connected in parallel.

III. CURRENT SHARING CONTROL STRATEGIES

Reference [26] presents a range of techniques to increase voltages and currents in equivalent power switches based on

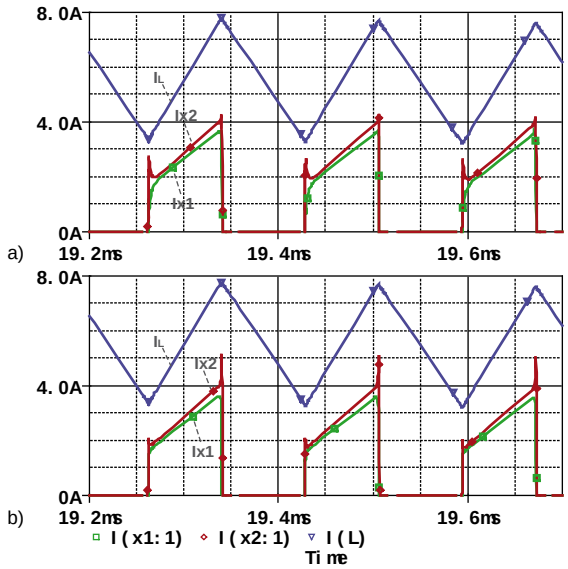

Fig. 4. Simulation results. Variation of gate resistor values: (a) R_{g1} = 150 Ω and R_{g2} = 22 Ω, (b) R_{g1} = 22 Ω and R_{g2} = 150 Ω.

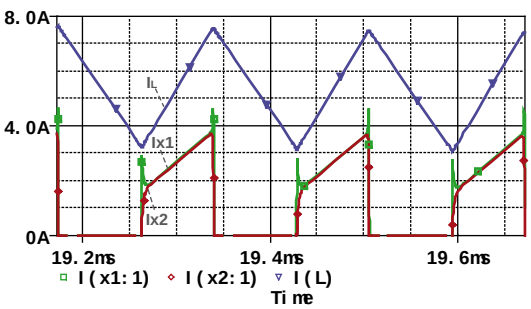

Fig. 5. Simulation results. Variation of V_{GE} values in two IGBTs connected in parallel with V_{GE1} = 15 V and V_{GE2} = 12.5 V. R_g is 22 Ω for both cases.

IGBTs by connecting these devices in series or in parallel. The proposed control strategies modify gate-emitter (V_{GE}) voltages to improve current balancing by sensing the current flowing through each transistor (I_{xi}). The reference of the control algorithm is obtained by calculating the average value of the current flowing through all transistors ($I_{C(AVG)}$). Eqs. (7) to (9) show the relationship between the level of control voltage (V_{GEi}) of each transistor and the current flowing through each transistor (I_{xi}).

$$V_{GEi} = V_{PWM} + \Delta V_i \tag{7}$$

$$\Delta V_i = k_p\left(I_{C(AVG)} - Ix_i\right) + k_i \int \left(I_{C(AVG)} - Ix_i\right) dt \tag{8}$$

$$I_{C(AVG)} = \frac{\sum_{i=1}^{n} Ix_i}{n} \tag{9}$$

where n refers to the number of parallel-connected IGBTs and ΔV_i is the voltage variation in the applied gate-emitter control signal (V_{PWM}).

Fig. 6 shows the implementation of the described control strategy when three IGBTs are connected in parallel.

The proposed current sharing algorithm is based on the setting of the measured current in the adjacent transistor as

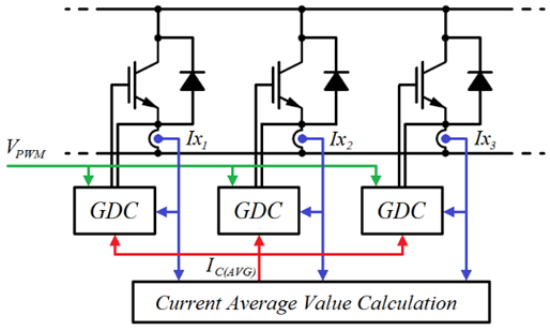

Fig. 6. Current sharing control strategy using the current average value as reference for a three-transistor implementation.

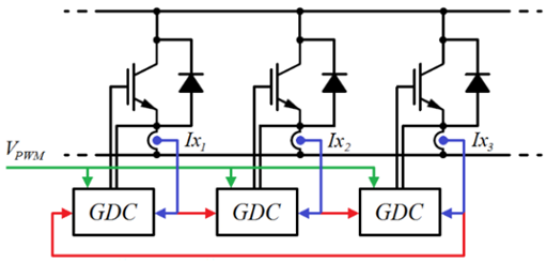

Fig. 7. Block diagram of the balanced current sharing control strategy for a three-transistor implementation based on current cross references.

the current reference. In a three-transistor implementation, the measured current of the first transistor is used as the current reference for the second transistor, the measured current of the second transistor is used as the current reference for the third transistor, and the measured current of the third transistor is used as reference for the first transistor. These current loops are based on a daisy chain structure and link measured currents and reference currents between transistors.

Fig. 7 shows the implementation of the proposed current sharing control algorithm in a three-transistor configuration.

The main difference of this approach versus the method shown in Fig. 6 depends on the suppression of the calculation of the current average value as a reference of the control loop. Errors may appear as a result of the tolerances of elements that perform the calculation of the current average value. By suppressing this calculation, the possible negative effects of an error are also suppressed.

IV. Simulation Results

With the aim of validating these control strategies, the current sharing schemes shown in Figs. 6 and 7 are simulated using *PSpice*. With this purpose, the boost converter shown in Fig. 8 is used. In this case, different technological switch characteristics are applied to obtain a heavy unbalanced current sharing through the parallel-connected transistors.

Fig. 9 shows the current evolution in the transistors in the case applying the same voltage level in the gate-emitter

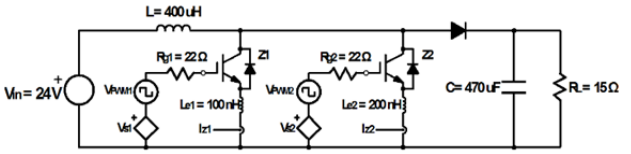

Fig. 8. Boost converter with two parallel-connected IGBT devices (Z1: IXGH10N100 y Z2: IXGH17N100).

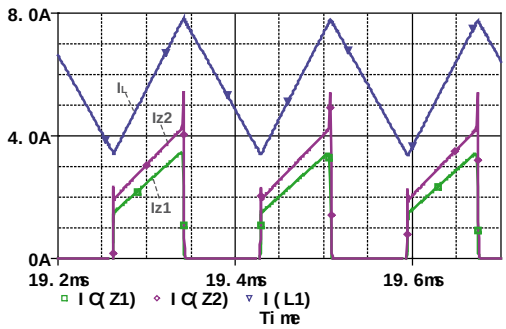

Fig. 9. Inductive current sharing in two parallel-connected IGBTs without balanced current sharing control.

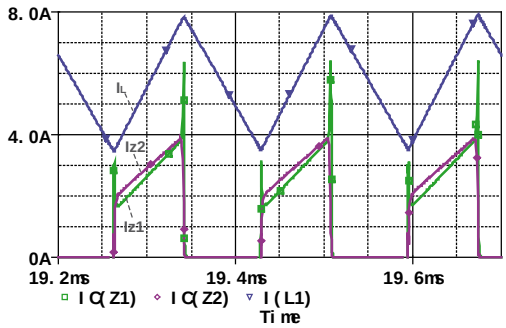

Fig. 10. Inductive current sharing in two parallel-connected IGBTs with balanced current sharing control based on the current average value control strategy.

control signals. As expected, different values of gfs and V_{GEth} cause an unbalanced sharing of current flowing through the IGBTs.

A. Current Sharing Control by Current Average Value Calculation

Fig. 10 shows the effect of the current sharing algorithm based on the calculation of the current average value. The evolution of the current flowing through each transistor shows an improvement in the current balance.

In this method, the error in calculating the current average value causes the saturation of the control. A series of simulations are performed with two to eight IGBTs connected in parallel. The results show that a negative error (smaller than 1.5% in the average value calculation) is enough to saturate the response of the control when tolerances of 5% in the values of g_{fs} and V_{GEth} are considered. For the IGBTs used in the performed simulations, the tolerances in the values of g_{fs} and V_{GEth} range from 30% to 50%.

A negative error means that the control tries to reduce the

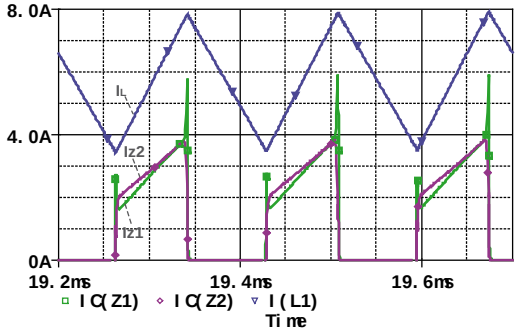

Fig. 11. Inductive current sharing in two parallel-connected transistors with balanced current sharing control based on current cross reference strategy.

current of each transistor; as a result, the control voltages applied in the gates continuously decrease. This decrease only ends when the lower limit of V_{GE} is reached. These limits prevent the gate from exceeding the maximum gate voltage, which is specified in the manufacturer datasheet, and prevent the transistor from switching out of the saturation region.

These results reveal that the current sharing method for average value calculation performs poorly when possible calculation errors are considered.

B. Current Sharing Control by Current Cross Reference

Fig. 11 shows the effect of the current sharing algorithm based on the current cross reference between transistors. According to previous simulation results, the evolution of the current flowing through each transistor shows a good balance.

According to the simulation results, static current control strategies show similar performances. However, the presence of errors in the calculation of the average value can saturate the response of the control and consequently increase current unbalance. Avoiding the calculation of the average value can solve this drawback.

The implementation of these two control strategies is presented in the next section.

V. CONTROL IMPLEMENTATION

The driver implemented for the tests is based on the voltage adder circuit shown in Fig. 12. The first Pulse Width Modulation (PWM) output of the microcontroller is used to generate the control signal for the power switch. The second PWM output is filtered and used to obtain ΔV for use in Eq. 7. An external offset adjustment is used to set the initial conditions. The push–pull output stage increases the current strength of the control signal.

The current measurement is obtained using a 5 mΩ Kelvin resistor (R_E) as a shunt. A low-pass filter is used to obtain the DC component or average value of the collector current on each transistor. In a DC/DC converter, such as the boost

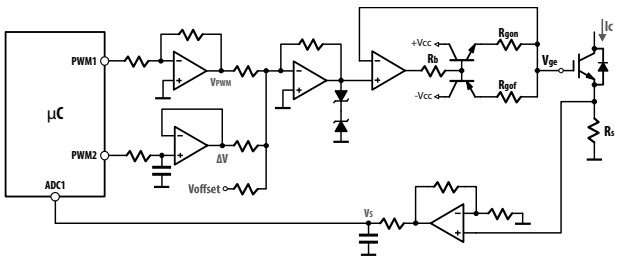

Fig. 12. Voltage adder circuit of the IGBT driver.

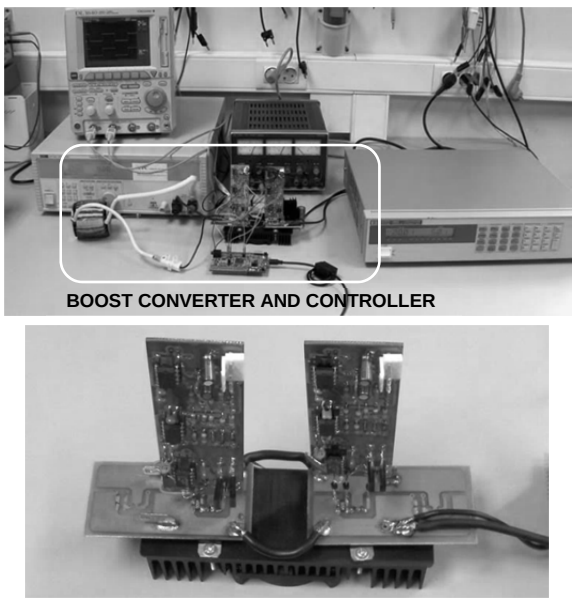

Fig. 13. Boost converter and detail of the driver implementation.

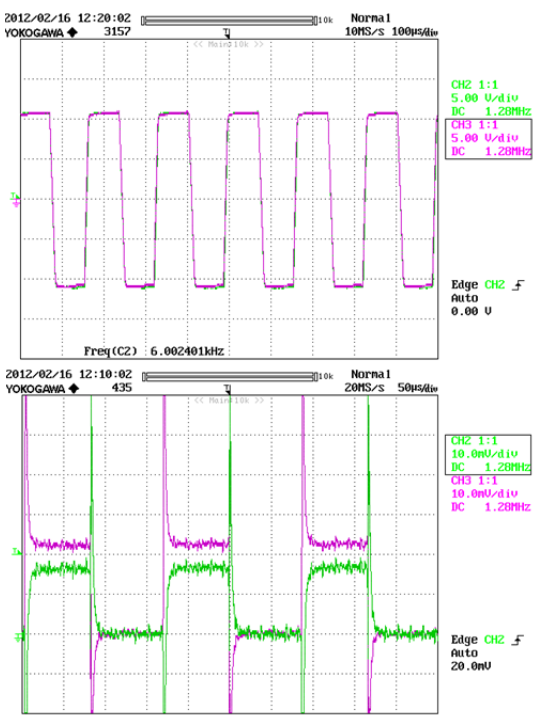

Fig. 14. Experimental results. Top: gate-emitter voltage. Bottom: current sharing between transistors without balanced current control.

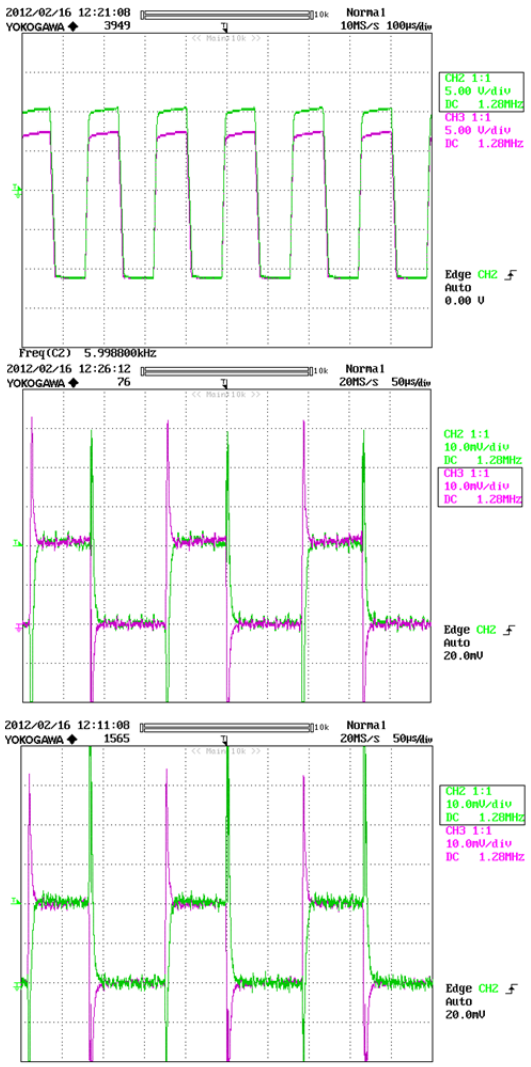

Fig. 15. Experimental results. Top: gate-emitter voltage. Middle: resistive current with balanced current sharing control based on the average value calculation. Bottom: balanced current sharing control based on current cross reference algorithm.

converter, an acquisition stage based on a non-inverting operational amplifier and a first-order low-pass filter allows the good performance of the control loop. The control algorithms are developed in a micro-controller platform.

VI. Experimental Results

Two parallel-connected IGBTs are employed to validate the proposed balanced current control strategy. For this test, both switches are based on the same IGBT model: *STGP7NC60HD* from *ST*. A comparison of the two control schemes is presented with the resistive and inductive currents flowing through the power switch.

The two IGBTs connected in parallel are mounted with a linear design, as shown in Fig. 13. The two transistors are thermally coupled via the same sink arranged symmetrically.

A. Resistive Current Sharing

TABLE II
TEST PARAMETERS

Symbol	Description	Value
z_1, z_2	IGBT: STGP7NC60HD	---
V_{in}	Boost input voltage	24 V
R_L	Load resistor	15 Ω
R_E	Shunt resistor	5 mΩ
L	Boost inductor	400 µH
C	Boost output capacitor	470 µF
f_s	Switching frequency	6 kHz

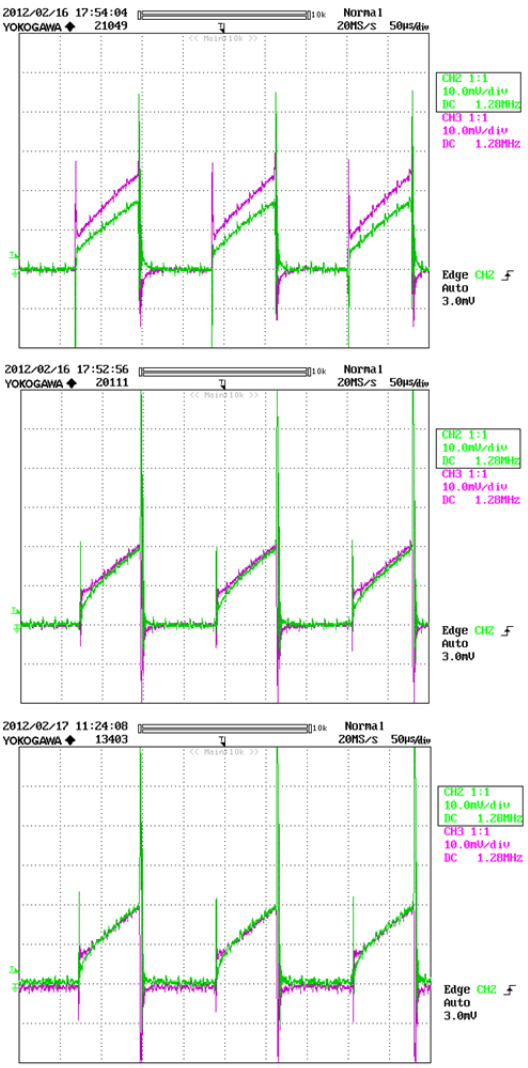

Fig. 16. Experimental results. Top: without balanced current control strategy. Middle: with balanced current sharing control based on the average value calculation. Bottom: balanced current sharing control based on current cross reference algorithm.

Figs. 14 and 15 show the current sharing under two different test conditions. The first test condition shows the current through the parallel-connected transistors without the use of a balanced current sharing control technique. The tolerances of the gfs and V_{GEth} result in an unbalanced current sharing, as presented in previous sections.

Fig. 15 shows a balanced current sharing in the IGBTs when the average value control technique and current cross reference strategy are used. In these cases, the voltage levels applied in the gates of the transistors differ for both transistors.

The peaks of the current observed in the ON and OFF states of the IGBTs reveal that as expected, the implemented strategies do not allow dynamic current balancing. A careful design of the power circuit and gate driver wiring should minimize dynamic current unbalance.

B. Inductive Current Sharing

Finally, a boost converter (Fig. 8) is implemented using the parameters listed in Table II. The results of three different test conditions can be observed in Fig. 16. The first test does not use any current sharing control technique. The second and third tests use a balanced current sharing method in the IGBTs on the basis of the current average value control and current cross reference control, respectively.

Similarly, the voltage levels applied in the gates of the transistors differ for both transistors to equalize the static current between the parallel-connected IGBTs.

The experimental results obtained confirm the behavior of the two implemented current sharing strategies observed in the simulation results.

VII. CONCLUSION

A balanced current sharing control algorithm is proposed for voltage-controlled transistors connected in parallel. Specifically, this study focuses on punch-through IGBTs because of their poor behavior in parallel operations.

The control strategy is validated with resistive and inductive current loads. The control strategy does not require high processing speed because it is based on the acquisition of average values.

This current sharing control scheme is suitable for DC/DC and DC/AC voltages or current-controlled converters, such as power inverters, because it offers active balanced current sharing.

The circuit implemented in the sensor stage must be customized for the topology of the converter and the requirements of the application according to the bandwidth of the current demanded by the load and the switching frequency of the transistors. In this work, a non-inverting operational amplifier with RC low-pass filter is used and is found to exhibit good performance in the DC/DC boost converter.

When the errors in the average value calculation are negligible, no remarkable differences are observed in the performances of the two current sharing control algorithms. The first control scheme based on average value calculation requires some signal processing, whereas the second scheme obtains the same results but simplifies the required

calculations for the average current value. When the error values caused by tolerances in the calculation of the average value are not negligible, they cause the saturation of the control circuit and then increase the current unbalance. Avoiding the calculation of the average value, as proposed in this work, can solve this problem.

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