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CHIRP FOURIER PROCESSOR DESIGN: A TIME-DOMAIN SIMULATION APPROACH

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ABSTRACT

The use of Chirp Fourier Processors as systems for digital Communications and/or Radar is common at the present. This fact is due to the existence of the SAW devices which can be used as real-time spectrum-analyser systems composed by Linear Frequency Modulators (LFM or Chirp filters) having group delay which increases or decreases linearly with frequency.

As far as the whole processor implementation is concerned a couple of configurations known as "Multiply-Convolve-Multiply" (MCM) and "Convolve-Multiply-Convolve" (CMC) transformers are possible. Both approaches have advantages and drawbacks. In this paper, the MCM approach is discused and considered. Since the digital simulation technique is becoming a powerful tool in the analysis and design of these systems, techniques for the efficient simulation of MCM chirp processor are considered here.

In fact, the MCM approach requires only one chirp filter so it is less time consuming. Moreover it is less sensitive to ripple amplitude and phase errors than CMC. Another advantage is that it allows time-domain windowing by product at the filter input. The importance of such question will be pointed out.

The purpose of this paper is to investigate, using a time-domain simulation approach, the possibilities offered by a chirp Fourier processor as a repetitive chirp receiver. Results about a test involving a chirp signal generator and a chirp filter in order to simulate a matched filter receiver are included, along with the relative errors between the output of the chirp Fourier processor and its ideal value.