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Discontinuous Modulation of Modular Multilevel Converters without the Need for Extra Submodules

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***Abstract*—In this paper, a new approach to the discontinuous modulation technique for the operation of the modular multilevel converter (MMC) is presented. Discontinuous modulation is based on adding a zero-sequence to the original modulation signals so that each MMC arm is clamped to the upper or lower terminals of the dc-link bus during some intervals. In combination with a circulating current control, the original discontinuous modulation can reduce the capacitor voltage ripple amplitudes and the switching power losses. However, additional submodules (SMs) are required to control the circulating current. This new approach presents a clamping algorithm that eliminates the requirement of additional SMs. As a result, the conduction losses are reduced while the capacitor voltage ripples are maintained low. Simulation and experimental results on a silicon-carbide-based MMC are reported and compared against the original discontinuous modulation and a conventional carrier-based pulse-width modulation.**

***Index Terms*—Capacitor voltage ripples, discontinuous modulation, efficiency improvement, modular multilevel converter, silicon carbide.**

I. Introduction

Multilevel converters are attractive power converter topologies for medium and high power applications [1]. Among the multilevel converter topologies, the modular multilevel converter (MMC) [2] offers several salient features which make it a competitive solution for high-voltage direct current (HVDC) transmission systems [3] and flexible alternating current transmission systems (FACTS) [4]. The most attractive features of the MMC are [2]: (i) its modularity and scalability to different power and voltage levels, (ii) its high efficiency, (iii) the high quality of the output voltages, and (iv) the absence of additional capacitors on the dc-link, as the storage is distributed among the capacitors in the submodules (SMs) of the converter.

The potential of the MMC in the area of medium-voltage motor drives has also been demonstrated [5]. However, there is a challenge that has to be addressed. Using standard modulation strategies, the capacitor voltage ripples are inversely proportional to the output frequency, producing excessive ripples when operating with low output frequencies, i.e., at low motor speeds.

Some solutions have been proposed for reducing the capacitor voltage ripples in motor-drive applications. Most of them are based on combining the injection of a high frequency component in the circulating current and the use of a zero-sequence signal [6], [7].

Another method that can be used for reducing the capacitor voltage ripples is discontinuous modulation [8], [9]. This technique is based on clamping one arm of the converter to a nonswitching position. The clamping effect is achieved through the addition of a zero-sequence component. Combined with a closed-loop strategy for the control of the circulating current [10], the discontinuous modulation can achieve a significant reduction in the capacitor voltage ripples and switching power losses. However, this technique requires the use of additional SMs in each arm to provide control of the circulating current during the clamping intervals. This fact might not be relevant in high power applications, where a large number of SMs is required and additional SMs are usually provided anyway for reliability purposes. However, in medium-power applications of the MMC, such as motor drives, including additional SMs in the arms is usually avoided because of the significant impact on the overall cost of the converter. A benefit of this is that the MMC has less conduction power losses. Moreover, in medium-power MMCs, the use of wide-band-gap semiconductor devices is being considered, particularly high-voltage silicon-carbide (SiC) devices, which present a higher influence of conduction losses than switching losses [11].

In this paper, a new approach to the discontinuous modulation that does not require the use of additional SMs is presented. Instead of by-passing the arm of the clamped phase-leg with less SMs activated, the arm with the highest or lowest modulation signal is clamped, without taking into account if it is the upper or lower arm. Since there is no requirement for increasing the number of SMs in the MMC with this approach, the conduction losses of the converter are reduced compared to the case of implementing the original discontinuous modulation [9].

The rest of the paper is organized as follows. Section II summarizes the principles of operation of the converter topology and the circulating current controller. Section III describes the basics of the discontinuous modulation and Section IV presents the new approach to this modulation technique. In Section V, simulation results are reported and the proposed discontinuous modulation is compared to the original closed-loop discontinuous modulation and a carrier-based space-vector pulse-width modulation (CB-SVPWM). Experimental results are obtained and compared in Section VI. Finally, Section VII concludes the paper.

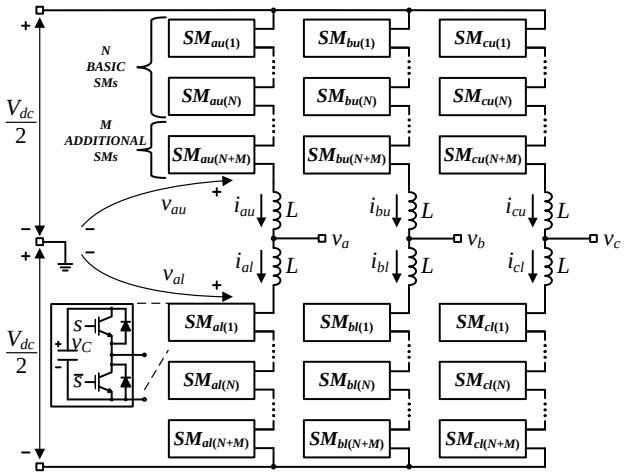


Fig. 1. Circuit diagram of a three-phase MMC with N basic SMs and M additional SMs per arm.

II. Principles of Operation of the MMC

A. MMC Fundamentals

The general topology of an MMC consists of two arms per phase-leg, where each arm comprises N series-connected, identical SMs and a series arm inductor, L. Each SM contains a half-bridge circuit and a capacitor C. The output voltage of each SM equals to its capacitor voltage (v_C) when the SM is activated, or equals to zero when it is deactivated. A schematic of the topology is depicted in Fig. 1. In this figure, in addition to the N basic SMs of each arm, M additional SMs have been included. These additional SMs are needed when operating the MMC with the discontinuous modulation introduced in [9], as explained in Section III.

The voltage waveforms at the ac-side of the MMC can be synthesized by using multiple modulation techniques [2]. Most of them are based on defining the number of SMs to be activated in each of the arms, and the particular SMs are determined by a voltage balancing algorithm. In this paper, the voltage reference is a sinusoidal waveform with amplitude defined by the modulation index m_a. It is modulated by a level-shifted PWM (LS-PWM) technique [12] and the capacitor voltages are balanced using the algorithm proposed in [13].

B. Circulating Current Controller

The current that flows through each arm is composed by half of the output current and a circulating current. The circulating current includes a dc component, related with the power exchange between the dc and the ac-side of the converter, and some harmonic components. In order to improve the converter dynamics, the circulating current should be controlled.

The circulating current is controlled with the voltage applied to the arm inductors. Applying a control signal Δv_{jm} to the upper and lower arm modulation signals, the voltage in the inductors can be controlled. In order not to affect the output voltage of the phase-leg, the control signal is applied symmetrically. That is, when the modulation signal of the upper arm v_{jum} is increased, the modulation signal of the lower arm v_{jlm} is decreased the same amount and vice versa:

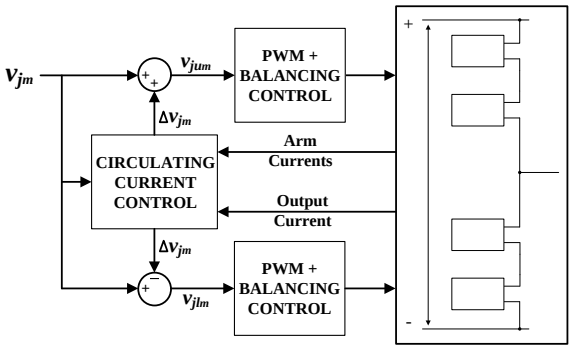


Fig. 2. Block diagram of the circulating current control.

$$v_{jum} = v_{jm} + \Delta v_{jm} \text{ and} \tag{1}$$

$$v_{jlm} = v_{jm} - \Delta v_{jm} \ , \tag{2}$$

where $j = \{a, b, c\}$ is the phase identifier.

Fig. 2 shows how the normalized reference signal of a phase-leg (v_{jm}) is modified by adding the differential control signal Δv_{jm}.

In this paper, the circulating current is controlled to achieve a further reduction in the capacitor voltage ripples. The current reference defined in [10] is used, which is calculated from the instantaneus values of output current and modulation signal:

$$i^*_{j\ circ} = \frac{i_j v_{jm}}{2} \ . \tag{3}$$

III. Discontinuous Modulation

A. Basics of Discontinuous Modulation

The discontinuous modulation consists in injecting a zero-sequence signal into the references of a multiphase converter [14]. The zero-sequence injected is such that one of the phase-legs is clamped to the upper or lower terminals of the dc-link for certain intervals (Fig. 3). With this modulation, the linear operation mode of the converter is increased and the switching power losses of the converter are reduced, since there is always one phase-leg that is not switching for some intervals.

When applying the discontinuous modulation to the MMC [8], [9], all the SMs of one arm of a particular phase-leg are deactivated (bypassed) for some intervals. Therefore, the phase-leg is clamped to the upper or lower dc-bus terminals. During those intervals, since one arm of the converter is not switching, the switching power losses are reduced.

Besides reducing the switching power losses, the discontinuous modulation also provides another benefit to the MMC: it reduces the capacitor voltage ripple amplitudes. The dynamic models of the converter [10] demonstrate that, when using the circulating current reference given by (3), the arm that has less SMs activated carries more output current. Therefore, when a

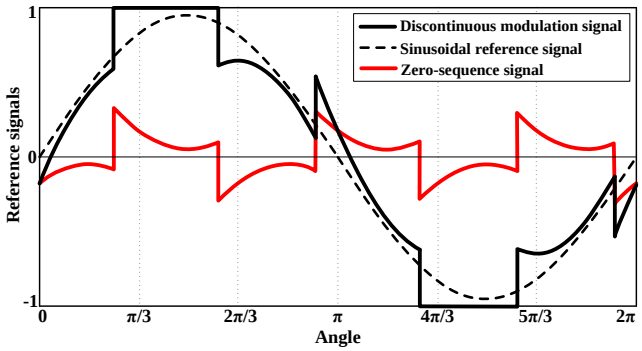


Fig. 3. Example of discontinuous modulation signal.

phase-leg of the MMC is clamped to a dc-link terminal, the arm that is clamped provides all the output current, while no current circulates through the unclamped arm of that phase-leg. Consequently, during the clamping process, no current circulates through any SM capacitor of the whole phase-leg. This is the reason why discontinuous modulation reduces the capacitor voltages ripples. This reduction is more significant when operating with low modulation indices. This is because when no zero-sequence is injected, a similar number of SMs are activated in the upper and the lower arms. In such operating conditions, the output current is equally shared between both arms of a phase-leg, flowing through N SMs and producing large capacitor voltage deviations. If discontinuous modulation is implemented, the zero-sequence shifts the reference signals of all the phases far from zero, reducing the currents in the capacitors and hence the capacitor voltage ripples.

In order to further reduce the switching power losses and capacitor voltage ripples, the clamping intervals are performed when the output current takes the maximum absolute value. As only one arm can be clamped at any time, the arm that should be clamped is decided through a feedback loop of the output current.

B. Circulating Current Reference and Additional SMs

As mentioned previously, the circulating current is controlled through the addition of a differential control signal Δv_{jm} to the modulation signal. When one arm is clamped and the differential control signal is positive, the reference of the opposite arm remains within the modulation limits $[1, -1]$. However, if the differential control signal is negative, the reference of the opposite arm presents a value higher than 1 or lower than -1. In order to avoid this overmodulation situation [9], a number M of additional SMs can be added to the N basic ones, allowing to work with a modulation signal out of the bounds $[1, -1]$.

IV. Virtual Clamping

The use of additional SMs provides the capability of controlling the circulating current of a clamped phase-leg. However, in medium-power applications with a low number of SMs, the use of one or more additional SMs implies a significant increase in the cost of the converter. Moreover, the

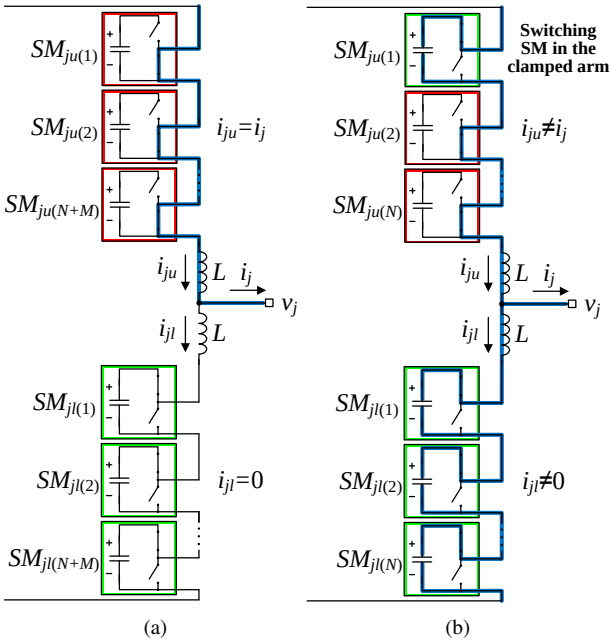


Fig. 4. Circuit diagram of an MMC phase-leg when performing (a) actual clamping with the original discontinuous modulation and (b) virtual clamping with the new approach to discontinuous modulation.

conduction power losses increase with the number of SMs, as the arm currents flow through a higher number of switching devices.

In order to avoid the use of additional SMs, this paper presents a new technique called virtual discontinuous modulation (VDPWM). It is based on the principles of the discontinuous modulation explained before, but changing the clamping methodology when the differential control is negative.

The original discontinuous modulation [9] always clamps the upper arm to the upper rail of the dc-link and the lower arm to the lower rail of the dc-link. In this new approach, one arm is considered clamped not only when all the SMs are deactivated (bypassed), but also when all of them are activated. Therefore, when one phase-leg is clamped, the arm that has an individual reference signal clamped to 1 (or -1) is the arm with the maximum (minimum) reference signal, without taking into account if it is the upper or lower arm. When the differential control signal is positive, the performance is the same than in the original discontinuous modulation. However, when the differential control signal is negative, the arm fixed to 1 or -1 is the one with all the SMs activated. As an example, if the lower reference signal of an arm that should be clamped up is higher than the upper reference signal, the lower arm is fixed to 1. This is a situation called "virtual clamping", since the arm that should have no SMs activated is the one that remains switching to control the circulating current. This new approach eliminates the requirement of working out of the modulation limits $[1, -1]$, and therefore, the need for additional SMs.

Fig. 4 depicts an example of actual and "virtual" clampings on the upper rail of the dc-link. Note in this figure that, in

TABLE I
SPECIFICATIONS OF THE SWITCHED MODEL OF THE MMC

Parameter	Value
Number of Basic SMs per Arm, N	3
Number of Additional SMs per Arm (only for DPWM), M	1
SM Capacitors, C	1500 μF
Arm Inductors, L	3 mH
DC-Link Voltage, V_{dc}	700 V
RMS Load Current, I_a	4 A
Carrier Frequency, f_{sw}	5 kHz
Output Frequency, f	50 Hz

the case of applying the original discontinuous modulation (Fig. 4(a)), the arms need to include M additional SMs to the N basic ones. During the clamping interval in this example, all the SMs of the upper arm are bypassed (deactivated) while some SMs of the lower arm switch to regulate the circulating current. On the other hand, with the proposed discontinuous modulation (Fig. 4(b)), no extra SMs are included. In this case, some SMs from the upper or the lower arms can switch to control the circulating current.

This implementation avoids the use of additional SMs, but in contrast, increases the capacitor voltage ripples with respect to the original discontinuous modulation. It also increases the switching power losses, as during the "virtual clampings", the arm that switches is the one that carries more current within the phase-leg. In converters with low-speed switching devices, the new approach may imply an increase in the total power losses. However, when using fast-speed switching devices, the savings in conduction losses can be higher than the increase in switching losses. Therefore, this new discontinuous modulation approach is expected to be useful for medium-power MMCs with a low number of SMs and implemented with fast-speed semiconductors, reducing the overall cost of the converter and the total power losses while slightly increasing the capacitor voltage ripples.

V. SIMULATION RESULTS

The proposed modulation technique has been simulated under MATLAB/Simulink environment. Simulation studies have been performed using a switched model of a three-phase SiC-based MMC. The model implemented has a nominal power of 3.5 kW and integrates three basic SMs per arm ($N = 3$). The specifications of this test converter for the simulations are given in Table I. In the simulations, a three-phase current source is used as a load.

The power losses are calculated considering the SiC Cree CMF20120D MOSFET and the SiC Cree C4D10120D diode. The main maximum ratings of the transistor are a forward current of 42 A and a direct voltage of 1200 V. The data of the MOSFET and diode for the calculation of the losses are obtained from the manufacturer datasheet.

Simulation studies evaluate the total power losses and the capacitor voltage ripple amplitude of the VDPWM. Results are

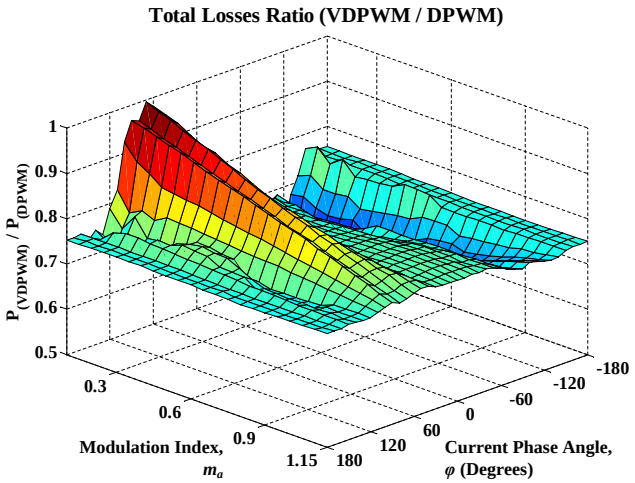


Fig. 5. Total power losses ratio between the new approach and the original discontinuous modulation (VDPWM over DPWM).

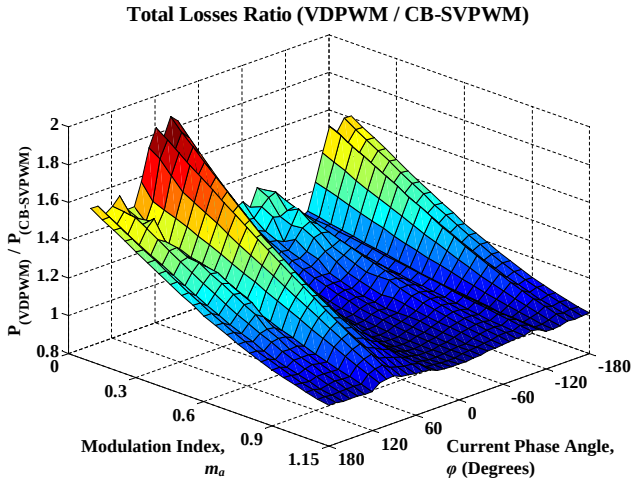


Fig. 6. Total power losses ratio between the new approach to the discontinuous modulation and the sinusoidal modulation (VDPWM over CB-SVPWM).

compared to the ones obtained with the original discontinuous modulation (DPWM) and with CB-SVPWM [14]. The model used for the simulation of the original discontinuous technique includes one additional SM ($M = 1$).

Results are presented for different operating points, where m_a is the modulation index before the injection of a zero-sequence (0.1 to 1.15), and φ corresponds to the current phase angle in degrees [-180°, 180°].

A. Power Losses

The main advantages of the VDPWM with respect to the original DPWM are a reduction in the number of SMs and in the conduction losses. However, the new approach produces an increase in the switching power losses. These losses are expected to be small in the SiC-based test converter. In order to evaluate the benefits of the proposed modulation technique, the total power losses are presented.

Fig. 5 depicts the total power losses ratio between VDPWM

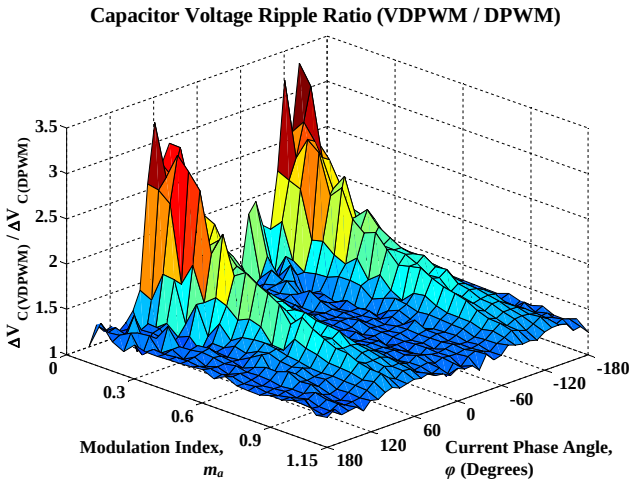


Fig. 7. Capacitor voltage ripple ratio between the new approach and the original discontinuous modulation (VDPWM over DPWM).

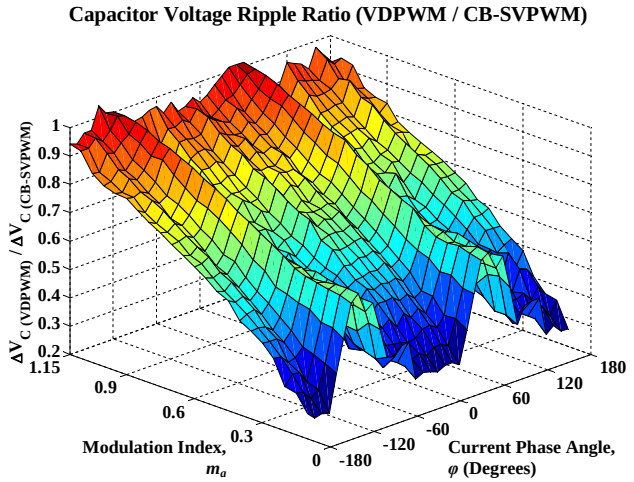


Fig. 8. Capacitor voltage ripple ratio between the new approach to the discontinuous modulation and the sinusoidal modulation (VDPWM over CB-SVPWM).

and DPWM for different operating points. It can be seen that the power losses with VDPWM are lower than with DPWM for all the operating points. On average, the losses produced with VDPWM are 25% lower than those produced with DPWM.

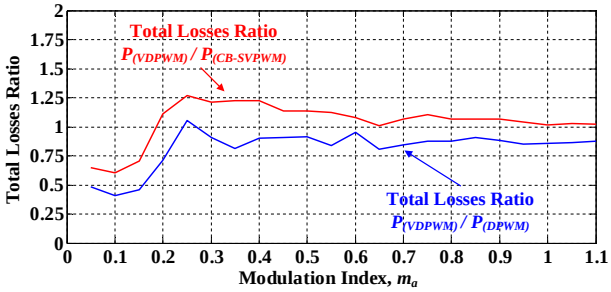
When using discontinuous modulation, the rms value of the circulating current increases when compared to CB-SVPWM. This fact can be observed in Fig. 6, where the losses of VDPWM and CB-SVPWM are compared. The losses ratio is always higher than one, having a mean value of 1.223.

B. Capacitor Voltage Ripples

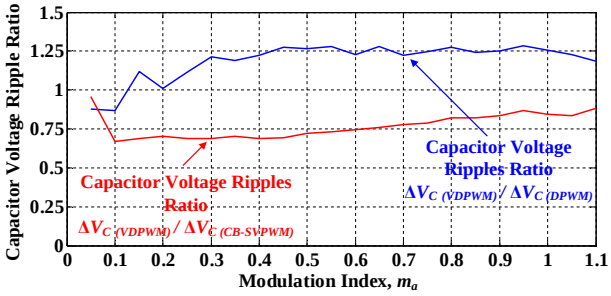
One of the main benefits of discontinuous modulation techniques respect to the traditional ones such as CB-SVPWM is a reduction in the capacitor voltage ripples [9]. In the case of VDPWM, such a reduction is slightly less than with DPWM. Moreover, the use of additional SMs in DPWM provides a further reduction in the capacitor voltage ripples [15]. Fig. 7

TABLE II
ADDITIONAL SPECIFICATIONS OF THE LABORATORY PROTOTYPE

DC-Link Voltage, V_{dc}	200 V
Load Resistor, R_a	25 Ω
Load Inductor, L_a	6 mH



(a)



(b)

Fig. 9. Experimental results ratio between the new approach and the original discontinuous modulation (VDPWM over DPWM) and between the new approach and the sinusoidal modulation (VDPWM over CB-SVPWM): (a) total power losses ratio and (b) capacitor voltage ripple ratio.

shows the ratio of the capacitor voltage ripple amplitudes between VDPWM and DPWM. It can be seen that ripples are higher with the new approach, especially at low modulation indices and highly reactive currents. On average, the capacitor voltage ripples with modulation indices from 0.3 to 1.15 are 46% higher with VDPWM than with DPWM. Nevertheless, the new approach to discontinuous modulation maintains a reduction in the capacitor voltage ripples for all the operating conditions with respect to CB-SVPWM, as it can be observed in Fig. 8. The reduction in the capacitor voltage ripples reaches a minimum ratio of 0.26 for a modulation index $m_a = 0.1$.

VI. EXPERIMENTAL RESULTS

The proposed modulation technique has been implemented and tested in a low-power laboratory prototype. The implemented system consists on a 3-phase MMC operating over an R-L load. The prototype has been implemented using SiC devices considered in simulation. Most of the parameters are the same with the simulation tests, given in Table I, except those that are given in Table II.

Experimental tests measure the same ratio measurements than simulation tests. Results are presented for different operating conditions of m_a, which ranges between 0.05 to 1.10.

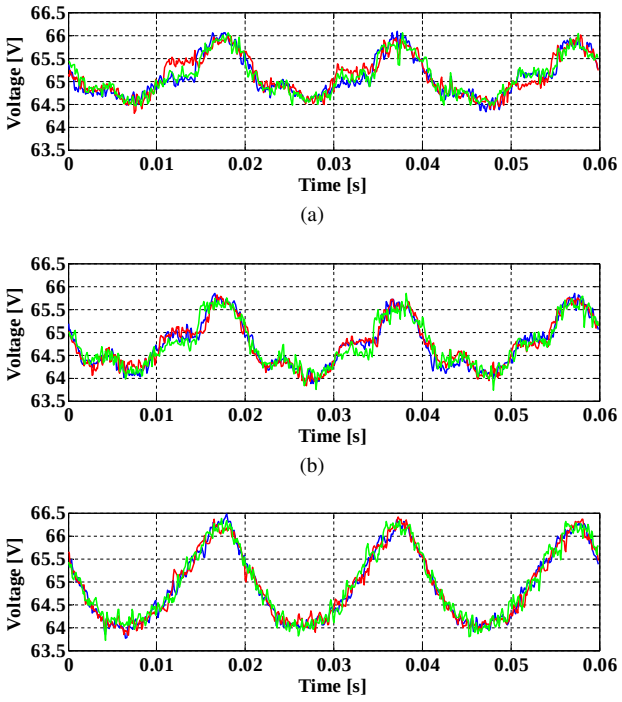


Fig. 10. Experimental results of the capacitor voltage ripples with $m_a = 0.8$ when using different modulation techniques: (a) DPWM, (b) VDPWM and (c) CB-SVPWM.

The phase of the output current respect to the output voltage (φ) is defined by the R-L load and is about -4°.

Main results of the experimental tests are depicted in Fig. 9. In Fig. 9(a), the total losses ratios are shown. It can be seen that the power losses with VDPWM are lower than with DPWM for almost all the operating conditions. On the contrary, the losses produced by VDPWM are higher than with CB-SVPWM. The comparisons about the capacitor voltage ripples are depicted in Fig. 9(b). As expected, the ratio between VDPWM and CB-SVPWM is lower than one, as the proposed technique reduces the capacitor voltage ripples. However, VDPWM is not as successful as DPWM in reducing the capacitor voltage ripples, this is why the ratio between VDPWM and DPWM is higher than one in most operation conditions. An example of the differences in the capacitor voltage ripples depending on the modulation technique can be observed in Fig. 10.

VII. Conclusion

In this paper, a new approach to discontinuous modulation for the MMC has been presented. By changing the clamping methodology, the new approach eliminates the requirement of additional SMs that the original discontinuous modulation has. With this new implementation the reduction in the capacitor voltage ripples and switching losses is less significant than with the original discontinuous modulation. Nevertheless, the reduction in the number of SMs required implies a reduction in the converter costs and also in the conduction power losses. This can be an important benefit for medium-power converters with a low number of SMs, such as those used in motor drive applications. Moreover, if a fast-switching technology of power devices like SiC is used, the reduction in conduction losses implies a total reduction of the overall power losses of the converter.

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