SINGLE-STEP MULTIPLE-LAYERS WAFER SLICING FROM MACROPOROUS SILICON

M. Garín[1], D. Hernández[1], T. Trifonov[2], D. Cardador[1], and R. Alcubilla[1,2]*.

[1] Grup de recerca en Micro i Nanotecnologies, Departament d'Enginyeria Electrònica
Universitat Politècnica de Catalunya, c/Jordi Girona 1—3, Mòdul C4, 08034 Barcelona, Spain.

[2] Centre de Recerca en Nanoenginyeria, Universitat Politècnica de Catalunya
c/ Pascual i Vilà 15, 08028, Barcelona, Spain.

* ramon.alcubilla@upc.edu

ABSTRACT: There is a rising interest, from both photovoltaics and microelectronics industry, in wafer thickness reduction. During the last decade, it has been steadily reduced from 350 µm to 180 µm, but benefits are foreseen for thicknesses well below these values. The current sawing technology, however, suffers from large kerf losses and further reductions are increasingly difficult. Several technologies have emerged aiming to produce thin Si foils from a wafer, such as layer transfer, induced cleaving, or pore reorganization. These methods produce a single layer by step. In this work we report on a method able to produce many crystalline layers from a single silicon wafer and in a single fabrication step.
Keywords: Crystallisation, Silicon-Films, Thin Film Solar Cell, Wafering

1 INTRODUCTION

Over the past decade, commercial silicon wafers have reduced their thickness from 350 µm down to 180 µm, but current roadmaps already claim for even thinner substrates in both photovoltaic and microelectronics industries. Up to now the progressive reduction in wafer thickness has been achieved by improvements in the sawing process. This technique, however, is reaching a point where further reductions are not possible without punishing yield and/or kerf losses (*i.e.* cut losses). In order to overcome the limitations of sawing, a few technologies have emerged following different approaches: induced cleaving [1,2,3], layer transfer [4,5], and macropore reorganization [6, 7, 8]. These techniques produce a single silicon layer per process and per substrate. Although the substrate can be recycled to produce more than one layer, this creates a bottleneck for cost-effective mass production. It would be desirable, therefore, to have a method able to produce more than one layer per substrate and per process; ideally as many layers as physically possible in the substrate.

Very recently we reported on a method [9] that can produce multiple free-standing crystalline-silicon layers from a single silicon wafer and in a single step. This method is based on the reorganization of porous structures but, unlike in the standard technique, that uses an array of shallow straight pores, we decided to create extremely deep pores with variations in pore diameter with the aim of creating many layers at once. To fabricate these pores we used electrochemical etching techniques [10], on which we had already many years of accumulated know-how in our group [11,12], allowing to create ordered arrays of pores with extreme aspect ratios (even wafer-through pores) and with a precise control over the pores' diameter in-depth. With this technique, and following an intuitive approach, we created ordered porous structures with alternating sections with low pore diameter and high pore diameter (see Fig. 1) and annealed them in Ar atmosphere at 1200 ºC. After the reorganization, low diameter regions produced crystalline silicon films while high diameter regions promoted to spacing layers, demonstrating that the formation of many simultaneous layers is feasible, and that layer thickness can be controlled through the initial pore profile. We call the resulting multilayer structure "silicon millefeuille" by analogy with the famous french pastry.

In the following we report on the silicon millefeuille process and our current achievements, and correlate the results with pore evolution simulations. From the calculations we estimate the range of attainable thicknesses considering the current pore profile shape.

2 EXPERIMENTAL

We produce pores by electrochemical dissolution of *n*-type silicon in HF solution under back-side illumination [11]. A square array (2x2 µm) of inverted pyramids is first created on the wafer surface to define where pores will nucleate. The electrochemical dissolution of silicon in HF consumes holes. Since holes are minority carriers in *n*-type silicon, the reaction is controlled by the supply of holes by photo-generation in the wafer's backside. Photogenerated holes diffuse towards the surface allowing silicon dissolution at the pore tips and promoting a stable pore growth. The porosity of the structure (*i.e.* diameter of pores) is proportional to the instantaneous current flowing through the system, which is in turn controlled by the intensity of the back-side illumination. By precisely controlling the current flowing during the etch, we can create pores with a defined pore diameter profile in depth. Porous silicon technology has the advantages of allowing full wafer surface processing, providing a good control over the pore profile in depth, and permitting to produce pores as deep as the wafer thickness.

Using the above process, we have fabricated samples with pores whose diameter alternate in-depth between narrow and wide diameter regions. The structural parameters of the profile are: the narrow pore diameter, d_m, wide pore diameter, d_w, length of narrow regions, L_n, length of wide regions, L_w, modulation length, $L=L_n+L_w$, and the number of periods (*i.e.* final layers) N.

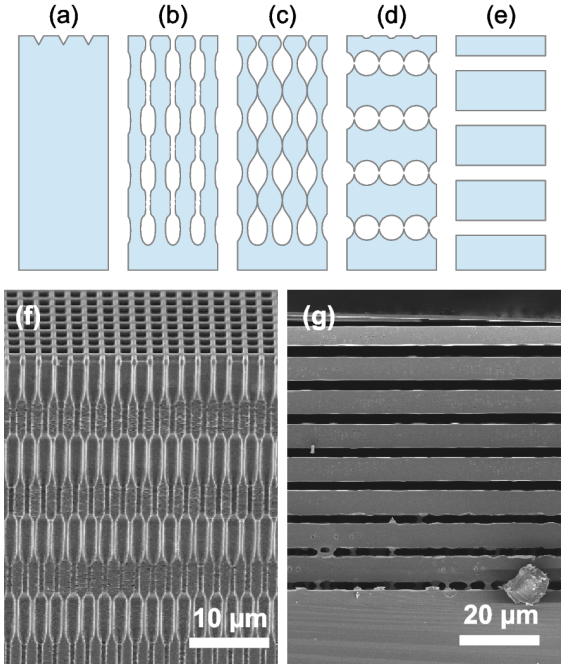

Figure 1: Schematic of the process. (a) Pore nucleation layer. (b) Electrochemical etching of pores. (c—e) During the annealing, pores collapse into bubbles which collapse with coplanar bubbles forming a stack of layers. (f) SEM image of a typical initial modulated structure. (g) SEM image of a typical final multilayer structure with 8+1 layers.

These structures have been annealed in a standard horizontal furnace in Argon ambient at 1200ºC for two hours, enabling the pore morphology evolution by surface diffusion. During this process, pores collapse forming bubbles first, which later coalesce laterally forming empty layers separating the different final Si foils. Fig. 1 shows schematically the process, along with a SEM image of the initial modulated structure and a final multilayer structure.

Finally, these layers can be detached one-by-one from the sample by exfoliation. As an example, figure 2 shows several layers exfoliated using standard office adhesive tape. The first six layers were exfoliated from the same sample. Notice that, although flexible, layers can break easily, especially if void layers have defects. The last two layers correspond to two higher quality layers detached from a different sample.

3 MODELLING

3.1 Profile evolution

The spatial and time evolution of the pores' surface during the annealing can be described using the macroscopic linear theory of surface diffusion. In this model, atoms diffuse from high curvature regions toward lower curvature ones. Integration of surface diffusion leads to the well-known Mullin's equation [13]

$$v_n = B\Delta_s H\,, \qquad (1)$$

where v_n is the normal velocity of the evolving surface, Δ_s is the surface Laplace operator and $H=½(k_1+k_2)$ is the mean curvature of the surface, defined as the average of

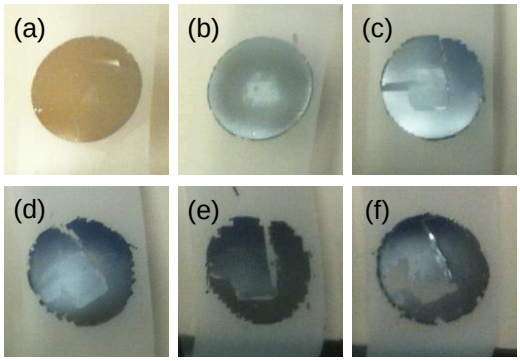

Figure 2: Consecutive films exfoliated from a silicon millefeuille. Notice that they are fragile.

the two principal curvatures, k_1 and k_2. The parameter B account for the material and temperature T through $B=D_s\gamma\nu\Omega^2/(k_bT)$, with D_s the diffusion constant, γ the surface tension, ν the atomic surface density, Ω the atomic volume and k_b the Boltzmann constant.

In order to model the effect of pore modulation on its evolution through the annealing, we have evolved equation 1 in time by finite differences for a single cylindrical pore with a defined diameter profile in depth. Instead of computing the pore evolution in terms of a 3D triangular mesh evolution, we exploited the cylindrical symmetry of the system and calculated just the evolution of the vertical cross-section C of the pore [14]. At any point of the surface, the first principal curvature is defined by the local curvature of C at that point:

$$k_1 = \frac{C_x'C_z''-C_z'C_x''}{(C_x'^2+C_z'^2)^{3/2}} \qquad (2)$$

where the partial derivatives of the components of C are with respect to the arc length s. The second principal curvature, on the contrary, is calculated from the radius of the pore at the point, r, applying the Meusnier's theorem

$$k_2 = \frac{1}{r}\cos(\theta)\,, \qquad (3)$$

with θ the angle between the surface normal at P and the plane perpendicular to the pore axis. At the bottom of a pore and at the bottom and top of a trapped bubble, equation (3) becomes undetermined. In the vicinity of these points we take $k_2=k_1$.

3.2 Calculation of layer thickness

With the cylindrical approach we can accurately describe the evolution of a single pore, but cannot describe the lateral coalescence of multiple bubbles (i.e. empty layer formation) due to the lack of cylindrical symmetry of such system. Nonetheless, and provided that the pores collapse before bubble start to coalesce, we can still determine the thickness and spacing of the final layers based on volume conservation principles. A pore, either smooth or periodically modulated, will evolve into a series of bubbles of radius r_b spaced periodically with a periodic distance λ. If pores are arranged in a square array with pitch $a<2r_b$, bubbles will coalesce into voids. Considering that the total volume of the coplanar bubbles and the final empty layer must be maintained, the final spacing layer thickness will be

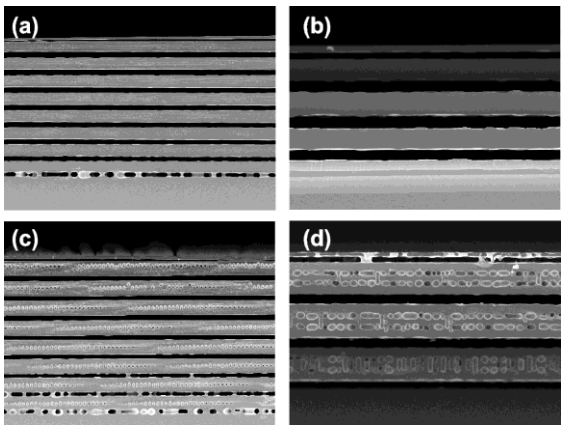

Figure 3: SEM images, cleaved side, of samples with different average thickness namely: (a) 5.5 µm (solid), (b) 6.5 µm (solid), (c) 7.4 µm (one row of bubbles) and (d) 15 µm average thickness (two rows of bubbles).

$$w_{void} = \frac{4\pi r_b^3}{3a^2}, \quad (4)$$

and the thickness of the silicon foils

$$w_{foil} = \lambda - w_{void}. \quad (5)$$

4 RESULTS & DISCUSSION

Aiming to explore the possibilities and versatility of this technique, we have fabricated samples with different number of layers and different low porosity lengths L_n. The typical pore diameters are d_n=0.4—0.8 µm and d_w=1.5—1.7 µm. The length L_w is choosen around 5 um, which leads to reliable empty layer formation.

One of the main goals we pursued in our set of experiments was to demonstrate that many layers can be created with this technique. As we increase the number of layers, pores become deeper revealing changes in the electrochemical etching conditions with depth. Overall, this creates deviations in the pore profile that leads, in the best case, to incomplete solid or space layers formation (see bottom spaces in figure 1(g)) or, in the worst case, to an unstable pore growth ruining the structure. In summary, we needed to follow an iterative process for refining the etching conditions in order to obtain the desired profile at high depths. Up to now we have been able to produce 9+1 *millefeuille* structures. The +1 layer corresponds to an extra thin layer (1—2 um) that forms at the top of the structure. Notice that we start our pore profiles with a highly porous band that should create a space layer, but a thin layer appears on top of this space due to surface closing during the annealing. As a matter of fact, we do not foresee any strong limitation in the maximum number of layers, and a greater number should be possible by further refining the etching at greater depths.

Another interesting feature of the silicon *millefeuille* technique is that the thickness of the produced silicon foils is defined not only by the pore arrangement periodicity, but by the particular pore profile, *i.e.* the pore diameters and lengths (d_n, d_w, L_n and L_w) of the different pore profile sections, that can be independently controlled. Furthermore, the layer thicknesses achieved are considerably thicker than what can be obtained with the standard (single-layer) pore reorganization technique.

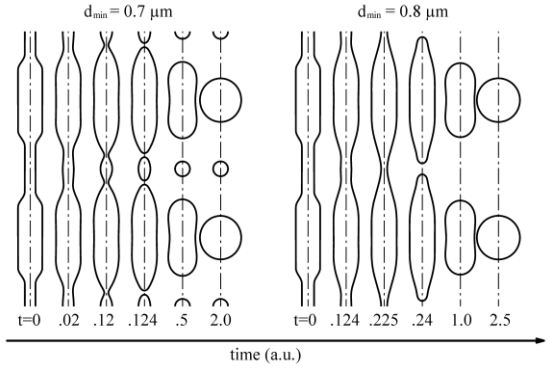

Figure 4: Evolution of a single pore for the case of d_{min}=0.7 µm and d_{max}=0.8 µm. The rest of parameters are identical.

Figure 3 shows the cleaved side of different multilayer structures obtained for different lengths L_n leading to different silicon foil thicknesses. For short L_n values around 4µm, (fig 3.a and b) usually solid layers around 6 µm thick form, whereas bubbles are trapped for layers slightly thicker (fig 3.c). For very thick layers, a long trapped void is left, that promote to two or more spherical voids if the annealing is large enough (fig 3.d).

It is well known that smooth cylinders of radius r become unstable under small perturbations of period larger than $2\pi r$ (Rayleigh criterion) due to capillary instabilities [15, 16]. Our profiles, however, weren't designed relying on Rayleigh instability criterion, but on nonlinear pore pinch off due to a strong modulation of the pore diameter. Since our pore profiles are composed of straight pore sections, it turns out that every section is subjected to capillary instabilities and spheroidization. This explains the appearance of bubbles as the length of the narrow-pore section increases. Furthermore, since spheroidization in a finite cylinder progresses from the endings [17], large trapped air cylinders will turn into two or more bubbles if the annealing process is long enough.

In order to get a more precise understanding of the phenomenon, we have simulated the profile evolution of a single modulated pore. In particular, we are interested in reproducing the collapsing and bubble formation in the narrow pore sections and we have found that the formation of a trapped bubble is very sensitive to the exact diameter d_n. More specifically, we have simulated the collapsing sequence for a pore profile with L_n=4 µm, L_w=5 µm, d_w=1.6 µm, and d_n values ranging from 0.6 to 0.9 µm. Figure 4 shows the pore evolution for two particular cases: d_n = 0.7 um and 0.8 µm. For d_n values below 0.75 um, roughly, the surface evolution at the sudden diameter changes triggers the pinching of the pore, trapping an empty space that rapidly becomes spherical. For d_n values above 0.75, a sudden behavior change occurs. Instead of a fast pore pinch-off on the edges, the narrow pore section tends to smooth slowly becoming instable and pinching the pore off in the center region, thus leaving no trapped void. This behavior resembles, in fact, a standard Rayleigh instability triggered by a small perturbation. Furthermore, as d_n is increased, the more the low perturbation case is approached. Regarding the pinch-off time (see fig. 5) it increases exponentially with d_n, but the curve makes a bump at d_n = 0.75 µm, signaling the change of behavior.

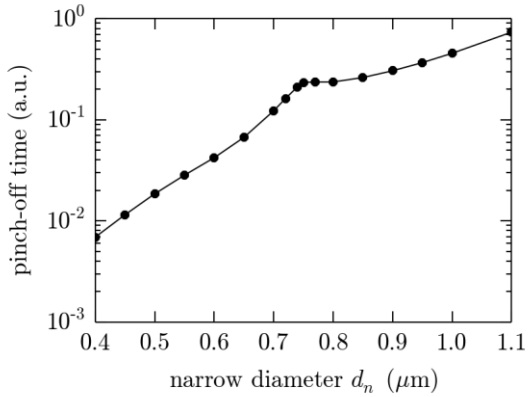

Figure 5: Dependence of the pore pinch-off time, during annealing, on the pore diameter in the narrow pore section.

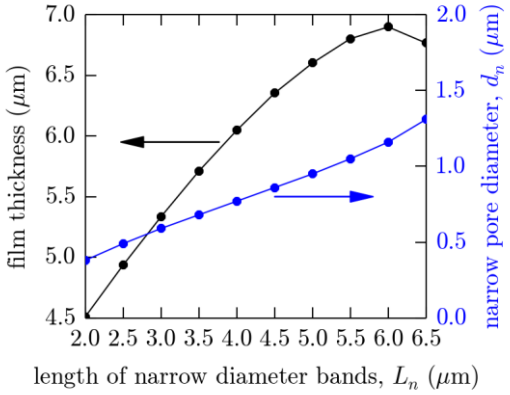

Figure 6: Estimation of the maximum layer thickness without bubbles, as a function of the narrow pore length. The narrow pore diameter, in blue, was adjusted to the minimum avoiding bubbles.

We have calculated the maximum layer thickness that can be achieved without bubbles for different L_n values considering a=2 µm, L_w=5 µm and d_w=1.6 µm. The narrow diameter was allowed to be the minimum value not leading to bubble trapping at every point. To determine the final layer thickness we have simulated the collapse of a single pore, measured the volumes and spacing between the spherical voids, and then applied equations (4) and (5). Results are shown in figure 6 for Ln values up to 6.5 µm. Beyond 6.5 µm, the modulation is so shallow that it takes very long to grow instable and the pores spheroidizes just as a straight pore. As a rule of thumb, pores can't be modulated at a periodicity shorter than the in-plane periodicity a; therefore, the minimum L_n considered was a=2.0 µm.

As can be seen in the figure 6, the final thickness can be adjusted by changing L_n and d_n, although the relation is not proportional peaking at L_n=6.0 with a maximum thickness value of 6.9 µm. This is not surprising since, as we increase L_n, we are also increasing d_n to avoid bubble formation, reducing the total amount of Si left in the structure, reducing also the final layer thicknesses and increasing the void spaces between them, even though the periodic distance between layers would stay the same. It is worth noticing that fig. 6 does not represent the absolute maximum thicknesses that can be achieved with the *millefeuille* technique. Here we have kept constant L_w and d_w, that have a main effect on the space formation, but also on the total silicon available in the porous structure before annealing and, thus, on the final layer thicknesses. Even more important, calculations have been performed for a rectangular-like pore modulation in depth, mimicking our early experiments. A different profile modulation, for instance following a simple triangular or sinusoidal shape (easily attainable with macroporous silicon technology) should help to improve the final layers thicknesses. As a matter of fact, we envisage that with an optimal pore profile it could be possible to achieve layers up to 10 µm for a=2 µm.

5 SUMMARY

Many crystalline silicon layers have been fabricated simultaneously by pore reorganization during annealing at 1200 ºC in Argon ambient. We call this structure *silicon millefeuille*. The number of layers and their thicknesses were controlled by adjusting the pore profile in-depth. Depending on the exact profile, layers can trap voids. Calculations show that layers up to 6.9 micrometers can be produced without bubbles using a rectangular pore profile. Thicker layers could be attained by further optimizing the profile shape. Layers of tenths of micrometers can be produced if trapped voids are allowed.

This work has been partially funded by TEC2008-02520 and the Network of Excellence "Nanophotonics for Energy."

[1] A. Brailove et al., Proc. of the 25th European Photovoltaic Solar Energy Conf., (2010) 1613.
[2] S. C. Baer, Patent No. US 2009/0056513 A1 (2009)
[3] F. Dross, et al. Appl. Phys. A-Mater 89, 149 (2007).
[4] J.H. Petermann, D. Zielke, J. Schmidt, *et al.* Prog. Photovolt.: Res. Appl. 20 (2012) 1.
[5] R. B. Bergmann, C. Berge, T. J. Rinke, J. Schmidt, and J. H. Werner, Sol. Energ. Mat. Sol. C. 74, 213 (2002).
[6] I. Mizushima, T. Sato, S. Taniguchi, and Y. Tsunashima Appl. Phys. Lett. 77 (2000) 3290.
[7] V. Depauw, I. Gordon, G. Beaucarne *et al.* J. Appl. Phys. 106 (2009) 033516.
[8] V. Depauw, Y. Qiu, K. Van Nieuwenhuysen *et al.* Prog. Photovolt: Res. Appl. 19 (2011) 844.
[9] D. Hernández, T. Trifonov, M. Garín, *et al.* Appl. Phys. Lett. 102 (2013) 172102.
[10] V. Lehmann, "Electrochemistry of Silicon. Instrumentation, Science, Materials and Applications" (Wiley-VCH, Weinheim, Germany, 2002).
[11] T. Trifonov, L. F. Marsal, A. Rodriguez, *et al.* Phys. Status Solidi C 2 (2005) 3104.
[12] T. Trifonov, M. Garín, A. Rodriguez, *et al.* Phys. Status Solidi A 204 (2007) 3237.
[13] W. W. Mullins, J. Appl. Phys. 28 (1957) 333.
[14] F. A. Nichols, and W. W. Mullins, J. Appl. Phys. 36 (1965) 1826.
[15] M. S. McCallum, P. W. Voorhees, M. J. Miksis, *et al.* J. Appl. Phys. 79 (1996) 7604.
[16] H. Wong, M. J. Miksis, P. W. Voorhees, and S. H. Davis, Scripta Materialia 39 (1998) 55.
[17] T. Sato, K. Mitsutake, I. Mizushima, and Y. Tsunashima, Jpn. J. Appl. Phys. 39 (2000) 5033.