High efficiency interdigitated-back-contact c-Si solar cells

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1. Abstract

In this work we describe a baseline fabrication process of interdigitated-back-contact IBC c-Si(p) solar cells, which combines conventional diffusion oven stages to define base p+ and emitter n+ regions at the back side, with outstanding front surface passivation using atomic layer deposited Al_2O_3 films. Best fabricated device reaches efficiency up to 20.3% (AM1.5G 1 kW/m^2, T=25ºC), with a short circuit density J_{sc}, open circuit voltage V_{oc} and fill factor *FF* of 40.6 mA/cm^2, 648 mV and 77.2% respectively.

2. Introduction

The interdigitated-back-contacted (IBC) solar cell concept is a promising photovoltaic structure for both laboratory and industrial crystalline silicon solar cells [1]. In this kind of cell, both base and emitter contacts are placed at the rear side of the cell, whereas light impinges on the opposite device surface (front side).

Some advantages of this structure are evident, such as the absence of metal shadow losses and the facility to assemble solar cells in modules with coplanar connection. However, in this type of device a high bulk lifetime, outstanding front and rear surface passivation, and low front reflectance are mandatory to obtain high efficiency solar cells. Atomic layer deposition ALD AL_2O_3 process is an excellent technique to achieve both outstanding surface passivation and very low reflectance combined with random pyramids [2] or other surface etching treatments, e.g. black silicon [3].

In the last decade, the Micro and Nanotechnologies Group at the Universitat Politecnica de Catalunya UPC MNT has been developing a baseline process to fabricate high efficiency (~20%) passivated emitter and rear cell PERC cells [4], [5]. In this work, we have adjusted this baseline process to manufacture high performance IBC devices combining conventional oven stages (boron and phosphorous diffusions and thermal oxidations), photolithography and front surface passivation with ALD Al_2O_3 over textured surfaces with random pyramids.

3. Baseline fabrication process and results

IBC solar cells were manufactured using high quality FZ <100> c-Si(p) 4" wafers with resistivity and thickness of 2.5±0.3 Ωcm and 280±20 µm respectively. Cells were fabricated using the flow process shown in Fig. 1, considering next main technological features, namely: 1) boron and phosphorous diffusions to form p+ (base contacts) and n+ (emitter regions) regions respectively, which are patterned using standard photolithography. 2) A front surface textured with random pyramids and passivated with 90 nm ALD Al_2O_3 films, resulting reflectance values below 0.5% at wavelengths λ~600 nm with effective surface recombination velocities below 3 cm/s (@ 1Sun). 3) A back reflector scheme consisting of a thermal SiO_2 (110 nm)/Al (~2 µm) stack was included at the rear side.

A total of 4 solar cells (3 cm × 3 cm area) with different emitter coverage f_e (67%, 75%, 80% and 86%) were fabricated in each wafer (see Fig. 2).

Cells were measured under AM1.5G 1 kW/m^2 solar spectrum (T=25ºC). Photovoltaic parameters are summarized in Table 1. The current-voltage (*J-V*) and power-voltage (*P-V*) characteristics of the best device (cell labelled #4 with f_e=75%) is shown in Fig. 3. Its external quantum efficiency *EQE* and front reflectance *R* curves are plotted in Fig.4. Measurements confirm outstanding efficiencies η's up to 20.3%, with a short circuit current density J_{sc}, open circuit voltage V_{oc} and fill factor *FF* of 40.6 mA/cm^2, 648 mV and 77.2% respectively for the best device. However, 3D simulations envisage even higher efficiency values (>~22%) in future runs using a selective emitter, lower substrate resistivities ~1Ωcm and increasing Al metallization thickness from 2 to 5 µm.

References

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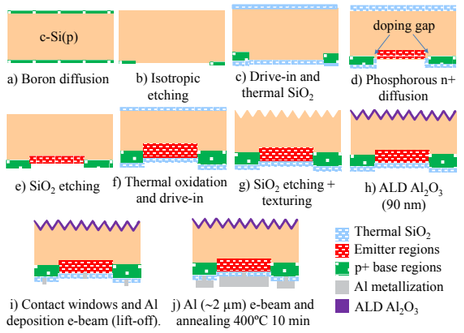

Fig. 1. Main stages of the baseline fabrication process with homogeneous emitter.

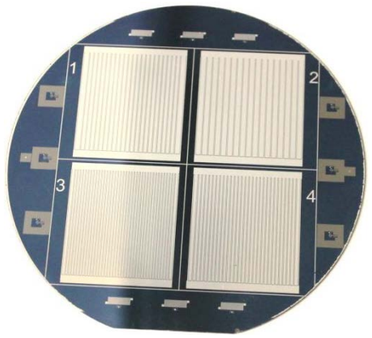

Fig. 2. Back side of a manufacturated wafer showing the four fabricated devices labelled #1, #2, #3 and #4, corresponding to emitter coverage values f_e's of 80%, 86%, 67% and 75% respectively.

Cell	f_e (%)	V_{oc} (mV)	J_{sc} (mA/cm^2)	*FF* (%)	η (%)
#2	86	652	41.0	75.0	20.0
#1	80	651	40.9	72.4	19.3
#4	**75**	**648**	**40.6**	**77.2**	**20.3**
#3	67	644	40.0	77.1	19.9

Table 1. Photovoltaic parameters of the fabricated devices. Measurements were performed under standard test conditions STC (AM1.5G 1 kW/m^2 solar spectrum and T=25ºC).

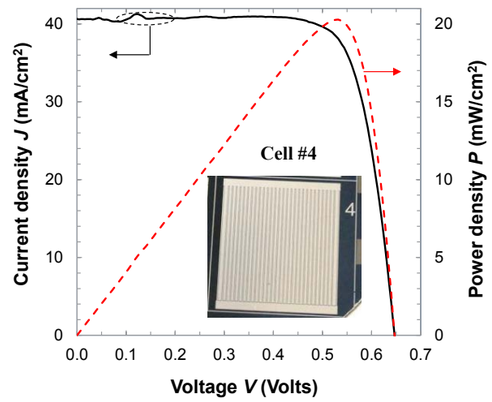

Fig. 3. *J-V* and *P-V* characteristics of the best device (cell #4).

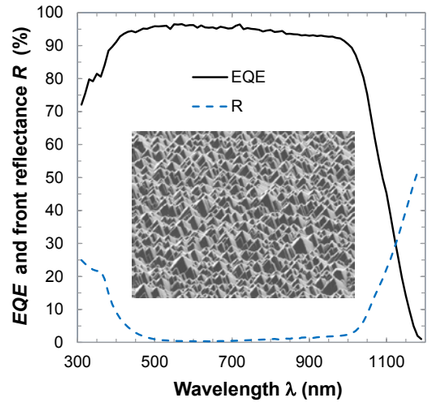

Fig. 4. *EQE* and front reflectance *R* curves of the best device (cell #4). Reflectance was measured in a precursor sample. A SEM image of the textured surface with random pyramids is also added in the inset.