A self-calibrating closed loop circuit for configurable constant voltage thermal anemometers

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This work describes a new circuit which applies a configurable voltage across an RTD while the current flowing through it is measured with a current mirror. The circuit also allows to work with voltages above the IC supply voltage to cope with the high power RTD dissipation normally required in thermal anemometers. The circuit is periodically calibrated to cancel the errors and amplifier offset and therefore improves measurement accuracy. Experimental measurements of the circuit fabricated using 0.35 μm AMS technology show the functionality and improved power efficiency.

Introduction: Thermal anemometers are widely used to measure flow velocity by sensing the heat transfer between the fluid and a hot element [1–3]. Open and closed loop strategies have been extensively used [4–7] to measure the convection heat transfer. Several challenges have to be faced, the first is how to increase the power efficiency as in a conventional anemometer bridge [7] at most 50% of the power goes to heat the sensing resistor. Moreover, the bridge arrangement does not allow four-wire measurement of the resistor value increasing noise and the measurement is sensitive to the amplifier offset. Finally, the anemometer bridge structure does not allow an easy programable target of the operation temperature.

In this work a measurement strategy based on controlling a loop to keep constant the voltage across the RTD and measuring the current I_{RTD} with a current mirror in series is proposed. At any value of the flow speed, the power delivered to the RTD is the maximum available $(V_A - V_B)^2/R_{RTD}$. The resistor value at a given flow speed can be calculated accurately using a four-wire measurement $(R_{RTD} = V_A - V_B/I_{RTD})$. The power efficiency can be greatly increased as the voltage drop in the current mirror can be kept much lower than the constant voltage drop across the sensing resistor.

The described circuit can be used with several control loop arrangements such as constant voltage (CVA) [4], thermal sigma-delta modulation ($\Sigma\Delta$) [5] or pulse width modulation (PWM) [6]. To implement $\Sigma\Delta$ or PWM modulation the voltage applied across the RTD is switched between two values (to deliver high or low power) depending on the value of the current at given time. This circuit allows the configuration of the loop to set different voltage values. Since the accuracy of current measurement can generally be affected by offset errors [8], the circuit includes calibration and offset cancelation.

Circuit description: The main architecture of the circuit is shown in figure 1. There are three operation modes : M1 and M2 are calibration and offset correction modes while M3 corresponds to the normal operation mode. Let us first describe the normal mode M3 where the error signal between the voltage drop across the RTD V_{DUT} and a target voltage V_{TG}, $Vd = V_{DUT} - V_{TG}$, (see Fig 1) is sensed and amplified. In order to provide high heating power to the RTD resistor, its terminals are wired to nodes V_A and V_B that are separated from the amplifier input by down level shifters composed by resistors R_A and R_B and cascode current sources delivering bias currents I_A and I_B respectively. This arrangements allow to apply, across the terminals of the RTD, voltages larger than the IC supply voltage by off-chip circuit or by on-chip circuits as described below. Linear feedback loops are used to adjust the values of I_A and I_B currents. In between the resistors R_A and R_B there are two analog multiplexers $MUX1$ and $MUX2$ that allow to implement the different operation modes and must withstand V_A and V_B, and therefore it could be necessary to implement them off-chip. In the normal mode of operation, the zero differential input voltage ($V_d = 0\,V$) of the amplifier must occur when $V_{RTD} = V_{TG}$. Then, both current sources must be properly adjusted to cause a voltage drop (V_{RA} and V_{RB}) across the resistors R_A and R_B for a desired V_{TG} (1).

$$V_{TG} = I_A R_A - I_B R_B = V_{RA} - V_{RB} \tag{1}$$

The two currents I_A and I_B are set in the calibration operation modes, M1 and M2. In fact, the feedback loops of the two current sources are

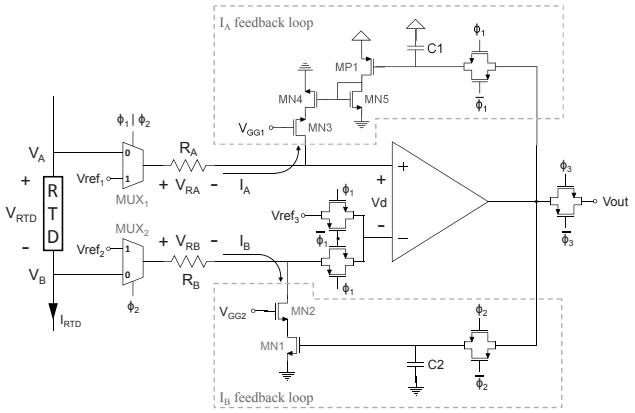

Fig. 1. Circuit diagram

controlled by three digital signals which control the circuit topology and select the corresponding operation mode (Fig.2).

In both calibration phases, three voltage references are used to adjust the voltage drops V_{RA} and V_{RB}. The voltage reference V_{ref3} determines the common-mode voltage at the input of the amplifier when the circuit is in the calibration phase.

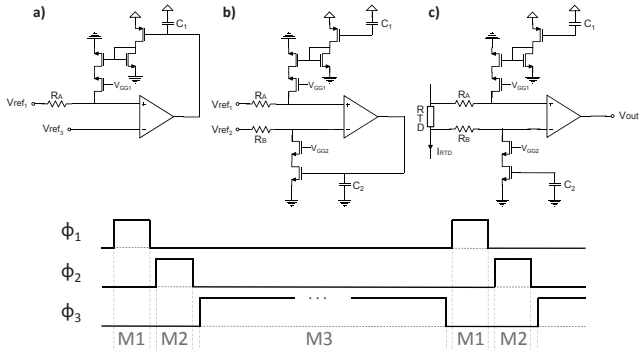

Fig. 2 *Top: equivalent circuit for M1, M2 and M3 operation modes (a,b and c respectively). Bottom: waveforms of the three digital signals which select the operation mode.*

In the first mode M1 (see Figure 2(a))($\{\phi_1\ ,\ \phi_2\ ,\ \phi_3\}$=$\{1\ ,\ 0\ ,\ 0\}$), V_{RA} is adjusted by switching the positive input to V_{ref1} and connecting V_{ref3} at the negative input of the operational amplifier while closing the positive feedback loop. V_{ref1} is set at the typical value of V_A and V_{ref3} is used to cause the desired voltage drop (2). Note that V_{ref3} must be within the input range of the operational amplifier.

$$V_{RA} = V_{ref1} - V_{ref3} \tag{2}$$

This closed loop adjusts the current I_A while sets the voltage at the capacitance C_A. This capacitance has been sized to maintain the voltage at the gate of MP1 when this operation mode comes to an end and sets the dominant pole of the active feedback loop. The phase of this loop is inverted by adding a current mirror (composed by MP1 and MN5) which provides loop stability.

In the second mode M2 (see Figure 2(b))($\{\phi_1\ ,\ \phi_2\ ,\ \phi_3\}$=$\{0\ ,\ 1\ ,\ 0\}$), the circuit adjusts I_B to cause the voltage drop V_{RB} (3). To do this, V_{ref1} is maintained at the positive input of the circuit while V_{ref2} is connected to the negative one. In this case a current mirror is not necessary to make the loop stable. As in the first mode, a capacitance (C_B) is set at the suitable voltage to maintain the current drain I_B once this mode ends. Note that V_{ref3} must be lower than V_{ref2}.

$$V_{RB} = V_{ref2} - V_{ref3} \tag{3}$$

Finally, in the third mode M3, or normal mode, as described earlier, ($\{\phi_1\ ,\ \phi_2\ ,\ \phi_3\}$=$\{0\ ,\ 0\ ,\ 1\}$), both calibration loops are open and the RTD is connected at the input of the circuit. Then, the output voltage (V_{OUT})

will be:

$$V_{OUT} = A(V_A - V_{RA} - V_B + V_{RB}) = A(V_{DUT} - V_{TG}) = AV_d \tag{4}$$

where A is the open-loop gain of the operational amplifier.

The anemometer sensor system is shown in Fig.3a. The circuit shown in Figure 1 is represented by the block diagram inside the dashed box . The amplifier is inside a feedback loop which forces the current through the RTD to keep the voltage drop across it stable at V_{TG}. The capacitance C_3 is used to maintain the current drain through the RTD while the calibration modes (M1 and M2) are activated. This capacitance also sets the dominant pole. Furthermore, the RTD current is sensed by a N:1 current mirror (MN6 to MN9, integrated inside the IC) generating a current I_{MEAS} that is externally accesible (5).

$$R_{RTD} = \frac{V_{TG}}{I_{RTD}} = \frac{V_{TG}}{NI_{MEAS}} \tag{5}$$

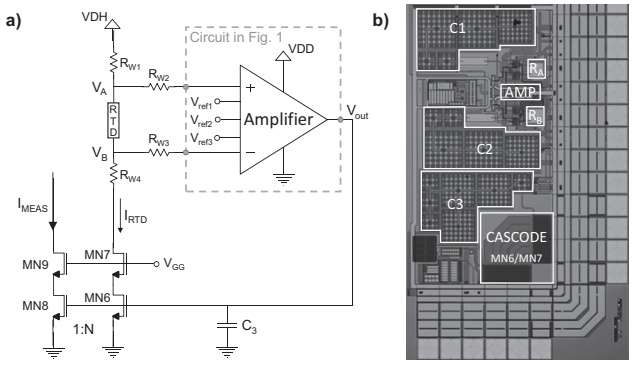

Fig. 3 *a) Anemometer system. R_{w1}, R_{w2}, R_{w3} and R_{w4} are the wire resistances. b) Layout of the fabricated circuit.*

Experimental results: The circuit has been implemented using AMS 0.35μm CMOS C35B4C3 process. Figure 3b shows a photograph of the circuit in Fig.3a, whose active area is 1260 μm x 630 μm. The sensor is supplied with $VDH = 5$ V while the circuit core supply voltage is $VDD = 3.3$ V. In this implementation, MUX1 and MUX2 have been integrated by using the thick oxide CMOS transistors of the specified process since they can withstand the VDH level. The amplifier has a symmetrical OTA topology and the resistors values are $R_A = R_B = 100\,k\Omega$. This value has been chosen to reduce power consumption and to make negligible the errors introduced by the resistance of the wires used to connect the sensor (Rw1 to Rw4). $C_1 = C_2 = 69$ pF, $C_3 = 67.5$ pF. The current scaling factor of the output cascode (MN6/MN7 and MN8/MN9) is N=32 to reduce the power consumption of the sensing current. The nominal value of the RTD used in the experiments is $R_{DUT} = 100\,\Omega$ at 0 °C.

Figure 4 shows an experimental result where different target voltages (V_{TG}) have been set to the RTD: 0.5 V, 1.5 V, 2.5 V and 3.5 V. The reference voltages for this experiment are: $V_{ref1} = 5$ V, $V_{ref2} = \{4.5\,V, 3.5\,V, 2.5\,V, 1.5\,V\}$ and $V_{ref3} = 1$ V. It can be seen that the different applied voltages are stable and that V_{DUT} changes after a calibration phase. Digital signals ϕ_1, ϕ_2 and ϕ_3 are also shown. The transient response of the RTD when $V_{DUT} = 3.5$ V is shown in Figure 5. The reference voltages are: $V_{ref1} = 5$ V, $V_{ref2} = 1.5$ V and $V_{ref3} = 1$ V. It can be seen how the current flowing through the RTD decreases due to the temperature increase in the RTD. After 50 seconds the current reaches the steady-state value $I_{RTD} = 855\mu$,A. The RTD value can be calculated by applying 5: $R_{DUT} = 3.5\,V/(32 \cdot 855\mu\,A) = 128\,\Omega$. Taking into account that the RTD is made from platinum and its coefficient temperature is $\alpha = 0.00385/°$C, this resistance value corresponds to a temperature of 72.5 °C. For $(V_A - V_B) = 4V$ a current $I_{RTD} = 30mA$ has been measured. For $VDH = 5$ V this means that the total power delivered to the RTD is approximately the 80% of the total power delivered to the anemometer. This figure can change when sigma-delta or PMW strategies are implemented but not significatively.

Conclusions: A new circuit for applying configurable constant voltages across an RTD while monitoring the current flowing through it is presented. The circuit allows over supply voltage actuation and provides offset cancelation. Experimental results are shown to demonstrate the functionality of this circuit, which has been fabricated using 0.35 μm AMS technology.

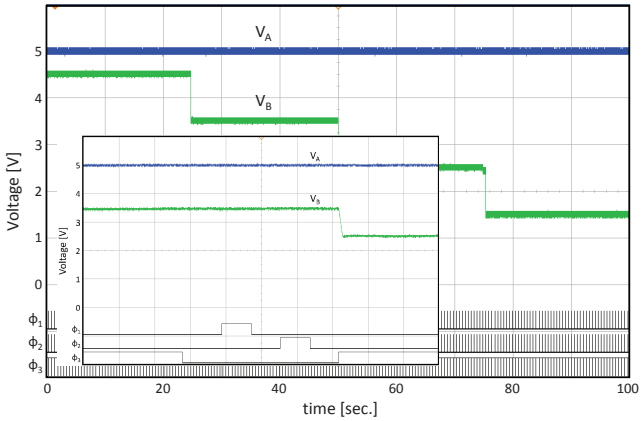

Fig. 4 *Result of a measurement in which V_{TG} has been set to four different values: 0.5 V, 1.5 V, 2.5 V and 3.5 V.*

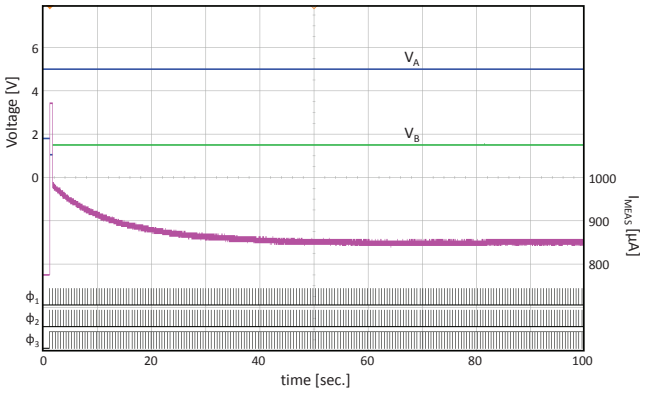

Fig. 5. Transient response of the RTD while applying $V_{RTD} = 3.5$ V.

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