On-chip thermal testing using MOSFETs in weak inversion

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Abstract—This paper analyses the feasibility of using metal-oxide-semiconductor field-effect transistors (MOSFET) operating in weak inversion as temperature sensors for on-chip thermal testing applications. MOSFETs in weak inversion are theoretically analyzed so as to know how their sensitivity to temperature depends on both dimensions and bias current. Theoretical predictions are then compared with simulations and experimental data resulting from MOSFETs fabricated in a commercial 0.35 μm CMOS technology. MOSFETs are experimentally subjected to changes of temperature generated by either a heating chamber or an on-chip power dissipating device. The performance of MOSFETs in weak inversion is also compared with that in strong inversion and with that of parasitic bipolar junction transistors (BJT). In the context of on-chip thermal testing, MOSFETs in weak inversion offer advantages in terms of layout area, linearity, current consumption and spread of the sensitivity to temperature due to process variations.

Keywords: MOSFET sensor; Subthreshold operation; Temperature sensor; Thermal testing; Weak inversion.

I. INTRODUCTION

Thermal testing and characterization of integrated circuits (IC), e.g. digital circuits [1, 2] and analogue radio frequency (RF) circuits [3, 4], through temperature sensors embedded into the same chip has been proved useful in the last years. The temperature sensor is placed close to the circuit under test (CUT) and measures on-chip thermal variations caused by the power dissipated by the CUT with the aim of extracting information, for example: (i) the efficiency (i.e. the DC power dissipated by the load divided by the DC power delivered by the DC source) of a RF power amplifier operating at 2 GHz [3], and (ii) the frequency response and the central frequency (at 830 MHz) of a RF low-noise amplifier [4]. In comparison with classical IC test techniques based on electrical measurements [5-7], thermal testing offers two main advantages for RF-ICs: the CUT is not electrically loaded, and measurements are performed at DC [3] or at low frequency [4, 8], which reduces the complexity and cost of the test.

On-chip thermal testing of RF-CUTs has been performed in [3, 4] using the well-known temperature dependence (i.e. –2 mV/K) of the base-emitter voltage of a parasitic BJT fabricated in CMOS technology [9]. However, the comparative analysis carried out in [10] shows that MOSFET-based temperature sensors (operating in strong inversion) offer attractive advantages for such applications: (i) fully compatibility with the fabrication process, (ii) less layout area (say, ten times less) required around the CUT, and (iii) more sensitivity (up to three times more) to on-chip thermal variations caused by the CUT. The main drawback of MOSFETs is that their sensitivity to temperature is more susceptible (say, four times more) to IC manufacturing process variations [10].

This paper goes a step further in the analysis of MOSFETs as temperature sensors for on-chip thermal testing applications. The approach proposed in [10] is applied herein to analyze the feasibility of using MOSFETs in weak inversion, instead of strong inversion, as

temperature sensors for such applications. Although MOSFETs in weak inversion have been already proposed as low-power temperature sensors [2, 11, 12], no comparative analysis (with respect to BJTs and MOSFETs in strong inversion) has been carried out in the context of on-chip thermal testing. After explaining the IC thermal testing technique behind the proposed temperature sensor, this paper provides theoretical models, simulations and experimental results of MOSFETs operating in weak inversion, and then it compares these results with those reported in [10] with the purpose of extracting the advantages and drawbacks of each sensing transistor.

II. ON-CHIP THERMAL TESTING TECHNIQUE

The temperature sensor analyzed herein is mainly intended for the on-chip thermal characterization of RF circuits using the heterodyne technique [4]. This technique operates as follows: two tones of high frequency f_1 and $f_2 = f_1 + \Delta f$ (Δf being, for instance, 1 kHz) are applied to the input of the RF-CUT (see Fig. 1a) and, as a consequence of the frequency mixing generated by Joule effect [13], the RF-CUT dissipates power at low frequency (i.e. at Δf) with information about the performance at high frequency (i.e. at f_1). Accordingly, the frequency response of a RF-CUT can be achieved by monitoring the amplitude of the power dissipated at Δf for different values of f_1 [4]. This power dissipated at Δf generates an on-chip temperature signal at the same frequency that can be measured by a nearby temperature sensor (T_1 in Fig. 1a) that is thermally coupled to the CUT through the semiconductor substrate; note that the low-pass filter response of the thermal coupling filters out other spectral components of the dissipated power (such as those at f_1, f_2, $f_1 + f_2$,…). The temperature sensor is then proposed to be connected to an amplifying band-pass filter (BPF) whose passband is centered at Δf so as to limit the bandwidth (and, hence, the noise) around the frequency of interest [8]. The BPF also rejects slow variations of the ambient temperature affecting the IC, and slow variations of on-chip temperature generated by the DC bias of the

CUT or by any other heating source.

The simplest temperature sensor that can be employed in Fig. 1a is a diode-connected MOSFET biased with a constant current source (I_B), as shown in Fig. 1b [8, 10]. In this circuit, the MOSFET carries out a small-signal temperature-to-voltage conversion at low frequency (i.e. at Δf) with the aim of extracting high-frequency information of the RF-CUT. Although the DC operating point of that circuit is quite susceptible to process variations, this is not a major concern since the DC level (and, hence, the corresponding absolute value of temperature) will be blocked out by the ensuing BPF shown in Fig. 1a. What it really matters here is the measurement of the temperature change at Δf generated by the RF-CUT when the heterodyne technique is applied. For this reason, next sections mainly focus on the ability of the sensor to detect changes of temperature (i.e. the sensitivity to temperature) rather than the accuracy. The amplitude of the temperature change to be detected depends on several factors (such as the operating frequency, the dissipated power, and the distance between the CUT and the temperature sensor), but values around tenths [8] or a few units of Kelvin [13] are expected. In the literature, we can find other thermal applications interested in measuring changes of temperature rather than the absolute value of temperature. For instance, the measurement of the amplitude (and also the phase shift) of temperature oscillations at a given frequency generated by the AC power dissipated by a heating element is used to determine thermal properties of fluids [14] and to monitor biofilm dynamics [15].

III. THEORETICAL ANALYSIS

This section analyses the same MOSFET-based temperature sensor proposed in [10] (i.e. a diode-connected n-type MOSFET biased with I_B, as shown in Fig. 1b) but in weak inversion (or subthreshold) operation. For the application of interest described in Section II, the current source I_B will be far from and, hence, not affected by the power dissipated by the CUT and, for this reason, I_B is assumed to be constant in the following analysis. Of course, I_B could be

affected by changes of ambient temperature, but such effects are not expected to be critical here whenever the IC test is faster than the temperature changes affecting I_B.

In weak inversion (i.e. $V_{GS} < V_{TH}$) and in saturation (i.e. $V_{DS} > 5U_T$), the current-voltage characteristic of a MOSFET can be modeled as follows [16]

$$I_D = \mu C_{OX} \frac{W}{L} (\eta - 1) U_T^2 \exp\left(\frac{V_{GS} - V_{TH}}{\eta U_T} \right), \tag{1}$$

where I_D is the drain current, V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage, W is the channel width, L is the channel length, V_{TH} is the threshold voltage, μ is the carriers mobility, U_T is the thermal voltage, η is a subthreshold slope factor, C_{OX} (= ε_{OX}/t_{OX}) is the gate oxide capacitance per unit area, ε_{OX} is the gate oxide permittivity, and t_{OX} is the gate oxide thickness. Unlike what happens in strong inversion where the current-voltage characteristic has a quadratic relationship [10], in weak inversion the relationship is exponential, as in BJTs; this is because in weak inversion the channel current flows by diffusion [17].

According to [18], three parameters involved in (1) depend on temperature:

$$U_T(T) = \frac{kT}{q} \tag{2}$$

$$\mu(T) = \mu_0 \left(\frac{T}{T_0} \right)^{\alpha} \tag{3}$$

$$V_{TH}(T) = V_{TH0} + \beta (T - T_0), \tag{4}$$

where T is the absolute temperature, T_0 is a reference temperature (e.g. 300 K), k is the Boltzmann constant ($1.38066 \cdot 10^{-23}$ J/K), q is the elementary charge ($1.60218 \cdot 10^{-19}$ C), μ_0 is the carriers mobility at T_0, α is a constant generally between –1.5 and –2, V_{TH0} is the threshold voltage at T_0, and β is a negative temperature coefficient; the value of such parameters for the

CMOS technology applied herein is reported in Table I [19]. Note that α and β are negative, so both μ and V_{TH} decrease with temperature.

For the circuit shown in Fig. 1b where the MOSFET is biased with $I_D = I_B$, the output voltage (which is equal to V_{GS}) can be expressed, from (1), as

$$V_o = \eta U_T \ln\left(\frac{I_B}{\mu C_{OX}\frac{W}{L}(\eta-1)U_T^2}\right) + V_{TH}. \tag{5}$$

Replacing now (2), (3) and (4) in (5) yields the temperature dependence of V_o

$$V_o(T) = V_{TH0} - \beta T_0 + T(\beta+\gamma) + (\alpha+2)\eta U_T \ln\frac{T_0}{T}, \tag{6}$$

where

$$\gamma = \eta\frac{k}{q}\ln\left(\frac{I_B}{\mu_0 C_{OX}\frac{W}{L}(\eta-1)U_{T0}^2}\right), \tag{7}$$

U_{T0} being the thermal voltage at T_0 (i.e. 26 mV). Assuming $(T_0/T) \approx 1$, the logarithmic function involved in (6) can be replaced by its first-order Taylor-series approximation, i.e. $\ln(T_0/T) \approx T_0/T - 1$. Consequently, Eq. (6) can be simplified to the following first-order temperature-dependent equation

$$V_o(T) \approx V_{TH0} - \beta T_0 + (\alpha+2)\eta U_{T0} + T\left(\beta+\gamma-(\alpha+2)\eta\frac{k}{q}\right), \tag{8}$$

whose sensitivity to temperature is

$$S_T = \frac{\partial V_o}{\partial T} = \beta+\gamma-(\alpha+2)\eta\frac{k}{q}. \tag{9}$$

Taking into account that k/q has a low value (i.e. 86 μV/K) and α is close to –2, the last term in (9) turns to be much smaller than the others and, therefore, S_T can be approximated to

$$S_T \approx \beta + \gamma . \qquad (10)$$

A MOSFET operating in weak inversion requires a high W/L and a low I_B [20, 21], so the term inside the logarithm in (7) is expected to be smaller than one and, hence, γ will be smaller than zero. Therefore, both β and γ are negative temperature coefficients and, consequently, the value of S_T resulting from (10) will be also negative. According to (7), higher values of $|\gamma|$ (and, hence, of $|S_T|$) can be achieved by operating deeper in weak inversion, i.e. higher values of W/L and/or lower values of I_B; these recommendations are opposite to those obtained in strong inversion [10]. Table II reports, for different MOSFETs biased with I_B = 10 nA, the theoretical value of S_T calculated by (10) using the technology information provided in Table I and assuming η = 1.5 [22]. Note that the values of S_T in weak inversion are not expected to be as high as those obtained in strong inversion [10] for a similar layout area occupied by the sensor.

The spread (or variability) of S_T (i.e. ΔS_T) due to IC manufacturing process variations can be evaluated by applying the law of propagation of uncertainties [23] in (10), thus resulting in:

$$\Delta S_T^{\,2} = \left(\eta \frac{k}{q}\right)^2 \left(\left(\frac{\Delta W}{W}\right)^2 + \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta I_B}{I_B}\right)^2 + \left(\frac{\Delta \mu_0}{\mu_0}\right)^2 + \left(\frac{\Delta t_{OX}}{t_{OX}}\right)^2 \right) + \Delta\beta^2 , \qquad (11)$$

where ΔW, ΔL, ΔI_B, $\Delta \mu_0$, Δt_{OX} and $\Delta\beta$ are, respectively, the spread (or variability) of W, L, I_B, μ_0, t_{OX} and β due to process variations. As in [10], ΔS_T depends on the relative variability of W, L, I_B, μ_0 and t_{OX}, but here these are multiplied by $\eta k/q$, which is a small value (129 μV/K for η = 1.5). For example, if the quadratic sum of the relative variability of W, L, I_B, μ_0 and t_{OX} equals 10 %, then the resulting value of ΔS_T equals 12.9 μV/K, which is less than 1 % of the nominal values of S_T reported in Table II. Accordingly, MOSFETs with a high W and/or a high L are not expected to carry major benefits in terms of spread of S_T when operating in

weak inversion, although they do in strong inversion [10]. On the other hand, the term $\Delta\beta$ is usually neglected [24] but here its effects on ΔS_T could be comparable to those discussed before.

As explained in Section II, the change of temperature (ΔT) to be detected by the MOSFET sensor shown in Fig. 1b is to be caused by a change of power (ΔP) dissipated by the CUT. Consequently, the change of the sensor output voltage (ΔV_o) can be expressed as a function of ΔP as

$$\Delta V_o = S_T \Delta T = S_T R_{th} \Delta P = S_P \Delta P , \tag{12}$$

where R_{th} is a thermal coupling resistance that relates the change of temperature at the MOSFET sensor to the change of power dissipated by the CUT, and S_P is the sensitivity of the sensor to the power dissipated, which depends on both S_T and R_{th}.

IV. SIMULATION RESULTS

The temperature sensor shown in Fig. 1b has been simulated with Cadence in 0.35 μm CMOS technology of AMS (AustriaMicroSystems) with $V_{DD} = 3.3$ V and using BSIM3v3 models. Table II summarizes the dimensions of the MOSFETs simulated, which have a high W/L so as to increase the sensitivity to temperature, as suggested by (7) and (10). The temperature dependence of such MOSFETs has been simulated through a DC temperature-sweep analysis assuming 300 K (27 ºC) as a reference (i.e. $\Delta T = T - 300$ K).

Figure 2 shows how the output voltage of the sensor in Fig. 1b depends on temperature for different MOSFET dimensions when $I_B = 10$ nA. For such dimensions, the output voltage decreases linearly with temperature, as predicted by (8). Furthermore, S_T increases (in absolute value) with the factor W/L, as expected from (7). MOSFETs M3 and M4, which have different values of W and L but the same W/L, show almost the same temperature dependence, as also expected from (7). The value of S_T of each of the cases represented in Fig. 2 and the corresponding value normalized to the maximum sensitivity (i.e. that of M3 or M4) are

summarized in Table II. Note that the values of S_T resulting from simulations are very similar (differences are smaller than 10 %) to those calculated by (10) and, therefore, the models developed in Section III seem to be useful for a first estimation of S_T.

Figure 3 shows how the output voltage of M3 depends on temperature for different bias currents (5 nA, 10 nA, and 20 nA). For the three currents simulated, the output voltage decreases linearly with temperature, as predicted by (8). In addition, as suggested by (7), $|S_T|$ decreases with I_B; to be precise: S_T equals −1.602 mV/K, −1.529 mV/K and −1.455 mV/K for 5 nA, 10 nA, and 20 nA, respectively. Note that decreasing I_B by a factor of 4 (e.g. from 20 nA to 5 nA) or increasing W/L by a factor of 4 (e.g. from M1 to M2, or from M2 to M3) brings about the same increase in $|S_T|$ (around 150 μV/K in the previous examples).

The effects of process variations on S_T have been simulated through a Monte Carlo analysis of 50 runs. Assuming one standard deviation of S_T as ΔS_T, we have $\Delta S_T \approx 10$ μV/K for the different MOSFET dimensions simulated. Taking into account the values of S_T provided in Table II, the resulting $\Delta S_T/S_T$ is smaller than 1 %, which is quite similar to that obtained with BJTs [10]. Note, however, that the Monte Carlo analysis assumes the spread due to process variations of some parameters (e.g. W, L, μ_0, t_{OX} and V_{TH0}) but not of others (such as α and β) and, therefore, the previous simulation results of $\Delta S_T/S_T$ could be too optimistic.

The sensor in Fig. 1b has also been simulated over the industrial temperature range (i.e. from −40 ºC to 85 ºC) with the aim of evaluating how S_T depends on the operating temperature (note that in Figs. 2 and 3, it is assumed to be 27 ºC). The relative change of S_T (calculated as $\left|\left(S_T(T)-S_T(27^\circ\mathrm{C})\right)/S_T(27^\circ\mathrm{C})\right|$) versus the operating temperature for different MOSFETs biased with $I_B = 10$ nA is represented in Fig. 4. Such simulations show that S_T undergoes a very small change (e.g. the change is smaller than 1 % for M2, M3 and M4) and, therefore, the linear thermal response modeled by (8) seems to be applicable in the industrial

temperature range. In comparison with the performance in strong inversion [10], MOSFETs in weak inversion offer a value of S_T that is more independent (up to ten times more) of the operating temperature and, consequently, they offer more linearity. Simulations have also shown that the effects of leakage currents coming from reverse-biased pn junctions (such as the drain-bulk junction) on the temperature dependence of the MOSFET are negligible, at least for temperatures lower than 85 ºC; for instance, the leakage current of the drain-bulk junction is around 10 pA at 85 ºC for M4, which is a thousand times smaller than the bias current (i.e. 10 nA).

V. EXPERIMENTAL RESULTS

A chip including MOSFET-based temperature sensors with the topology shown in Fig. 1b and with different values of W/L (those listed in Table II) has been implemented in 0.35 µm 2P4M (2 levels of poly, 4 levels of metal) CMOS technology of AMS. The designed chip also includes heaters that are placed at 5 µm from each of the sensors, as shown in Fig. 5a, with the purpose of testing the capability of the sensors to monitor on-chip thermal variations caused by the power dissipated by other embedded circuits; the device used as a heater is another diode-connected n-type MOSFET with W_h = 450 µm, L_h = 1 µm and 15 fingers. Two additional blocks have been embedded into the chip (see Fig. 5b): (a) a current mirror that converts an external current (I_{ext}) from microampere to nanoampere range, and (b) an opamp-based voltage follower that avoids the loading effects of external instrumentation. This opamp has (i) an input common mode voltage with a minimum value of 200 mV, which enables us to read the low voltage coming from the MOSFETs in weak inversion, and (ii) a maximum input offset voltage (V_{IO}) of 2 mV, whose effects are not expected to be critical here since we will represent the change of voltage with respect to that obtained at the beginning of the test (i.e. at $\Delta T = 0$ or $\Delta P = 0$). Furthermore, note that the MOSFET sensor is close to the heater (at 5 µm) and its sensitivity is around 1-2 mV/K, whereas the opamp (and also the current mirror) is far

from the heater (more than 200 μm) and the temperature coefficient of V_{IO} is much lower (typical values are 1-10 μV/K). Consequently, the effects of the dissipated power on V_{IO} (or other non-idealities of the opamp) are expected to be much lower than those on the sensor.

The temperature sensors have been initially tested by means of a heating chamber (MEMMERT, type UM-100), as shown in Fig. 5c; in this experiment, the embedded heaters did not dissipate power. A bench-top DC current source (Advantest R6240A) provided a stable I_{ext} that was converted to the nanoampere range through the on-chip current mirror, whereas a digital multimeter (HP 34401A) measured the output (V_o) of the voltage follower. Moreover, the actual value of temperature inside the chamber was monitored by a reference temperature sensor (Pt100 IEC-751 Class A) whose value was measured by another digital multimeter (HP 3458A) applying the four-wire measurement method. Using this set-up, the output voltage of different MOSFETs biased with $I_B = 10$ nA was measured at different temperatures. The results are represented in Fig. 6, where the output voltage decreases linearly with temperature and, in addition, the higher the factor W/L, the higher the sensitivity, the same as in Fig. 2. If a straight line is fitted to the experimental data in Fig. 6 by means of the least-square method, the resulting maximum nonlinearity error (expressed as a percentage of the full-scale span, FSS) for the four MOSFETs is around 0.5 % FSS, which is an acceptable value for IC testing purposes. The experimental values of S_T resulting from Fig. 6 and the corresponding value normalized to the maximum are reported in Table II. Note that the experimental values of S_T are very similar to those resulting from simulations (differences are smaller than 5 %). Experimental tests with the heating chamber also showed that the voltage follower was not able to correctly read the sensor output voltage at high temperatures (say, over 70 ºC) because the voltage was smaller than 200 mV.

The temperature sensors have been then tested at room temperature to monitor on-chip thermal variations generated by the embedded heaters, as shown in Fig. 5d. The sensor was biased and measured using the same instrumentation indicated in Fig. 5c, whereas the heater

was driven externally by a DC voltage source (Agilent E3631A); the current-voltage characteristic of the heater was previously acquired using R6240A and, therefore, the current (and, hence, the power) applied to the heater was accurately known for any voltage supplied later by E3631A. Using this set-up, the steady-state output voltage of the sensors was measured for different values of DC power applied to the heater and, then, S_P was calculated.

The effects of the power dissipated by the heater on the sensor output voltage are represented in Fig. 7 for different MOSFETs biased with $I_B = 10$ nA, and in Fig. 8 for different bias currents applied to M3. In both figures, the output voltage decreases linearly with the dissipated power, as expected. Comparing the simulation results in Fig. 2 with the experimental results in Fig. 7, we realize that in both cases the sensitivity increases with W/L, but such an increase is smaller in Fig. 7. This discrepancy can also be observed by contrasting the normalized values of S_P resulting from Fig. 7 with those of S_T resulting from Fig. 2, as reported in Table II. Maybe the effective temperature change detected by the sensor was smaller than that expected for MOSFETs with a high W (i.e. when the dimensions of the sensor were comparable to those of the heater) and, for this reason, there are such differences between Figs. 2 and 7. On the other hand, comparing the simulation results in Fig. 3 with the experimental results in Fig. 8, we can see that the effects of bias current on S_T and S_P are very similar. In both figures, the sensitivity increases with the same factor as the bias current decreases.

The spread of S_P due to process variations has also been experimentally evaluated by testing nine samples of the designed chip from the same batch. For example, $\Delta S_P/S_P$ was 1.2 % for M3 using $I_B = 10$ nA; ΔS_P is assumed to be one standard deviation of S_P, in such a case: 20 μV/mW over 1.72 mV/mW. Such an experimental value of $\Delta S_P/S_P$ is slightly higher than the simulated value of $\Delta S_T/S_T$ presented in Section IV and, consequently, the limitations of the Monte Carlo analysis indicated before do not seem so critical for a first estimation of

the spread. In comparison with the experimental results reported in [10], MOSFETs operating in weak inversion offer values of $\Delta S_P/S_P$ very similar to those obtained with BJTs.

VI. DISCUSSION AND CONCLUSIONS

The work presented herein together with that in [10] enable us to compare the performance of MOSFETs in weak inversion with that in strong inversion and also with that of parasitic (vertical) BJTs, always in the context of on-chip thermal testing. As summarized in Table III, several topics can be compared:

(a) CMOS compatibility: MOSFETs (either in strong or in weak inversion) are fully CMOS compatible and, therefore, they are preferable for the on-chip thermal testing of ICs fabricated in a CMOS process.

(b) Area: In CMOS technology, the use of parasitic BJTs is not as flexible as that of MOSFETs in terms of area. The well-characterized parasitic BJTs available in the design kits generally occupy a layout area that is much larger (say, ten times more) than that required using MOSFETs (either in strong or in weak inversion); for instance, the emitter area is 10 x 10 μm^2 in 0.35 μm from AMS, 10 x 20 μm^2 in [9], and 15 x 15 μm^2 in [25]. For the application described in Section II, a parasitic BJT with a smaller emitter area could be valid, but no reliable simulations could be carried out because of the lack of models; a preliminary tape-out intended for the experimental characterization of those small parasitic BJTs could solve such a limitation but at the expense of a higher cost. Note that this discussion about area mainly focuses on that occupied by the sensing transistor (and not that of the bias circuit or the BPF) since it is the most critical for the testing application of interest: the sensing transistor must be small enough to fit within the empty areas of the layout of the CUT with minimum impact on its design.

(c) Sign of S_T: The output voltage of both MOSFETs in weak inversion and BJTs has a negative temperature coefficient, whereas that of MOSFETs in strong inversion usually shows a positive temperature coefficient.

(d) Magnitude of $|S_T|$: Using the sensitivity to temperature of BJTs as a reference, the sensitivity of MOSFETs in weak inversion is lower (around 20-30% lower), whereas that in strong inversion can be significantly higher (more than three times higher).

(e) Advices to increase $|S_T|$: The guidelines to increase the sensitivity to temperature in weak inversion (i.e. high W/L and low bias current) are opposite to those obtained in strong inversion (i.e. low W/L and high bias current). In terms of output noise voltage and output resistance, it is preferable to increase $|S_T|$ by using a higher value of W/L in weak inversion and a higher value of the bias current in strong inversion. The fact of using a lower value of the bias current in weak inversion or a lower value of W/L in strong inversion not only increases $|S_T|$, but also the output noise voltage (to be precise, the white noise component) and the output resistance and, therefore, the circuit in Fig. 1b becomes more susceptible to interference and the loading effects of the ensuing BPF (Fig. 1a) could be higher. As for the flicker noise component, the higher the factor $W \cdot L$, the smaller the output noise voltage [20], but the higher the area required around the CUT.

(f) Spread of S_T due to process variations: MOSFETs in weak inversion and BJTs have a similar susceptibility to process variations (i.e. $\Delta S_T/S_T \approx 1\%$), which is around four times better than that obtained with MOSFETs in strong inversion. Note, however, that these results come from the experimental test of a reduced number of samples from the same batch and, therefore, higher values of spread could be expected if samples from different production batches were tested.

(g) Linearity: In the industrial temperature range, MOSFETs in weak inversion offer a higher linearity (up to ten times more) and, therefore, the change of the output signal is expected to be almost the same regardless of the operating temperature.

(h) Current consumption: The required bias current is in the range of nanoamperes for MOSFETs in weak inversion, nanoamperes or microamperes for parasitic BJTs [9], and microamperes for MOSFETs in strong inversion [10]. If the opamp needed for the BPF in Fig. 1a has a current consumption of tens of microamperes, then the bias current of the MOSFET sensor becomes negligible in weak inversion but not in strong inversion and, consequently, the overall current consumption of the temperature sensor circuit is expected to be higher in strong inversion; note that the current consumption of the bias circuit is not assumed before because the temperature sensor circuit could easily make a good use of the bias circuit of the CUT.

According to the previous discussion, the major benefits of using MOSFETs in weak inversion in comparison with BJTs are: higher CMOS compatibility and lower layout area around the CUT. On the other hand, in comparison with MOSFETs in strong inversion, MOSFETs in weak inversion offer the following advantages: lower spread of S_T due to process variations (but always taking into account that the study here has been limited to a reduced number of samples from the same batch) and lower current consumption; this is, however, at the expense of a lower value of S_T. The CUT to be tested applying the technique explained in Section II will also play a significant role in the selection of the most appropriate sensing transistor. For instance, for the on-chip thermal testing of a CUT that generates low changes of temperature, a MOSFET in strong inversion seems more appropriate because it offers higher values of S_T. On the other hand, for a CUT that causes significant changes of temperature, a MOSFET in weak inversion could be more attractive since it enables us to optimize the testing sensor circuit in terms of power consumption.

For CMOS technologies different than that tested herein (i.e. 0.35 μm from AMS), we can

expect results similar to those shown in Table II provided that their technology parameters are similar to those presented in Table I; this has been proved through simulations carried out in 0.18 μm CMOS technology from United Microelectronic Corporation (UMC). For technologies whose parameters are not so similar to those in Table I, the numerical results in Table II are not valid, but the qualitative conclusions given in Table III (for instance, advices to increase the sensitivity) are applicable; this has been proved through simulations performed in a 65 nm CMOS technology. Regardless of the technology being used, it is not recommended to design a MOSFET temperature sensor with the smallest value of L or W, as usually happens in analog IC design, since it could increase both the output noise voltage and the spread of the sensitivity to temperature, as suggested by (11).

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SHORT BIOGRAPHIES

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Figure 3. Simulated output-voltage change of M3 versus temperature for different bias currents.

Figure 4. Simulated relative change of S_T versus the operating temperature for different MOSFETs biased with $I_B = 10$ nA.

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Figure 6. Experimental output voltage versus temperature for different MOSFETs biased with $I_B = 10$ nA. The horizontal axis represents the increase of temperature (ΔT) applied through the heating chamber, whereas the vertical axis represents the change of voltage (ΔV_o) with respect to that obtained at $\Delta T = 0$.

Figure 7. Experimental output voltage versus power for different MOSFETs biased with $I_B = 10$ nA. The horizontal axis represents the increase of power (ΔP) dissipated by the heater, whereas the vertical axis represents the change of voltage (ΔV_o) with respect to that obtained at $\Delta P = 0$.

Figure 8. Experimental output voltage of M3 versus power for different bias currents. The horizontal axis represents the increase of power (ΔP) dissipated by the heater, whereas the

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Table III. Comparative analysis between BJT- and MOSFET-based temperature sensors operating in either strong or weak inversion.

Figure 1

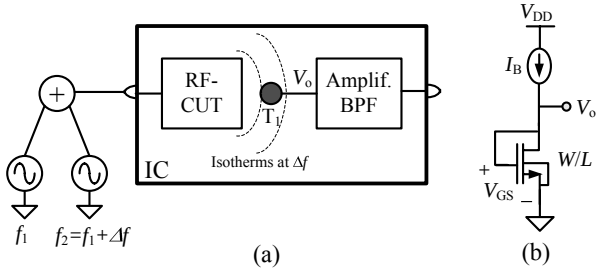

Figure 2

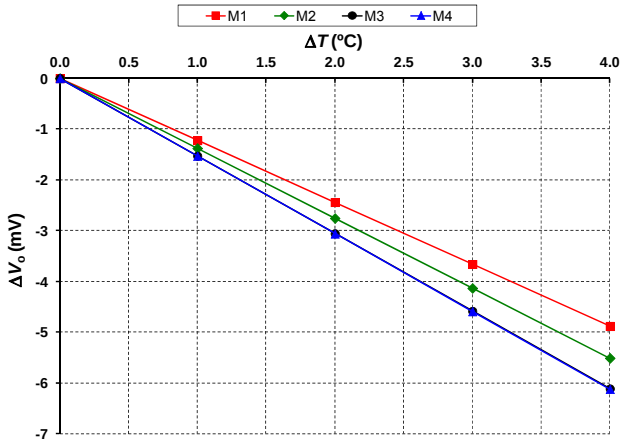

Figure 3

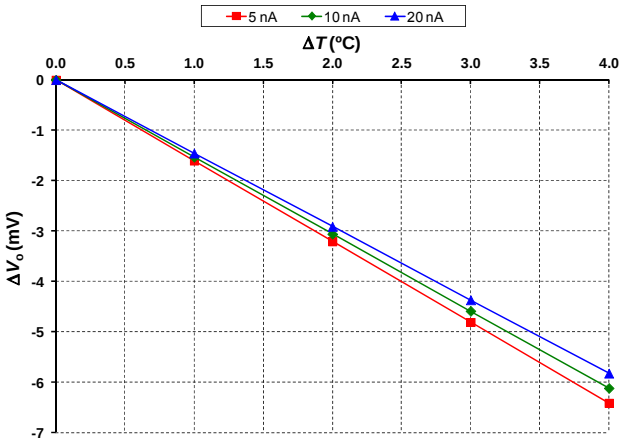

Figure 4

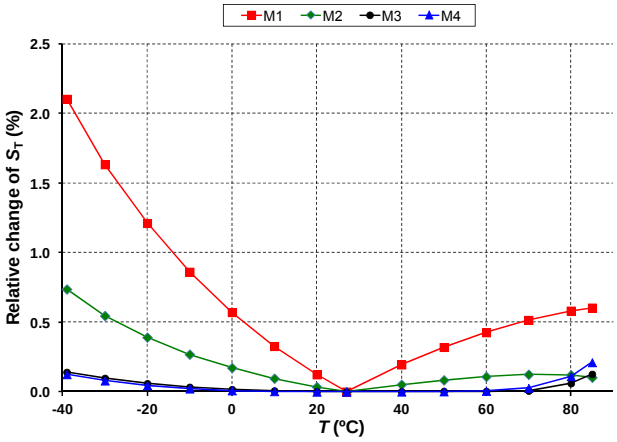

Figure 5

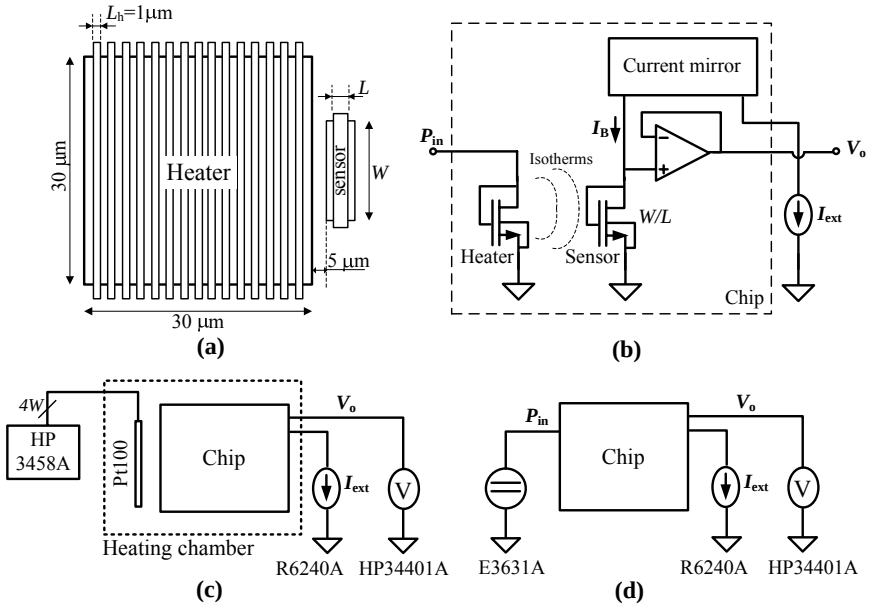

Figure 6

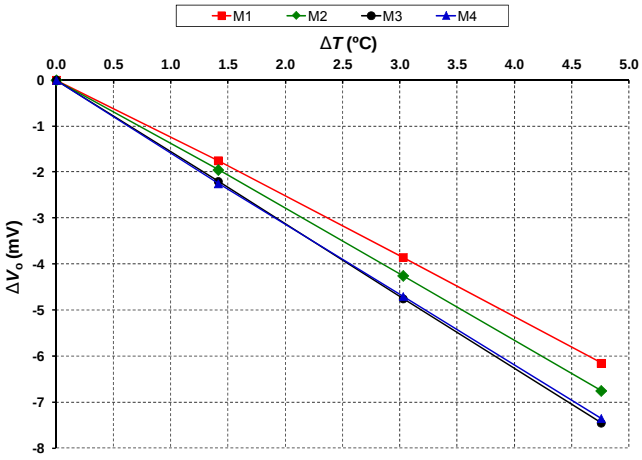

Figure 7

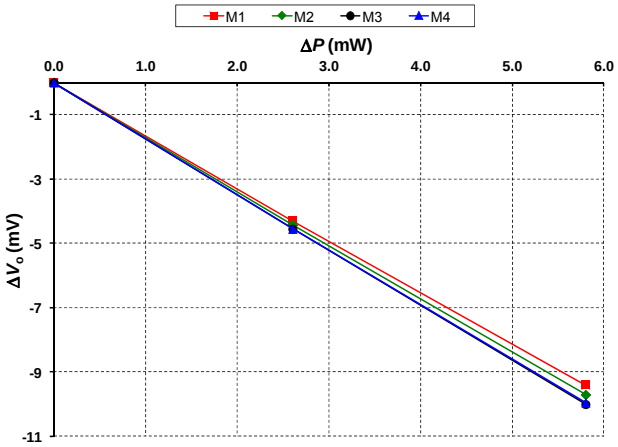

Figure 8

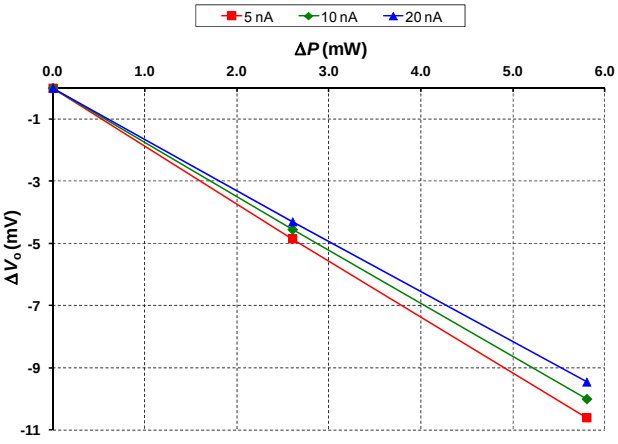

Table I

Parameter	Value
μ_0	370 $cm^2/V/s$
V_{TH0}	0.4979 V
α	−1.8
β	−1.1 mV/K
t_{OX}	7.6 nm

Table II

Sensor	W (μm)	L (μm)	Theoretical results	Simulation results		Experimental results			
						Heating chamber		Power applied to the heater	
			S_T (mV/K)	S_T (mV/K)	Norm. S_T	S_T (mV/K)	Norm. S_T	S_P (mV/mW)	Norm. S_P
M1	1	1	-1.32	-1.22	0.80	-1.29	0.82	-1.62	0.94
M2	4	1	-1.50	-1.38	0.90	-1.42	0.90	-1.67	0.97
M3	16	1	-1.68	-1.53	1	-1.57	1	-1.72	1
M4	24	1.5	-1.68	-1.53	1	-1.54	0.98	-1.72	1

Table III

	BJT	MOSFET in strong inversion	MOSFET in weak inversion
CMOS compatibility	Low-Medium	High	High
Area	High	Low	Low
Sign of S_T	Negative	Positive	Negative
Magnitude of $\|S_T\|$	Medium	Medium-High	Low-Medium
Advices to increase $\|S_T\|$	--	$(W/L)\downarrow$ and $I_B\uparrow$	$(W/L)\uparrow$ and $I_B\downarrow$
Spread of S_T due to process	Low	Medium	Low
Linearity in [-40,85]ºC	Medium-High	Medium-High	High
Current consumption	Low-Medium	Medium	Low