Evaluation by Simulation of Merit Figures for Different Grid Connected Photovoltaic Inverter Topologies

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Al iaio, que ens va deixar durant la realització d'aquest projecte, per transmetre'm el gust per l'electrònica, per les bones estones i pels magnífics consells que ens vas donar.

A tota la meva familia, per ser sempre al meu costat i donar-me tot el que he necessitat a la vida per tirar endavant i ser on sóc. I especialment a la Carme, per tota l'estima, suport i comprensió durant aquest temps.

Als meus amics i amigues, que m'han trobat a faltar uns quants mesos, ja torno.

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Chapter 1

Introduction

1.1 The energy in the world

Energy is necessary for all. As Albert Einstein established, matter and energy are essentially the same thing, so the world where we live is made basically of energy.

However, our world, as any system, has energy leakages, so it needs an exterior net energy contribution to be maintained.

The solar energy is the most primary energy source in our planet. The irradiance of the sun over all the surface of the earth is the responsible of most of the other energy sources that we have in our world. The capacity of the sun light to be transformed in other type of energy sources is amazing and it can be profited by lots of ways.

1.1.1 Non-Renewable Energy

The term “non-renewable” energy is not true at all. In fact, all the energy sources are renewable, because the energy cannot be created, nor destroyed, only can be transformed. The problem is that non renewable of energy sources require millions of years to be created, so the consumption rate that the humanity requires is not compatible with the creation necessary time. Therefore, if we consume these sources at the present rate, they will disappear in few years and will not be created until millions of years later. That’s the reason for what they are called ”non-renewable”. These energy sources are created due to the sun light energy, as are the result of the accumulation of organic material during millions of years, and this organic material is created due to the photosynthesis of the vegetables and the life cycle present in our planet. Petrol, coal and natural gas are examples of this type of energy. Nowadays are the most used sources of energy and from which had been sustained all the industrial revolutions that we have lived until now.

1.1.2 Renewable Energy

The sources of energy called “renewable” are the energies which are continuously generated from natural sources. They can be consumed at the same rate that are generated, without generating any harmful waste for the natural environment and transforming this consumption into an harmonic cycle in the nature Despite this ideal point of view, environmentally aggressive

processes are needed to create the machines capable of transforming these energies to utile energy for the humanity.

The wind energy, one of these sources of energy, is caused by the unequal warming of the atmosphere, resulting on imbalance of pressures that causes the air fluxes in all the world. The energy source known as "eolic energy", in reference to the greek god of the wind "Eolos", profits those air fluxes to move turbines that are capable to generate thousands of kilowatts. Specifically, the latest wind turbines models being installed can generate up to 8MW by each one. These type of wind turbines are normally designed to work offshore, so the dimensions of one of these eolic parks can be considerably big, and can generate up to hundreds of megawatts.

The hydropower is another type of energy source caused by the sun light. When the sun evaporates the water of the sea causing all the water cycle, a great amount of energy is directly accumulated, and it can be profited by the use of great dams. Although the hydropower is considered a renewable source of energy, the environmental impact caused by the construction of dams is not negligible.

The geothermal energy is an example of renewable source energy that does not come from the energy of the sun. It consist on taking advantage of the magma bags that are close to the crust, to heat water and create the appropriate pressure to move a turbine in charge to create the final energy. This type of energy is not present in most places of the world but, for example, in Iceland, where almost all the electricity of the country is generated by this method due to the unique geological conditions of the country.

The solar light energy, in fact, can be directly transformed into usable energy, without the collaboration of any natural process. There are three ways to collect the solar energy.

One of them is the thermal solar panels, which basically collect the warm of the sun irradiance and transmit it through some metals, which transport the warm from one point to another, such as a water tank of a house.

Another thermal way to collect the solar energy is the technology known as "CSP" technology, which is not fully developed yet but, for sure, it will have an important paper in the future. The CSP technology consists on collecting the sun light by the use of dozens or hundreds of mirrors into a point, where special salts are heated. This collected hot, heats the water to produce the steam which is used to move the turbine and produce electricity. As the warmth can be stored in the salt tank, the central can produce electricity even at night, when the sun is not present.

The third way is the photovoltaic solar energy production. It consists on profiting the energy of the photons to free electrons and, therefore, generating energy. This process is called the *photoelectric* effect. This thesis will be onwards focused on this type of energy production.

1.1.3 Why photovoltaic solar panels?

The only way to transform the solar energy to electricity without any other conversion (nor natural nor artificial) is the use of the photovoltaic solar panels technology.

Based on the use of the semiconductors, the photovoltaic solar panels are capable of transforming the photons (light quantums), into electrical power. This techonology has lots of advantages over other options, but, of course, has other disadvantages.

Main weak points of photovoltaic technology.

- The technology must be developed to improve the efficiency of the solar panels.

- The necessary area per kilowatt is big.
- In isolated installations some accumulator is needed (normally batteries).
- The materials and chemical processes that are necessary to produce the solar panels are not environmental friendly [1] [2].

In the other hand, main strong points of photovoltaic technology.

- Decentralized points of energy production.
- The production area can take advantage of other human activities, for example, buildings.
- The production cannot be controlled by the energetic oligopoly.
- It's a clean energy and do not require any consumption nor produces any waste during the generation process.

Indeed, this thesis tries to rich the present knowledge about this technology, the solar photovoltaic energy.

The importance of this technology is not only that it is a clean and renewable type of energy, nor it is the fact that it will be able to be applied into lots of surface types, such as clothes, what gives to it huge economic and innovative opportunities.

It is important to be conscious that, for its characteristics, solar panels are the only renewable energy which will make us capable to recuperate our energetic sovereignty. While the other types of renewable and clean energies require a great infrastructure and great investment, only available to great energetic companies, the photovoltaic technology can outline a different energetic model, based on popular control of the energy generation, and therefore the democratization of its benefits. Indeed, the prices of solar panels nowadays are cheap enough to make this energy viable to be installed at any building, giving to the owner of the building the corresponding benefits or discount into the electricity bill.

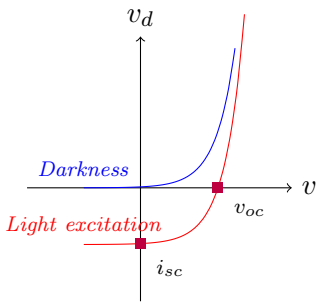
Another contribution of this energy is the possibility to eliminate great energetic highways, which are the responsible of several damages to humans who are exposed to its electric fields, and other environmental problems [3]. Of course, it involves a radical change in the energy model of generation and consumption, so the implementation of this change will not be easy, and will require the implication of all the people and governments. Unfortunately, in some countries, like the spanish state, the legality has turned against some photovoltaic generation strategies, like the auto-consumption of solar energy [4], and against the decentralization of the energy generation.

1.2 Photovoltaic Panels: A technical review

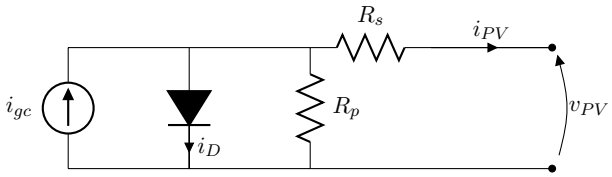
1.2.1 The solar cell

A solar cell is a basic element based on p-n junction. A p-n junction is the junction of a silicon base doped with other chemical elements that provide an excess of electrons ("n" material) or holes ("p" material). When those material are united, the recombination between the holes and the electrons cause a voltage field to appear, in the called "transition region". The resultant device is known as diode.

When a photon impacts against an electron, the energy transferred to this electron allows it to pass to the conduction band, so an inverse current is generated, and that current is a net energy generation that can be profited. Anyway, the objective of this thesis is not focusing on the photovoltaic effect, so for more information, reference [5] can be consulted. The circuital model of a solar cell is presented in figure 1.1.



(a) Response of a solar cell under darkness and light excitation



(b) Circuital model of a solar cell

Figure 1.1: The solar cell model

Where:

- i_{gc} is the current generated by the light irradiance, so it depends on this irradiance and the temperature.
- i_D is the current through the intrinsic diode of the solar cell.
- R_p represents the leakage current of the cell, and has its origin in the imperfections of the P-N union.
- R_s represents the losses resistances due to the resistance of the metal contacts, the metal mesh and the resistance of the semiconductor.

The mathematical model is represented by the equation 1.1

$$i_{PV} = i_{gc} - i_{sat}(e^{\frac{v_{PV}+i_{PV}R_s}{\eta V_T}} - 1) - \frac{v_{PV} + i_{PV}R_s}{R_p} \tag{1.1}$$

Which can be simplified, considering $R_s = 0$ and $R_p = \infty$, to:

$$i_{PV} = i_{gc} - i_{sat}(e^{\frac{v_{PV}}{\eta V_T}} - 1) \tag{1.2}$$

Where:

- i_{sat} is the current saturation of the diode.
- η is a constant which represents the emission coefficient, that can vary between 1 and 2 depending on the fabrication of the cell.

- V_T is the thermal voltage which is defined as $V_T = \frac{kT}{e}$ where k is the Boltzmann constant ($1.3810^{-23} J/K$), T is the temperature in Kelvin and e is the electron charge ($1.610^{-19} C$).

As can be seen in equation 1.2, the power that can be provided by the solar cell rises with the light irradiance and decreases when the temperature rises. As both variables are environmental dependant (so not controllable by human process), there must be a continuous calculus of the maximum power point where the panel can work depending on these variables.

1.2.2 The solar photovoltaic panel

A solar panel is formed by multi-string arrays of solar cells, connected in series or parallel in order to achieve the desired values of current and voltage. A solar panel is characterized by its current-voltage curve, that is, in essence, the same curve presented in figure 1.1, but considering the positive sense of the current when it goes out and scaling the values of voltage and current having into account the number of cells present in the panel. In this thesis, the basic panel used will be characterized in section 1.4. The key parameters of solar panel curve are the maximum power point, the short-circuit current and the open-circuit voltage. Another important panel parameter is the efficiency. More efficient does not mean better quality of the power provided, but it means that less area will be necessary to produce the same amount of energy. The efficiency depends on the material used and the manufacturing process. The commercial solar panels are mainly three types; the mono-crystalline silicon (efficiency close to 20%, the most expensive), the poly-crystalline silicon (cheaper, but less efficient, close to 15%) and the amorphous silicon (the cheapest, efficiency is close to 8%, and only used in little chargers applications).

But the world of the solar panels is much more extensive and there are lots of different materials. In the future very interesting investigations are leading to the development of new "portable" chargers based on organic cells, and the efficiencies of the multiple junction solar panels are today close to 50%. These new technologies have been developed in the laboratory by now, but when they will enter into the market, the possibilities in different applications will be significantly numerous. A table with all the technologies and materials used by the moment and their efficiency is presented in figure 1.3.

The basic symbol that will be used in this thesis to represent a panel or a panel array is presented in figure 1.2.

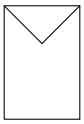


Figure 1.2: Basic Solar Panel Symbol

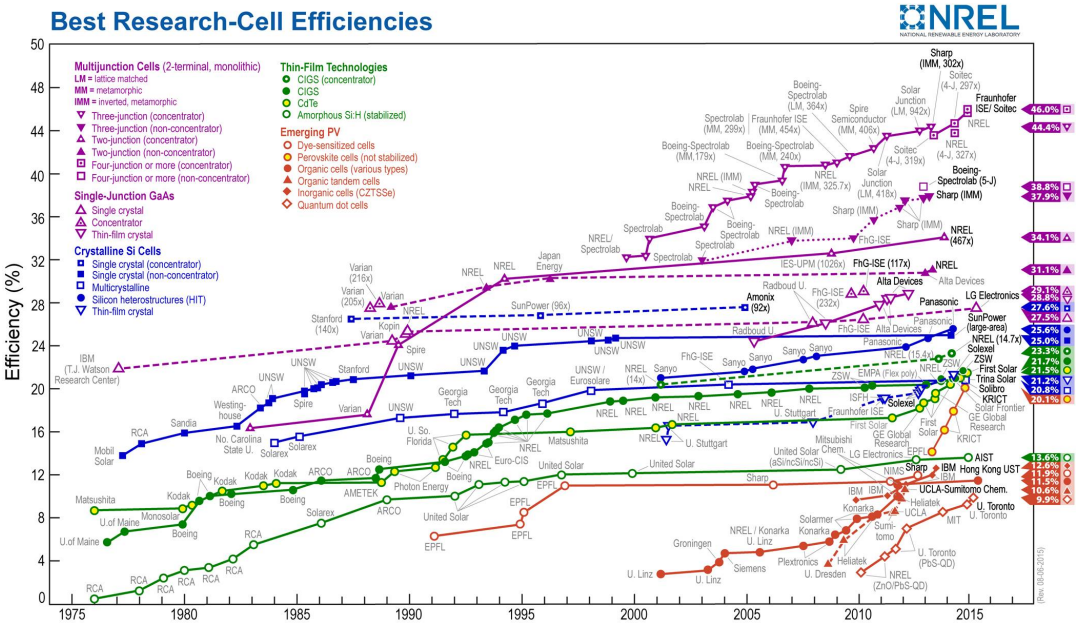


Figure 1.3: Materials and technologies for Photovoltaic Panels and their effiency

1.2.3 Interconnection of solar panels

Like the solar cells, solar panels can be interconnected between them to achieve different values of current and voltage. The panels can be connected in series or in parallel, but, in connections between solar panels or solar cells, problems of shadows and damaged components can appear. These problems consist on having some cell or panel which is under a partial shadow or partially damaged, committing the efficiency of the whole structure.

1.2.3.1 Parallel Panel Interconnection

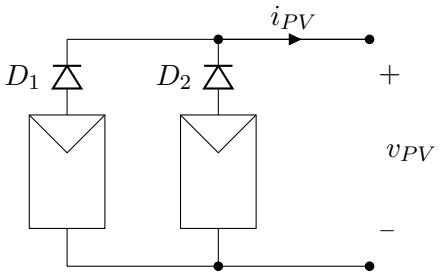


Figure 1.4: Parallel connection of two solar panels

The parallel connection of the panels allow getting higher currents. The problems of the shadowed or damaged panels, in this case, can be solved by placing blocking diodes in series with all the branches of panels. The main problem of this connection are the high output currents, and the low voltage; this will require an elevator power stage to connect them to the grid, with the correspondent efficiency loss, but can be acceptable for direct connections to a battery. As shown in figure 1.4, series connected diodes will be required to avoid that a panel working on a lower voltage point can perform as a charge. It must be remarked that with this connection, the

solar panel working at lower voltage point of its curve (due to, for example, a lower irradiance on it) will not provide any energy, so the whole array efficiency will be reduced.

1.2.3.2 Series Panel Interconnection

The series connection of panels allow getting higher voltages. The problems with damaged panels and shadows with this topology, cannot be avoided. Bypass diodes can be used when a panels limits its series current due to a shadow, but these diodes also reduce the total voltage, so the power loss is not avoidable. Moreover, the power curve can present local maximums due to the use of these bypass diodes, as presented in [6] [7].

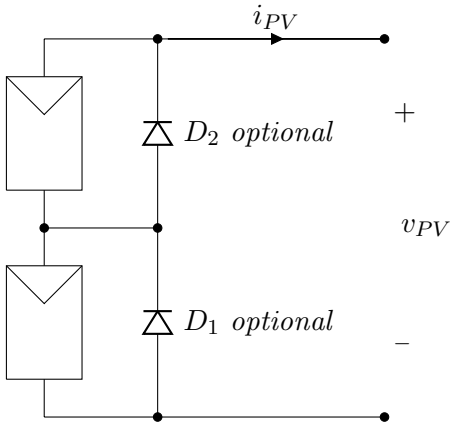


Figure 1.5: Series connection of two solar panels

1.2.3.3 Mixed Panel Interconnection

The desired power curves of solar panels can be achieved by interconnecting them combining both connection types. As seen, when panels are connected in any type, problems related to efficiency loss, can appear. Hence, panel arrays must be placed ensuring that all the panels are working at the same point. Of course, these panel arrays can be divided into different stages, and that is the most important point of this thesis, to study and analyse different kinds stages divisions. A mixed connection for four panels is shown in figure 1.6, and it can be reproduced for as much panels as wanted. In further sections, panels combination will be represented in a simplified way to, as shown in figure 1.7.

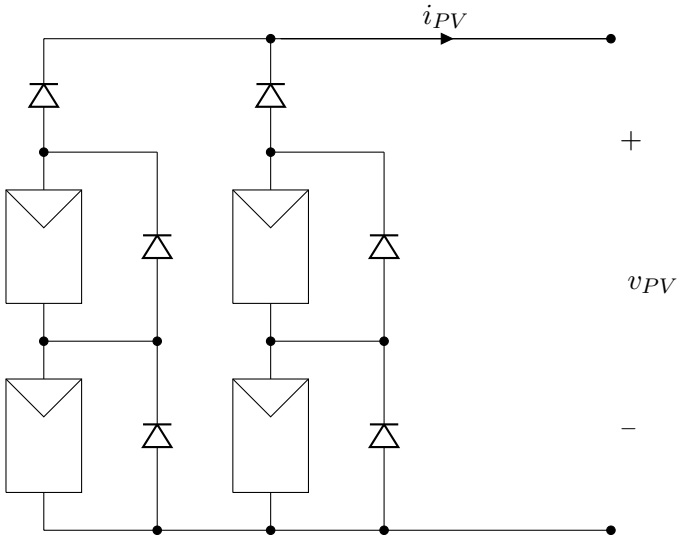


Figure 1.6: Mixed connection of four solar panels

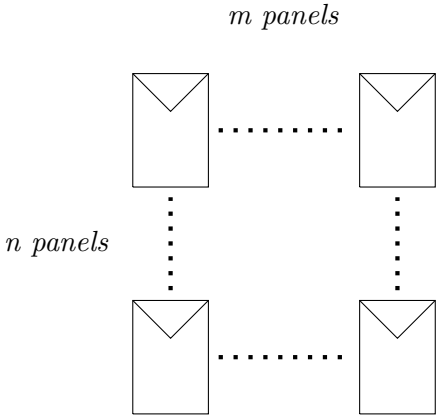


Figure 1.7: General block diagram for panel multi-string array

1.3 The Power Conversion stage

The power conversion stage is the module in charge to transform the output energy from the panels to an energy that can be stored in some type of accumulator (typically batteries, but there are other types) or injected directly into the grid, so it has the function of giving to this energy the proper characteristics in voltage and current to make it possible.

This thesis will focus on the power modules which directly inject the power to the grid, without any accumulator.

In general, a photovoltaic inverter connected directly to the grid, must assure the next conditions:

- Extract the maximum power available in the power generators. In this case, the solar panels must be brought to the maximum power point of each panel curve.
- The efficiency of the conversion stage is a parameter that must be maximized.
- The price of the module is normally a priority for any company, so the number of stages

and variables sensed, must be reduced to the minimum.

- The output current injected to the grid must accomplish a unit power factor, and its harmonic content must accomplish the European regulations (EN-61000-3-2, EN-61000-3-4, EN-50081-1, EN-50081-1) [8].

Different power conversion stages are designed to extract the power from different PV arrays distributions presented in 1.4.

1.4 Solar Panel Characterization

The solar panel that is going to be used and its interconnection for each topology are described in this section. The two premises had into account have been, in one hand, choosing a realistic panel, and in the other hand, choosing a panel that, when associated with other panels of the same type, could produce the desired voltage and power levels.

The panel chosen has a size of $425mm$ x $273mm$ x $50mm$ and its curve at $1000W/m^2$ irradiance point is specified in figure 1.8. It is considered enough realistic because there are some commercial panels with similar dimensions and characteristics, but it is important to remark that it does not coincide exactly with any commercial characteristic.

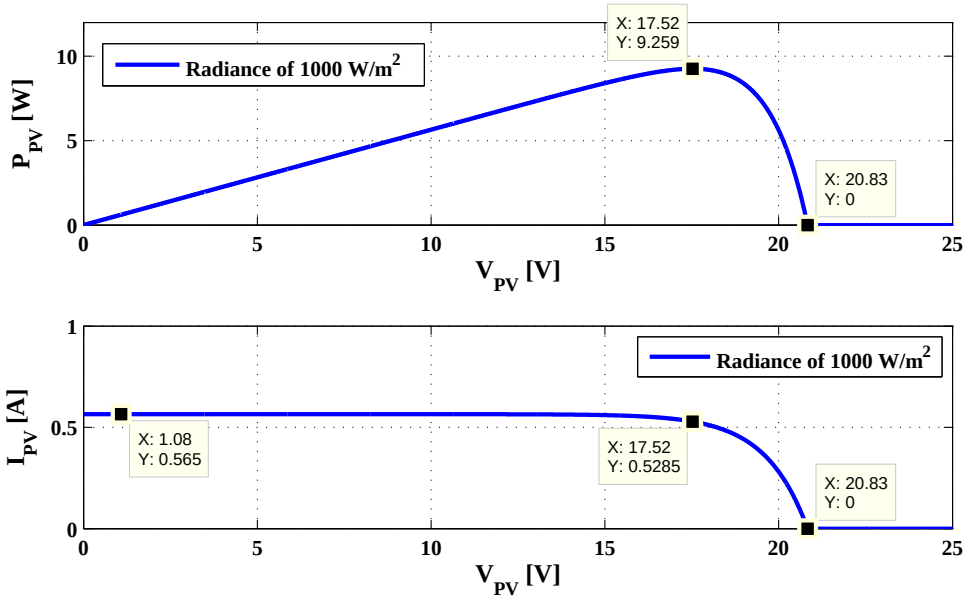


Figure 1.8: Basic panel curves for an irradiance of $1000W/m^2$

With more than one of the characterized PV panels, different arrays of them can be created. Therefore, different values of voltage and current can be achieved to extract the same amount of power from PV panels. In this thesis three possibilities of interconnection of the PV panels are proposed. Each one of these options leads to different power conversion stage to extract the power the panels.

1.4.1 Multi-string PV panel Array for Central Inverter Topology

If all the panels are connected forming one single array, a central inverter will be necessary to extract the energy.

The central inverter topology, presented in chapter 2, requires a single PV panel array in charge to provide the $3000W$, and a voltage higher than the grid voltage. The number of panels connected in series and parallel are shown in figure 1.9. The power curves generated by

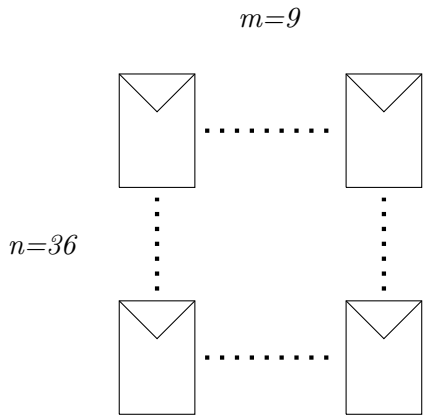


Figure 1.9: Panel Array for Central inverter topology

this panel array at different irradiances values are exposed at figure 1.10 As can be seen, at

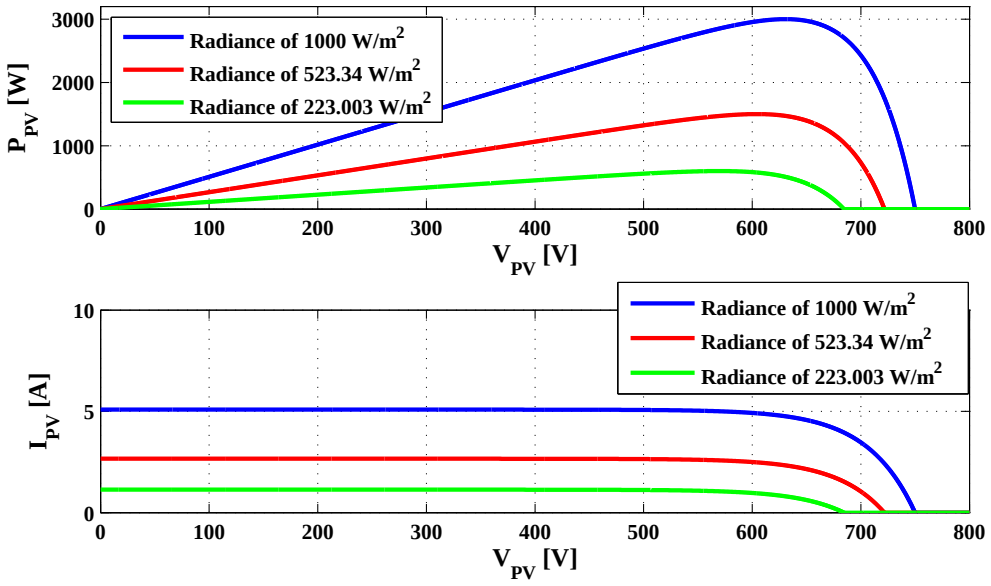


Figure 1.10: Curves for central inverter panel array

the maximum irradiance, $3000W$ are generated if the panel works at maximum power point, which is situated near $630V$. The characteristic points for different output power percentages are exposed in table 1.1. These percentages of output power coincide with the percentages necessary to perform a calculus called euro-efficiency, which is presented in chapter 5. The parameters shown are:

- **Percentage (%).** This is the percentage from the maximum output power ($3000W$).
- **Irradiance**. Is the absolute irradiance over the panel array to generate the desired output power.
- **Voc.** Is the open circuit voltage, which is the output voltage of the panel when there is no load. This value is the one from where the output voltage will start in all the simulations onwards.
- **Isc.** Is the short-circuit current. This is the output current of the panels when there is an overload.
- **Vmp.** Is the voltage where the PV panel array works at the maximum output power point. The output voltage will have to tend to this voltage value in all the simulations excepting these where it will be explicitly changed.
- **Imp.** Is the output current of the PV panel array at the maximum power point.
- **Pmp.** Is the output power of the PV panel array at the maximum power point.

This table will be provided for the PV panel arrays of series and parallel inverters connection.

% From $3000W$	Irradiance (W/m^2)	Voc [V]	Isc [A]	Vmp [V]	Imp [A]	Pmp [W]
5%	61.786	628.824	0.314	517.584	0.289	150
10%	117.248	656.688	0.596	543.488	0.552	300
20%	223.003	684.648	1.133	569.560	1.053	600
30%	325.132	701.056	1.653	584.888	1.538	900
50%	523.340	721.760	2.661	604.272	2.482	1500
75%	764.167	738.224	3.886	619.712	3.630	2250
100%	1000	749.920	5.084	630.696	4.756	3000

Table 1.1: Curve characteristic values for Euro-Efficiency of Central Topology Solar Panel Arrays

Central inverter topology will be examined in depth in chapter 2.

1.4.2 Multi-string PV panel Array for Series Connected Inverters Topology

The panels can be connected forming multiple arrays. When diving the single array into n arrays, the power of these arrays is also divided by n. If the power is divided by dividing the voltage of each PV panel array, then it will be necessary to connect n power stages in series to generate the necessary voltage to extract the maximum power from these panel arrays. It leads to the series connected inverters topology. In this case, the series connected panel arrays must be divided by 3. The number of panels connected in series or parallel for each stage are presented in figure 1.11 The power curves generated by each stage of this interconnection topology are shown in figure 1.12

The characteristic points for each panel array for this topology are shown in table 1.2

Series connected inverters topology will be examined in depth in chapter 3.

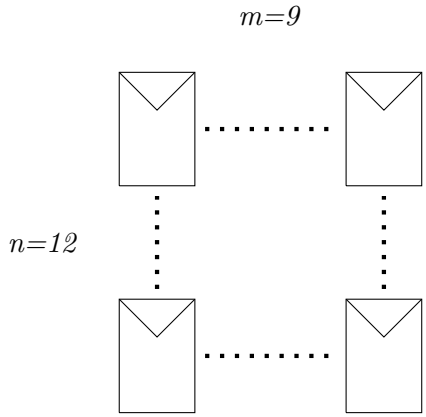


Figure 1.11: Panel Array for each stage of Series Connected inverter topology

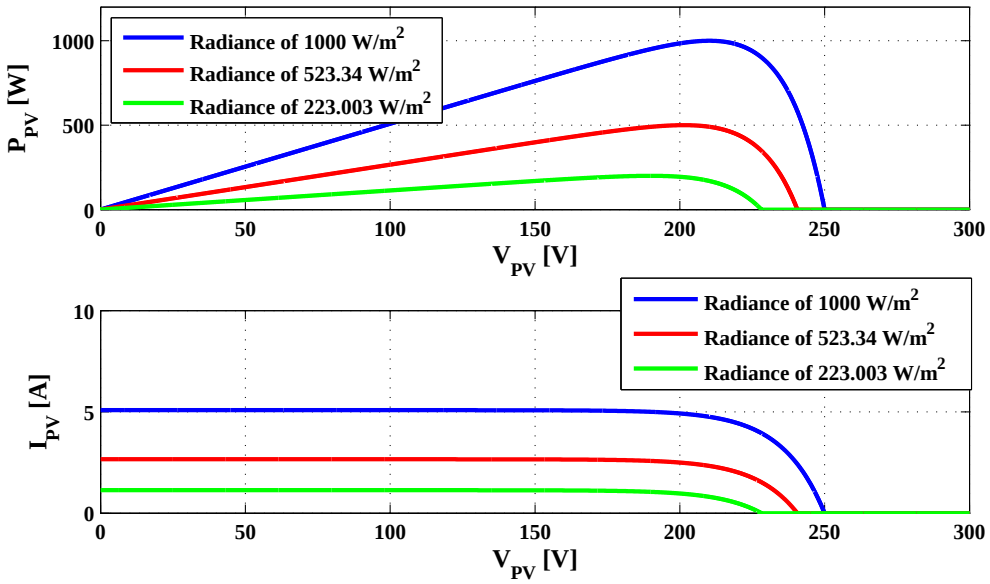


Figure 1.12: Curves for series connected inverters panel arrays

% From $3000W$	Irradiance (W/m^2)	Voc [V]	Isc [A]	Vmp [V]	Imp [A]	Pmp [W]
5%	61.786	209.608	0.314	172.528	0.289	50
10%	117.248	218.896	0.596	181.16	0.552	100
20%	223.003	228.216	1.133	189.856	1.053	200
30%	325.132	233.688	1.653	194.960	1.538	300
50%	523.340	240.592	2.661	201.424	2.482	500
70%	764.167	246.08	3.885	206.568	3.630	750
100%	1000	249.976	5.084	210.232	4.756	1000

Table 1.2: Curve characteristic values for Euro-Efficiency of Series Topology Solar Panel Arrays

1.4.3 Multi-string PV panel Array for Parallel Connected Inverters Topology

If the power is divided by dividing the current of each PV panel array, then it will be necessary to connect n power stages in parallel to extract the maximum power from these panel arrays. It leads to the parallel connected inverters topology. In this case, the series connected panel arrays must be divided by 3. The number of panels connected in series or parallel for each stage are presented in figure 1.13.

The power curves generated by each stage of this interconnection topology are shown in figure 1.14.

Table 1.3 provides the characteristic points for the panel array for this topology.

Parallel connected inverters topology will be examined in depth in chapter 4.

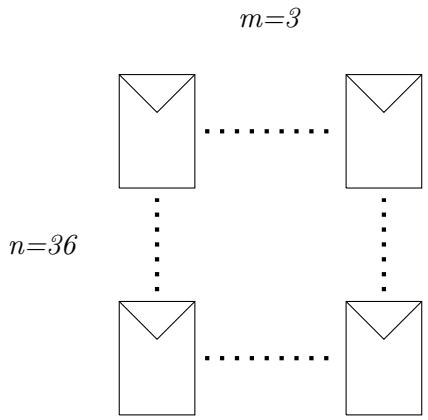


Figure 1.13: Panel Array for Parallel Connected inverter topology

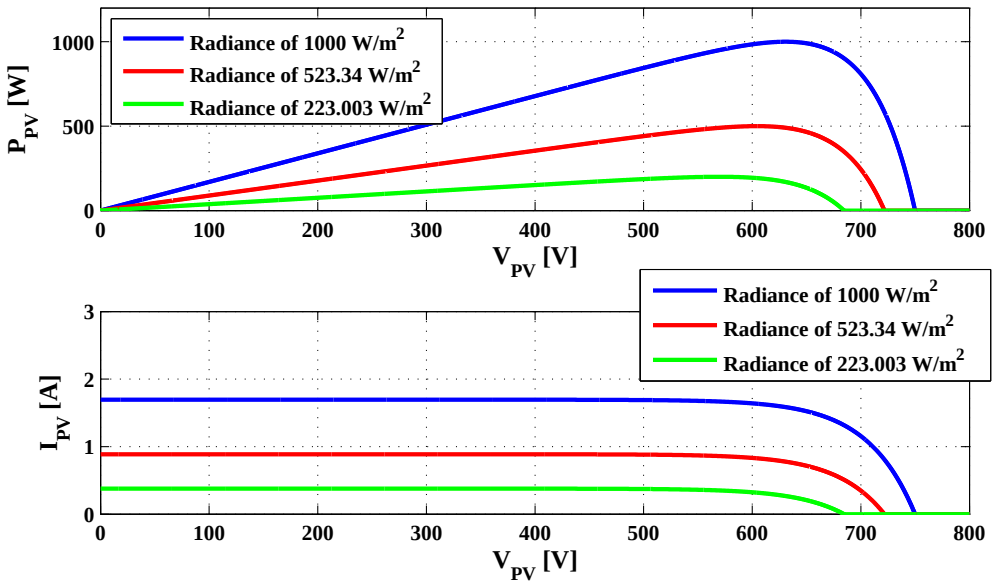


Figure 1.14: Curves for parallel connected inverters panel arrays

% From $3000W$	Irradiance (W/m^2)	Voc [V]	Isc [A]	Vmp [V]	Imp [A]	Pmp [W]
5%	61.786	628.824	0.104	517.584	0.096	50
10%	117.248	656.688	0.198	543.488	0.184	100
20%	223.003	684.648	0.378	569.56	0.351	200
30%	325.132	701.056	0.551	584.888	0.512	300
50%	523.340	721.760	0.887	604.272	0.827	500
75%	764.167	738.224	1.295	619.712	1.210	750
100%	1000	749.920	1.694	630.696	1.585	1000

Table 1.3: Curve characteristic values for Euro-Efficiency of Parallel Topology Solar Panel Arrays

1.5 The Plant Component Tolerances

In this thesis several simulations are going to be performed. These will be based on different plant types.

- **Ideal plant** is formed by balanced components and no losses. Balanced components are described as components with the value that they are supposed to have, and the same value for all the phases.
- **Real plant** is formed by balanced components but with losses. However, as in the ideal plant, all losses and components are balanced.
- **Real plant with tolerances** is formed by unbalanced components and losses. Unbalanced components are defined as components with an aleatory value between realistic margins. In this thesis, these realistic margins are described as:
  - 10% for resistances (losses)
  - 20% for inductances and capacitors.

As the values of the components will depend on the simulation. In each simulation, values will be provided in the corresponding table.

1.6 Previous Studies and Objectives

1.6.1 Previous Studies

This thesis is an extension of previous studies presented in [6], [8], [9]. In these thesis important studies are exposed about the central and multilevel inverters connected topologies. The main points of these studies that have been used in this thesis are:

- The MPPT. Maximum Power Tracking algorithm in charge to deliver the maximum power point voltage reference to the external control. In this thesis, a classical Perturb and observe MPPT algorithm is assumed [10].
- The external control. It is in charge of driving the panel array output voltage to its reference. This control is also in charge to deliver the current amplitude reference to the

internal control. The design of external control is based on the energy balance control described in [11], [12].

- The internal control. It is in charge to drive the current injected to the grid. The design of this block is based on a Proportional Resonant (P+R) controller according to the design steps suggested in [13] and [14]. The proper operation of this loop leads to a current in phase with the grid voltage.
- Modulation Block. It is in charge of generating the PWM signal to drive the MOSFET transistors of the full-bridge inverter. The modulating signal is the output of the internal control and the carrier one is assumed to be triangular to shift the current spectrum to higher frequencies.

All these points and their utility to the present thesis will be deeper presented and explained in the chapters 2 and 3.

1.6.2 Objectives

Having into account the previous studies developed, this thesis is going to be focused on three main objectives.

- The study of the use of LCL filters in the topologies described in section 1.6.1. This will include the validation of the theory of the energy balance when adding the LCL filter, and the implications that it will have in the stability of the whole system.
- The study of a parallel connected inverters topology. This will include the design of the control and the study of modulation strategies to improve the harmonic content of the current injection.
- A comparative between central, series and parallel topologies, evaluating the efficiency, control complexity and volume of each topology.

The different points that will be studied in this thesis will be presented in different chapters.

- Chapter 2 will present the previous studies about the central inverter topology, connected to the grid through a single inductor. And also will present the behaviour of this topology working with an LCL filter. Stability margins are studied and gains of the control will be recalculated to work under the LCL filter. Simulations will be also presented to prove that the calculus done are valid.
- Chapter 3 will follow the same structure of the chapter 2 for the multilevel series connected inverters topology. The previous studies will be presented and also the behaviour of the topology working with LCL filter at the output. The modulation strategy used will be also presented.
- Chapter 4 will present the parallel inverter connected topology. As this topology does not have any sense without the LCL filter, it will be directly presented with it. The main problems with the proportional-resonant control will be presented. A new control strategy for the parallel inverter topology will be proposed in this chapter. The main strengths and weaknesses points of this control will be exposed, as will be evaluated its performance under different conditions.

- Chapter 5 will present comparative simulations that have been performed to test the different topologies under different conditions of irradiance and switching frequency. The MOSFET used to perform the comparative is based on silicon carbide (SiC) technology. A PSIM based model of this transistor has been used in order to evaluate its performance under the specified conditions.

Chapter 2

Central Inverter Topology

In this chapter, following subjects are presented.

- Central inverter topology and its stability analysis, connected to the grid by one inductor.
- Central inverter topology and its stability analysis, connected to the grid by an LCL filter.

Both points presented above have been studied by other authors ([11]). However, it is necessary to explain and recalculate the values of the elements and the control parameters, in order to expose the conditions considered to perform the comparative. The schematic circuit of the central inverter topology is depicted in figure 2.1. It can be seen that, as mentioned in chapter 1, one single array of panels provide the whole energy that will be injected to the grid.

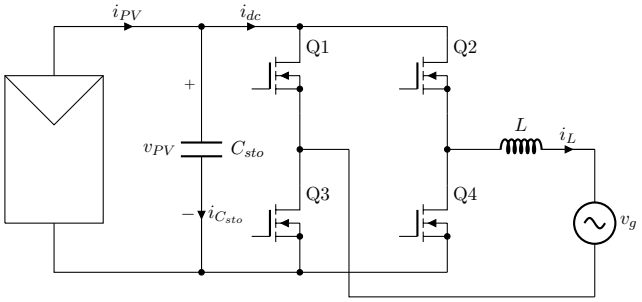


Figure 2.1: Central inverter topology circuit

The only storage element used as input capacitor for the H bridge is the capacitor at the output of the solar panels. Therefore, unifying all the commutation sequences, it is possible to condensate all the expressions into two general equations that define the system and relation the state variables.

$$\begin{aligned} v_L &= L\frac{di_L}{dt} = u \cdot v_{PV} - v_g \\ i_C &= C\frac{dv_{PV}}{dt} = i_{PV} - u \cdot i_L \end{aligned} \tag{2.1}$$

Where u is the control variable which can take the values $\{-1,0,1\}$. The commutation sequence of the half bridge is shown in table 2.1. Despite these equations define the system, the mathematical analysis becomes very complex due to the non-linearity of i_{PV} (see equation 1.1). For that reason, an alternative method based on energetic balance is proposed.

u	$Q1$	$Q2$	$Q3$	$Q4$	v_h
1	OFF	ON	ON	OFF	$+v_{PV}$
0	ON	OFF	ON	OFF	0
0	OFF	ON	OFF	ON	0
-1	ON	OFF	OFF	ON	$-v_{PV}$

Table 2.1: Unipolar Conmutation Sequence

2.1 Modelling the System from Energetic Balance

In this section, model of the whole system is derived from the concept of energy balance. The main hypothesis necessary to start with this concept is to assume that:

$$P_{PV} = P_{inv} + P_{out} \tag{2.2}$$

Where P_{PV} is the output power of the solar panels, P_{inv} is the power stored in the reactive elements of the inverter and P_{out} is the power injected to the grid. Losses are not included in this power balance, so in the real application the output power will be less than what is going to be calculated.

Developing the expression:

$$i_{PV} v_{PV} = v_{PV} C \frac{dv_{PV}}{dt} + i_L L \frac{di_L}{dt} + v_g i_L \tag{2.3}$$

The second hypothesis that must be taken into account is that the grid voltage and the current injected are sinusoids and are in phase between them. So the voltage responds to an expression like $v_g = A_g \sin(w_g t)$. The current injected can be expressed as $i_L = v_g K$, where K is a scalar variable provided by the control to maintain the energy balance for each input energy from the panel.

The equation obtained when both hypothesis are applied to equation 2.3 is:

$$\begin{aligned} i_{PV}\ v_{PV} &= v_{PV} C_{sto} \frac{dv_{PV}}{dt} + K v_g L \frac{di_L}{dt} + v_g v_g K \\ i_{PV}\ v_{PV} &= v_{PV} C_{sto} \frac{dv_{PV}}{dt} + \frac{L K^2 A_g^2 w_g}{2} \sin(2 w_g t) + \frac{K A_g^2}{2} - \frac{K A_g^2 \cos(2 w_g t)}{2} \end{aligned} \tag{2.4}$$

Using the energy balance, an equation which does not depend on the control variable u has been obtained. However, the equation is still no lineal because the dynamic information of the panel is still present. To advance in that field, three more hypothesis must be raised.

First, a discrete model of the system equation is necessary to eliminate the double grid frequency components.

Second, it is necessary to linearize the equation of the panel in order to be able to include it in the linear discrete model of the system.

Third, the energy supplied by the photovoltaic panels is invariable during one grid period. It means that the scalar factor K will be able to vary every one cycle grid period. This hypothesis is acceptable because the energy provided depends on the environmental variables (irradiance and temperature) which are supposed to have a slow dynamics, at least much slower than the grid period.

2.1.1 Grid Period Average Model of the Central Inverter

The averaged model of the central inverter system can be achieved considering the equation 2.4, which describes the system dynamics, and integrating it in one grid period, having into account the three last hypothesis described.

$K(\epsilon) = K(n-1)$ during a whole grid period $(n-1)T_g \leq t \leq nT_g$

Integrating the equation for a grid period and remaking the K expression.

$$\begin{aligned} \int_{(n-1)T_g}^{nT_g} i_{PV} v_{PV} dt = \int_{(n-1)T_g}^{nT_g} v_{PV} C_{sto} \frac{dv_{PV}}{dt} + \int_{(n-1)T_g}^{nT_g} \frac{L[K(n-1)]^2 A_g^2 w_g}{2} \sin(2w_g t) dt \\ + \int_{(n-1)T_g}^{nT_g} \frac{K(n-1)A_g^2}{2} dt + \int_{(n-1)T_g}^{nT_g} \frac{K(n-1)A_g^2}{2} \cos(2w_g t) dt \end{aligned} \tag{2.5}$$

If the integral is evaluated, the components of double grid frequency disappear. Defining E_{PV} as the energy supplied in one grid period by the panels, the final equation of the system is:

$$E_{PV} = \frac{C_{sto}}{2}[v_{PV}^2(n) - v_{PV}^2(n-1)] + \frac{K(n-1)A_g^2}{2} T_g \tag{2.6}$$

- E_{PV}: Energy supplied by the panels
- $\frac{C_{sto}}{2}[v_{PV}^2(n) - v_{PV}^2(n-1)]$: Energy stored in the capacitor
- $\frac{K(n-1)A_g^2}{2} T_g$: Energy injected to the grid

If the energy stored in the capacitor is described as E_{sto}, the equation that defines it is:

$$E_{sto}(n) - E_{sto}(n-1) = E_{PV} - \frac{K(n-1)A_g^2 T_g}{2} \tag{2.7}$$

2.1.2 Discrete and Averaged Model of the Photovoltaic Panel

In the equation 2.6, E_{PV} is the only term that is not linear. In this section the averaged, discrete and linearized model of E_{PV} is developed. Following the methodology of section 2.1.1 applied to equation 1.2, leads to:

$$E_{PV} = \int_{(n-1)T_g}^{nT_g} i_{PV} v_{PV} dt = \int_{(n-1)T_g}^{nT_g} [I_{gc} - I_{sat}(e^{\frac{v_{PV}}{\eta V_T}} - 1)] v_{PV} dt \tag{2.8}$$

In this equation, all the variable parameters are environmental depending parameters (so non-controllable variables) except one, the v_{PV}, that can be controlled because depends on the point where the panel is forced to work, through the control variable. For that reason, the linearization will be made with respect to this variable, evaluated at the point where it is going to work. In order to engage the resultant equation to the complete equation of the system, it has to be expressed in energy terms, that means, expressing the output voltage of the solar

panels as the result of the energy stored in the capacitor:

$$\begin{aligned} v_{PV} &= \sqrt{\frac{2}{C_{sto}} E_{sto}} \\ E_{PV} &= \sqrt{\frac{2}{C_{sto}} E_{sto}} (I_{gc} + I_{satc}) T_g - \sqrt{\frac{2}{C_{sto}} E_{sto}} I_{satc} [e^{\frac{\sqrt{\frac{2}{C} E_{sto}}}{V_T \eta}}] T_g \end{aligned} \tag{2.9}$$

This equation can be linearized using Taylor series and taking only the first order of this. To be coherent with the notation of the previous studies, the voltage point where the panel is working will be called v^*_{PV}, so the notation for the energy stored by the capacitor evaluated at this point will be E^*_{sto} and the total energy provided by the panel evaluated at this point from equation 2.9 will be E^*_{PV}. The development of the equation can be found in [6] or [8], and the final result is:

$$E_{PV} \simeq E^*_{PV} + m(E_{sto} - E^*_{sto})$$

Where:

$$m = \left.\frac{dE_{PV}}{dE_{sto}}\right|_{E_{sto}=E^*_{sto}} \rightarrow m = \frac{T_g}{2\sqrt{E^*_{sto}}} (\alpha_a - \alpha_b e^{\alpha_c \sqrt{E^*_{sto}}} (1 + \alpha_c \sqrt{E^*_{sto}})) \tag{2.10}$$

$$\alpha_a = \sqrt{\frac{2}{C_{sto}}} (I_{gc} + I_{satc}) \ , \ \alpha_b = \sqrt{\frac{2}{C_{sto}}} I_{satc} \text{ and } \alpha_c = \sqrt{\frac{2}{C_{sto}}} \frac{1}{\eta V_T}$$

2.1.3 Discrete and Linearized Model of the Inverter System

From equation 2.7, the Z transform must be applied to get the discrete equation of the system. The notation for the transformed variables will be $X(z) = \hat{X}$.

$$\begin{aligned} E_{sto}(n) - E_{sto}(n-1) &= E_{PV} - \frac{K(n-1) A_g^2 T_g}{2} \\ \hat{E}_{sto} - \hat{E}_{sto} z^{-1} &= \hat{E}_{PV} - \frac{\hat{K} z^{-1} A_g^2 T_g}{2} \\ \hat{E}_{sto} (\frac{z-1}{z}) &= \hat{E}_{PV} - \frac{\hat{K} A_g^2 T_g}{2z} \\ \hat{E}_{sto} &= \hat{E}_{PV} (\frac{z-1}{z}) - \frac{\hat{K} A_g^2 T_g}{2(z-1)} \\ \hat{E}_{sto} &= (\hat{E}^*_{PV} + m[\hat{E}_{sto} - \hat{E}^*_{sto}]) (\frac{z}{z-1}) - \frac{\hat{K} A_g^2 T_g}{2(z-1)} \end{aligned} \tag{2.11}$$

So, finally, a linearized and discrete model for the whole system of the central inverter is obtained. Its block diagram is presented in figure 2.2.

Due to linearization, this model does not contemplate the whole system dynamics and is only valid when the system is working near the defined working point. The control that must be designed to fix the working point will be defined in a discrete interval equal to a grid period, but not for the dynamics inside this interval.

The two main considerations on which the model is based are that the i_L is sinusoidal and in phase with the grid voltage, and the invariability of the scalar term K for a whole grid period. This means that the control of the output current will have to be faster than the control to fix the working point of the panels. The output current will determinate the voltage of the central capacitor, and therefore, the point where the panel will work.

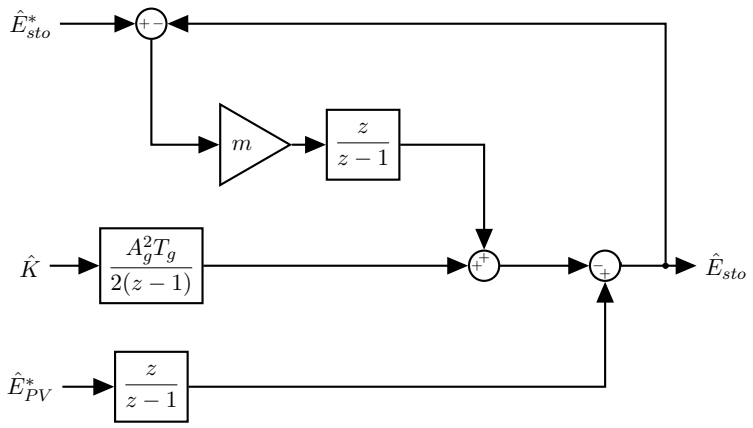


Figure 2.2: Block diagram of the discrete linear model of the inverter system

2.2 The Energy Balance under LCL Filtering

The use of an LCL filter is proposed in order to reduce the ripple of the current injected to the grid and improve its quality. In this section, the effects that the use of this filter can have over the energy balance and, therefore, over the external control, are discussed. Figure 2.3 shows the schematic of the topology. The analysis of energy balance can be done beginning from the

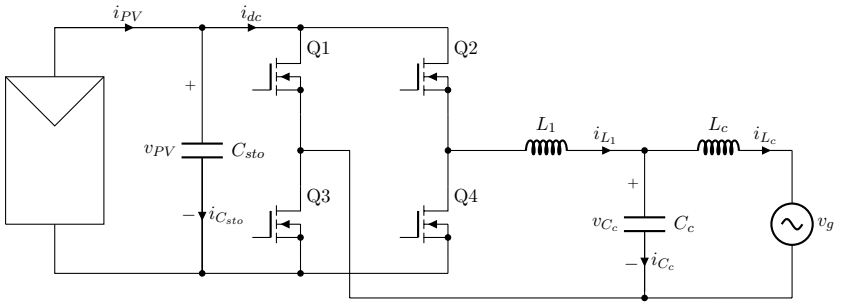


Figure 2.3: Schematic of central inverter topology with LCL filter

same assumptions of section 2.1.

$$v_g = A_g \sin(w_g t) \qquad i_{L_c} = K A_g \sin(w_g t)$$
$$E_{PV} = E_{C_{sto}} + E_{L_1} + E_{C_c} + E_{L_c} + E_{out} \tag{2.12}$$

All the terms of the equation of the energy balance will be analysed one by one, in order not to create excessive long equations.

Before starting to analyse all these terms, it is important to show some trigonometric identities that are going to be used in the analysis.

$$\cos^2\theta = \frac{1+\cos(2\theta)}{2} \qquad \sin^2\theta = \frac{1-\cos(2\theta)}{2} \qquad \sin(2\theta) = 2\sin(\theta)\cos(\theta) \tag{2.13}$$

All the terms of the equation will be analysed separately, in order not to create excessive long equation.

The term E_{out} is defined as:

$$\int_{(n-1)T_g}^{nT_g} P_{out}\ dt = \int_{(n-1)T_g}^{nT_g} v_g i_{L_c} = \int_{(n-1)T_g}^{nT_g} K(n-1)A_g^2 \sin^2(w_g t)\ dt$$

Applying the corresponding trigonometric identity:

$$\begin{aligned}
&\int_{(n-1)T_g}^{nT_g} P_{out}\ dt = \frac{K(n-1)A_g^2 nT_g}{2} - \frac{K(n-1)A_g^2}{4w_g}\sin(2w_g nT_g) \\
&- \frac{K(n-1)A_g^2(n-1)T_g}{2} + \frac{K(n-1)A_g^2}{4w_g}\sin(2w_g(n-1)T_g) \\
&E_{out} = \int_{(n-1)T_g}^{nT_g} P_{out}\ dt = \frac{K(n-1)A_g^2 T_g}{2}
\end{aligned} \tag{2.14}$$

As can be seen, it coincides with the part of output energy of the equation 2.6. It is normal, as the output current and grid voltage are the same.

The next term is the E_{L_c}.

$$\begin{aligned}
P_{L_c} &= i_{L_c} v_{L_c} = i_{L_c} L_c \frac{di_{L_c}}{dt} \\
P_{L_c} &= KA_g \sin(w_g t) L_c K A_g w_g \cos(w_g t)
\end{aligned}$$

Applying the corresponding trigonometric identity:

$$\begin{aligned}
&P_{L_c} = K^2 A_g^2 L_c w_g \frac{\sin(2w_g t)}{2} \\
&\int_{(n-1)T_g}^{nT_g} P_{L_c} dt = \int_{(n-1)T_g}^{nT_g} K^2 A_g^2 L_c w_g \frac{\sin(2w_g t)}{2}\ dt \\
&E_{L_c} = [-\frac{K^2 A_g^2 L_c w_g}{4w_g}\cos(2w_g t)]_{(n-1)T_g}^{nT_g} \rightarrow \\
&E_{L_c} = -\frac{K^2 A_g^2 L_c w_g}{4w_g}\cos(2w_g nT_g) + \frac{K^2 A_g^2 L_c w_g}{4w_g}\cos(2w_g(n-1)T_g)
\end{aligned} \tag{2.15}$$

Taking into account that $w_g = \frac{2\pi}{T_g}$:

$$\begin{aligned}
&\cos(4w_g nT_g) = \cos(8\pi n) = 1 \\
&\cos(4w_g(n-1)T_g) = \cos(8\pi(n-1)) = 1
\end{aligned}$$

As the values of n can be only integers, the angle of the cosine will be always a multiple of 2π. Therefore, the value of cosine will be always 1 and, therefore:

$$E_{L_c} = \frac{K^2 A_g^2 L_c w_g}{4w_g} - \frac{K^2 A_g^2 L_c w_g}{4w_g} = 0 \tag{2.16}$$

The energy stored by the inductor, if it is integrated by one grid period, has a net value of 0. Therefore, the dynamics during this period will not be contemplated, but this does not affect the energy balance.

The next term to analyse, is E_{C_c}:

$$P_{C_c} = v_{C_c} i_{C_c} = (v_g + v_{L_c}) C_c \frac{d(v_g + v_{L_c})}{dt}$$

$$\begin{aligned} P_{C_c} &= [A_g \sin(w_g t) + L_c K A_g w_g \cos(w_g t)][A_g w_g \cos(w_g t) \\ &- L_c K A_g w_g^2 \sin(w_g t)] C_c \end{aligned} \tag{2.17}$$

$$\begin{aligned} P_{C_c} &= A_g^2 C_c w_g \cos(w_g t) \sin(w_g t) - A_g^2 L_c C_c K w_g^2 \sin^2(w_g t) \\ &+ A_g^2 L_c C_c K w_g^2 \cos^2(w_g t) - L_c^2 A_g^2 w_g^3 K^2 C_c \cos(w_g t) \sin(w_g t) \end{aligned}$$

At this point, it can be seen that all the terms in the equation of the power have a product with a sine or a cosine, and the terms of these sines and cosines are multiples of π or 2π respectively. Therefore, the integral of this power over one grid period will be 0, for the same reason exposed in the previous term. So:

$$E_{C_c} = \int_{(n-1)T_g}^{nT_g} P_{C_c} dt = 0 \tag{2.18}$$

The next term is the E_{L_1}, same steps of previous terms must be applied:

$$P_{L_1} = i_{L_1} v_{L_1} = (i_{C_c} + i_{L_c}) L_1 \frac{d i_{L_1}}{dt}$$

$$\begin{aligned} P_{L_1} &= [K A_g \sin(w_g t) + C_c A_g w_g \cos(w_g t) - L_c C_c K A_g w_g^2 \sin(w_g t)] \cdot \\ &[K A_g w_g L_1 \cos(w_g t) - C_c A_g w_g^2 L_1 \sin(w_g t) - L_c L_1 C_c A_g K w_g^3 \cos(w_g t)] \end{aligned} \tag{2.19}$$

As can be seen in the last expression of the equation, the terms without any sine or cosine or a product of them are cancelled between them, other terms that depend on a sine or a cosine will be 0 when integrting into a grid period. Therefore, the result of total integration in one grid period will be, again, 0.

$$E_{L_1} = \int_{(n-1)T_g}^{nT_g} P_{L_1} dt = 0 \tag{2.20}$$

So, finally, the equation 2.12 becomes:

$$E_{PV} = E_{C_{sto}} + E_{out} \tag{2.21}$$

Which is the same than the equation 2.6.

Thus, it can be concluded that the LCL filter does not affect the energy balance and the derivation of the external control will be the same of the section 2.3.1.

2.3 Control design for the Central Inverter Connected to the Grid by a Single L

Once modelled using the energy balance concept, the inverter system can be analysed and controlled using three main blocks:

- MPPT: The Maximum Power Point Tracking, it is in charge of fixing the value of the voltage in order to achieve the maximum power point at the output of the panel. This block has been largely discussed in several papers and scientific publications, and will be not discussed in this thesis. In front of any temperature or irradiance change, this block will give different voltage points where the panel must be situated. Therefore, the output of this block will be the input of the next block, the external control.
- External control: It is the responsible for the generation of scalar value K. It's input is the voltage point where the output voltage of the panel must be fixed and that coincides with the voltage of the central capacitor that is the other input of this block. So, knowing the voltage point where the panel is situated (voltage in capacitor) and the voltage point where it should be situated (output of the MPPT), it must decide how many power must be extracted from the panel (factor K) and send it to the next block, the internal control. That will guarantee that the maximum power is extracted from the panel.
- Internal control: It is the responsible to guarantee that the injected current to the grid is in phase with the grid voltage and is the current ratio imposed by the external control, so the equation $i_L = v_g K$ is accomplished. This control will govern the transistors of the inverter and is where all the modulation improvements can be applied.

Let's explain that with a little scheme of the system that is going to be designed:

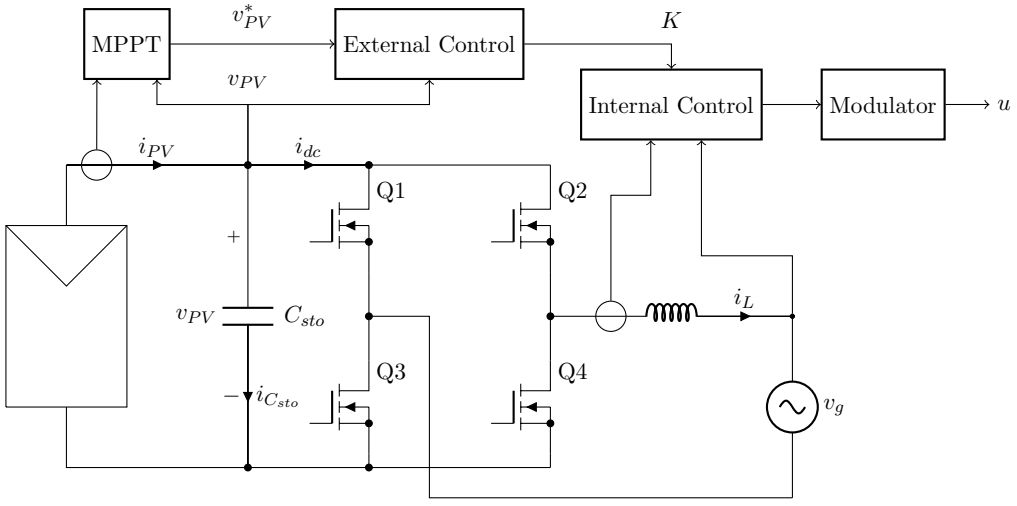


Figure 2.4: Central inverter topology circuit and controls block diagram

2.3.1 Design of the External Control for the Central Inverter Topology

As explained, the external control has to give to the internal control the value of parameter K that can assure that the power balance is accomplished and the maximum power is extracted

from the panels. The inputs of this block are the output voltage of the panel and the proper voltage where the panel should be to situate its working point in the maximum power point. Figure 2.5 shows how the control must be situated in the system diagram block to transform the input $\hat{K}$, into the output of this control. This block diagram shows the closed loop system.

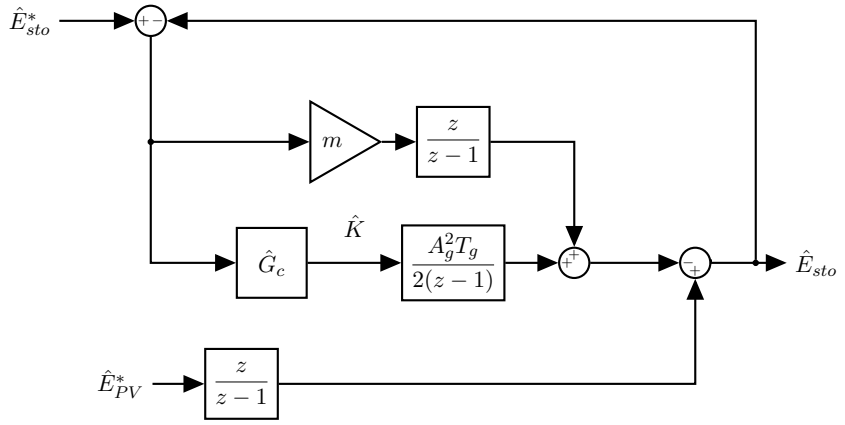


Figure 2.5: Block diagram of the discrete linear model of the inverter system with the controller $\hat{G}_c$ applied

Despite the output of the external block is the term $\hat{K}$, all the diagram is presented because the stability of the whole system must be analysed to validate the work margin over the panel curve. And that is the next step that should be done,the analysis of the stability of the system.

Expressing the bock diagram as a closed loop equation, the term $\hat{E}_{sto}$ must be isolated.

$$\hat{E}_{sto} = \frac{\hat{E}^*_{PV} z - \hat{E}^*_{sto}(mz + 0.5\hat{G}_c A_g^2 T_g)}{z - 1 - (mz + 0.5\hat{G}_c A_g^2 T_g)} \tag{2.22}$$

As can be seen, the output $\hat{E}_{sto}$ (the real voltage in the central capacitor) depends on $\hat{E}^*_{PV}$ and $\hat{E}^*_{sto}$. These two variables can vary at any moment due to the environmental conditions, but their dynamics are supposed to be slow. However, to study the most restrictive condition, it will be supposed that the changes can be abrupt (Heaviside function). So the abrupt change must be added to these variables.

$$E^*_{PV} = E^*_{PV} u(t) \rightarrow \hat{E}^*_{PV} = \hat{E}^*_{PV}(\frac{z}{z-1})$$
$$E^*_{sto} = E^*_{sto} u(t) \rightarrow \hat{E}^*_{sto} = \hat{E}^*_{sto}(\frac{z}{z-1})$$

Redoing the equation 2.22, it leads to:

$$\hat{E}_{sto} = (\frac{z}{z-1})\frac{\hat{E}^*_{PV} z - \hat{E}^*_{sto}(mz + 0.5\hat{G}_c A_g^2 T_g)}{z - 1 - (mz + 0.5\hat{G}_c A_g^2 T_g)} \tag{2.23}$$

The control proposed is a PI (Proportional-Integral), because it is the simplest control that guarantees two special conditions. The integral part guarantees that the error at the steady state is zero, and the proportional part can be adjusted to guarantee the stability of the system. Therefore, the expression for the control in the Laplace domain is $G_c = k_p + \frac{k_i}{s}$, but the system

is being analysed in the Z plane (the discrete domain), so the bilateral transform must be applied to the control expression.

The bilateral transform is a method to convert expressions from Laplace S plane to Z plane. A more detailed explanation can be found in several books and publications, like in [15].

$$\hat{G}_c = k_p + k_i \frac{T_g(z+1)}{2(z-1)} = (k_p + k_i \frac{T_g}{2}) \frac{z + \frac{k_i T_g - 2k_p}{k_i T_g + 2k_p}}{z-1} \tag{2.24}$$

That can be expressed, in a general way, as:

$$\hat{G}_c = \gamma \frac{z-\alpha}{z-1} \qquad \gamma = k_p + k_i \frac{T_g}{2} \qquad \alpha = -(\frac{k_i T_g - 2k_p}{k_i T_g + 2k_p}) \tag{2.25}$$

To design the control the values of γ and α must be specified. Following the the typical design of lineal dicrete controllers, the α value will be near $z = 1$ because in this position the destabilizing effect of the integral is minimized. In the other side, γ will have to be adjusted to guarantee the stability of the system.

The stability can be evaluated using the Jury criterion. Then, it is necessary to obtain the characteristic equation of the system. This can be found mixing equations 2.25 and 2.22. Redoing the whole equation once mixed, it leads to:

$$\hat{E}_{sto} = \frac{\hat{E}^*_{PV} z(z-1) - \hat{E}^*_{sto}(mz^2 + z(0.5\gamma A_g^2 T_g - m) - 0.5\gamma\alpha A_g^2 T_g)}{(1-m)z^2 + (m - 2 - 0.5\gamma A_g^2 T_g)z + 0.5\gamma\alpha A_g^2 T_g + 1} \tag{2.26}$$

The conditions to determine the stability following the Jury criterion must be applied on the denominator characteristic polynomial of the equation.

$$P(z) = (1-m)z^2 + (m - 2 - 0.5\gamma A_g^2 T_g)z + 0.5\gamma\alpha A_g^2 T_g + 1 \tag{2.27}$$

The conditions of the Jury criterion determine if any root exists out of the unit circle of the Z plane, what would lead the system to instability. The conditions are the following ones:

- **Condition 1:** The coefficient of the superior degree must be positive.

  $$(1-m) > 0 \rightarrow m < 1$$

- **Condition 2:** The characteristic polynomial evaluated for $z = 1$ must be greater than zero.

  $$P(1) = (1-m)1^2 + (m - 2 - 0.5\gamma A_g^2 T_g)1 + 0.5\gamma\alpha A_g^2 T_g + 1$$

  Then:

  $$P(1) = -0.5\gamma A_g^2 T_g (1-\alpha)$$

  Then:

  $$P(z)|_{z=1} > 0 \rightarrow -0.5\gamma A_g^2 T_g (1-\alpha) > 0$$

  So there are two possible solutions:

  $$\text{Solution 1: } \begin{cases} \alpha < 1 \\ \gamma < 0 \end{cases} \qquad \text{Solution 2: } \begin{cases} \alpha > 1 \\ \gamma > 0 \end{cases}$$

  The second solution is not possible to be applied because $\alpha > 1$ is out of the unit circle.

- **Condition 3:** The characteristic polynomial evaluated for $z = -1$ must be greater than zero.

$$P(-1) = (1-m)(-1)^2 + (m - 2 - 0.5\gamma A_g^2 T_g)(-1) + 0.5\gamma\alpha A_g^2 T_g + 1$$

Then:

$$P(-1) = 4 - 2m + 0.5\gamma A_g^2 T_g(1+\alpha)$$

Then:

$$P(z)|_{z=-1} > 0 \rightarrow \gamma > \frac{4(m-2)}{A_g^2 T_g(1+\alpha)}$$

- **Condition 4:** It must be accomplished that $|a_0| < a_n$ where a_n and a_0 are the last and the first coefficient of the polynomial $P(z)$.

$$P(z) = a_n z^2 + a_1 z + a_0$$

So:

$$|0.5\gamma\alpha A_g^2 T_g + 1| < (1-m)$$

Then:

$$|\gamma| < \frac{(1-m)-1}{0.5\alpha A_g^2 T_g}$$

Then:

$$|\gamma| < \frac{-2m}{\alpha A_g^2 T_g}$$

To extract the module it must be considered that:

$$|\gamma| < \frac{-2m}{\alpha A_g^2 T_g} \begin{cases} (1): \gamma < \frac{-2m}{\alpha A_g^2 T_g} \\ (2): -\gamma < \frac{-2m}{\alpha A_g^2 T_g} \rightarrow \gamma > \frac{2m}{\alpha A_g^2 T_g} \end{cases}$$

The second condition cannot be accomplished due to the second condition of the Jury criterion, which says that $\gamma < 0$ and $0 < \alpha < 1$. So the condition to be accomplished is the first one.

The conditions 3 and 4, can be unified in one single expression as shown:

$$\frac{4(m-2)}{A_g^2 T_g(1+\alpha)} < \gamma < \frac{-2m}{\alpha A_g^2 T_g}$$

So a little summary of the conditions that must be accomplished to design the control are presented in table 2.2. As can be seen, the parameters depend on the point where the panel

Condition 1	$m < 1$
Condition 2	$\alpha < 1$; $\gamma < 0$
Condition 3 and 4	$\frac{4(m-2)}{A_g^2 T_g(1+\alpha)} < \gamma < \frac{-2m}{\alpha A_g^2 T_g}$

Table 2.2: Design conditions for the external control

is working, therefore it will be necessary to define the working margin of the system and to calculate the values of α and γ for the most restrictive condition.

2.3.2 Design of the Internal Control for the Central Inverter

The internal control, as said, is the responsible for controlling the transistors. Its input is the scalar factor K provided by the external control and the output of this control is the carrier signal that, once compared with the modulating signal, will generate the commutation for the transistors of the bridge, guaranteeing the maximum energy transfer to the grid.

In order to get a sinusoidal current at the output in phase with the grid voltage, it is important to have a control with faster dynamics than the grid period. This can be achieved with linear control techniques or non-linear control techniques. In [9], a linear control has been chosen, so in this thesis the same method will be exposed.

The controller chosen is the proportional-resonant control, which consist on a proportional gain, and an integrator formed by a resonant filter at the grid frequency.

The output equation of the system is:

$$L\frac{di_L}{dt} = v_H - v_g \tag{2.28}$$

Having into account that v_H is the output modulation signal of the control, and that the relation between the reference of the injected current is K times the grid voltage, the whole system can be graphically represented like in figure 2.6. From the block diagram of the system, it can be

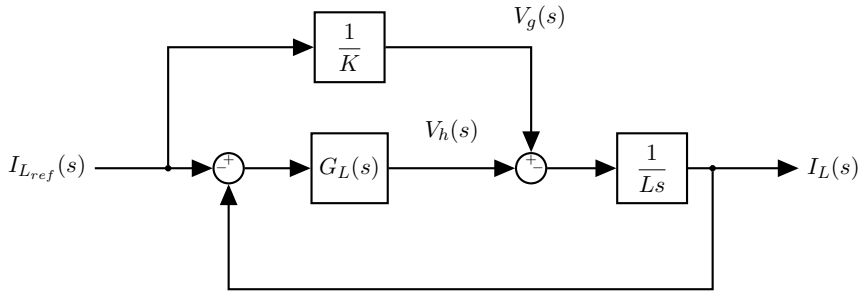


Figure 2.6: Block diagram of inverter system with the internal control

seen that:

$$I_L(s) = \frac{I_{L_{ref}}(s)G_L(s) - V_g(s)}{Ls + G_L(s)} \tag{2.29}$$

Considering the v_g and $i_{L_{ref}}$ in the Laplace domain.

$$\begin{aligned} v_g(t) = A_g \sin(w_g t) \rightarrow V_g(s) = \frac{A_g w_g}{s^2 + w_g^2} \\ i_{L_{ref}} = KA_g \sin(w_g t) \rightarrow I_{L_{ref}}(s) = \frac{KA_g w_g}{s^2 + w_g^2} \end{aligned} \tag{2.30}$$

Substituting these equation into the transfer function, the expression of I_L is obtained.

$$I_L(s) = \frac{KA_g w_g G_L(s) - A_g w_g}{(s^2 + w_g^2)(Ls + G_L(s))}$$

And this equation can be rewritten as:

$$\begin{aligned} I_L(s) = I_{L_{ref}}(s) - H(s) \\ I_{L_{ref}}(s) = \frac{KA_g w_g}{s^2 + w_g^2} \quad H(s) = \frac{KA_g w_g Ls + A_g w_g}{(s^2 + w_g^2)(Ls + G_L)} \end{aligned} \tag{2.31}$$

Observing 2.31, it can be said that the I_L will follow the reference $I_{L_{ref}}$ only if, in steady state, $H(s) = 0$ and therefore the error is 0. That means that the theorem of the final value must be applied for $H(s)$, so:

$$\lim_{t\to\infty} \mathcal{L}^{-1}H(s) = 0 \rightarrow \lim_{s\to 0} sH(s) = 0 \tag{2.32}$$

However, this theorem can only be applied if the roots of the characteristic equation of the system are located into de negative part of the Laplace plane (which means that the system is stable and tends to a fixed point when $t \to \infty$). In the equation of $H(s)$, two complementary and pure imaginary poles can be found due to the frequency grid. Therefore, the control G_L must be designed to cancel these two poles and get an expression of $H(s)$ which only contain negative real poles, and moreover, it will correspond to a under damped response of the system.

The equation of the resonant-proportional controller which has been chosen is:

$$G_L(s) = K_p + \frac{K_i s}{s^2 + w_g^2} \rightarrow G_L(s) = \frac{K_p s^2 + K_p w_g^2 + K_i s}{s^2 + w_g^2} \tag{2.33}$$

The final expression of the injected current is:

$$I_L(s) = \frac{K A_g w_g}{s^2 + w_g^2} - \frac{K A_g w_g L s + A_g w_g}{L s^3 + K_p s^2 + (K_i + L w_g^2)s + K_p w_g^2} \tag{2.34}$$

And the characteristic polynomial of the $H(s)$ function is its denominator:

$$P(s) = L s^3 + K_p s^2 + (K_i + L w_g^2)s + K_p w_g^2 \tag{2.35}$$

The stability of the system (in order to make the final value theorem applicable) can be found by the Routh-Hurwitz criterion. To determine if the system is stable, two conditions must be accomplished.

- All the coefficients of the polynomial must exist and must be positive.
- All the coefficients of the first column of the formation algorithm must be positive.

Accomplishing all these premises, a proper internal control of the inverter can be achieved. As it is not the objective of this thesis, numerical design will not be developed here, but it can be found in [8].

2.3.3 Design Evaluation for External Control of the Central Inverter Topology

Following the conditions exposed in the previous sections, the practical design of the external control can be achieved. The values of elements that appear in the equation are shown in table 2.3.

- **Condition 1:** The parameter m must less than one ($m < 1$). The value of m will depend on the number of series connected cells, the temperature, and the irradiance. Below are presented the curves for the value m.

  In figure 2.7 it is showed that the most restrictive case in terms of irradiance is for $1000W/m^2$. As can be seen, the voltage value to get $m = 1$ is higher than for other irradiances. However, for the case of central inverter, the minimum voltage value will not

$A_g = 220\sqrt{2}$ $f_g = 50Hz$ $C_{sto} = 1200\mu F$ Temperature $= 25^oC$

Table 2.3: Values for external control evaluation

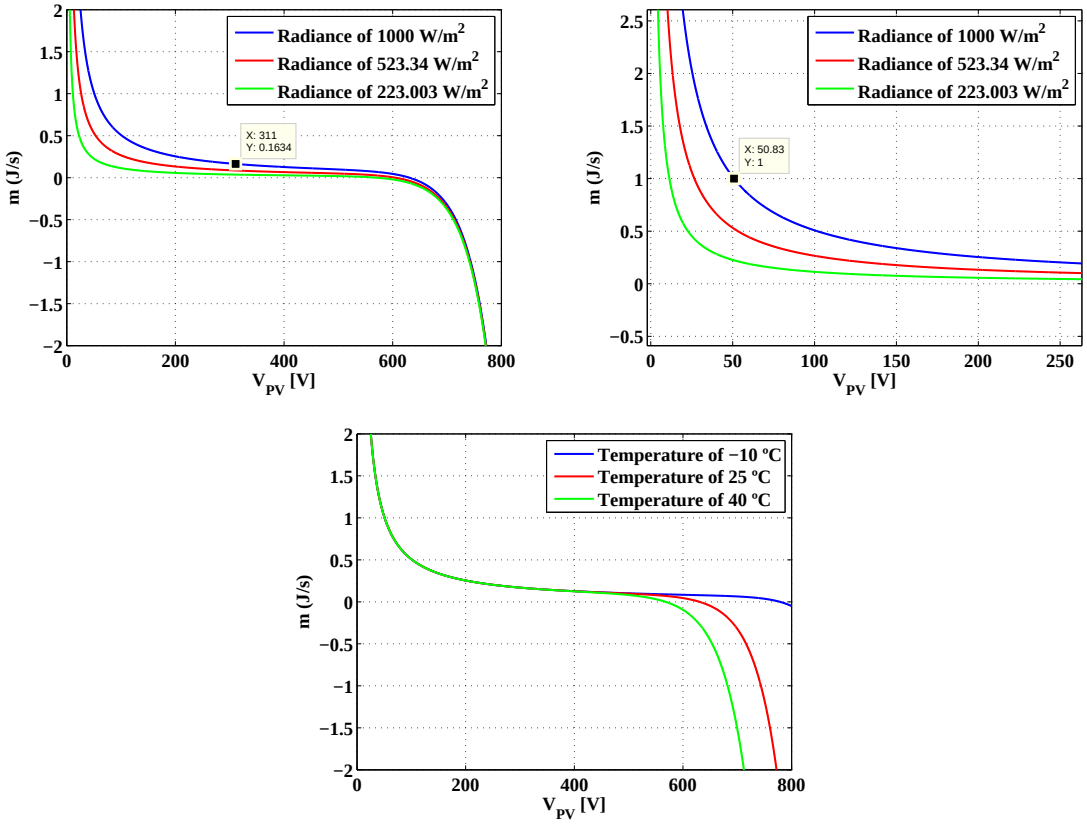


Figure 2.7: m parameter curves

depend on the inequality $m < 1$ but will depend on the minimum voltage value which is higher than the voltage grid. In this case, $220\sqrt{(2)} \simeq 311V$. For the case of different temperatures, it can be seen that all the curves have the same crossing point where $m = 1$, and the point for voltage value of $311V$ is also the same, so it can be concluded that the temperature is not determinant. Therefore, a temperature of 25^oC will be considered, as it is an standard value.

In conclusion, as the stability of the control must be guaranteed the most restrictive value of m parameter, the value of $m = 0.1634$ is chosen. This value assures that first condition is accomplished by the whole possible working points of the system.

- **Condition 2:** This condition imposes that $\alpha < 1$. However, the value of α must be as close as possible to 1, because this value corresponds to the value of the zero of the controller, and therefore must be positioned near $z = 1$ in order to minimize the destabilizing effect introduced by the integrator element. Therefore, a value of $\alpha = 0.875$ is chosen.

- **Conditions 3 and 4:** As shown before, conditions 3 and 4 can be mixed in only one condition. The value of γ, which is chosen by these conditions, depend on the value of m parameter. Therefore, having chosen the value for $m = 0.1606$, the inequality can be solved, and γ will have to be between values of:

$$\frac{4(m-2)}{A_g^2 T_g(1+\alpha)} < \gamma < \frac{-2m}{\alpha A_g^2 T_g} \rightarrow -0.002023801653 < \gamma < -0.000192916175 \tag{2.36}$$

  The intermediate value of γ is chosen, so $\gamma = -0.0011084$

Having chosen the values, the root locus can be represented for different values of m by expressing the open loop function of the characteristic polynomial in terms of m.

$$1 + G_{ol} = 0 \rightarrow 1 + \frac{m(-z^2 + z)}{z^2 + (-2 - 0.5\gamma A_g^2 T_g)z + 0.5\gamma\alpha A_g^2 T_g + 1} \tag{2.37}$$

Figure 2.8 shows the root location for large different values of $m = [-7.5, 1]$. It can be seen that

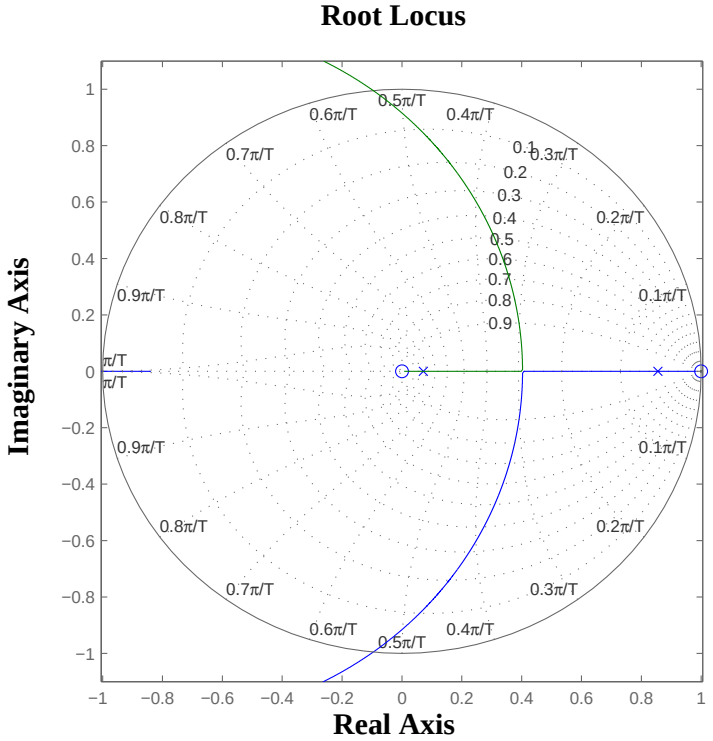


Figure 2.8: Root Location of G_{ol} for values of $m = [-7.5, 1]$

for certain values of m, the root locus are outside of the unit circle, which means the system would be unstable. However, what is really interesting is to analyse the values of m that will be possible working points of the system. Therefore, the root locus must be evaluated between values of $m = -1.17$, which corresponds to the maximum voltage values that the panels can provide (open circuit voltage, $750V$), and $m = 0.17$, which is the value of $m = 0.1634$ rounded, and is the minimum value of voltage for what the system can inject energy to the grid, and corresponds to the grid voltage. As can be seen, the poles obtained for the system will be

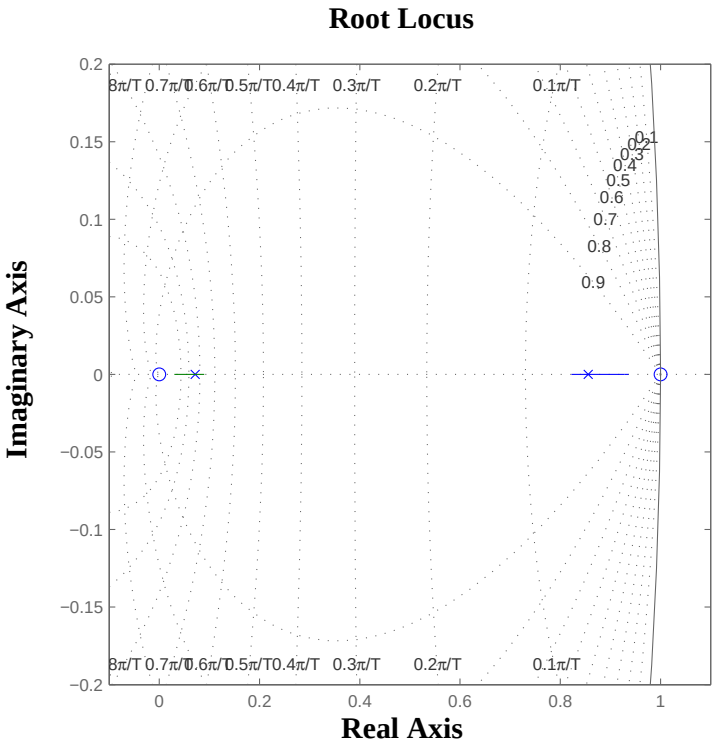


Figure 2.9: Root Location of G_{ol} for values of $m = [-1.17, 0.17]$

always real for these working points, and therefore the system will be stable and an overdamped response is obtained.

The external control is valid for both topologies of the central inverter, with and without the LCL. However, the design of the internal control is not the same for both topologies, so a design example will not be provided. Section 2.4 exposes the design for the internal control of the central inverter topology.

2.4 Control Design for the Central Inverter Connected to the Grid by LCL Filter

In this section, effects of the LCL filter over the internal control are discussed.

2.4.1 Single Stage LCL Filter Calculus

Several studies have been published about the issue of designing properly and efficiently the LCL output filter. As this is not a focus point of the present thesis, the calculus of the LCL filter is based on the article [16].

As can be seen, the value of the components of the filter depend on the output power, the switching frequency, the attenuation rate, the grid voltage, the grid frequency, the DC voltage before the inverter and the maximum ripple allowed in the output current. In this thesis these values chosen are presented in table 2.4. The values chosen respond to various reasons. On one

$v_g = 220V_{rms}$
$P_{out} = 3000W$
$v_{PV} = 700V$
$f_{sw} = 20kHz$
$f_g = 50Hz$
$I_{ripple} = 10\%$
$K_a = 0.1$

Table 2.4: Starting values to calculate the LCL filter

side, there the obvious reasons, for example for the value of v_g or f_g, that are standard grid values in Europe. But on the other side there are the values chosen for other motives. Output power has been fixed at $3000W$. The switching frequency has been chosen so low because it's an standard value and will cause more ripple than higher switching frequency values, so we will obtain conservatives values of the filter that will guarantee proper functionality from this "worst case" value to higher values. The values of current ripple and attenuation factor have been chosen so restrictive for the same reason, to obtain values of the filter that will guarantee the high quality of the current injected to the grid. The value for the ripple recommended by the paper is the same that has been chosen, and the value recommended for the attenuation factor is 20% (based on other articles); the value chosen in this thesis is 10% (as smaller is more restrictive). K_a is an attenuation factor used in the calculus, that determines the ripple of the output current, and, thus, it affects directly the value of the output inductor (L_c). Finally, V_{PV} is an approximate value of the output voltage of the panel arrays, working in a normal point. But, despite this, this value is actually a variable which depends on the irradiance received by the panels and the point where the MPPT decides that the panels must work (normally maximum power point).

Following the steps provided by [16], the calculus of the filter has been performed. Even so, having into account the values that condition the results, two different calculus must be implemented. In both central inverter topology and series connection of the inverter stages topology, the filter is only one, and it must carry on with all the output power; but in the parallel topology with LCL shared, the inductors of each phase must be dimensioned according to it's power specifications, discussed later.

Following the steps exposed in [16] and having the initial values shown in table 2.4, calculus can be performed. The calculation is based on two merit figures, the base impedance and the base capacitance.

$$\begin{aligned} Z_b &= \frac{v_g^2}{P_{out}} = \frac{220^2}{3000} = 16.13\Omega \\ C_b &= \frac{1}{w_g Z_b} = \frac{1}{2\pi 50 \cdot 17.63} = 197.3\mu F \end{aligned} \tag{2.38}$$

The value of the capacitor of the filter can be directly obtained from the base capacitance.

$$C_f = C_b \cdot 0.05 \rightarrow C_f \simeq 9\mu F \tag{2.39}$$

And with the value of C_f and K_a can be obtained the value of the output inductance of the

filter.

$$L_c = \frac{\sqrt{\frac{1}{K_a^2}} + 1}{C_f w_{sw}^2} \simeq 80\mu H \tag{2.40}$$

Finally, to find the value of phase inductance, it is necessary to calculate first the current ripple, and this one is calculated compared to the maximum current amplitude.

$$\begin{aligned} I_{1\ max} &= \frac{P_{out}}{V_g}\sqrt{2} \\ \Delta I_1 &= I_{1\ max} 0.1 \\ L_1 &= \frac{V_{PV}}{6 f_{sw} \Delta I_1} \simeq 3.2mH \end{aligned} \tag{2.41}$$

2.4.2 Stability under the LCL Filter

Once having studied the effects of the LCL filter over the stability of the external control, and having seen the method to calculate this filter, the last subject to study about this filter is the effect over the stability of the internal control.

This study was exposed by [17], and the design of the correction of the control presented in this thesis is based on this reference study.

The block diagram of the LCL filter is presented below: As known, the objective of the internal

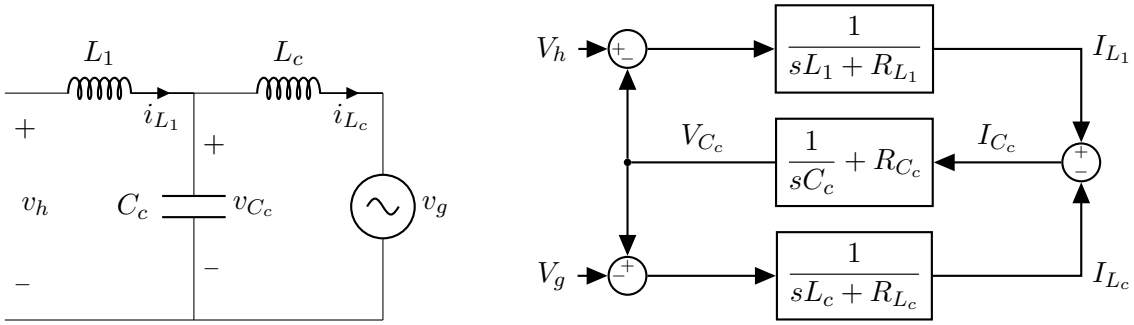


Figure 2.10: LCL Schematic Circuit and Block Diagram

control is to control the injected current to the grid. The voltage V_h showed in the diagram represents the voltage generated by the mosfets when switching (the voltage of the H bridge), this voltage is a function of the control signal, therefore the expression which describes the control system is:

$$\begin{aligned} \frac{I_{L_c}(s)}{V_h(s)} &= \frac{sR_{C_c}\gamma + 1}{\alpha s^3 + \beta s^2 + \gamma s + R_{L_c} + R_{L_1}} \\ \alpha &= L_c L_1 C_c \\ \beta &= C_c(L_c(R_{C_c} + R_{L_1}) + L_1(R_{C_c} + R_{L_c})) \\ \gamma &= L_c + L_1 + C_c(R_{C_c}R_{L_c} + R_{C_c}R_{L_1} + R_{L_1}R_{L_c}) \end{aligned} \tag{2.42}$$

Having the expressions of the plant for LCL filter, we evaluate its frequency response for an ideal filter.

$L_c = 80uH$	$R_{C_c} = 0\Omega$
$R_{L_c} = 0\Omega$	$L_1 = 3.2mH$
$C_c = 9\mu F$	$R_{L_1} = 0\Omega$

Table 2.5: Values of ideal filter elements

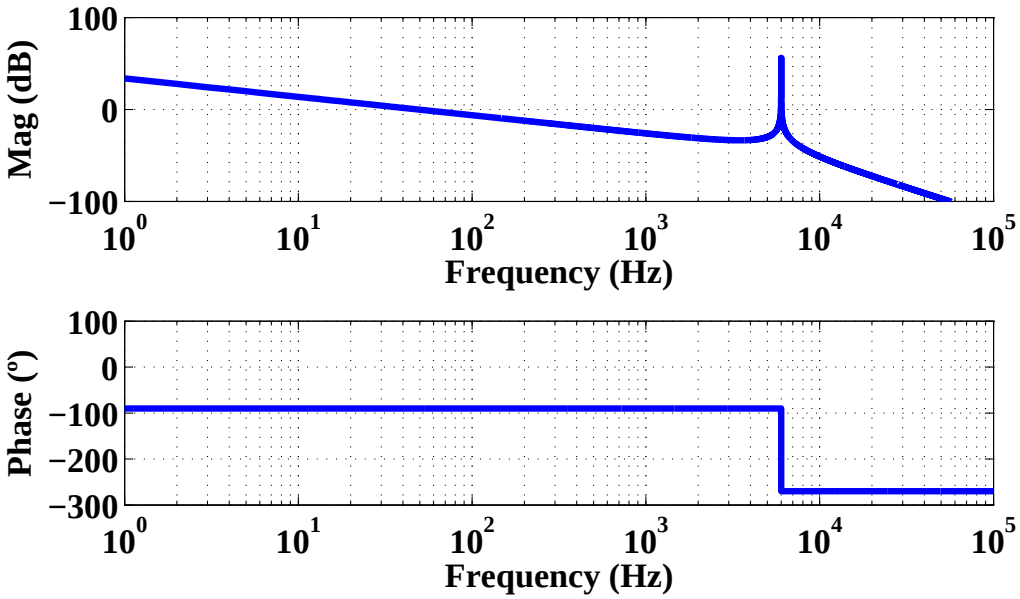


Figure 2.11: Bode diagram $\frac{I_{L_c}}{V_h}$ (LCL plant)

As can be seen, the system presents a gain peak at the resonant frequency. This gain peak leads the system to instability, so it must be attenuated to restore the stability of the system. As exposed in [17], the natural losses of the system will help to attenuate the gain peak (figure 2.12), but not enough to assure the stability of the system. Therefore, some way must be found in order to make this response stable.

$L_c = 80uH$	$R_{C_c} = 8m\Omega$
$R_{L_c} = 10m\Omega$	$L_1 = 3.2mH$
$C_c = 9\mu F$	$R_{L_1} = 100m\Omega$

Table 2.6: Values of Real Filter Elements

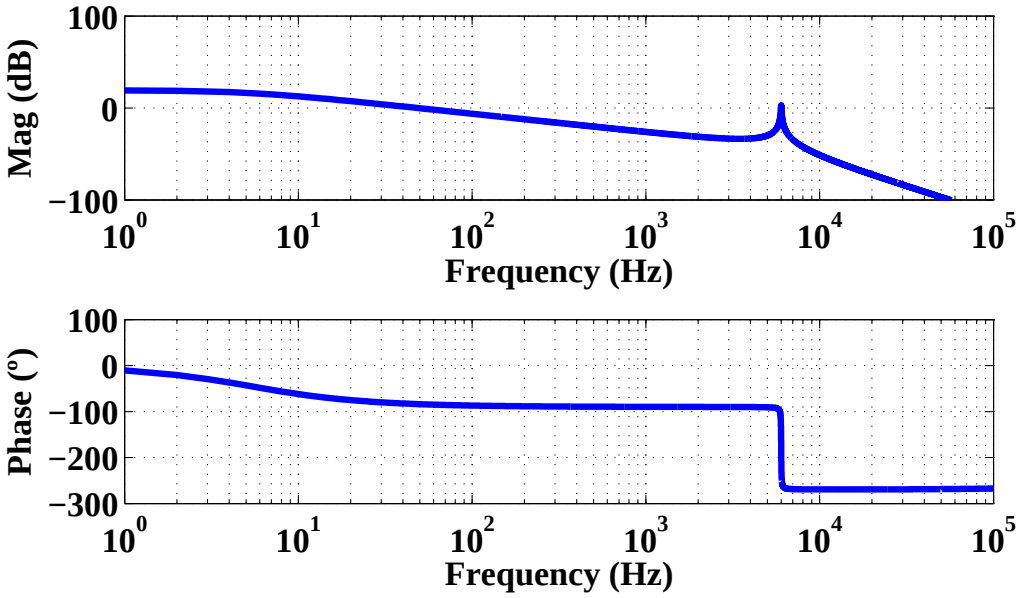


Figure 2.12: Bode diagram $\frac{I_{L_c}}{V_h}$ with losses (LCL plant)

2.4.3 The Feed-forward solution

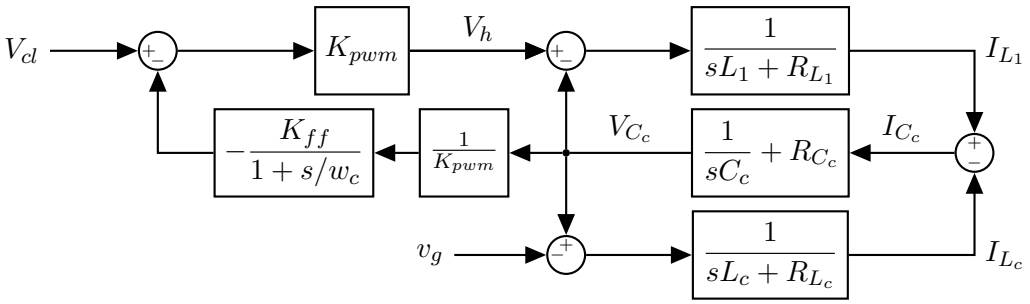


Figure 2.13: Block diagram of feed-forwarded control

In [17] are presented some methods to attenuate the undesired resonance without increasing the real losses, but in this thesis the focus will be put on feed-forward method. The principle of this method is to inject the capacitor voltage as the reference signal, with the control signal added to it. The cut-off frequency of the sensing filter of the capacitor voltage can be harnessed to attenuate the resonance, but must be properly tuned. The block diagram of this proposed control is shown in figure 2.13. This block can be mathematically expressed as shown in equation 2.43

$$V_{cl} + D(s)V_{C_c} = V_h \qquad \frac{V_h - V_{C_c}}{Z1} \qquad (I_{L_1} - I_{L_c})Z_c = V_{C_c} \qquad \frac{V_{C_c} - V_g}{Z_{L_c}} = I_{L_c} \tag{2.43}$$

Where $D(s)$ is the transfer function of the feed-forward shown in equation 2.44.

$$D(s) = -\frac{K_{ff}}{1 + s/w_c} \qquad K_{pwm} = 1 \tag{2.44}$$

Z_{L_1}, Z_{L_c} and Z_c are the simplified impedances of the inductances and the capacitor of the filter, in order not to make the final transfer function and its calculus cumbersome. Their expressions are shown in equation 2.45.

$$Z_{L_1} = sL_1 + R_{L_1} \qquad Z_c = \frac{1}{C_c} + R_{C_c} \qquad Z_{L_c} = sL_c + R_{L_c} \tag{2.45}$$

In equation 2.46 there is the expression of the transfer function of output current in respect of control voltage.

$$\frac{I_{L_c}(s)}{V_{cl}(s)}|_{V_g(s)=0} = \frac{Z_c}{Z_c Z_{L_1} + Z_{L_c} Z_{L_1} + Z_{L_c} Z_c (1 + D(s))} \tag{2.46}$$

And the transfer function of output current in respect of grid voltage is shown in equation 2.47. This transfer function will be used to determine the rejection to disturbances in the grid voltage.

$$\frac{I_{L_c}(s)}{V_g(s)}|_{V_{cl}(s)=0} = -\frac{Z_{L_1} + Z_c(1 + D(s))}{Z_{L_c} Z_{L_1} + Z_{L_c} Z_c (1 + D(s)) + Z_c Z_{L_1}} \tag{2.47}$$

The value of the gain of the feed-forward, K_{ff}, and the cut-off frequency of its filter,f_c, must be tuned to find a compromise between a correct perturbation rejection and a good attenuation of the resonance peak. To make the simulations of the transfer functions, losses have been added. It is not the worst case for what it can be analysed, but it is the most realistic case. Table 2.6 shows the values used.

Figure 2.14 shows the value of the peak depending on the values of f_c and K_{ff}. The figure shows how, for higher value of K_{ff}, higher attenuation of the peak. The best attenuation is achieved for $f_c = 5800Hz$.

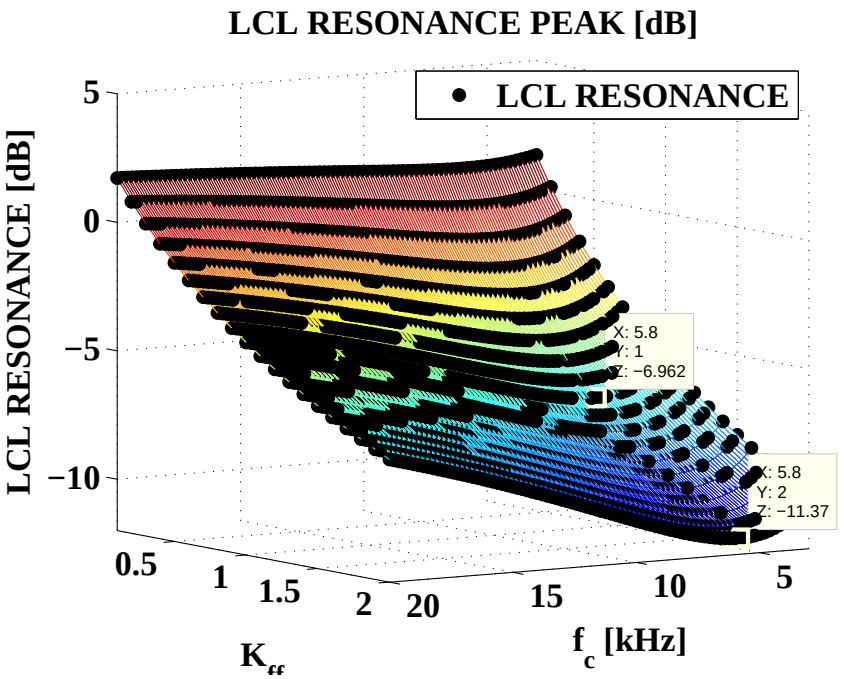


Figure 2.14: Peak attenuation depending on the value of K_{ff} and f_c

Despite this, if the gain has a different value from $K_{ff} = 1$, the DC rejection has not an acceptable value. Figure 2.15 the DC rejection for different values of K_{ff}. As can be seen, the gain of feed-forward can onlvy be fixed to $K_{ff} = 1$. In other cases, the rejection is not acceptable and can lead to output current offset, what is completely undesired. The value of f_c is not enough relevant in this case.

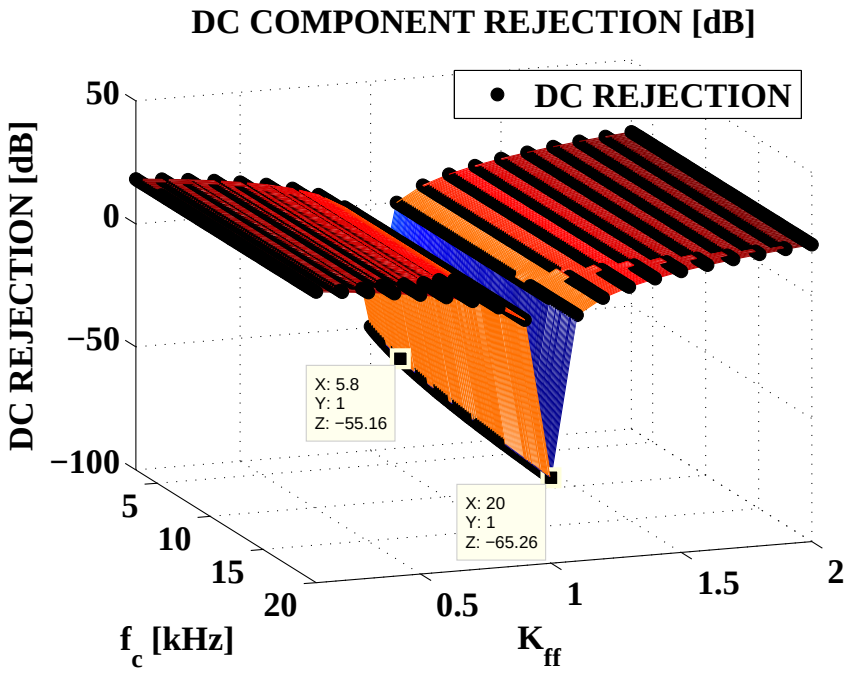


Figure 2.15: DC rejection depending on the value of K_{ff} and f_c

So, finally, the values chosen are $K_{ff} = 1$ and $f_c = 5800Hz$. With these values, the gain of the resonance peak is fixed to $-6.96dB$. The bode diagram of the plant with the feed-forward added is shown in figure 2.16.

The rejection of the plant to disturbances in the grid voltage is showed in figure 2.17. As can be seen, it presents an infinite attenuation in DC frequency, which that the injected current will be free of offset.

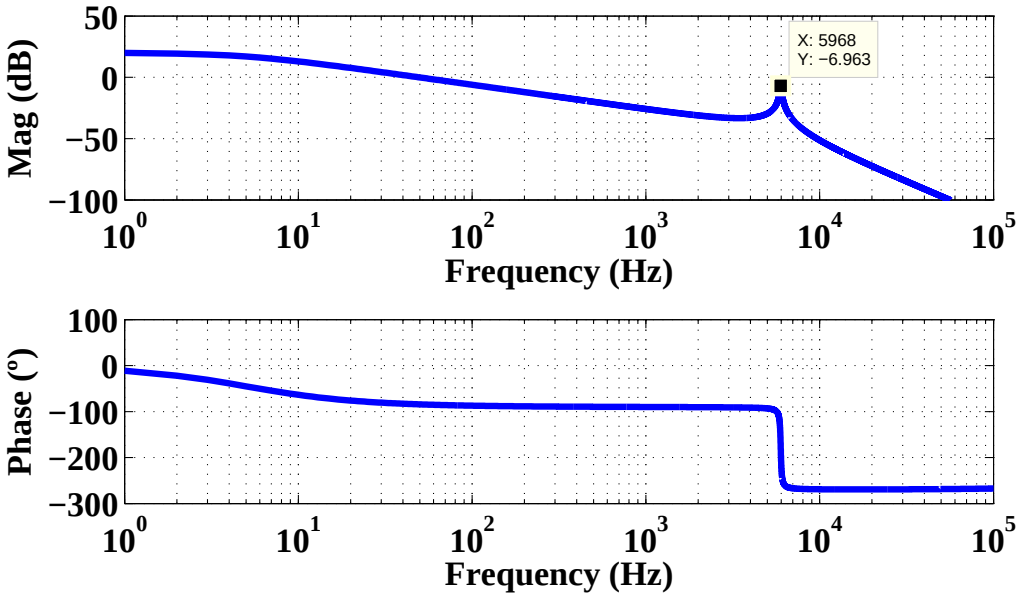


Figure 2.16: Bode diagram of $\frac{I_{Lc}(s)}{V_{cl}(s)}|_{V_g(s)=0}$

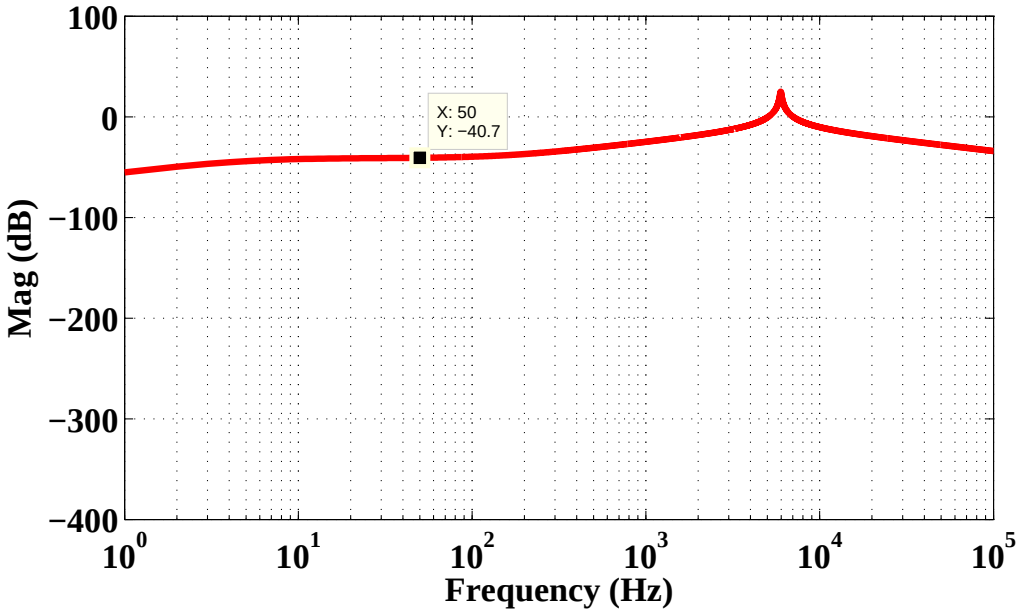


Figure 2.17: Bode diagram of $\frac{I_{Lc}(s)}{V_g(s)}|_{V_{cl}(s)=0}$

2.4.4 Verification of Internal Control under LCL Filtering

Once having stabilized the plant of the LCL filter, the response of the closed loop must be verified again, in order to determine if the gains of the proportional resonant control must be recalculated or not.

The external control is not affected by the usage of LCL filter. However, as seen, the internal control can be affected. Having calculated the values for the feed-forward, the whole plant of

the system will be treated as a single transfer function. Thus, figure 2.18 can be simplified to a block diagram like the showed in figure 2.19.

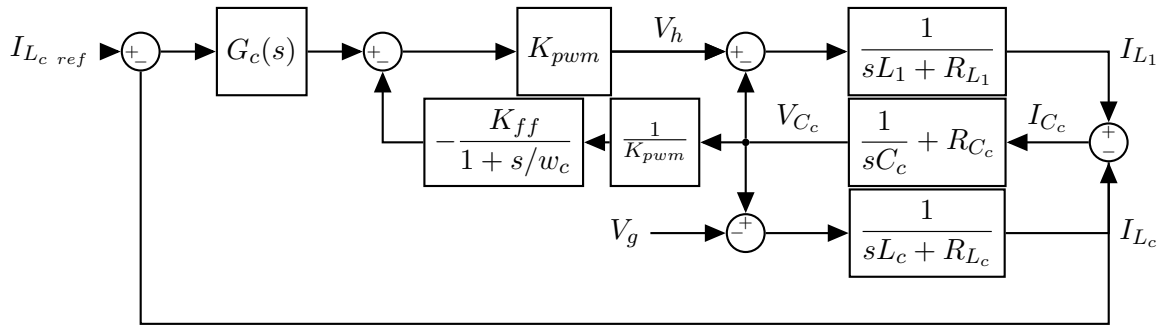


Figure 2.18: Block diagram of Internal Control with feed-forward added

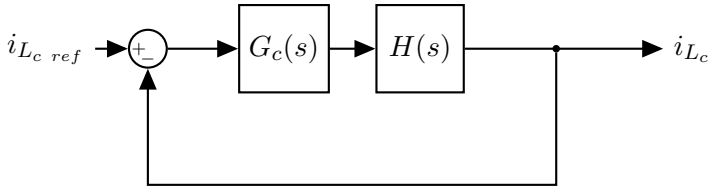


Figure 2.19: Simplified Block diagram of Internal Control with feed-forward added

The transfer function of the system when the loop is closed is presented in equation 2.48.

$$\frac{I_{L_c}(s)}{I_{L_c\ ref}(s)}|_{V_g(s)=0} = \frac{Z_c G_c(s)}{Z_{L_c} Z_{L_1} + Z_{L_c} Z_c(1 + D(s)) + Z_c G_c(s) + Z c Z_{L_1}} \tag{2.48}$$

The transfer function of the rejection to grid voltage disturbances is presented in equation 2.49

$$\frac{I_{L_c}(s)}{V_g(s)}|_{i_{Lc\ ref}(s)=0} = -\frac{Z_{L_1} + Z_c(1 + D(s))}{Z_{L_c} Z_{L_1} + Z_{L_c} Z_c(1 + D(s)) + Z_c G_c(s) + Z c Z_{L_1}} \tag{2.49}$$

The expression of the $G_c(s)$ control is the typical of a proportional resonant control, and is shown in equation 2.50.

$$G_c(s) = K_p + \frac{K_i s}{s^2 + w_g^2} \tag{2.50}$$

Values of K_p and K_i must be determined in order to have an stable response of the system. Due to the complexity of the mathematical expressions, the control will be evaluated through bode diagram method.

The value of K_i only determines how selective is the filter [13]. Greater values of K_i leat to higher perturbation rejection. However, the gain peak at the resonant frequency is increased, and therefore an intermediate value must be chosen. In this thesis the value is fixed at $K_i = 50000$. The value of K_p will be adjusted in function of the bode diagram, to achieve an stable response of the system, so, the beginning value is fixed at $K_p = 1$.

With the values chosen for the control gains, the response presents a gain in the resonance peak of $-2.5dB$. It is a little stability margin, and the system is close to instability, but, however, it is stable, so the value of K_p will not be changed and will remain to $K_p = 1$. The value of $K_i = 50000$ is maintained.

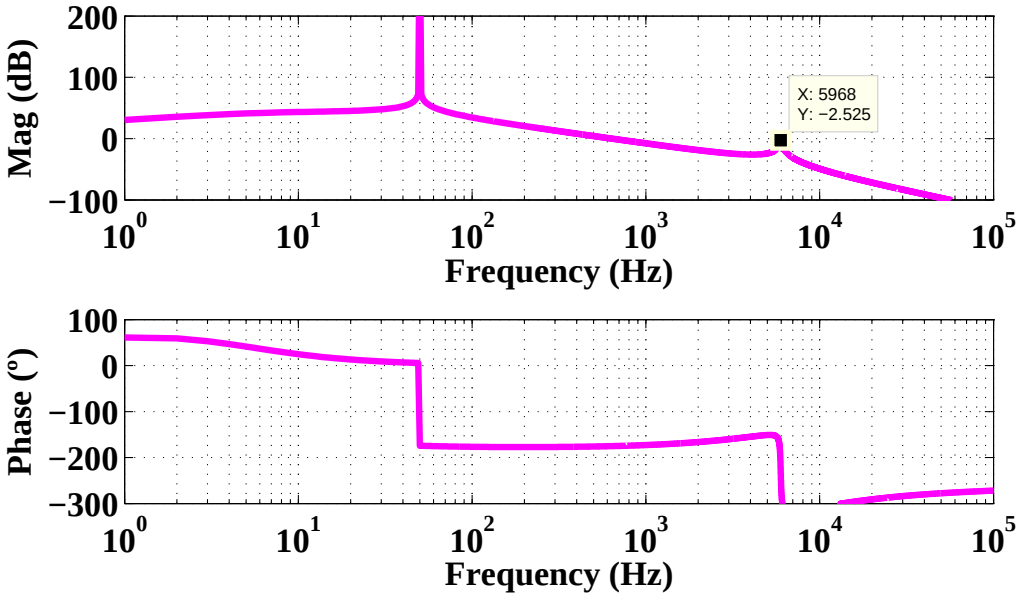


Figure 2.20: Bode of transfer function $\frac{I_{L_c}(s)}{I_{L_c\ ref}(s)}|_{V_g(s)=0}$

The rejection bode diagram with these gains is shown in figure 2.21. As can be seen, the rejection at $50Hz$ is very high ($-365dB$) due to the effect of the resonant control, and tends to infinite for DC frequency. Therefore, the perturbations on the grid voltage and on DC currents (undesired offset) will be properly rejected.

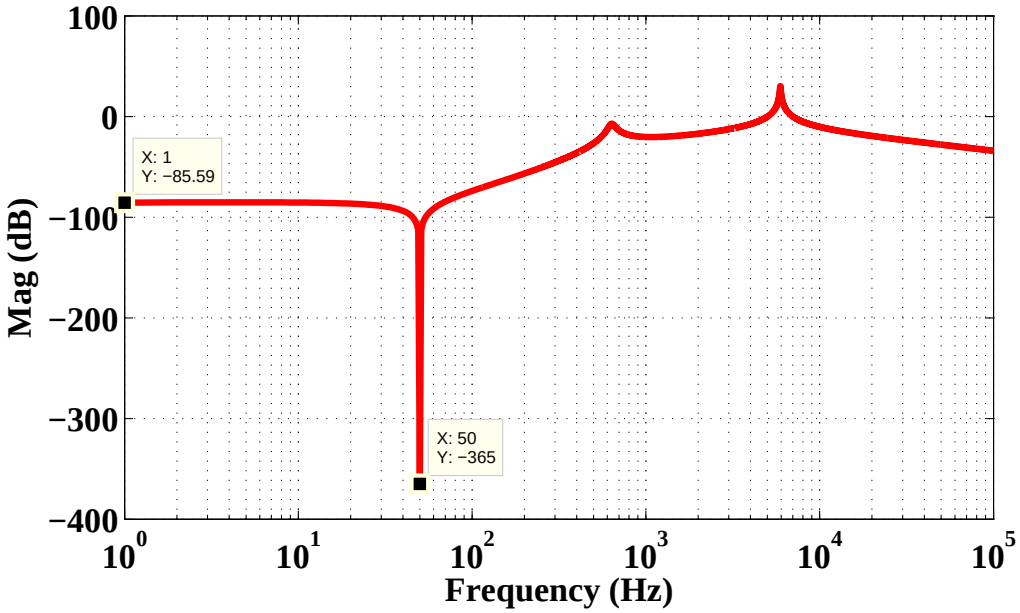


Figure 2.21: Bode of transfer function $\frac{I_{L_c}(s)}{V_g(s)}|_{i_{L_c\ ref}(s)=0}$

Once the different controls of the central inverter topology have been studied, some simulations

will be performed in order to test the correct functionality of the system.

Simulation 2.1. Irradiance Transient in Central Inverter Topology

The first simulation tests the response of the system in front of a abrupt irradiance transient. The values used in the simulation are shown in table 2.7. The values of the transient irradiance and the reference voltage given by the MPPT are also exposed. As can be seen, the transient implemented consists on reducing suddenly the irradiance and return to the same point after some seconds.

$L_1 = 3.2mH$	$R_{L_1} = 100m\Omega$
$L_c = 80\mu H$	$R_{L_c} = 10m\Omega$
$C_c = 9\mu F$	$R_{C_c} = 8m\Omega$
$A_g = 311V$	Temp=25^oC
$f_{sw} = 40kHz$	
Irradiance transients:	
$764.1678W/m^2$ $(2250W)$	$0\ s < t \leq 1.3\ s$
$223.003W/m^2$ $(600W)$	$1.3\ s < t \leq 2.5\ s$
$764.1678W/m^2$ $(2250W)$	$2.5\ s < t$
Panel Array Voltages references:	
$619.712V$	$0\ s < t \leq 1.3\ s$
$569.56V$	$1.3\ s < t \leq 2.5\ s$
$619.712V$	$2.5\ s < t$

Table 2.7: Values used in simulation 2.1

Figures 2.22 and 2.23 show the results of the simulation. The first figure shows the current and the grid voltage. The behaviour of the currents is, for this case, satisfactory. The injected current is always in phase with the grid voltage and only presents a little amplitude transient during the irradiance one. This is because the currents are not limited by software (the K scalar factor) and therefore in front of an abrupt transient of irradiance the external control gives the order to empty the output panels capacitor, so the current at the first moment is very high. In the next transient, the inverse effect is observed, as the capacitor must store energy, the value of the current is reduced at the first moment, and recuperated later.

Figure 2.23 shows perfectly how the external control is properly designed and can face the abrupt irradiance transient. The output voltage of the panels suffers a sudden change, but it is recuperated and stabilised at the corresponding point for both transients. So it can be concluded that the system has in general a good response when a irradiance change occurs.

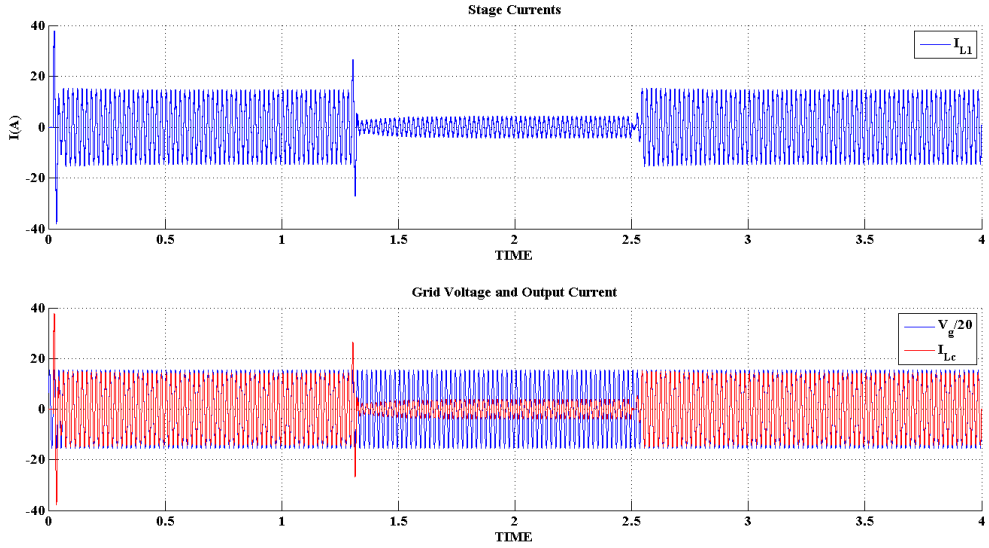


Figure 2.22: Currents and Grid Voltage

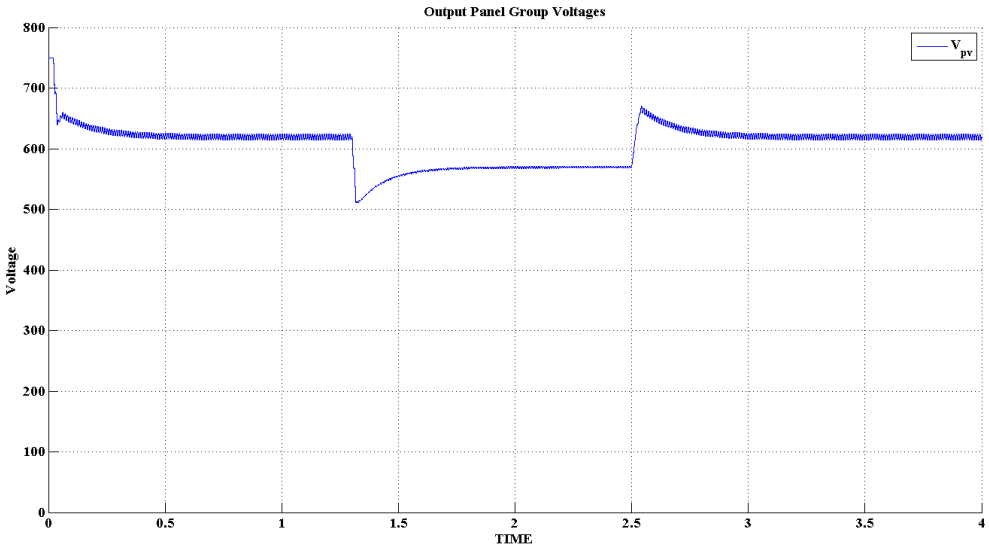


Figure 2.23: Panel Arrays Voltages

Simulation 2.2. MPPT Reference Abrupt Transient in Central Inverter Topology

In this case, the simulation consists on moving the output voltage of the panel array over the $1000W/m^2$ curve, by moving the voltage reference given by the MPPT. Doing this, the output power given by the panels is also changed. The purpose of this simulation is to determine how the system respond to abrupt voltage reference change. Table 2.8 shows the values of the plant and the transient values for this simulation. As in this case the output power is reduced, the effects on currents amplitudes are inverted in respect to the last simulation. However, in essence, what can be observed is the same effect.

$L_1 = 3.2mH$	$R_{L_1} = 100m\Omega$
$L_c = 80\mu H$	$R_{L_c} = 10m\Omega$
$C_c = 9\mu F$	$R_{C_c} = 8m\Omega$
$A_g = 311V$	Temp=25^oC
$f_{sw} = 40kHz$	Irradiance=$1000W/m^2$
Panel Array Voltages references:	
$630.696V$ $(3000W)$	$0\ s < t \leq 1.3\ s$
$736.4V$ $(1000W)$	$1.3\ s < t \leq 2.5\ s$
$630.696V$ $(3000W)$	$2.5\ s < t$

Table 2.8: Values used in simulation 2.2

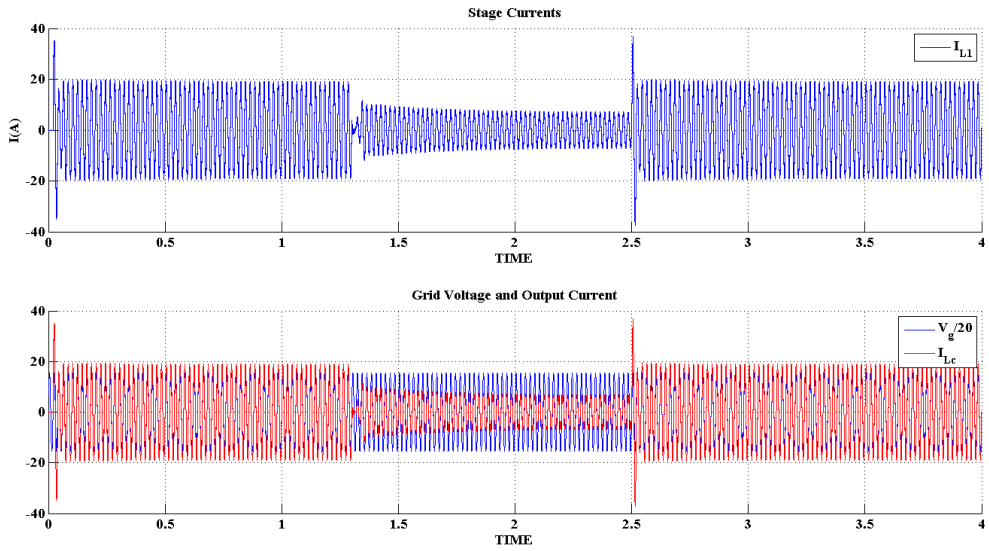


Figure 2.24: Currents and Grid Voltage

Figure 2.25 is more interesting as it shows how the output voltage evolution is smoother than in the last simulation. This shows that the external control responds better, or is less affected, facing a change in the MPPT reference than facing a sudden irradiance change. However, in both case, the external and the internal controls work properly. The output current is always in phase with the grid voltage and the output panel array voltage value stabilises at its setpoint.

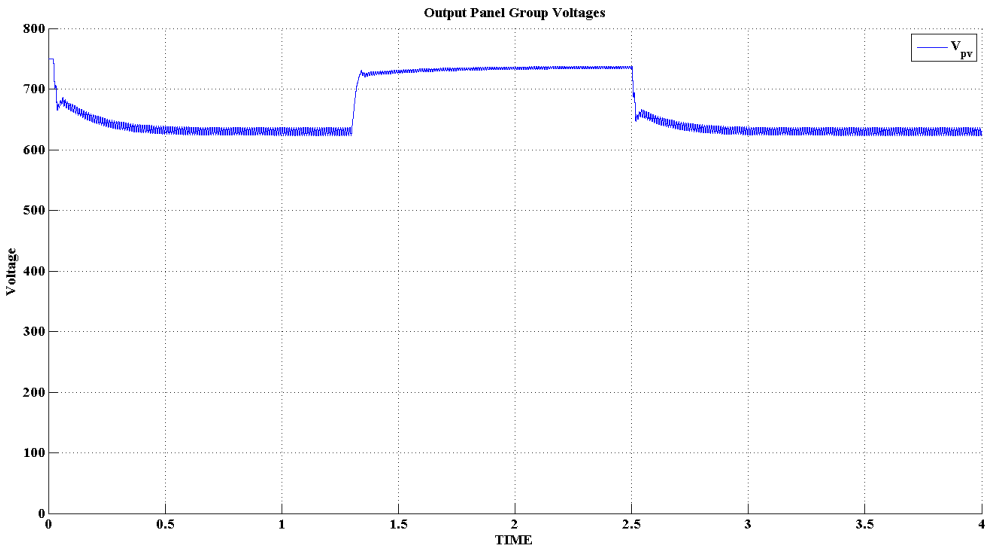


Figure 2.25: Panel Array Voltages

Simulation 2.3. MPPT Reference Tracking in Central Inverter Topology

This simulation is in essence the same as the last one. It is performed to determine if the system is capable to respond properly to changes at the output voltage reference, like in simulation 2.2. These change will be smoother but with less time between them. Table 2.9 shows the values used to perform the simulation.

$L_1 = 3.2mH$	$R_{L_1} = 100m\Omega$
$L_c = 80\mu H$	$R_{L_c} = 10m\Omega$
$C_c = 9\mu F$	$R_{C_c} = 8m\Omega$
$A_g = 311V$	Temp=25^oC
$f_{sw} = 40kHz$	Irradiance=$1000W/m^2$
Panel Array Voltages References:	
$630.696V$ $(3000W)$	$0\ s < t \leq 1.2\ s$
$707.168V$ $(2250W)$	$1.2\ s < t \leq 1.8\ s$
$720.512V$ $(1800W)$	$1.8\ s < t \leq 2.4\ s$
$727.288V$ $(1500W)$	$2.4\ s < t \leq 3\ s$
$737.984V$ $(900W)$	$3\ s < t \leq 3.6\ s$
$742.384V$ $(600W)$	$3.6\ s < t$

Table 2.9: Values used in simulation 2.3

Figure 2.26 shows how the current follows its reference (the given by the external control) without problem and it is always in phase with the grid voltage. Any change is appreciated that deserves to be commented. The output voltage panels also follows the reference given by the MPPT. Voltage abrupt transients are not appreciated in this simulation due to the smoother characteristic of the reference changes. Having seen the three simulations for this topology, it

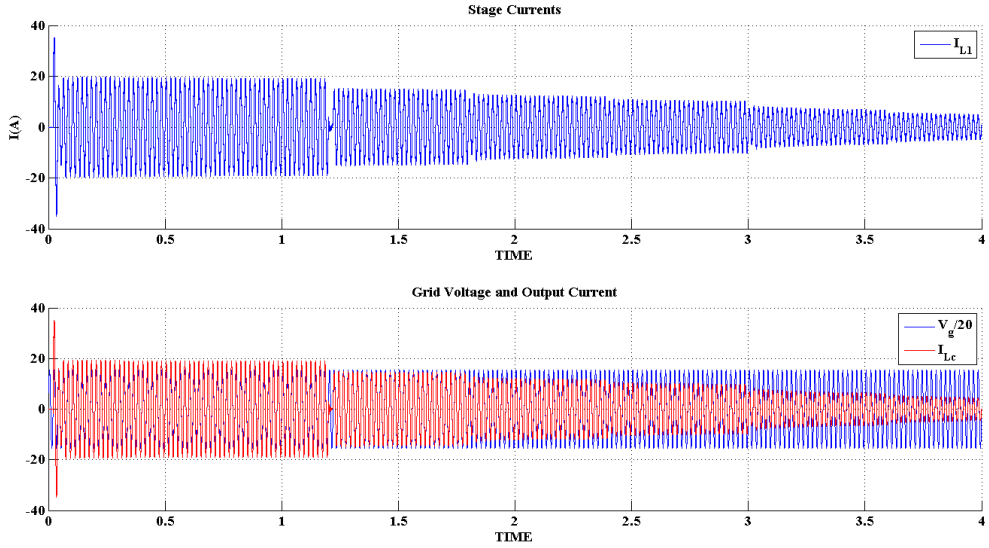


Figure 2.26: Currents and Grid Voltage

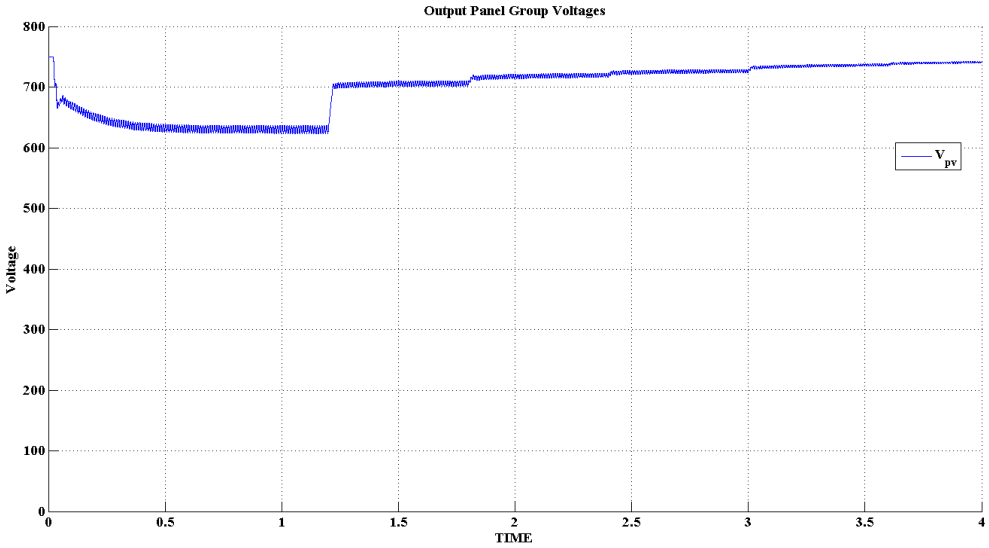


Figure 2.27: Panel Array Voltages

can be concluded that the response of the system for different transients is satisfactory.

Chapter 3

The Series Connected Inverters Topology

The series inverter connection topology consists on having the inverter of each stage connected in series with the inverters of other stages. The panel array is divided in voltage terms for each stage. The output of this multilevel inverter is connected to the grid through an inductor or another type of filter (by the moment is only one inductor). The DC voltage sources (the solar panels) are floating and are not connected between them, and is the commutation of the mosfets what must give the total voltage combining the different voltage levels. Figure 3.1 exposes the scheme of this topology.

The advantages of this topology are:

- As the stages are completely independent between them, the construction can be modularized, so there is no complexity on building it.
- If the sum of voltages of the active stages is higher than the grid voltage, the whole array can work even if one of the stages is not active, which can happen if the panels are partially shadowed, if a panel breaks for any reason or other motives.
- The output voltage waveform can be similar to a sinusoid, this means that the harmonic content of the output signal will be less than the generated by a single stage (the central inverter).To do this, the sequence which manages the transistors must be properly designed.
- Depending on the modulation strategy used, the stress in the transistors can be reduced, this means that the losses of the system are reduced and hence, the efficiency of the while system is increased.

In the next subsections the design of the controls (both internal and external) are presented.

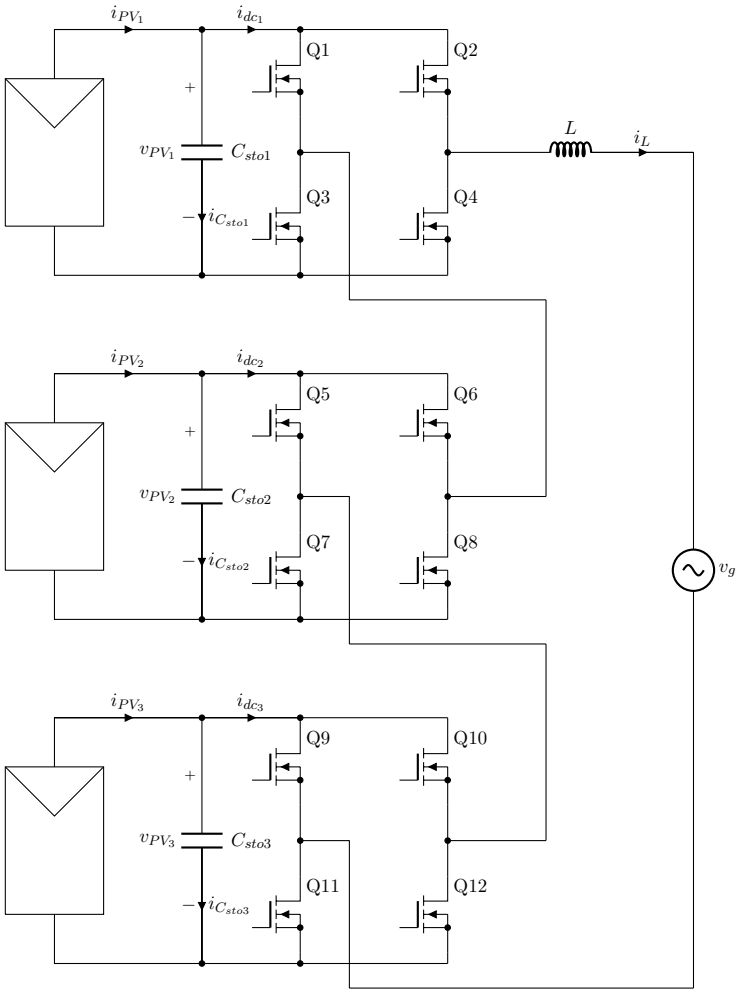


Figure 3.1: Schematic of series connected inverters topology

3.1 Modelling the System from Energetic Balance

The model from the energetic balance for this topology can be achieved beginning from the same hypothesis of section 2.1, which were:

- Assuming that there are no losses in the system, the balance between the power supplied by all the stages, the power stored in the reactive elements and the power injected to the grid must be maintained. Beginning from a topology connected to the grid by a single inductor (figure 3.1), it can be mathematically expressed as:

$$\begin{aligned} P_{inT} &= P_{inv} + P_{out} \\ P_{in1} + ... + P_{inn} &= P_{C_{sto1}} + ... + P_{C_{ston}} + P_L + P_{out} \end{aligned} \tag{3.1}$$

  Where:

  - P_{inn} is the power supplied by the panel array of each stage.
  - $P_{C_{ston}}$ is the power stored in the capacitor connected to the output of each panel array.
  - P_L is the power stored at the output inductor

– P_{out} is the power injected tot the grid

The general equation of the system can be expressed in terms of the state variables.

$$\sum_{n=1}^{i} i_{PV_n} v_{PV_n} = \sum_{n=1}^{i} v_{PV_n} C_{ston} \frac{dv_{PV_n}}{dt} + L \frac{di_L}{dt} i_L + v_g i_L \tag{3.2}$$

- The injected current is considered to be in phase with the grid voltage. It can be expressed as:

$$v_g = A_g sin(w_g t) \qquad i_L = K A_g sin(w_g t) \tag{3.3}$$

Where, $w_g = 2\pi f_g$, and f_g is the grid frequency, $50Hz$ in Europe.

From these hypothesis, a linearised and discrete model can be obtained by manipulating the equations like in sections 2.1.2 and 2.1.3. The mathematical development will not be presented in this thesis, it can be consulted in [8].

$$\hat{E}_{stoTOT} = \sum_{n=1}^{i} \hat{E}_{ston} = \sum_{n=1}^{i} (\hat{E}^*_{PVn} + m_n(\hat{E}_{ston} - \hat{E}^*_{ston})) \frac{z}{z-1} - \sum_{n=1}^{i} \frac{\hat{K} A_g^2 T_g}{2(z-1)} \tag{3.4}$$

The final expression of the whole linearised and discrete system is shown in equation 3.4. From this equation, a block diagram cannot be represented directly, but it can be done by grouping all the terms. If the variable $\hat{K}$ is defined as the sum of K parameters of the i stages:

$$\hat{K} = \sum_{n=1}^{i} \hat{K}_n \tag{3.5}$$

Then, equation 3.4 can be rewritten as:

$$\hat{E}_{stoTOT} = \sum_{n=1}^{3} \hat{E}_{ston} = \sum_{n=1}^{3} (\hat{E}^*_{PVn} + m_n(\hat{E}_{ston} - \hat{E}^*_{ston})) \frac{z}{z-1} - \sum_{n=1}^{3} \hat{K}_n \frac{A_g^2 T_g}{2(z-1)} \tag{3.6}$$

The equation 3.6 can be represented as the block diagram shown in figure 3.2. Therefore, the variable $\hat{K}$ is the scalar factor that defines the total power injected to the grid, and it is the addition of the scalar values of each stage. This means that each stage will have its own external control, independent between them, but the energy balance have to be accomplished by the sum of all of them.

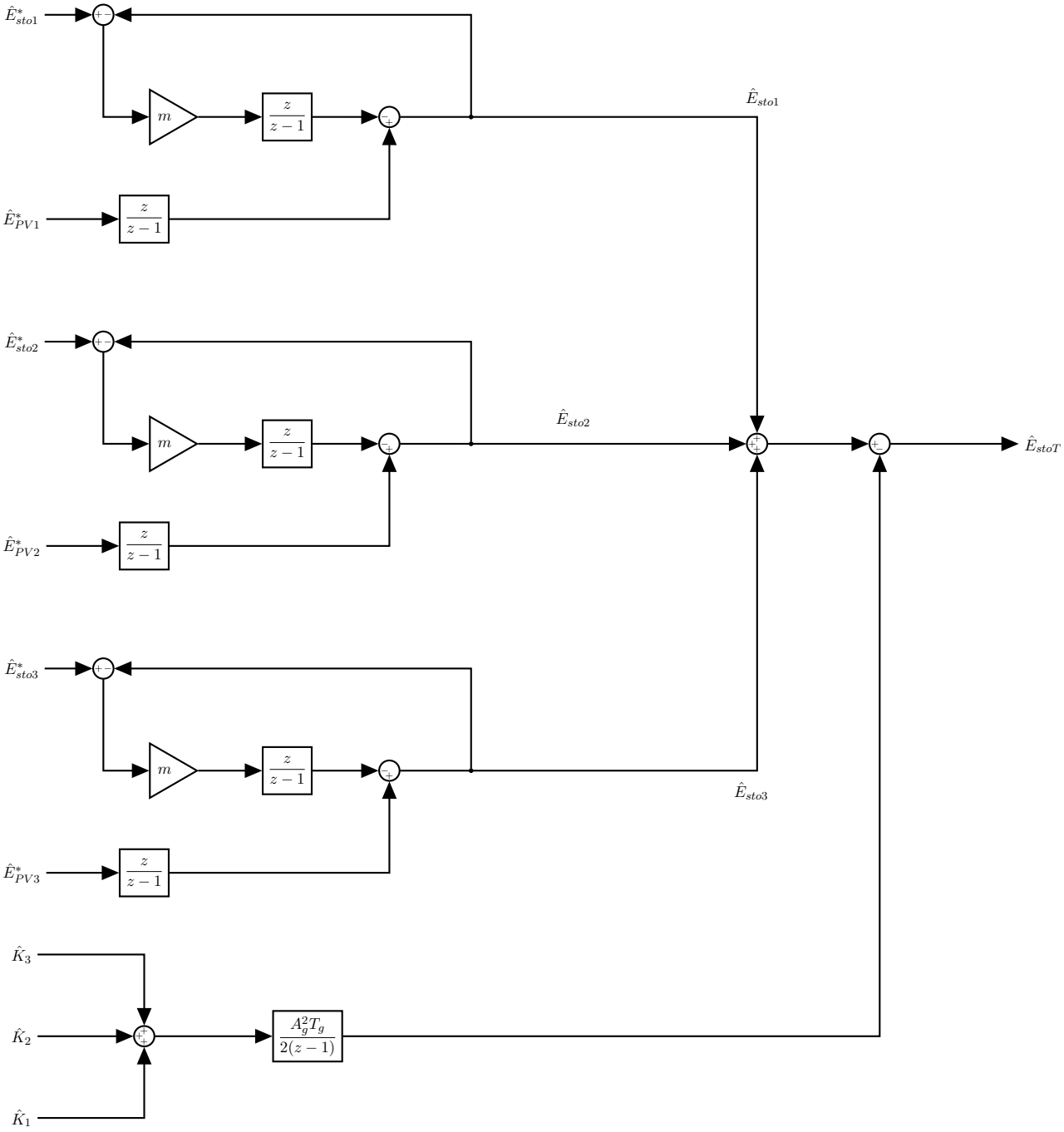


Figure 3.2: Extended open loop block diagram of the series connected inverters topology

3.2 The Energy Balance under LCL filtering in Series Connected Inverters Topology

Following the steps of the central inverter topology, the LCL will be applied to the series connected inverter topology, as described in figure 3.3. The energy balance can be raised by

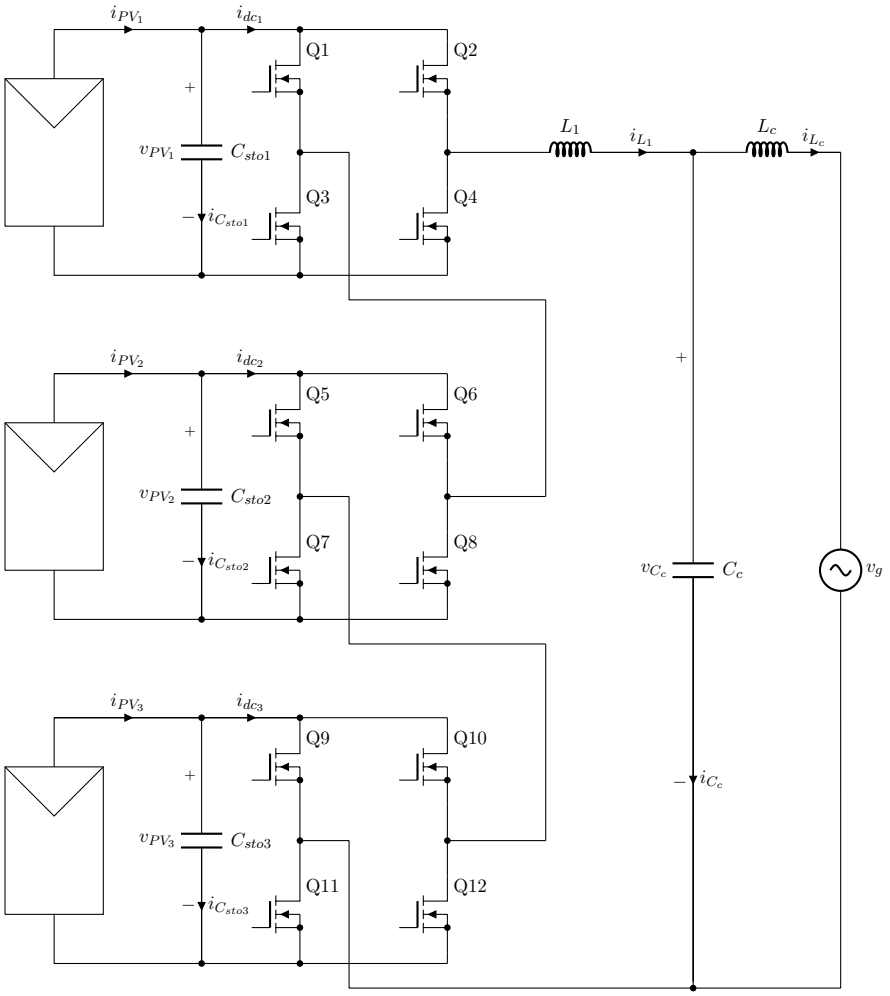


Figure 3.3: Schematic of series connected inverters topology with LCL filter

rewriting the equation 3.1

$$\begin{aligned} &P_{inT} = P_{inv} + P_{out} \\ &P_{in1} + ... + P_{inn} = P_{C_{sto1}} + ... + P_{C_{ston}} + P_{L_1} + P_{C_c} + P_{L_c} + P_{out} \end{aligned} \tag{3.7}$$

As it was described in section 2.2, the terms P_{L_1}, P_{C_c} and P_{L_c}, when integrated and averaged over one grid period, become 0, and therefore can be erased from the energetic balance. If this is done, equation 3.7 becomes the same as the equation 3.1.

For this reason, the LCL, again, does not affect the energy balance and the external controls of each stage can be calculated in the same way of the central inverter topology, despite some little changes that will be presented in next sections.

3.3 Controls Design for Series Connected Inverters Topology

As seen in previous chapters, the controls for the series connected inverters will follow the diagram presented in figure 3.7. This figure is a representation of the topology with 3 stages. The external controls are presented independently as has been explained in section 3.1, and the

internal control is the same for all the stages, as only the output current will be controlled. The way to generate three different voltages for each stage from one single control is based on the modulation strategy, which is presented in section 3.4.

3.3.1 Design of the External Control for the Series Connected Inverters Topology

The external control design for each stage can be achieved in the same way than it was in the central inverter. The block diagram for each stage is presented in figure 3.4.

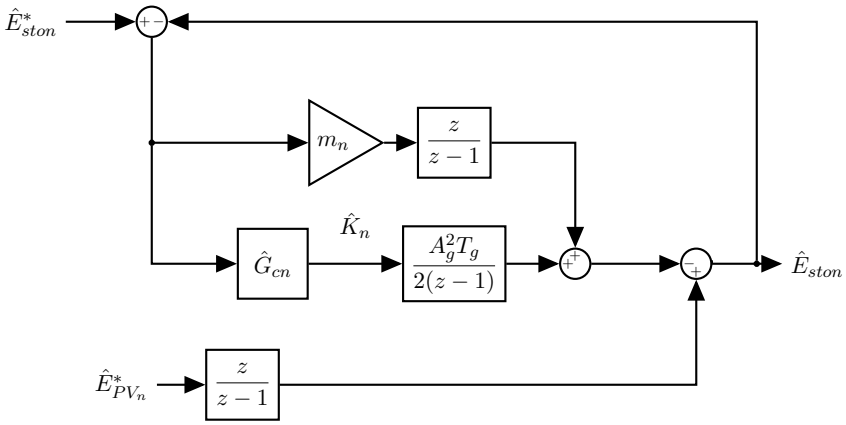


Figure 3.4: Block diagram of the discrete linear model of the inverter system with the controller $\hat{G}_c$ applied for each stage

As can be seen, the diagram is the same than for the central inverter topology. However, as the panel array will differ from the single array of the central inverter, the working margin will have to be redefined, because the design parameters of the control depend on the working point.

To design the external control for the series inverter topology, the characteristic polynomial for each stage system must be analysed. As it is the same than for the central inverter, the conditions of Jury criterion exposed in table 2.2 will be also the same.Therefore, the same steps can be followed.

3.3.2 Design Evaluation for External Control of The Series Connected Inverters

To accomplish the first condition, the m parameter curve must be analysed. As the variable transmitted by the MPPT is given in voltage units, the m parameter is represented in figure 3.5 versus the output voltage of the panel array. The values of irradiance and temperature are chosen because they are the most restrictive, according to the studies made in section 2.3.1 As the topology is evaluated for 3 stages, the minimum voltage point where a panel array can work is equal to the maximum voltage point for other 2 stages, as shown in equation 3.8. To determine the open circuit voltage (maximum voltage) of one panel array, table 1.2 can be consulted.

$$v_{PVmin} = A_g - 2V_{oc}(1000W/m^2) = 220\sqrt{(}2) - 2 \cdot 249.98 = -188.83 \tag{3.8}$$

The result is negative. This means that one of the panel arrays could not work and other two arrays could maintain the output power. If one array of panels can work at 0 voltage point for

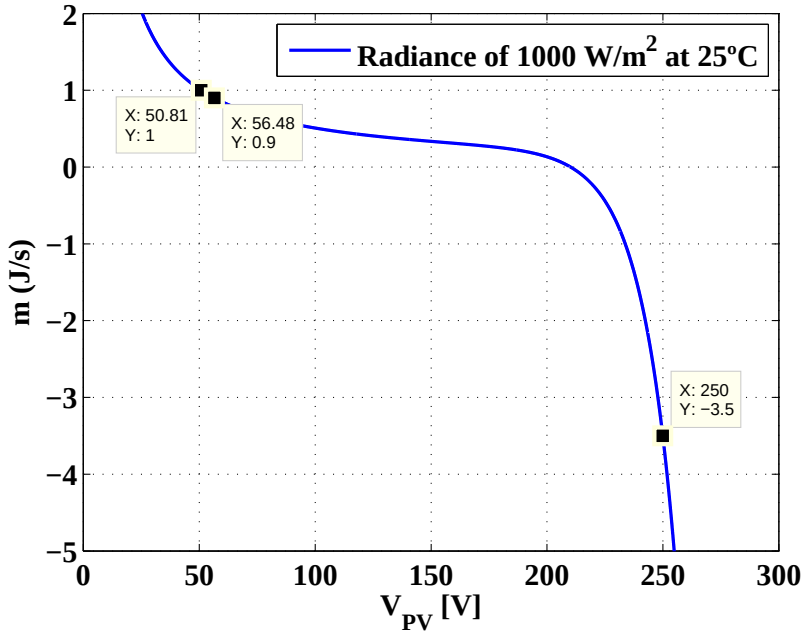


Figure 3.5: m parameter versus voltage for a single panel array in series connected inverters topology

this condition, then the minimum voltage point to have an stable system is the point where the parameter m reaches the value 1. In figure 3.5 is shown that this happens for a voltage of $50.83V$. The maximum value is shown in other point of the figure, where the open circuit voltage is reached ($m = -3.5$), so for between these two points, the stability of the system is guaranteed. However, the value of $m = 0.9$ is chosen because it guarantees the stability of the system, so the minimum voltage imposed will be $56.48V$.

The second condition imposed by the Jury criterion is $\alpha < 1$, so the value $\alpha = 0.875$ chosen for the central inverter will be maintained. This value is close to the unit circle of the z plane, so it will minimize the unestabilizer effect of the integral part of the control.

The third and fourth condition stablish:

$$\frac{4(m-2)}{A_g^2 T_g(1+\alpha)} < \gamma < \frac{-2m}{\alpha A_g^2 T_g}$$

Taking the value chosen for m, the intermediate value for $\gamma = -0.0011373$ is chosen. In figure 3.6 root location for different values of m is shown. As can be seen. The poles will not be real, therefore an under-damped response is expected. Considering that the control is designed to work always at the maximum power point, perhaps it could be said that there is no point on allow an stability margin for all the curve. However, during abrupt irradiance changes, abrupt changes on voltage are produced, and the system must be maintained into the stable region until it can fix the correct working point again.

For the case of having different panel types in different stages, the work margin must be considered for each one, and its control must be designed for the most restrictive case. However in this thesis, it is considered that all the panels are the same type.

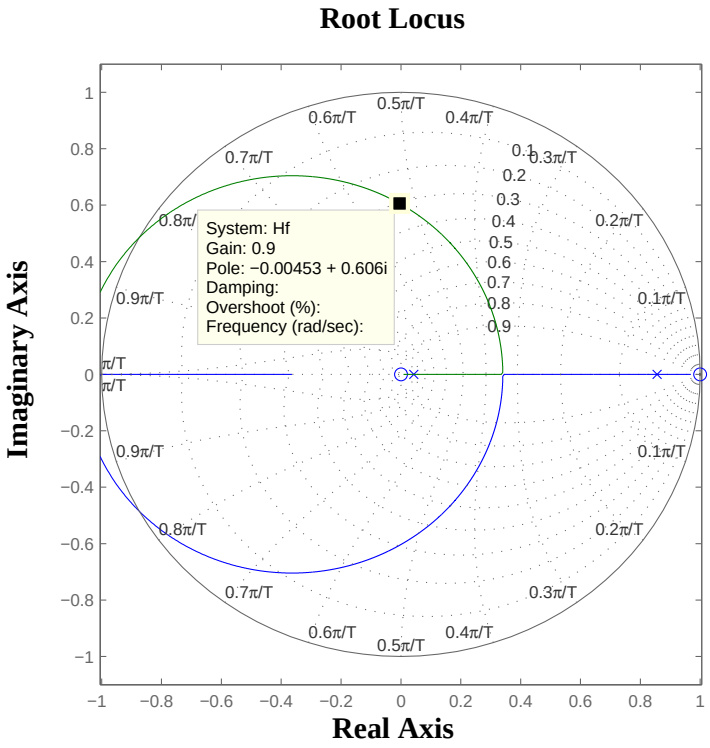


Figure 3.6: Root location for different m values

3.3.3 Design Evaluation of the Internal control for the series Inverter Connection Topology

The internal control will not be exposed in this thesis, as the design is exactly the same exposed for the central inverter topology.

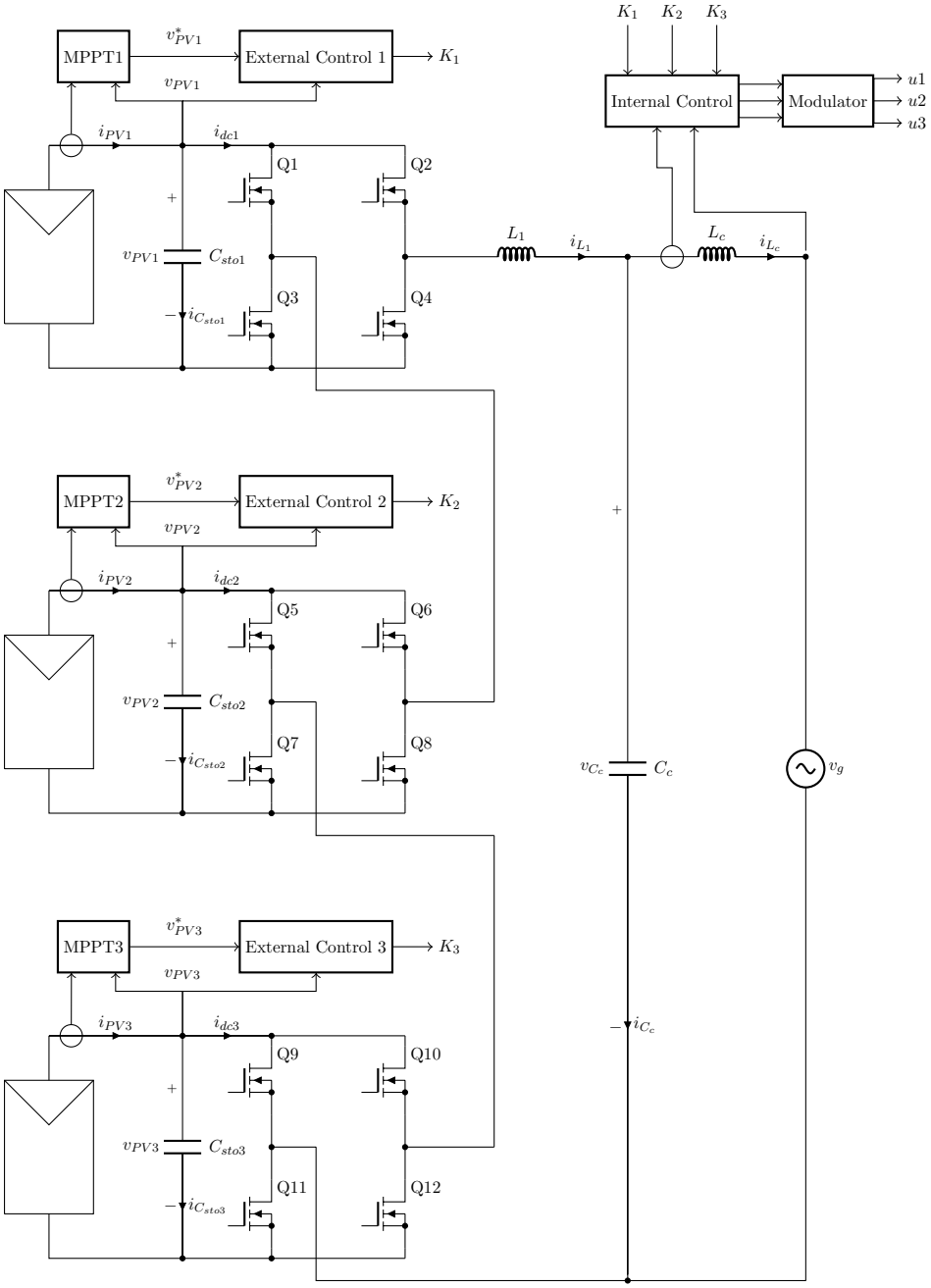


Figure 3.7: Schematic of series connected inverters topology controls block diagram

3.4 Modulation Strategy for Series Connected Inverters Topology

The modulation strategy used in this thesis is the *Phase-shifted Pulse Width Modulation*. This technique is based on generating the inverse of the modulator signal (which is the signal present at the output of the PR filter) and compare both signal with n carrier signals for n inverter stages. The carrier signals are phase shifted depending on the number of stages, as presented

in equation 3.9

$$\Delta phase = \frac{360^o}{n} \tag{3.9}$$

In this thesis, as said, three stages will be considered ($n = 3$). The commutation sequence obtained using the described technique is presented in figure 3.8.

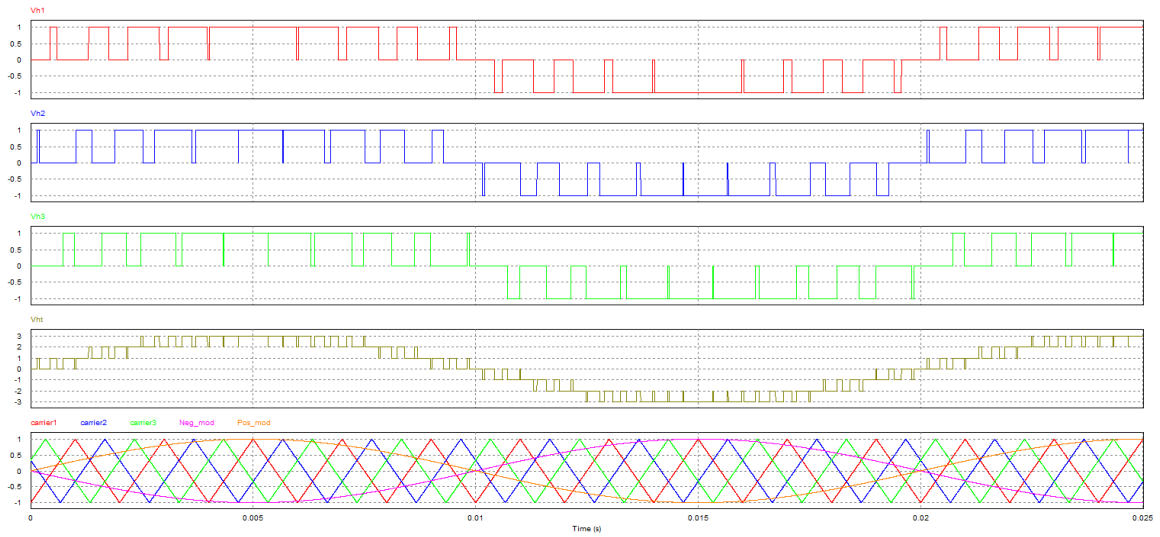


Figure 3.8: PS-PWM Modulation sequence

The final voltage applies to the LCL (v_{hT}) has seven possible levels. It can be verified by the equation 3.10.

$$k = 2n + 1 \rightarrow k = 2 \cdot 3 + 1 = 7 \tag{3.10}$$

The different transistor bridges are always commutating, so a ripple of frequency equal to the double frequency of the carrier signals is generated in the inductor. This modulation strategy, by itself, make the different stages to have the same commutation intervals in one grid period, as the modulator signal is the same for all of them. This causes that the different stages tend to work at the same output voltage panel point, and therefore, if the irradiance is different, the panel arrays cannot work each one at their maximum power point.

To correct this, the modulation strategy is modified. The modulator signals for each stage are weighted depending on the scalar K_n coefficient for each stage, as shown in equation 3.11.

$$d_n = \frac{K_n}{K_t} d \quad \text{Where: } K_t = K_1 + K_2 ... + K_n \tag{3.11}$$

Doing this, independent cycles are get for each stage, so they can fix their working point to its maximum power point. This also means that with one single internal control stage, n outputs are provided, and therefore, n stages can be controlled. The commutation sequence for any stage is specified in table 3.1.

u_n	$Q(4(n-1)+1)$	$Q(4(n-1)+2)$	$Q(4(n-1)+3)$	$Q(4(n-1)+4)$	v_{hn}
1	OFF	ON	ON	OFF	$+v_{PVn}$
0	ON	OFF	ON	OFF	0
0	OFF	ON	OFF	ON	0
-1	ON	OFF	OFF	ON	$-v_{PVn}$

Table 3.1: Unipolar Conmutation Sequence for n Stages

Simulation 3.1. Irradiance Transient in Series Connected Inverter Topology

As the controls of the series inverter topology are very similar to the controls of centrla inverter topology, similar responses can be expected. However, is must be tested.

The simulation tests the response of the system in front of an abrupt irradiance transient. The values used in the simulation are shown in table 3.2. The values of the transient irradiance and the reference voltage given by the MPPT are also exposed. As can be seen, the transient implemented consists on reducing suddenly the irradiance and return to the same point after some seconds.

$L_1 = 3.2mH$	$R_{L_1} = 100m\Omega$
$L_c = 80\mu H$	$R_{L_c} = 10m\Omega$
$C_c = 9\mu F$	$R_{C_c} = 8m\Omega$
$A_g = 311V$	Temp=25^oC
$f_{sw} = 40kHz$	
Irradiance transients for all stages:	
$764.1678W/m^2$ $(750W)$	$0\ s < t \leq 1.3\ s$
$223.003W/m^2$ $(200W)$	$1.3\ s < t \leq 2.5\ s$
$764.1678W/m^2$ $(750W)$	$2.5\ s < t$
Panel Array Voltages references:	
$206.586V$	$0\ s < t \leq 1.3\ s$
$189.856V$	$1.3\ s < t \leq 2.5\ s$
$206.586V$	$2.5\ s < t$

Table 3.2: Values used in simulation 3.1

Figure 3.9 shows the currents and the grid voltage. As can be seen, the same transients in the currents observed in central inverter, are observed here. As said, this is not a problem, but an expected effect due to the non limitation of the stages scalar factors(Kn).

Figure 3.10 shows the panel array output voltages. As seen, all the voltage follow the same curve. This is because the irradiance is the same for all the panel arrays. Again, the abrupt irradiance transient causes an abrupt voltage transient. However, the external control is capable to return the voltages the their reference point. Both irradiance transients present a similar response. It can be concluded that the external control for more than one stage works as good as the simulated for one single stage. It was an expected result, as the external control in any case depends on the number of stages.

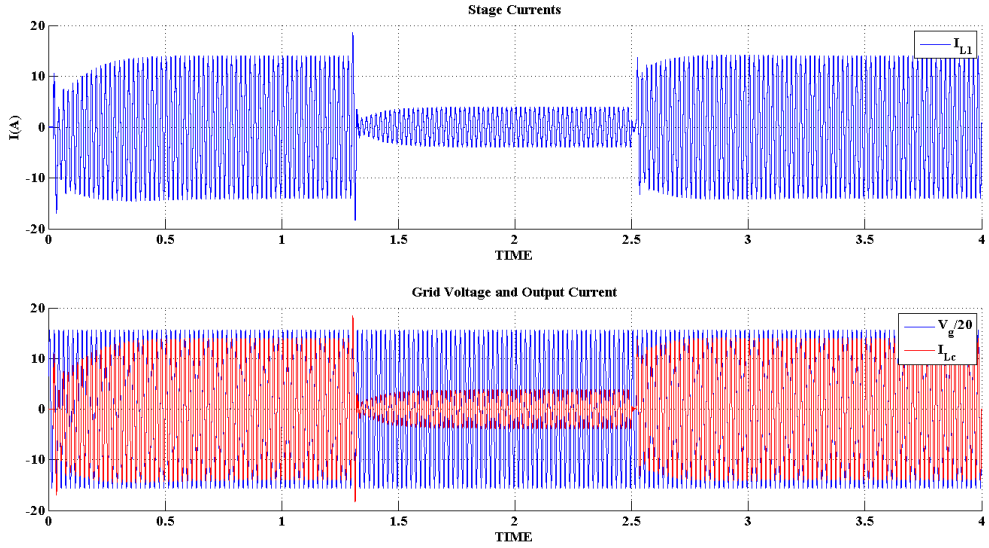


Figure 3.9: Currents and Grid Voltage

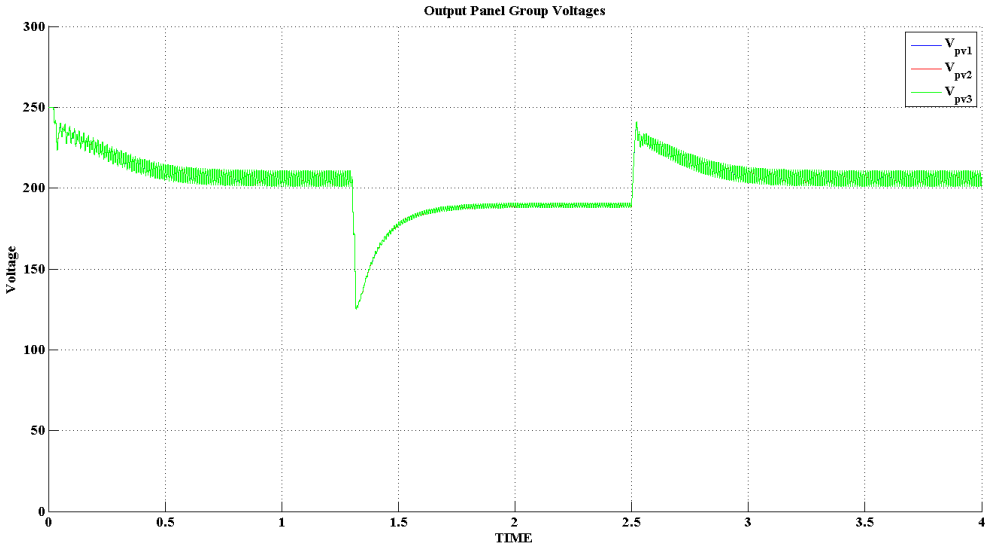


Figure 3.10: Panel Arrays Voltages

Simulation 3.2. MPPT Reference Abrupt Transient in Series Connected Inverter Topology

This simulation consists on testing the response of the system in front of an abrupt transient in the reference voltage provided by the MPPT. Table 3.3 shows the values of the plant and the transient performed. Different transient points are applied to different stages.

Figure 3.11 shows the currents and the grid voltage. As can be seen, the response of the system is smoother than in simulation 3.1. The stage current and the output injected current tend to a new value without abrupt transients. The injected current is always in phase with grid voltage, so it is following its reference without any problem.

$L_1 = 3.2mH$	$R_{L_1} = 100m\Omega$
$L_c = 80\mu H$	$R_{L_c} = 10m\Omega$
$C_c = 9\mu F$	$R_{C_c} = 8m\Omega$
$A_g = 311V$	Temp=25^oC
$f_{sw} = 40kHz$	Irradiance=$1000W/m^2$
Panel Array Voltages references. Stage 1:	
$210.232V$ $(1000W)$	$0\ s < t \leq 1.3\ s$
$242.424V$ $(500W)$	$1.3\ s < t \leq 2.5\ s$
$210.232V$ $(1000W)$	$2.5\ s < t$
Panel Array Voltages references. Stage 2:	
$210.232V$ $(1000W)$	$0\ s < t \leq 1.3\ s$
$245.992V$ $(300W)$	$1.3\ s < t \leq 2.5\ s$
$210.232V$ $(1000W)$	$2.5\ s < t$
Panel Array Voltages references. Stage 3:	
$210.232V$ $(1000W)$	$0\ s < t \leq 1.3\ s$
$247.456V$ $(200W)$	$1.3\ s < t \leq 2.5\ s$
$210.232V$ $(1000W)$	$2.5\ s < t$

Table 3.3: Values used in simulation 3.2

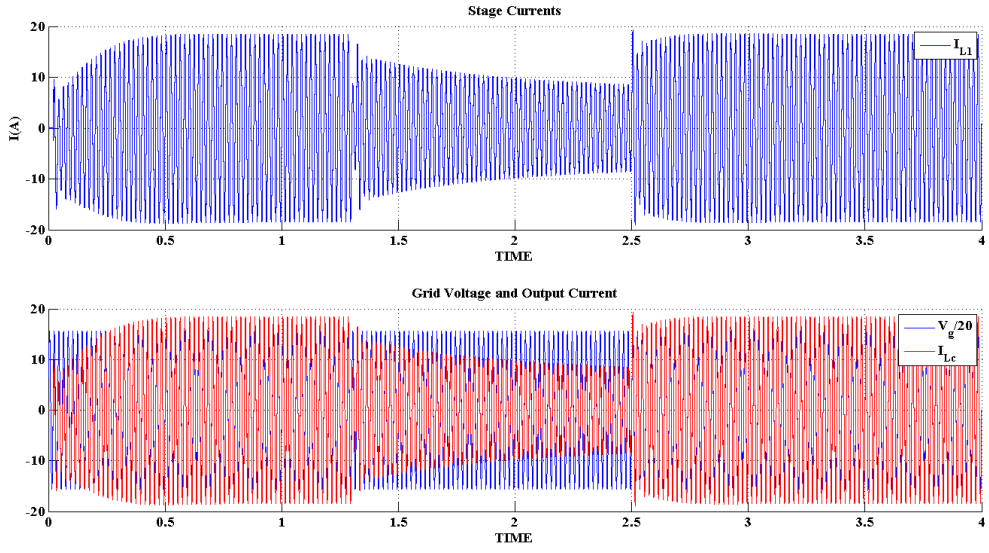


Figure 3.11: Currents and Grid Voltage

Figures 3.12 and 3.13 show the output voltages of each stage. They have a similar smooth transient, and each one tends to go to its reference point. It can be seen that all of them respond perfectly to its stage transient and can return to its original reference value without any problem.

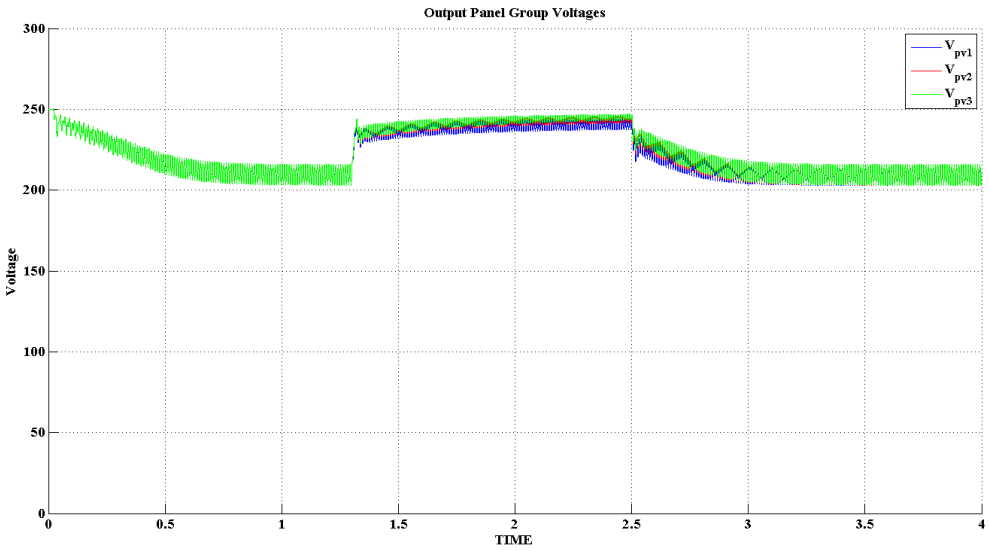


Figure 3.12: Panel Arrays Voltages

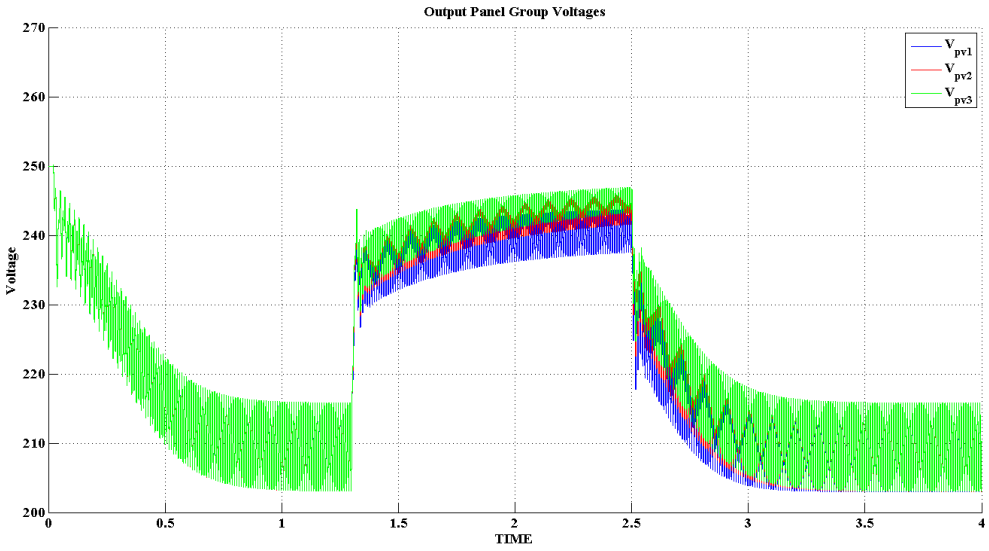


Figure 3.13: Panel Arrays Voltages. ZOOM

It can be concluded that the response to an abrupt reference voltage transient for this topology is smoother than the observed for the irradiance transient.

Simulation 3.3. MPPT Reference Tracking in Series Connected Inverter Topology

This simulation is in essence the same as the last one. It is performed to determine if the system is capable to respond properly to changes at the output voltage reference, like in simulation 3.2. These change will be smoother but with less time between them. Table 3.4 shows the values used to perform the simulation.

$L_1 = 3.2mH$	$R_{L_1} = 100m\Omega$
$L_c = 80\mu H$	$R_{L_c} = 10m\Omega$
$C_c = 9\mu F$	$R_{C_c} = 8m\Omega$
$A_g = 311V$	Temp=25^oC
$f_{sw} = 40kHz$	Irradiance=$1000W/m^2$
Panel Array Voltages references. All Stages:	
$210.232V$ $(1000W)$	$0\ s < t \leq 1.2\ s$
$235.72V$ $(750W)$	$1.2\ s < t \leq 1.8\ s$
$240.168V$ $(600W)$	$1.8\ s < t \leq 2.4\ s$
$242.424V$ $(500W)$	$2.4\ s < t \leq 3\ s$
$245.992V$ $(300W)$	$3\ s < t \leq 3.6\ s$
$247.456V$ $(200W)$	$3.6\ s < t$

Table 3.4: Values used in simulation 3.3

Figure 3.14 shows how the current follows its reference (the given by the external control) without problem and it is always in phase with the grid voltage. Any change is appreciated that deserves to be commented.

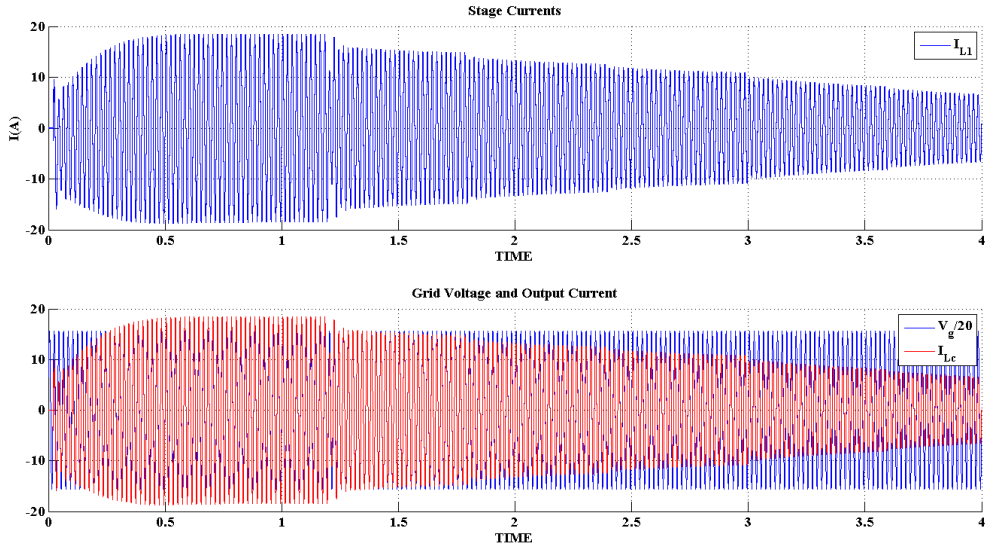


Figure 3.14: Currents and Grid Voltage

The output voltages also follow the reference given by the MPPT. Voltage abrupt transients are not appreciated in this simulation due to the smoother characteristic of the reference changes.

Having seen the simulations for this topology, it can be concluded that both external and internal controls are correctly developed and have a good response for different abrupt transients. Despite the internal control was developed for the central inverter control, it works good in a series inverter connected topology. The modulation strategy is, therefore, validated.

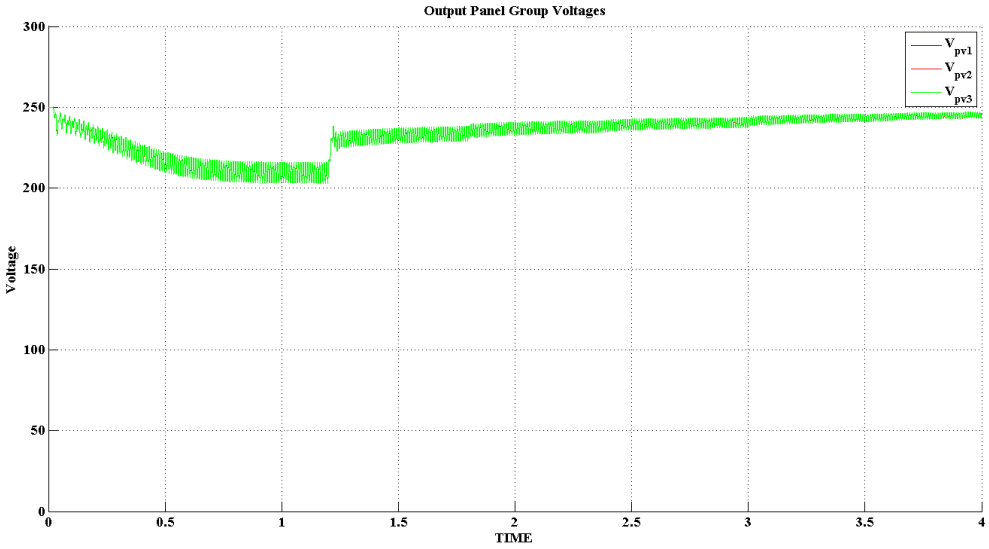


Figure 3.15: Panel Arrays Voltages

Chapter 4

Parallel Connected Inverters sharing LCL filter

One of the main objectives of this thesis is to design the control of 3 stages paralleled inverters. These inverters are not going to be connected to the grid separately, but, following the philosophy of the series connected inverters topology, they are going to share the LCL filter. This means that the output current will be the addition of all other currents, and they are going to be injected trough the same inductor. Figure 4.1 shows the scheme of the topology proposed.

Having seen the designed internal controls for the series connected inverters topology, and the central inverter topology, it can be thought that a similar internal control can be applied in this topology, and the objective is to implement a control which does not need more sensed variables than the series connected inverter topology. This means that apart from the external control for each stage, only the output injected current and the grid voltage can be sensed to implement the internal control. Not any stage current nor, if possible, the capacitor voltage (which has been sensed in the series and central connected inverter topologies for the use of the feed-forward, due to the instability caused by the LCL filter). Of course, the implementation of this control involves an investigation and, therefore, these premises can be modified or including not having into account if finally it is impossible to achieve this control.

As in the other topologies, the objective of the internal control will be to extract the power from the panels given by K_n factor of the external control of each stage, in order to fix the working point panel to guarantee the maximum power injection to the grid.

The parallel connected inverter topology can not be raised with one single inductor connected to the grid, as it would be the same as connecting multiple central inverters to the grid. Thus, the study begins directly from the LCL filter calculus. Moreover, as will be seen in next sections, the control will be completely rethought.

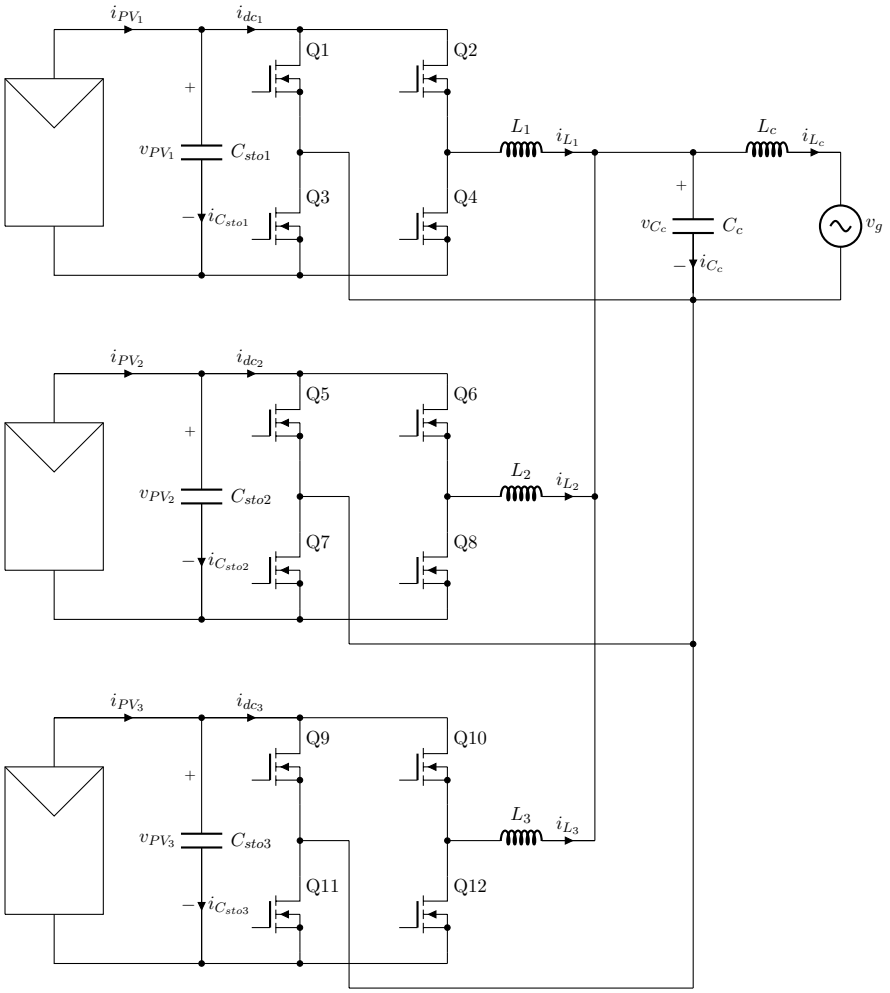


Figure 4.1: Schematic of parallel connected inverters topology

4.1 Multi-stage LCL filter calculus

For the parallel topology, there are two options to calculate the L_{ph} of the different phases.

The first option is to consider that the n outputs can guarantee the total power output each one. In that case, the LCL filter can be considered as a single LCL for each stage, and the calculation of the L_{ph} does not have to be changed from the exposed in section 2.4.1.

The other option is to consider that the maximum output power for each phase is the n division of the total output power (where n is the number of stages chosen). In this case, the values must be recalculated, but, as the total output power has not changed, the C_f and L_{out} values do not have to be recalculated, only the L_{ph} value must. So, dividing the power by n stages, it leads to.

$$\begin{aligned} I_{n\ max} &= \frac{\frac{P_{out}}{n}}{v_g}\sqrt{2} \\ \Delta I_n &= I_{n\ max}0.1 \\ L_n &= \frac{v_{PV}}{6 f_{sw} \Delta I_n} \end{aligned} \tag{4.1}$$

In this thesis $n = 3$, so, the calculus leads to

$$L_n \simeq 9.5mH \tag{4.2}$$

It is interesting to remark that as higher is the number of stages, higher is the value of L_n. That happens due to the relation dependence between the maximum value of output current and the percentage of ripple. Of course, there would be the option of not changing the ΔI_{ph} with respect to the single phase calculus; in that case, the percentage of ripple current with respect to the total current per phase, will not be accomplished.

However, the continuous volume increment of the stage inductors when additional stages are added is absolutely not desirable. If this happens, then the physical limit of the inductor, or the price of them, will limit the number of stages that can be used, and this is not acceptable in any case. To maintain the value of $3.2mH$ calculated for the central and series topologies, the usage of phase shifting techniques is proposed. Phase shift consists on shifting the carrier signals of the PWM of each stage. The phase value that these signals must be shifted will depend on the number of stages and is shown in equation 4.3.

$$ph_n = \frac{360}{n} \qquad \text{Where } n \text{ is the number of stages} \tag{4.3}$$

Implementing the phase shift, ripples of the different stages will be reduced when added. Note that, for the case when all the stages would be completely shadowed excepting one of them, the ripple will be the same as for the central inverter topology, but the output current will be divided by n. Therefore, the ripple will exceed the percentage in respect to the stage current. As the output current (i_{L_c}) ripple is the one important, I_{ripple} percentage can be reduced, what will lead to an increased value of the L_c inductance value. In this design, $I_{ripple} = 10\%$. Despite the smaller value of L_n can be compensated by increasing the value of L_c, it must be assumed a great current ripple in L_n.

4.2 External control for Parallel Connected Inverters Topology

For the case of paralleled inverters topology, the theoretical derivation of the external control coincides with the derivation shown for the series connected topology. The stages are considered as single ones, and their external control generate different and independent scalar factors K_n that are later treated in the internal control in order to generate the correct voltages in the transistor bridges. A better explanation is provided in section 3.3.1. The concept of the control is graphically shown in figure 4.2.

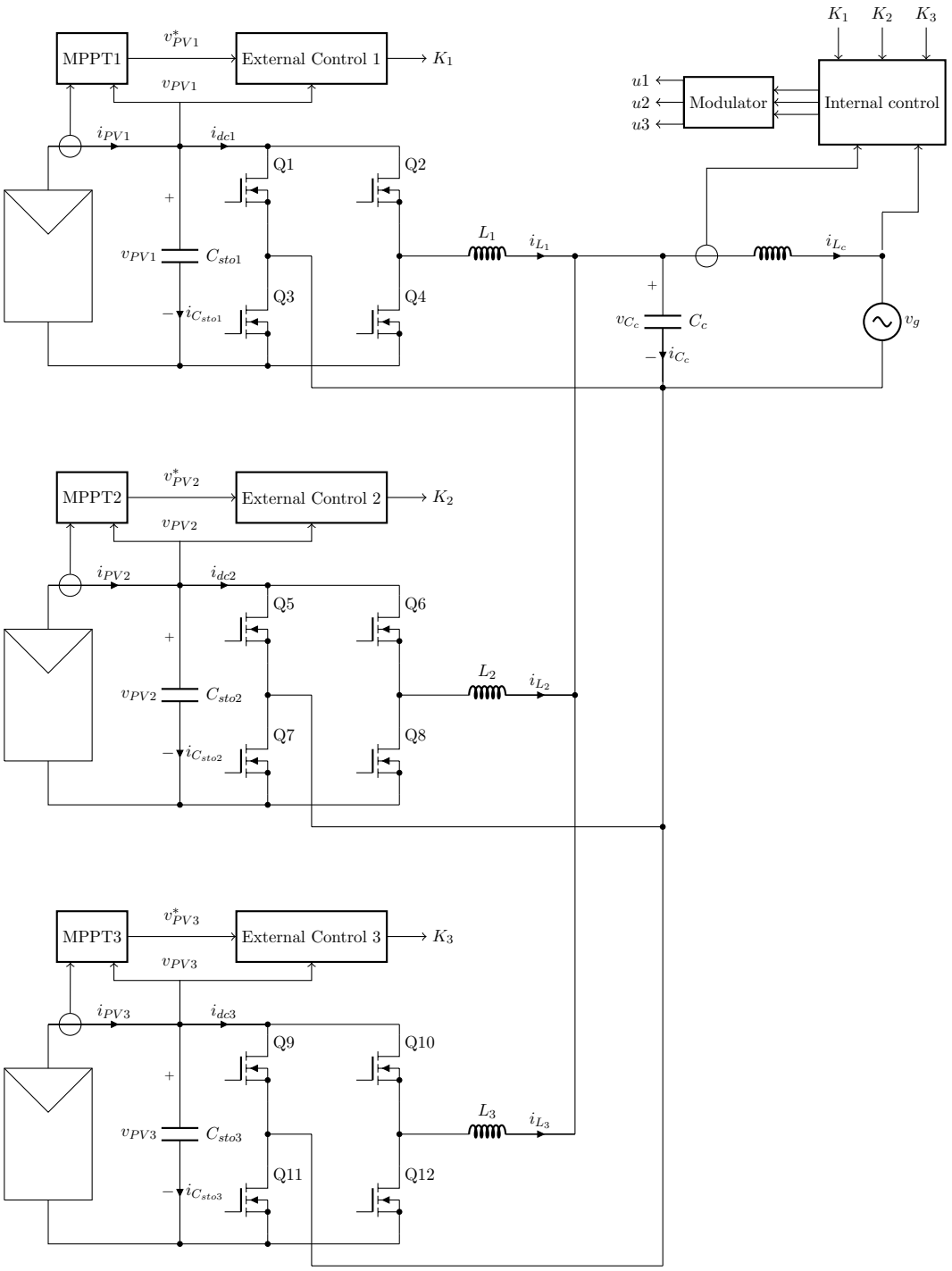


Figure 4.2: Schematic of parallel connected inverters topology with LCL filter and controls block diagram

4.3 Internal control for Parallel Connected Inverters Topology

Intuitively, the first idea of the internal control for this topology was using the same resonant control as in the central and series connected inverters topologies. However, this idea was left because of the complexity of the plant behaviour. Several approaches, that are not going to

be exposed here, were tested. However, any of them achieved satisfactory results. Therefore, the resonant control was considered a invalid control for this topology, and it was completely rethought.

The cause of this non proper behaviour was analysed. If the stages currents were continuous currents, the addition of them would lead to another continuous current, and that is all. However, for the case of sinusoidal currents, the addition of two or more sinusoids that are not in phase produce a sinusoid with a different phase from the phases of the added currents.

It can be understood if the currents are treated as vectors. One vector presents a module and an angle. If the currents are going to be treated as vectors (or phasors), the module will represent the amplitude and the angle will represent the phase of the current. It is important to have into account that, to add sinusoidal currents by this method, all the currents must be expressed as a sinusoidal relation, not as a cosine relation or vice versa (sine and cosine are the same wave with phase shift of $\pi/2$ and it must be reflected in the angle of the vector), and must have the same frequency.

The transform from sine to cosine can be made by using a simple trigonometric relation presented in equation 4.4.

$$\sin(x) = \cos(\frac{\pi}{2} + x) \tag{4.4}$$

Once the sinusoidal currents are correctly expressed as vectors, the addition can be made by another simple trigonometric operation.

$$A\angle\underline{\alpha} + B\angle\underline{\beta} = C\angle\underline{\gamma}$$

Where:

$$C = \sqrt{(A\cos(\alpha) + B\cos(\beta))^2 + (A\sin(\alpha) + B\sin(\beta))^2} \tag{4.5}$$

And:

$$\gamma = \arctan(\frac{A\sin(\alpha) + B\sin(\beta)}{A\cos(\alpha) + B\cos(\beta)})$$

The properties shown in equations 4.4 and 4.5 will be used onwards several times to deduce all the expressions of the system, and are not going to be explained again, the expressions will be solved directly.

As can be seen in equation 4.5, the phase of the resultant current from the addition of two sinusoidal currents depends both on the amplitude and the phase of the added currents. In the same way, the amplitude of the resultant current depends also on the same values, the amplitude and the phase of the added currents. This non linear relation was not contemplated by the internal control, and has lead this control to instability.

Moreover, the variable where the control is applied is the voltage generated in the transistor bridge of each stage. This means that the stages currents are not directly controllable and will depend on the phase and module of these voltages.

The next sections of this chapter are the result of an investigation to solve this problem, and is one of the most important parts of the present thesis.

4.4 Circuital analysis. The Nominal Duty Generator

The internal control proposed in this thesis is based on a circuital analysis and a nominal duty generator to guarantee that all the currents of each stage are in phase between them and have

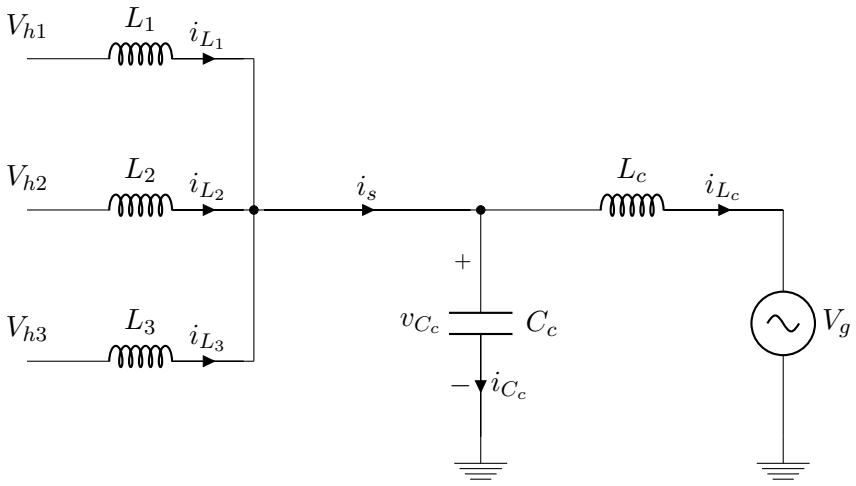


Figure 4.3: Simplified Ideal Circuital scheme of Parallel Connected Inverters Plant

not any offset. A proportional-integral controller, mixed with the nominal duty generator, guarantees that the injected current is in phase with the grid voltage.

The main conclusion deduced from section 4.3 is that there is a relation between the phase and the module of the voltages generated by each phase that proportional resonant control can not manage by itself. Finding the relation that allows to control the final value of the injected current by acting over the voltages of the transistor bridges is the objective of this section. Moreover, in order to avoid the circulation of energy between stages, or at least minimize it, a relation to put all the currents of each stage in phase must be found.

The method proposed to determine the values of the phase and module for the voltages is a circuital analysis of the system plant. In a way similar to what is done to determine the energy balance, the analysis must start from the known values, that is, from the voltage grid and the injected current (the hypothesis that it is in phase with the grid voltage must be still valid). From this circuital analysis, a nominal duty generator will be implemented and tested.

The calculus of this nominal duty generator will be divided into two parts. The first part is the circuital analysis of the common components of the topology, and will be called *common part*. These components are L_c and C_c. Figure 4.4 shows the components of the general schematic that will be involved in this calculus. The result of this part will be the variable i_s, which expresses the sum of the injected current and the capacitor current, and is also the sum of the currents of all the stages.

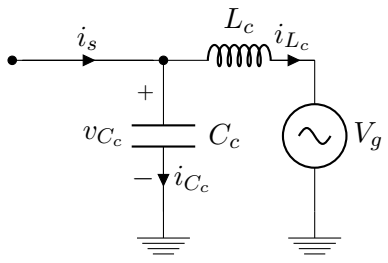


Figure 4.4: Elements that take part in Common part of circuital analysis

Before explaining what is the second part of the circuital analysis, the calculation of the common part is performed. Starting from initial known values:

$$v_g = A_g \sin(w_g t) \quad , \quad i_{L_c} = K A_g \sin(w_g t) = I_{L_c} \sin(w_g t) \tag{4.6}$$

$$\begin{aligned} v_{C_c} &= v_g + v_{L_c} = v_g + L_c \frac{di_{L_c}}{dt} \\ v_{C_c} &= A_g \sin(w_g t) + K A_g L_c w_g \cos(w_g t) \end{aligned} \tag{4.7}$$

Using the trigonometric property presented in equation 4.4, the expression of the voltage in the capacitor becomes:

$$v_{C_c} = A_g \sin(w_g t) + K A_g L_c w_g \sin(\frac{\pi}{2} + w_g t) \tag{4.8}$$

It can be considered that the grid voltage and the current injection have a null phase ($\varphi_g = 0$). So:

$$v_g = A_g \sin(w_g t + \varphi_g) \qquad i_{L_c} = K A_g \sin(w_g t + \varphi_g) \tag{4.9}$$

The derivative of the injected current shows a phase which is $\frac{\pi}{2}$. As exposed in equation 4.5, two vectors with different phase or angle, can be added using the phasor sum method.

$$v_{C_c} = v_g + L_c \frac{di_{L_c}}{dt} = A_c \sin(w_g t + \varphi_c)$$

Where:

$$A_c = \sqrt{A_g^2 + (A_g L_c K w_g)^2} \quad , \quad \varphi_c = \arctan(K w_g L_c) + \varphi_g \tag{4.10}$$

The current trough the capacitor can be deduced as:

$$i_{C_c} = C_c \frac{dv_{C_c}}{dt} = C_c A_c w_g \cos(w_g t)$$

Which can be expressed as:

$$i_{C_c} = I_{C_c} \sin(w_g t + \varphi_c + \frac{\pi}{2}) \tag{4.11}$$

The sum between the injected current and the capacitor current is the sum of the currents given by all the stages paralleled. This value will be called i_s.

$$i_s = I_s \sin(w_g t + \varphi_s)$$

Where:

$$I_s = \sqrt{(I_{C_c} \sin(\frac{\pi}{2} + \varphi_c) + I_{L_c} \sin(\varphi_g))^2 + (I_{C_c} \cos(\frac{\pi}{2} + \varphi_c) + I_{L_c} \cos(\varphi_g))^2}$$

$$\varphi_s = \arctan(\frac{I_{C_c} \sin(\frac{\pi}{2} + \varphi_c) + I_{L_c} \sin(\varphi_g)}{I_{C_c} \cos(\frac{\pi}{2} + \varphi_c) + I_{L_c} \cos(\varphi_g)}) \tag{4.12}$$

Being:

$$I_{C_c} = C_c w_g \sqrt{A_g^2 + (A_g L_c K w_g)^2} = A_g C_c w_g \sqrt{1 + (L_c K w_g)^2}$$

$$\varphi_c = \arctan(K w_g L_c) + \varphi_g$$

$$I_{L_c} = K A_g \quad , \quad \varphi_g = 0$$

The second part of the circuital analysis will be called the *modular part*. It will be called like that because it is a calculus that must be computed independently for each stage. This also means that this calculus allow a modular topology, so the number of stages can vary according to the needs of the final application. In this thesis $n = 3$ stages are used. Figure 4.5 presents the components that take part in the calculus.

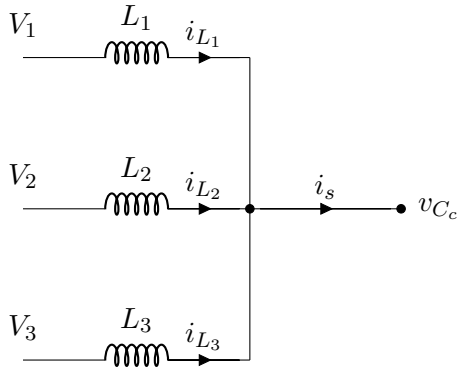


Figure 4.5: Elements that take part in Modular part of circuital analysis

As said before, the sum of the currents of each stage must be equal to the sum of the current injected and the current of the capacitor. But this does not necessarily mean that the currents of each stage are in phase between them. Therefore it will have to be imposed by the nominal duty generator. Another important point that must be remarked here, is that the module of the currents of each stage will be scaled by the factor K_n given by the external control of each stage. Therefore, the expression that defines the current of different stages is:

$$i_s = \sum_{n=1}^{n=i} i_{L_n} \qquad i_{L_n} = \frac{K_n}{K_t} i_s$$

Where: (4.13)

$$K_t = \sum_{n=1}^{n=i} K_n \quad \text{and} \quad i = 3 \quad \text{in this case}$$

This means that the currents of each stage will share the phase with the sum of i_{L_c} and i_{C_c}, but their module will be scaled by their K_n factor.

$$i_{L_n} = I_{L_n} \sin(w_g t + \varphi_s) \tag{4.14}$$

The voltage over the inductance of each stage is:

$$v_{L_n} = L_n \frac{di_{L_n}}{dt} = I_{L_n} L_n w_g \cos(w_g t + \varphi_s)$$

Which can be grouped as: (4.15)

$$v_{L_n} = A_{L_n} \sin(w_g t + \frac{\pi}{2} + \varphi_s)$$

Finally, the expression of the voltage which must be derived in the transistor bridge of each stage, and its phase, can be deduced:

$$v_n = v_{L_n} + v_{C_c} = A_n \sin(w_g t + \varphi_n)$$

Where:

$$A_n = \sqrt{(A_{L_n} \sin(\frac{\pi}{2} + \varphi_s) + A_c \sin(\varphi_c))^2 + (A_{L_n} \cos(\frac{\pi}{2} + \varphi_s) + A_c \cos(\varphi_c))^2}$$

$$\varphi_n = \arctan(\frac{A_{L_n} \sin(\frac{\pi}{2} + \varphi_s) + A_c \sin(\varphi_c)}{A_{L_n} \cos(\frac{\pi}{2} + \varphi_s) + A_c \cos(\varphi_c)}) \tag{4.16}$$

Being:

$$A_{L_n} = \frac{K_n}{K_T} L_n w_g I_s$$

$$A_c = A_g \sqrt{1 + (L_c w_g K)^2}$$

$$\varphi_c = \arctan(K w_g L_c) + \varphi_g$$

And I_s and φ_s are given by equation 4.12.

The calculation leads to one single result for each stage voltage, and one single result for the phase of each stage.

Simulation 4.1. Ideal Nominal Duty Generator over an Ideal Plant

This simulation is done to validate the behaviour of the circuital analysis. It has been performed with ideal power supplies, just generating the correct voltage values and the correct phases for these voltages. The values of the scalar factors K_n are not provided by the external control, but are fixed to test the system under different conditions for each stage. The value K_n is basically simulating different irradiances.

$K_1 = 0.1$	$R_{L_1} = 0\Omega$
$K_2 = 0.2$	$R_{L_2} = 0\Omega$
$K_3 = 0.05$	$R_{L_3} = 0\Omega$
$L_1 = 3.2mH$	$L_c = 80uH$
$L_2 = 3.2mH$	$R_{L_c} = 0\Omega$
$L_3 = 3.2mH$	$C_c = 9\mu F$
$A_g = 311V$	$R_{C_c} = 0\Omega$
Temp=25^oC	

Table 4.1: Values used in simulation 4.1

Figures 4.6 and 4.7 show how the calculations performed are correct since the currents are in phase between them, and the injected current is in phase with the grid voltage. However, a great ripple is appreciated in the output injected current, which was not expected by the calculations.

If the stages inductors of the LCL filter are considered as a current source, then, the transfer function between the output current i_{L_c} and input currents i_{L_n} presents a conjugated complex pole at frequency exposed in equation 4.17.

$$\frac{i_{L_c}(s)}{i_{L_n}(s)} = \frac{1}{L_c C_c s^2 + 1} \quad , \quad s = \pm j \frac{1}{\sqrt{L_c C_c}} \tag{4.17}$$

Therefore, for any excitation signal, the response will oscillate, as it is in the simulation. In next simulations the presence of the losses will attenuate this effect, but however, it should be studied in the future.

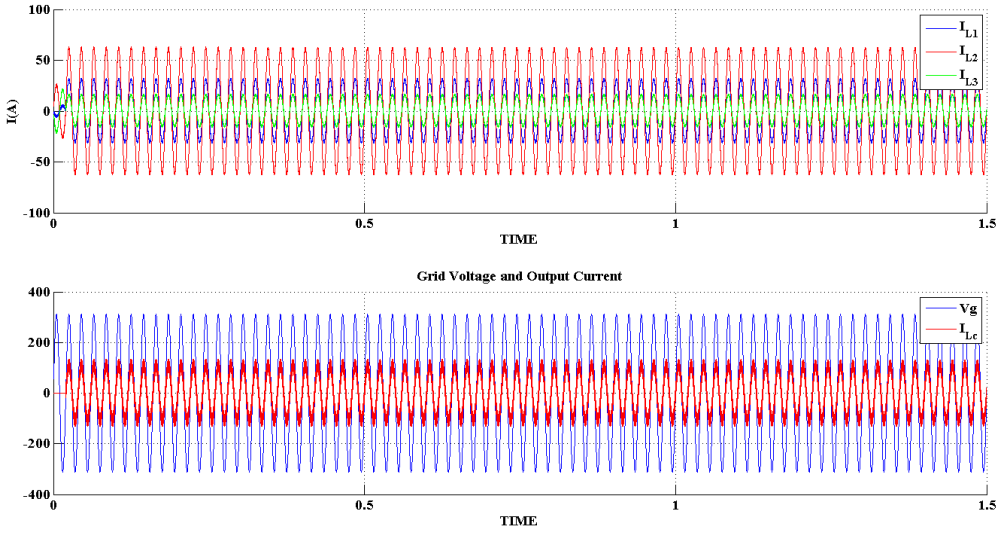


Figure 4.6: Currents and Grid Voltage

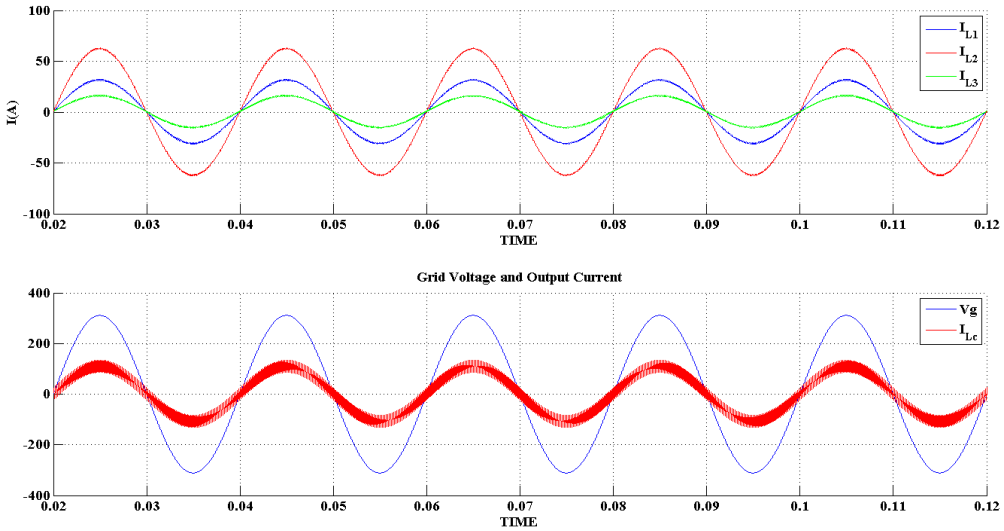


Figure 4.7: Currents and Grid Voltage. ZOOM

Anyhow, the model is validated, and therefore must be tested with some non ideal conditions, what is going to be done in next simulations.

Simulation 4.2. Ideal Nominal Duty Generator over Real Plant

In this simulation, the nominal duty generator is tested into a realistic plant. As known, the ideal generator performs the calculus of the circuital analysis without having into account the losses of the system. This time, it is going to be tested over a plant which presents losses. Table 4.2 shows the values of different elements in this plant. The values fo the losses will be used onwards, only with slight changes when the tolerances will be considered. The values of these losses have been chosen to be similar to what can be found in a commercial element of these characteristics. The capacitor is supposed to be a MKP capacitor with little ESR.

Irradiance Stage 1 = $1000W/m^2$	$R_{L_1} = 100m\Omega$
Irradiance Stage 2 = $523.34W/m^2$	$R_{L_2} = 100m\Omega$
Irradiance Stage 3 = $117.2482W/m^2$	$R_{L_3} = 100m\Omega$
Panel Array 1 Output voltage reference = $630.7V$	$L_c = 80\mu H$
Panel Array 2 Output voltage reference = $604.3V$	$R_{L_c} = 10m\Omega$
Panel Array 3 Output voltage reference = $543.5V$	$C_c = 9\mu F$
$L_1 = 3.2mH$	$R_{C_c} = 8m\Omega$
$L_2 = 3.2mH$	Temp=25^oC
$L_3 = 3.2mH$	$A_g = 311V$

Table 4.2: Values used in simulation 4.2

Figures 4.8 and 4.9 show the behaviour of the currents of each stage and the injected current, compared with the grid voltage. The currents of each stage are almost in phase between them. The little difference between their phases have not a critical value. This means that the reactive power circulating through the stages will tend to be very small, and this leads to a first conclusion. The application of realistic losses to the plant do not cause a significant phase difference between stages currents, and it leads to a phase difference between the grid voltage and the injected current that can be considered acceptable in some applications. Indeed, with PSIM simulator, power factor can be evaluated and, in this case, the value is 0.992, which is very close to the desired value, 1.

Figure 4.10 shows the evolution of scalar factors and the panel array output voltage of each stage. As can be seen, the voltages get a stable value over its reference values, provided by MPPT. The scalar factors also get stabilised onto their own value. This means that the external control works properly. The internal control does not lead the external control, so the, focusing on these aspects, the behaviour of the system is correct. In conclusion, if the losses are not considered, the voltage grid and the injected current will never be in phase. This is a normal result, as the generator implemented is just a circuital analysis, and any current is really controlled, but predicted without having theses losses into account.

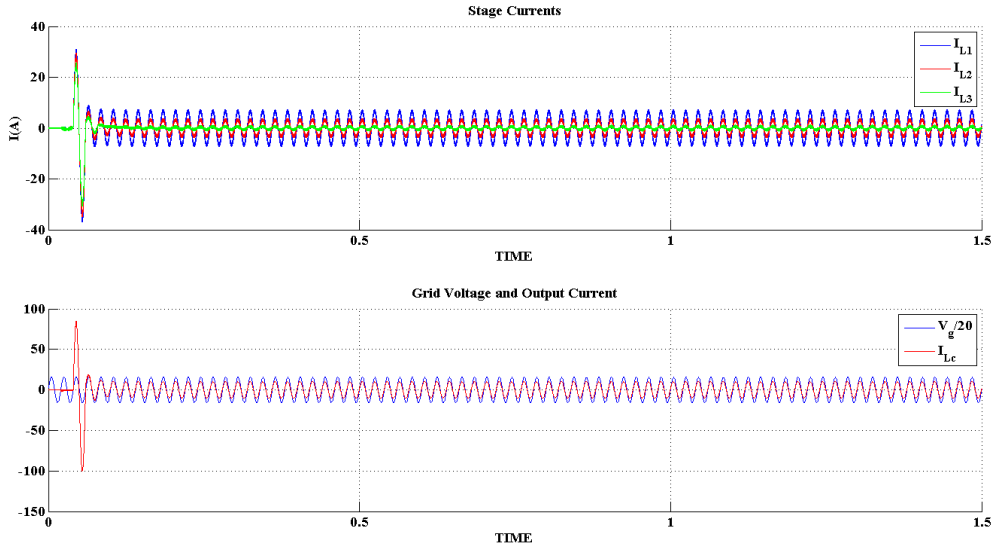


Figure 4.8: Currents and Grid Voltage

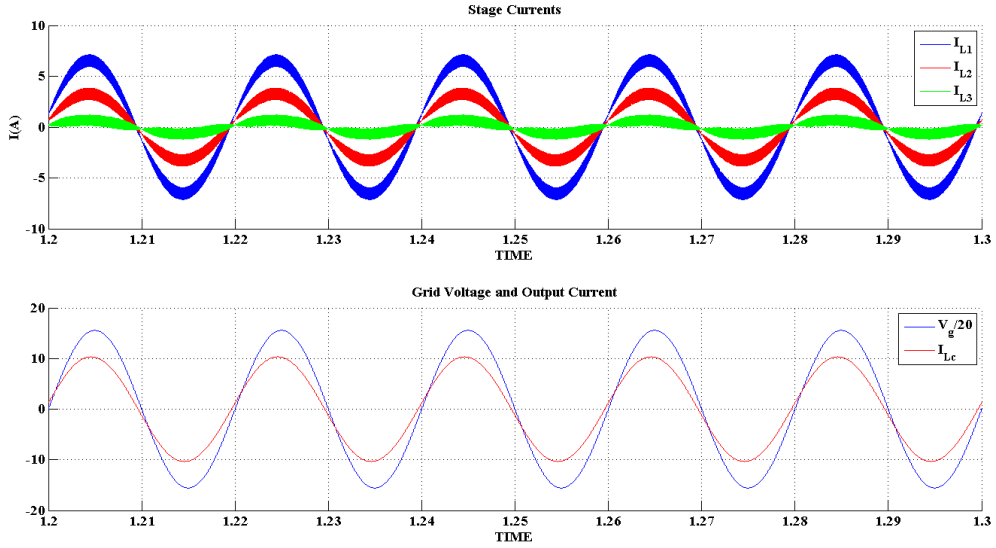


Figure 4.9: Currents and Grid Voltage. ZOOM

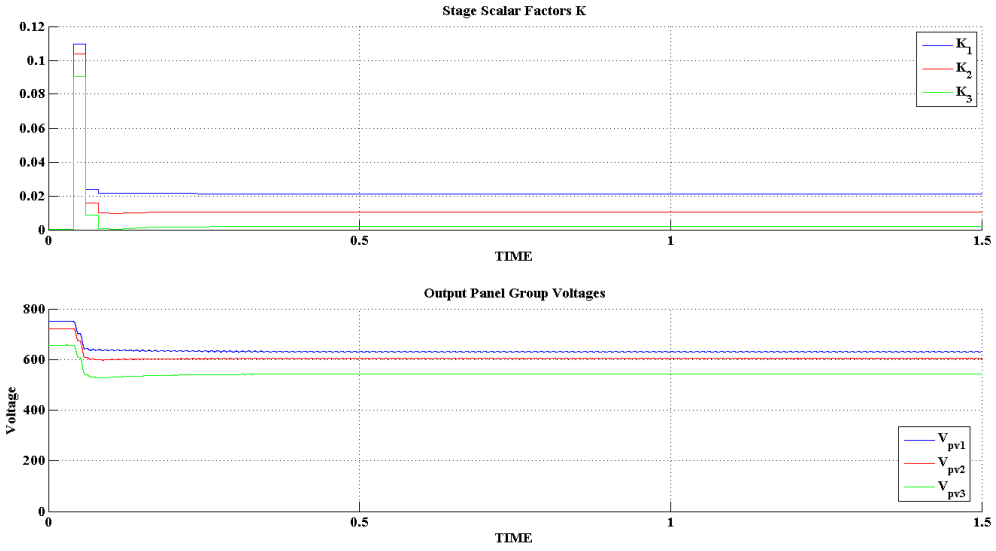


Figure 4.10: Scalar Factor values for each stage and Panel Array Output Voltages

Simulation 4.3. Ideal Nominal Duty Generator over Real Plant and Grid Voltage Unbalanced

This simulation has been performed in order to test the effect of an incorrect sensing of grid voltage over the system. The amplitude value of grid voltage is used in the circuital analysis. Despite the grid voltage is continuously sensed and can be corrected each period, it is necessary to test how it can affect the system. The conditions of the present simulation are the same as exposed in simulation 4.2, but changing the real value of grid voltage from the one used in the circuital calculus. Table 4.3 exposes these values.

Irradiance Stage 1 = $1000W/m^2$	$R_{L_1} = 100m\Omega$
Irradiance Stage 2 = $523.34W/m^2$	$R_{L_2} = 100m\Omega$
Irradiance Stage 3 = $117.2482W/m^2$	$R_{L_3} = 100m\Omega$
Panel Array 1 Output voltage reference = $630.7V$	$L_c = 80\mu H$
Panel Array 2 Output voltage reference = $604.3V$	$R_{L_c} = 10m\Omega$
Panel Array 3 Output voltage reference = $543.5V$	$C_c = 9\mu F$
$L_1 = 3.2mH$	$R_{C_c} = 8m\Omega$
$L_2 = 3.2mH$	Temp=25^oC
$L_3 = 3.2mH$	$A_g = 315V$

Table 4.3: Values used in simulation 4.3

The results of this simulation are exposed in figures 4.11 and 4.12. The whole evolution of the currents has been ignored this time. The main issue here is the phase difference between the stages currents, and on the other side the phase difference between the grid voltage and the injected current. As can be seen, currents have a higher amplitude than the presented in simulation 4.2. However, in figure 4.12 the voltages are stabilised at the point where they are supposed to be. Therefore, the question is: how can the panels work at their reference point if the currents extracted form the panels are so higher than they are supposed to be?. The answer is that the currents are not in phase, so the energy is flowing between the stages, and the capacitors placed at the output of the panel arrays are continuously charged and discharged by the energy of other stages. Moreover, as the grid voltage and the injected current are not in phase between them, all the stages are also sharing reactive energy with the grid. However, despite all these mismatches, the external control is capable to lead the system to a stable position, confirming that it is a robust control. The power factor of the injected current and the grid voltage is 0.645, which is a totally unacceptable value, as means that there is a great amount of reactive power (35.5% of the total)

This great amount of useless energy flowing through the stages and the grid, will cause for sure a poor efficiency of the system, as the conduction losses will increase significantly. It must be remarked that this poor response of the system has taken place just with a $3V$ difference in the voltage sensing. Thus, it can be concluded that the effect that this parameter have over the behaviour of the system is much more significant than the losses had. Therefore, an accurate voltage sensing is necessary. Otherwise, some kind of control must be implemented to put the currents at their proper phase.

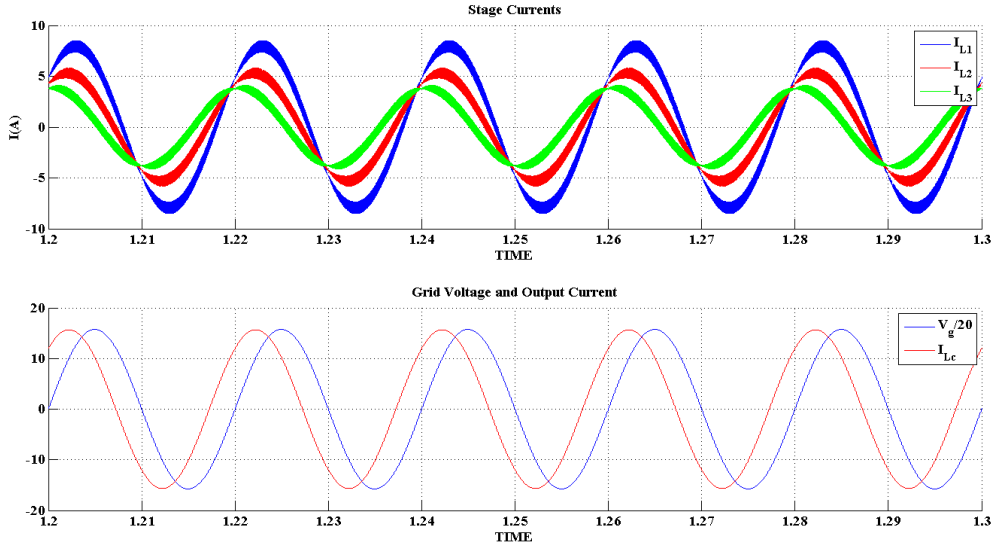


Figure 4.11: Currents and Grid Voltage

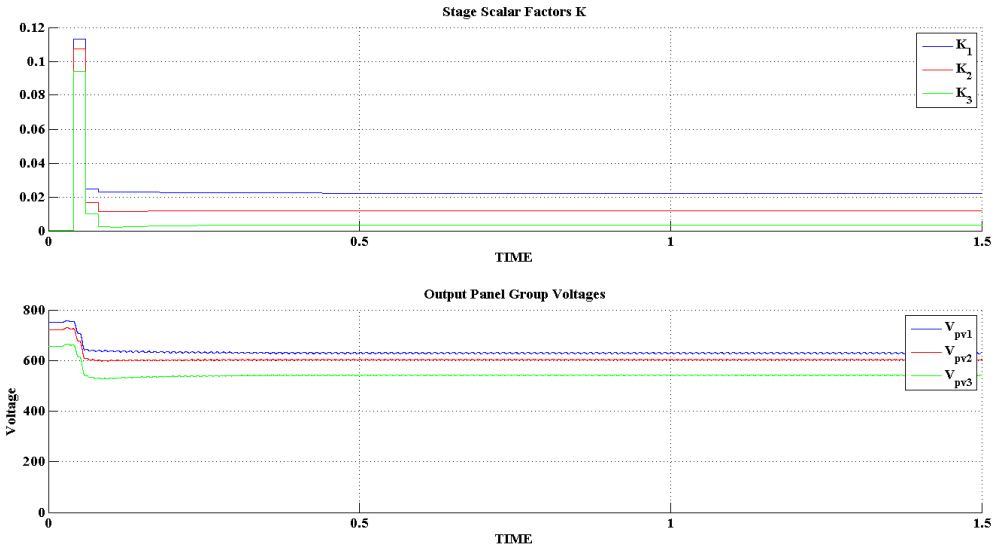


Figure 4.12: Scalar Factor values for each stage and Panel Array Output Voltages

4.5 The Phase Control

The objective of this section is to explain the proposed control to put in phase the injected current and the grid voltage in a realistic system (with losses and unbalanced component values).

One of the advantages of the proposed circuital analysis in section 4.4 is the capability of modifying any of the internal calculated variables as wanted. The control takes advantage of this and is based on modifying the phase of the addition of the injected current and the capacitor current (φ_s). Figure 4.13 shows the block diagram of this control. As explained in section 4.4 the output of the common part of the circuital analysis (common part) are the amplitude (I_s) and the phase (φ_g) of the sum of stage currents. It corresponds to the output of equation 4.12.

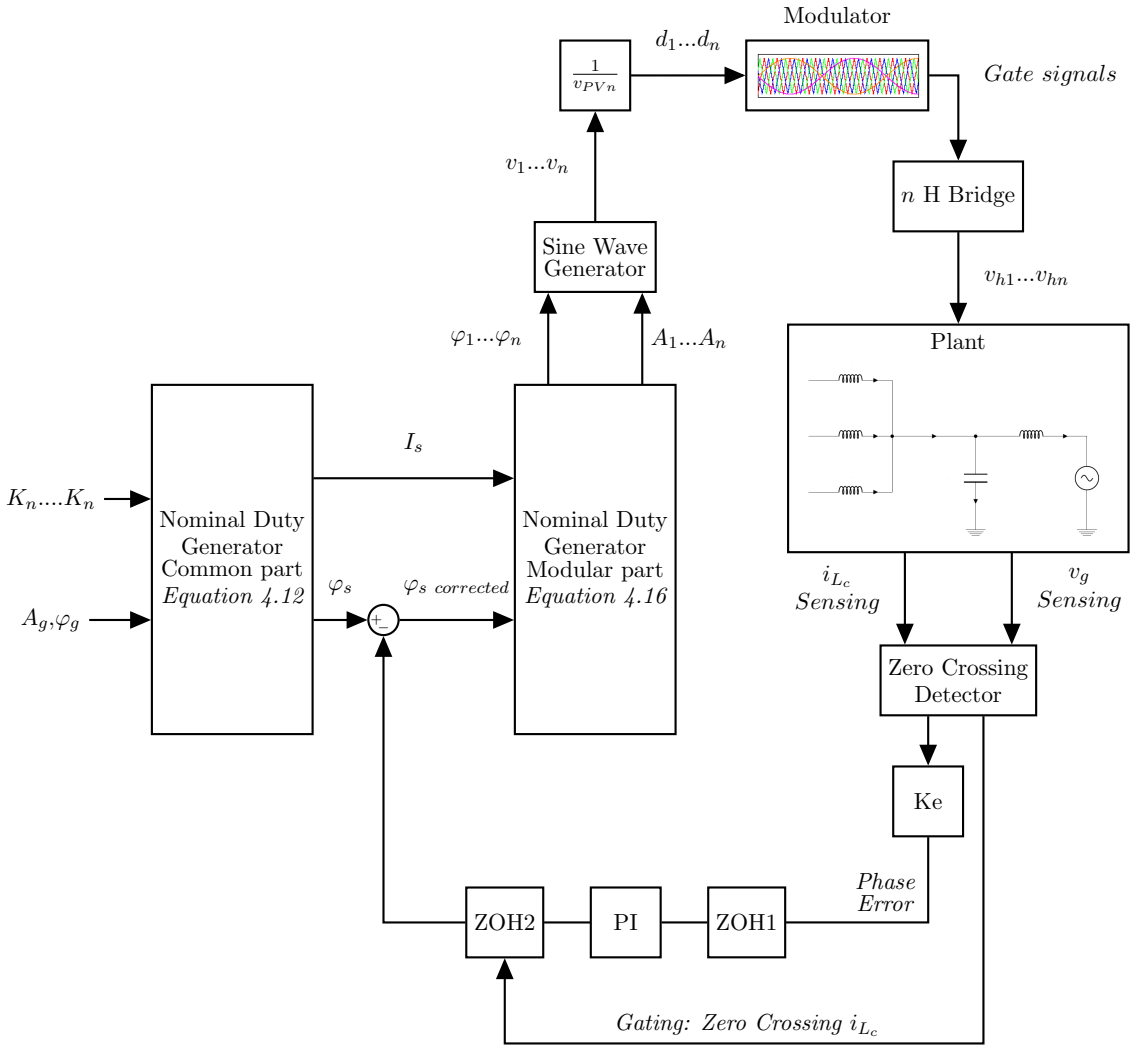


Figure 4.13: Block diagram of internal control for parallel topology

At this point, a correction to the phase is applied, and therefore, the modular part of the circuital analysis of the nominal duty generator is modified. The output of this second part corresponds to the result of equation 4.16. If the control is properly implemented, then these outputs (A_n and φ_n) will be correctly modified in order to put the injected current and the grid voltage in phase.

After this block, the sine-wave generator generates a sinusoid of A_n apmplitude and φ_n phase. The amplitude is divided with the V_{PV} voltage of the corresponding stage, so the output waveform is the modulation signal of the PWM converter, which is injected to the half-bridge transistors.

4.5.1 The Error Detector

The error detector must be a delay detector between the output current and voltage signals, and must determine if the phase of the current is advanced or delayed in reference to the grid voltage. Figure 4.14 illustrates two delayed signals, and the time delay between them, this is the time that must be sensed. The are different methods to determine the time delay between two

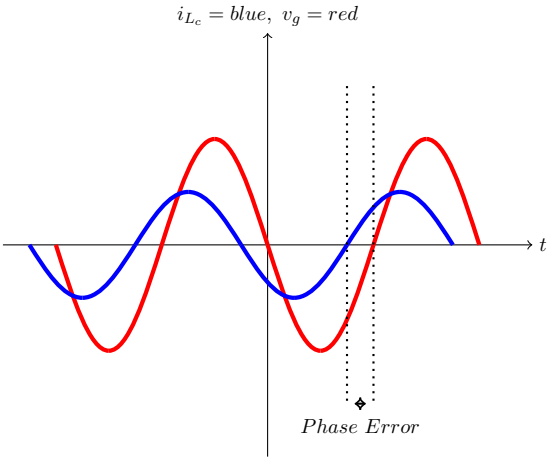


Figure 4.14: The error signal

signals. Some microprocessors have specific peripheral circuits to do it. In other cases methods based on phase locked loop are used. For the case of this thesis, a PSIM sub-circuit has been used. This sub-circuit is based on a C language block, that have two inputs and one output. The inputs are the injected current and grid voltage. The single output can present the outputs exposed in equation 4.18.

$$\begin{aligned} &1 \text{ during the time that current is positive and voltage is negative} \\ &0 \text{ during the time where both signals are equal} \\ &-1 \text{ during the time that current is negative and voltage is positive} \end{aligned} \tag{4.18}$$

The input signals are only evaluated for the rising edge in the zero crossing moment. If the current is advanced with respect to the grid voltage the output of the C block will be 1 during the time that signals of the waveforms are different, if it is delayed with respect to the grid voltage, then the output will be -1 during the time that signals of the waveforms are different. Output will be 0 when the waveforms have the same signal. At the output of this C block a simple resetable integrator is put in order to integrate the time. If the integrator presents a gain, the output will be be a signal proportional to the time delay, if not, the output will be exactly the time delay. This error detector has been implemented in PSIM, and the scheme is presented in figure 4.15

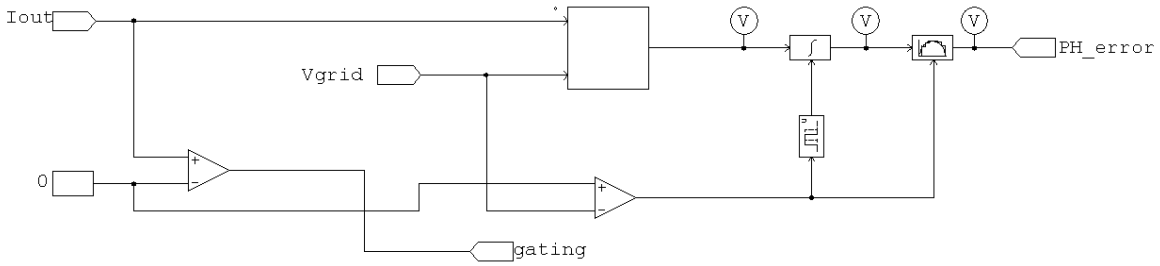


Figure 4.15: Phase error detection circuit

The code of C block is very simple and it is provided in figure 4.16. The error by itself has a

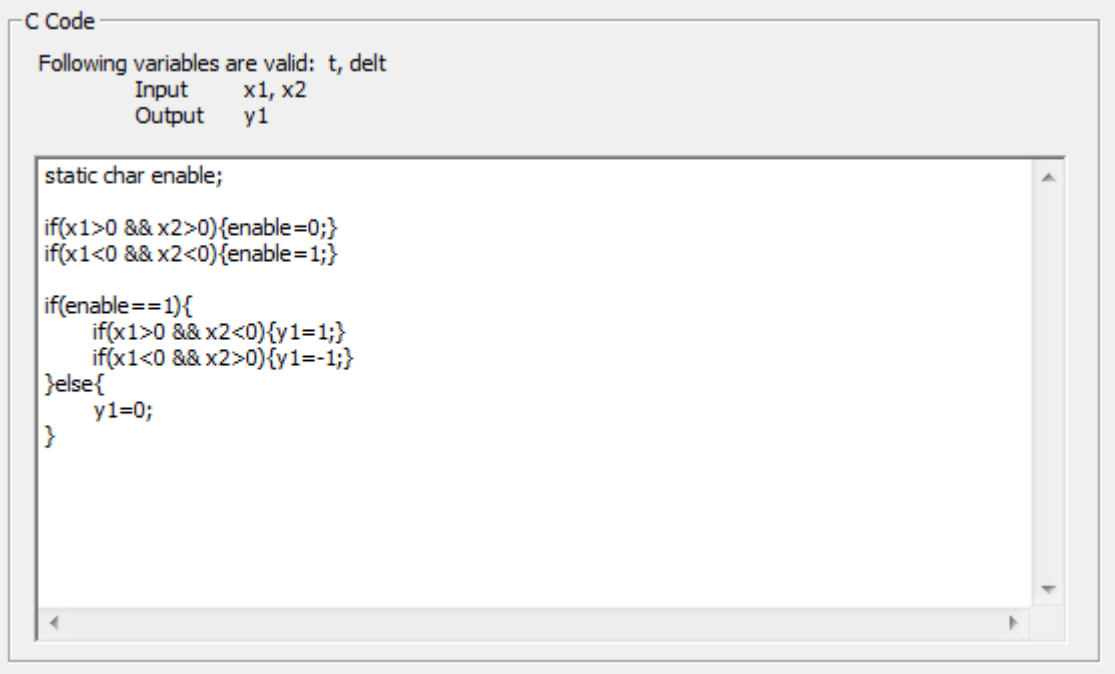


Figure 4.16: C Block Code

little value, and needs a proportional gain that can be applied in the control constants (α and γ) or directly to the output of the error (K_e). In this thesis, the chosen gain of the integrator is $K_e = 1000$. A ZOH (Zero Order Hold) is put after this integrator in order to sense the error each grid period. This corresponds to the ZOH1 in figure 4.13

4.5.2 The digital PI. Controlling the Phase

The control proposed is a simple digital PI controller. It must be digital because the error is only sensed each grid period. Having as reference the figure 4.13, ZOH1 is in charge of sensing this error at the grid frequency, $50Hz$ in this case.

The digital filter has been adjusted manually, without the mathematical expression. Equation 4.19 is the expression of the digital filter. It is the same as used for the external control.

$$G_c(s) = \gamma \frac{z - \alpha}{z - 1} \tag{4.19}$$

The values of γ and α should be chosen by the Jury criteria, but to do this, the expression of $\frac{\varphi_{i_{L_c}}}{\varphi_s}$ should be found. In this thesis the control has not been deepened enough to find this expression, and therefore, the control has been adjusted manually, by testing simulations until achieving a satisfactory response of the system. The values for the filter parameters are presented in table 4.4.

$K_e = 1000$ $\alpha = -1.000350061$ $\gamma = 0.0199965$

Table 4.4: Values for digital filter parameters and output error gain

4.5.3 Applying the Phase Correction

The output of the filter is not immediately applied to the calculated value of φ_s. As said in section 4.4, a change in this phase leads to different values of phase and amplitude of the voltage induced in the transistor bridge. The change in the voltage is a delta which goes from one value to another, this change happens in a period of $50Hz$. If the change in the voltage is applied when the current is not zero (for example in peak of the waveform), the current cannot follow the voltage change immediately, as they are related through an inductor. If this happens, the currents of the inductors do not follow the circuital analysis results, so the calculus is no longer valid. In that case, the control becomes unstable and the phase quadrature cannot be achieved.

Another point of view to understand this effect is just thinking that the current in a inductor is the result of integrating its voltage as shown in equation 4.20.

$$i_L = \frac{1}{L} \int v_L dt \tag{4.20}$$

If the initial conditions of the integrations are not 0, then the current will not follow the sinusoidal shape of the voltage, and that is what happens if the changes are applied when the current is not 0.

For that reason, the changes must be applied at the zero crossing point of the current. The zero crossing detector used to sense the phase error is profited to generate the signal called *gating*, and this is the signal that activates ,by edge, the ZOH2, which applies the correction to the phase. Therefore it can be concluded that ZOH2 is an asynchronous zero order hold.

Simulation 4.4. Ideal Nominal Duty Generator with Phase Control over Real Plant

This simulation is performed to test the behaviour of the phase control, in junction with the circuital analysis proposed in this thesis. The plant that will be applied is a real plant, with losses, but without tolerances in the values of these losses and the components. The grid voltage is supposed to be sensed ideally here, so in this simulation the behaviour of the control will be tested only under losses condition. Table 4.5 shows the values applied to the plant.

The control is in charge of putting the injected current in phase with the grid voltage. Figure 4.17 shows the current waveforms at the start-up time. At this moment, the injected current presents a little offset due to the transitory discharge of the output panel capacitors, and is not in phase with the grid voltage. As seen in figure 4.9 from simulation 4.2, these two signals never get the same phase. However, applying the phase control, they are finally in phase, as figure 4.18 exposes. It can also be seen that the stages currents are close to be in phase between them. With the control proposed, this currents will never be in phase, as they are not directly controlled, but, thanks to the nominal duty generator, this error is minimized and the system can operate close to the ideal behaviour.

Irradiance Stage 1 $= 1000W/m^2$	$R_{L_1} = 100m\Omega$
Irradiance Stage 2 $= 523.34W/m^2$	$R_{L_2} = 100m\Omega$
Irradiance Stage 3 $= 117.2482W/m^2$	$R_{L_3} = 100m\Omega$
Panel Array 1 Output voltage reference $= 630.7V$	$L_c = 80\mu H$
Panel Array 2 Output voltage reference $= 604.3V$	$R_{L_c} = 10m\Omega$
Panel Array 3 Output voltage reference $= 543.5V$	$C_c = 9\mu F$
$L_1 = 3.2mH$	$R_{C_c} = 8m\Omega$
$L_2 = 3.2mH$	Temp=25^oC
$L_3 = 3.2mH$	$A_g = 311V$

Table 4.5: Values used in simulation 4.4

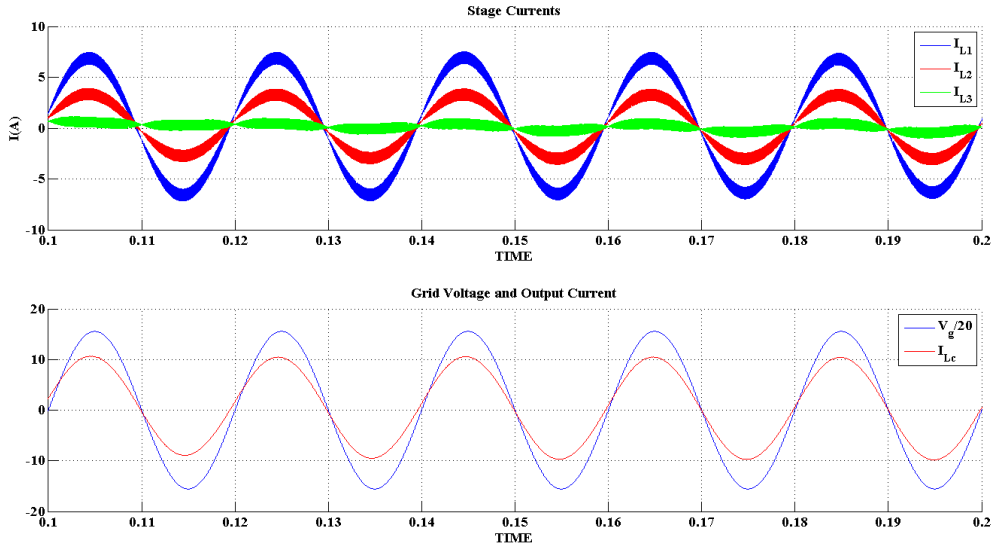


Figure 4.17: Currents and Grid Voltage. ZOOM at initial time

Figure 4.19 shows the modulation signal of stage 1, and the control action. This value is what is added to the φ_s, which is one of the outputs of the common part of the circuital analysis. The value of this phase correction stabilises over a value in, approximately one second. It is important to remark that, differently from the proportional resonant control applied to central and series connected inverters, here the control is much more slow, as it is not capable to correct the phase of the current in less than one grid period. This was an expected response, as the error can only be read each grid period. Thus, it must be assumed that, with the proposed control, reactive power is generated during, approximately, the first second after the start-up. Moreover, offset in the injected current must be assumed during this time, this is perhaps the worst characteristic of the control proposed, because an imbalance of the neutral can cause serious problems to the grid.

As the amplitude of the currents keeps uncontrolled, and only depends on the circuital calculus, the external control is in charge of put the system at its reference point. Once more, the external control is capable to do it, and the scalar factors and panel arrays voltages get an stable value before approximately $0.5s$. Figure 4.20 shows the whole evolution of these two parameters.

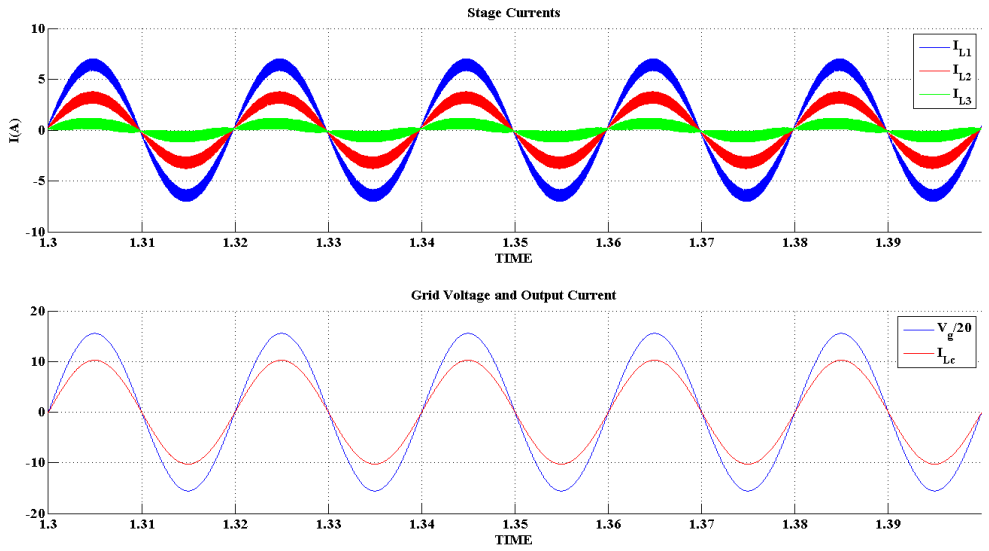


Figure 4.18: Currents and Grid Voltage. ZOOM at final time

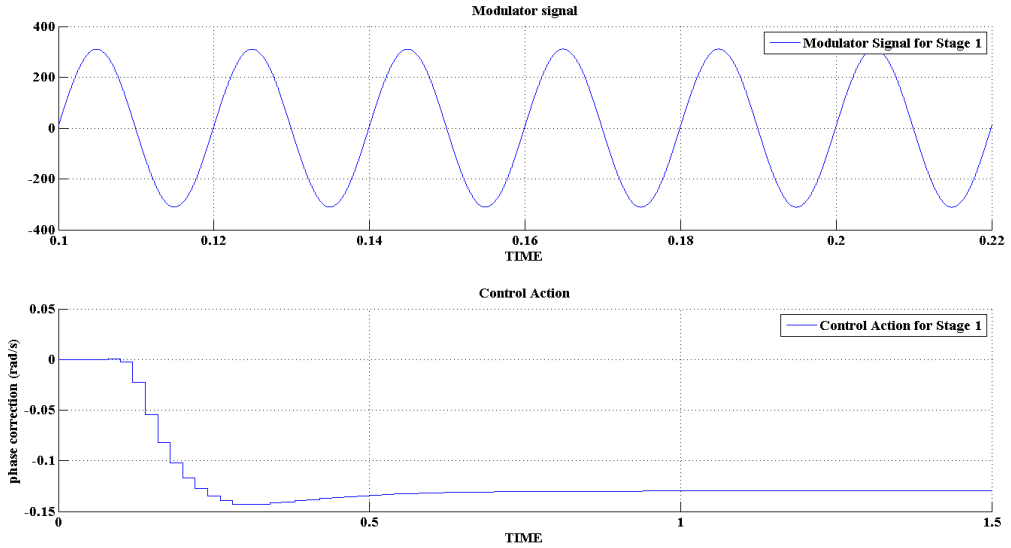


Figure 4.19: Modulation signal for Stage 1 and Control Action

Finally, it can be concluded that the control proposed has an acceptable response over a real plant with losses, after approximately 1 second, which is the settling time of the system.

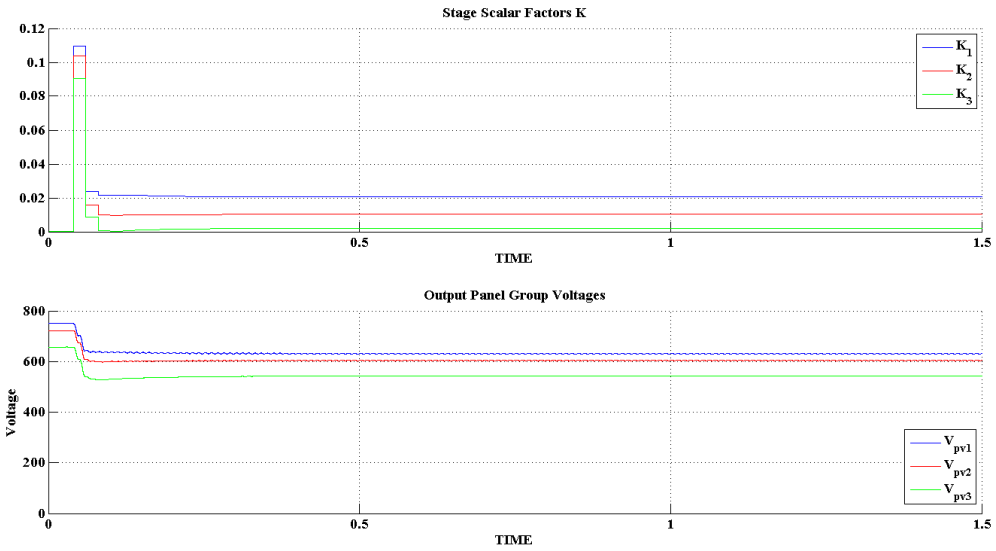


Figure 4.20: Scalar Factor values for each stage and Panel Array Output Voltages

Simulation 4.5. Ideal Nominal Duty Generator with Phase Control over Real Plant and and Grid Voltage unbalanced

Following the steps that were followed for the simulations of the system without any control, this simulation analyses the behaviour of the control over a plant real plant and the voltage grid incorrectly sensed. Table 4.6 shows the values used for the simulation.

Irradiance Stage 1 $= 1000W/m^2$	$R_{L_1} = 100m\Omega$
Irradiance Stage 2 $= 523.34W/m^2$	$R_{L_2} = 100m\Omega$
Irradiance Stage 3 $= 117.2482W/m^2$	$R_{L_3} = 100m\Omega$
Panel Array 1 Output voltage reference $= 630.7V$	$L_c = 80\mu H$
Panel Array 2 Output voltage reference $= 604.3V$	$R_{L_c} = 10m\Omega$
Panel Array 3 Output voltage reference $= 543.5V$	$C_c = 9\mu F$
$L_1 = 3.2mH$	$R_{C_c} = 8m\Omega$
$L_2 = 3.2mH$	Temp$=25^oC$
$L_3 = 3.2mH$	$A_g = 315V$

Table 4.6: Values used in simulation 4.5

Figure 4.21 shows the currents at start-up time. Here this time is longer than it was in previous simulations. As can be seen, during this time, currents of the stages and the injected current present a little offset, which, as commented, is highly undesired. Moreover, the currents of the stages are not in phase between them. The injected current and the grid voltage are also not in phase, and, therefore, there is reactive power circulating through the phases and through the grid and the inverter. Due to the control action, the power factor is constantly changing, but a mean of its value during the time that the simulation shows can be evaluated, and the result is a power factor of 0.86.

Figure 4.22 shows that at 1.4 seconds, the injected current has not any offset and is completely

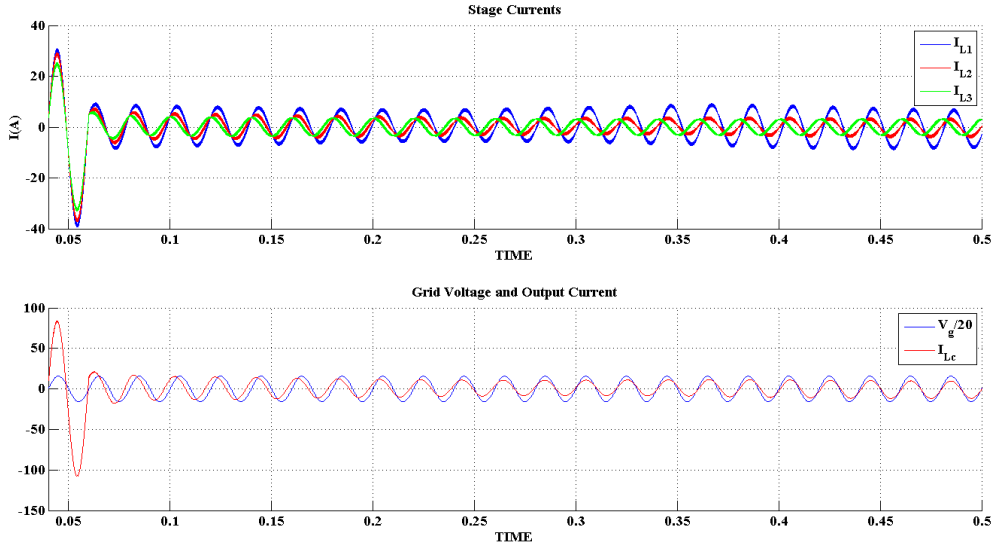


Figure 4.21: Currents and Grid Voltage. ZOOM at initial time

in phase with the grid voltage, so the control has done its work. Figure 4.23 shows how the control action's settling time is bigger than in previous simulations, but the value tends to a stable value, which is reached near the 1.3 seconds. However, the stages currents are still not in phase between them. This is, again, because they are not controlled. Its amplitude is once more far away from what it is supposed to be, and it can be appreciated also in figure 4.24, where the scalar factors (which are directly proportional to the currents) have a higher value than what they had in previous sections. Therefore, the way to maintain the working point of the panels is, again, the exchange of reactive power between the stages, which is continuously charging and discharging the output panel capacitor.

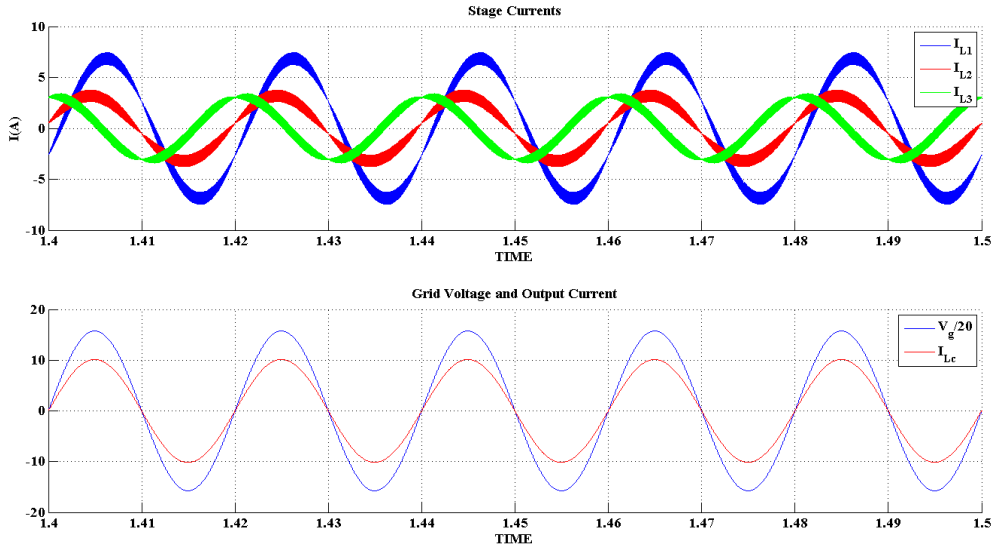


Figure 4.22: Currents and Grid Voltage. ZOOM at final time

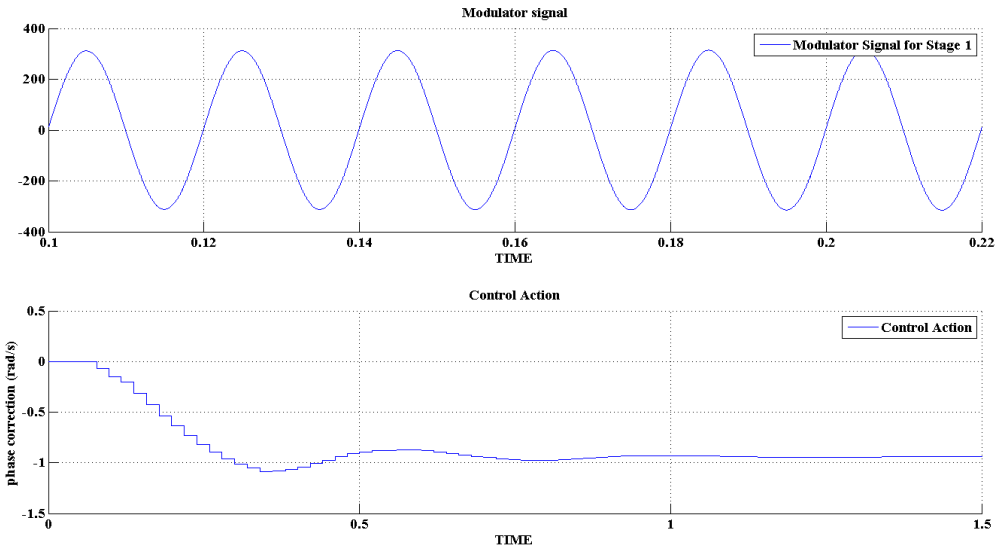


Figure 4.23: Modulation signal for Stage 1 and Control Action

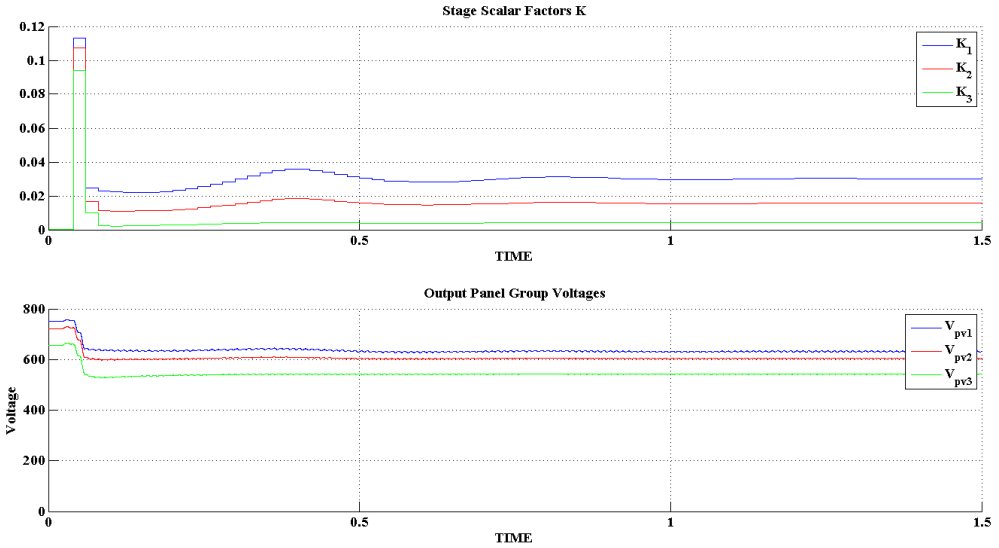


Figure 4.24: Scalar Factor values for each stage and Panel Array Output Voltages

Simulation 4.6. Ideal Nominal Duty Generator with Phase Control over Real Plant with Tolerances

This simulation is essentially the same simulation as 4.4 but, this time, tolerances will be applied tot the passive components. This is the most realistic plant that can be tested, because, when doing the circuital analysis calculations, the exact values of the components are unknown. Table 4.7 shows the values that have been applied to the plant. AS exposed in the introduction, the tolerance applied for the passive components is a 20%, and a 10% for the losses.

The resulting figures from this simulation does not reveal any new information about the response of the system. The time response and the values where all the variables tend to are very

Irradiance Stage 1 $= 1000W/m^2$	$R_{L_1} = 110m\Omega$
Irradiance Stage 2 $= 523.34W/m^2$	$R_{L_2} = 105m\Omega$
Irradiance Stage 3 $= 117.2482W/m^2$	$R_{L_3} = 90m\Omega$
Panel Array 1 Output voltage reference $= 543.5V$	$L_c = 96\mu H$
Panel Array 2 Output voltage reference $= 604.3V$	$R_{L_c} = 12m\Omega$
Panel Array 3 Output voltage reference $= 630.7V$	$C_c = 9\mu F$
$L_1 = 2.56mH$	$R_{C_c} = 7.2m\Omega$
$L_2 = 3mH$	Temp=25^oC
$L_3 = 3.84mH$	$A_g = 311V$

Table 4.7: Values used in simulation 4.6

similar to the ones obtained in simulation 4.4. The external control remains stable, and the working point of the panels tends correctly to its reference value.

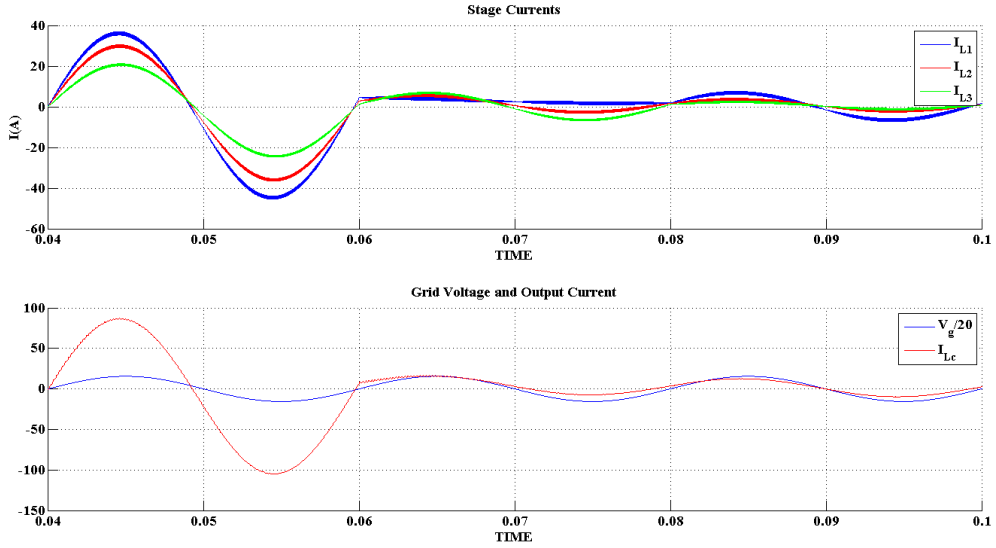


Figure 4.25: Currents and Grid Voltage. ZOOM at initial time

The most important difference between the cases studied until now, are the control action necessary to put the injected current in phase with the grid voltage, and the phase difference between stages currents when an incorrect grid voltage sensing happens.

The issue with the grid voltage can be solved by sensing this variable with a high precision, but, if this is not possible, the control will put anyhow in phase the injected current and the grid voltage, with the inconvenient that the reactive power flowing through the stages will cause higher losses, and the system will present a poorer efficiency. Therefore, it can be affirmed that for worse grid voltage lecture, the worse efficiency of the system.

The control action will have to act more strongly if the different parameters are worse predicted. It is logical. Figure 4.29 shows how the control action is higher and less damped as worse is the prediction of the elements and the sensing of the grid voltage, so, it can be thought that an enough bad prediction could lead it to instability. If the prediction of the elements help the

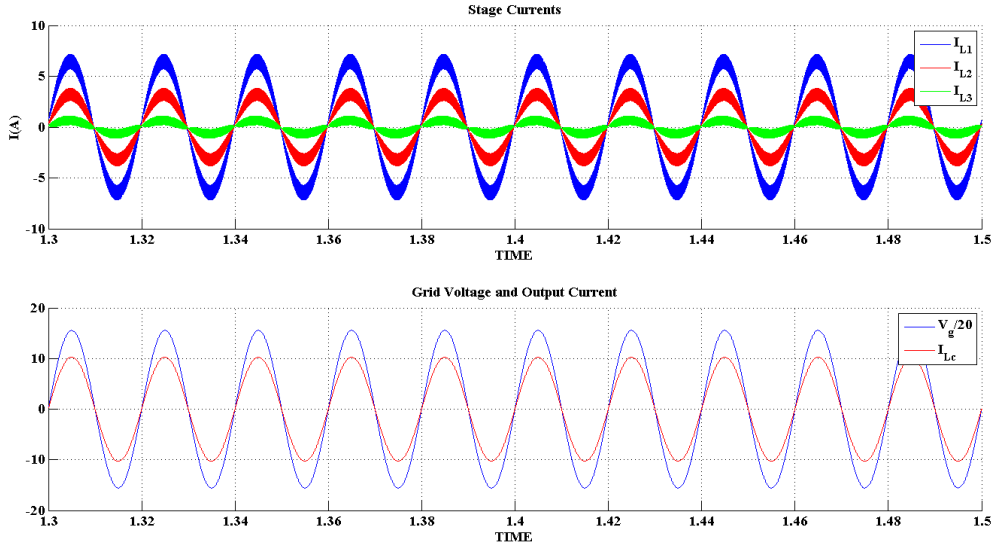


Figure 4.26: Currents and Grid Voltage. ZOOM at final time

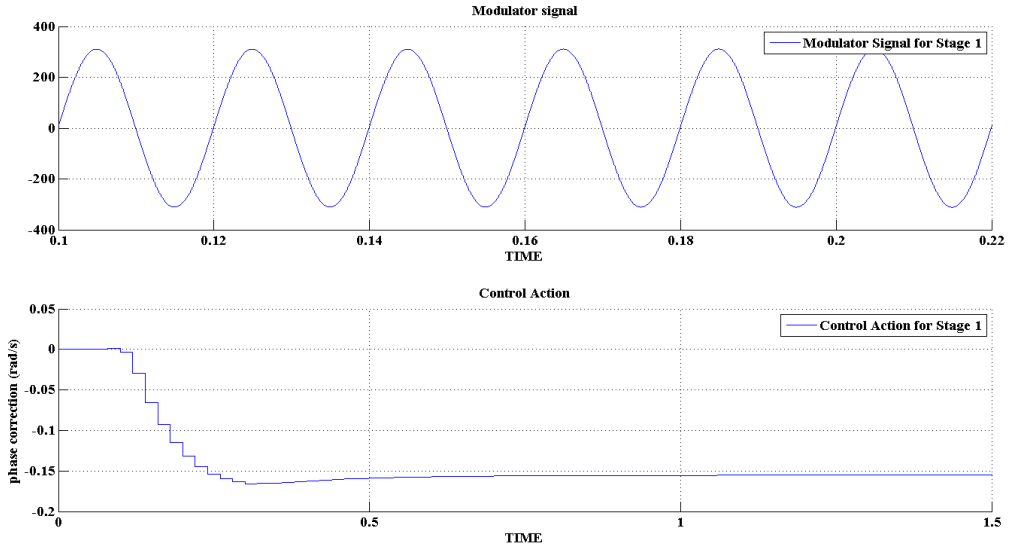


Figure 4.27: Modulation signal for Stage 1 and Control Action

control to actuate softly, then it can be concluded that a prediction of the losses in the circuital analysis would lead to a better response of the system. It will reduce the settling time of the control action, reducing also the time when undesired characteristics as offset in the stages and injected currents, for example.

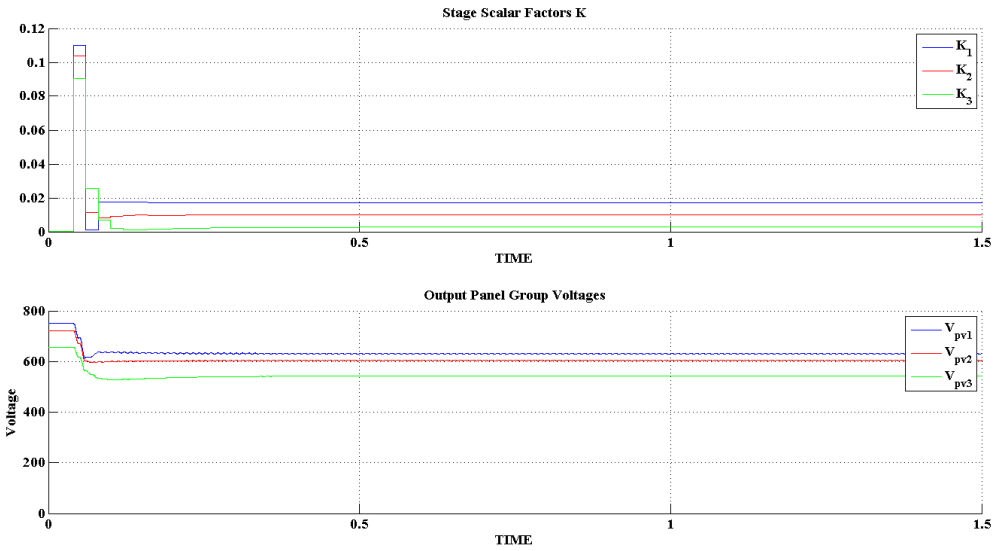


Figure 4.28: Scalar Factor values for each stage and Panel Array Output Voltages

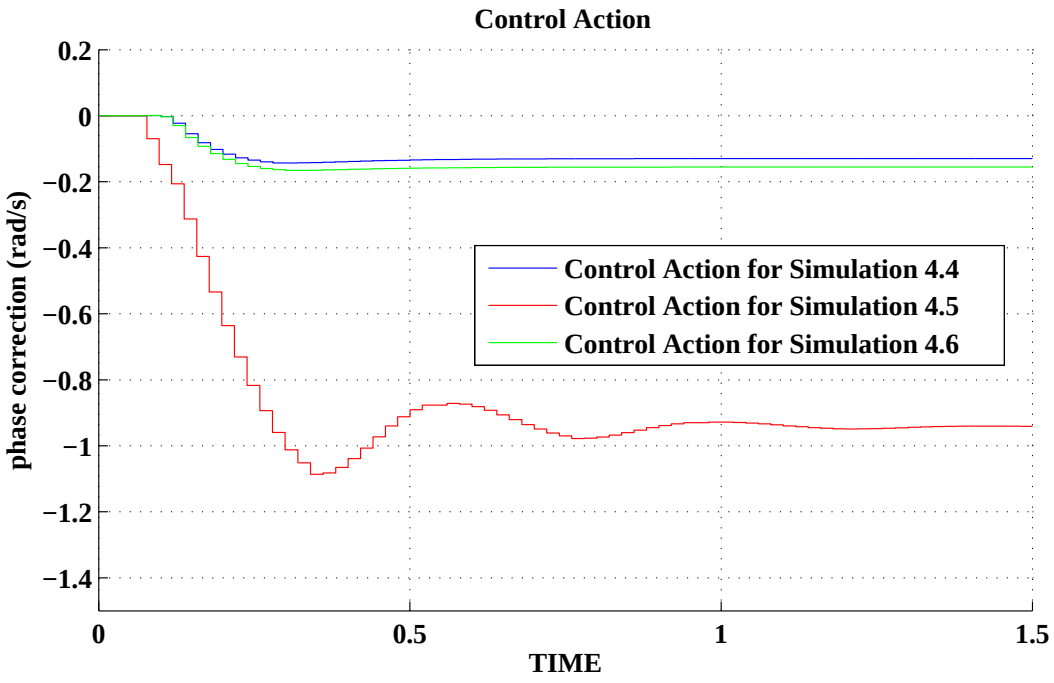


Figure 4.29: Control Actions Comparative for different simulations

4.6 Redefining Circuital Analysis to work with Losses

The losses must be included in the circuital analysis to improve the response of the stage currents, as seen in the previous sections. The intention is to include them and test if the variability between the real losses and the values used for the calculus cause a significant phase difference or not. The schematic of the plant including the losses of the elements is presented in figure 4.30.

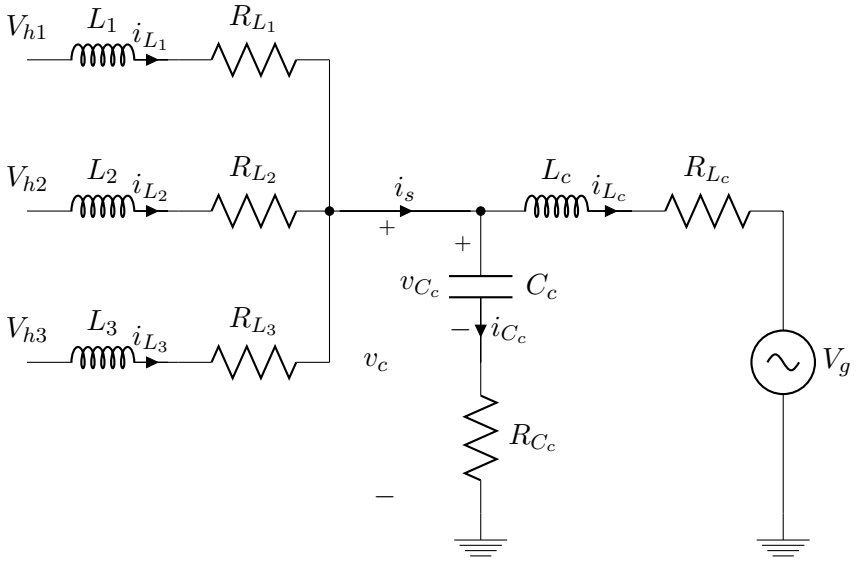


Figure 4.30: Simplified Real Circuital scheme of Parallel Connected Inverters Plant

The proceeding is the same as the exposed in section 4.4 but including the losses in all the inductors and in the ESR in the capacitor.

$$v_g = A_g \sin(w_g t + \varphi_g) \qquad i_{L_c} = K A_g \sin(w_g t + \varphi_g)$$

The first assumption is the same, the grid voltage and the injected current are in phase and related by the scalar factor K. The expression of the voltage in the node of all the inductors and the capacitor will be:

$$\begin{aligned} v_c &= L_c \frac{di_{L_c}}{dt} + R_{L_c} i_{L_c} + v_g \\ v_c &= L_c A_g K w_g \cos(w_g t + \varphi_g) + R_{L_c} A_g K \sin(w_g t + \varphi_g) + A_g \sin(w_g t + \varphi_g) \\ v_c &= L_c A_g K w_g \sin(w_g t + \varphi_g + \frac{\pi}{2}) + (A_g + R_{L_c} A_g K) \sin(w_g t + \varphi_g) \end{aligned} \tag{4.21}$$

Again, the use of phasor sum is necessary to solve the equation. Therefore, the expression of the capacitor voltage will be:

$$v_c = A_c \sin(w_g t + \varphi_c)$$

Where:

$$A_c = \sqrt{(L_c A_g K w_g \sin(\varphi_g + \frac{\pi}{2}) + (A_g + R_{L_c} A_g K) \sin(\varphi_g))^2 + \\ (L_c A_g K w_g \cos(\varphi_g + \frac{\pi}{2}) + (A_g + R_{L_c} A_g K) \cos(\varphi_g))^2} \tag{4.22}$$

And:

$$\varphi_c = \arctan(\frac{(L_c A_g K w_g \sin(\varphi_g + \frac{\pi}{2}) + (A_g + R_{L_c} A_g K) \sin(\varphi_g)}{L_c A_g K w_g \cos(\varphi_g + \frac{\pi}{2}) + (A_g + R_{L_c} A_g K) \cos(\varphi_g)})$$

Having found the expression in the capacitor node, it is necessary to find the expression of the

current through the capacitor.

$$i_{C_c} = C_c \frac{dv_{C_c}}{dt}$$

Where:

$$v_{C_c} = v_c - i_{C_c} R_{C_c} \tag{4.23}$$

Therefore:

$$i_{C_c} = C_c \frac{dv_c}{dt} - R_{C_c} C_c \frac{di_{C_c}}{dt}$$

As can be seen, a differential equation must be resolved. There are lots of methods to solve a differential equation, but in this thesis the method of integral factor is going to be used. A little reminding about this method is exposed next:

To solve a differential equation by the method of integral factor, it is necessary to have an expression like:

$$y' + p(x)y = g(x)$$

The integration factor $u(x)$ is defined as:

$$u(x) = e^{\int p(x)dx}$$

And the solution for the equation is:

$$y = \frac{1}{u(x)} \int u(x)g(x)dx$$

For the case of the equation that must be solved:

$$y = i_{C_c} \qquad p(x) = \frac{1}{R_{C_c} C_c} \qquad g(x) = \frac{1}{R_{C_c}} \frac{dv_c}{dt} \qquad u(x) = e^{\frac{t}{R_{C_c} C_c} + C_i}$$

Where C_i is the integration constant. From here, the solution to the differential equation is:

$$i_{C_c} = \frac{1}{e^{\frac{t}{R_{C_c} C_c} + C_i}} \int e^{\frac{t}{R_{C_c} C_c} + C_i} \frac{dv_c}{dt} \frac{1}{R_{C_c}} dt \tag{4.24}$$

Due to the complexity for solving this equation, Mapple software has been used to do it. The final expression for i_{C_c} is:

$$i_{C_c} = \frac{A_c w_g C_c}{(1 + (w_g R_{C_c} C_c)^2)} (\cos(w_g t + \varphi_c) + w_g R_{C_c} C_c \sin(w_g t + \varphi_c)) \tag{4.25}$$

The equation can be expressed as the phasor sum.

$$i_{C_c} = I_{C_c} \sin(w_g t + \varphi_{ic})$$

Where:

$$I_{C_c} = \frac{A_c w_g C_c}{(1 + (w_g R_{C_c} C_c)^2)} \sqrt{(\sin(\varphi_c + \frac{\pi}{2}) + R_{C_c} C_c w_g \sin(\varphi_c))^2 + (\cos(\varphi_c + \frac{\pi}{2}) + R_{C_c} C_c w_g \cos(\varphi_c))^2} \tag{4.26}$$

And:

$$\varphi_{ic} = \arctan(\frac{\sin(\varphi_c + \frac{\pi}{2}) + R_{C_c} C_c w_g \sin(\varphi_c)}{\cos(\varphi_c + \frac{\pi}{2}) + R_{C_c} C_c w_g \cos(\varphi_c)})$$

The addition of both currents, expressed as i_s.

$$i_s = i_{C_c} + i_{L_c} = I_s \sin(w_g t + \varphi_s)$$

Where:

$$I_s = \sqrt{(I_{C_c} \sin(\varphi_{ic}) + K A_g \sin(\varphi_g))^2 + (I_{C_c} \cos(\varphi_{ic}) + K A_g \cos(\varphi_g))^2} \tag{4.27}$$

And:

$$\varphi_s = \arctan(\frac{I_{C_c} \sin(\varphi_{ic}) + K A_g \sin(\varphi_g)}{I_{C_c} \cos(\varphi_{ic}) + K A_g \cos(\varphi_g)})$$

At this point, the currents of each stage are distributed giving them the proportional part of I_s according to the scalar value K_n (where n is the studied stage) given by the external control of each stage. Therefore, the currents of each stage are fixed as:

$$i_{L_n} = \frac{K_n}{K} i_s \tag{4.28}$$

This means that the phase of the currents of all the stages present in the topology are fixed as φ_s. For that reason, the circuital analysis and therefore the nominal duty generator are the responsible of putting in phase all the stages currents. Once solved the expression of the current, the value of the voltage that must be generated into the transistor bridge can be found.

$$v_n = A_n \sin(w_g t + \varphi_n) = v_c + i_{L_n} R_{L_n} + L_n \frac{i_{L_n}}{dt}$$

Therefore:

$$\frac{A_n = \sqrt{(A_c \sin(\varphi_c) + I_{L_n} R_{L_n} \sin(\varphi_s) + I_{L_n} w_g L_n \sin(\varphi_s + \frac{\pi}{2}))^2 +}}{(A_c \cos(\varphi_c) + I_{L_n} R_{L_n} \cos(\varphi_s) + I_{L_n} w_g L_n \cos(\varphi_s + \frac{\pi}{2}))^2} \tag{4.29}$$

And:

$$\varphi_n = \arctan(\frac{A_c \sin(\varphi_c) + I_{L_n} R_{L_n} \sin(\varphi_s) + I_{L_n} w_g L_n \sin(\varphi_s + \frac{\pi}{2})}{A_c \cos(\varphi_c) + I_{L_n} R_{L_n} \cos(\varphi_s) + I_{L_n} w_g L_n \cos(\varphi_s + \frac{\pi}{2})})$$

Simulation 4.7. Real Nominal Duty Generator over Real Plant

The first simulation of this section is performed just tot test that the expressions extracted are valid. In this case, the nominal duty generator is supposed to know exactly the values of the elements in the circuit and its losses. Therefore, after the start-up time, the system is supposed to arrive to stable conditions and, if the calculus are correct, all the current phases must be in phase between them, as the injected current with the voltage.

Figures show that the behaviour of the system acts as it is supposed. The same phase between stages currents and the same phase for the grid voltage and injected current are achieved. Thus, the calculations are validated.

Irradiance Stage 1 $= 1000W/m^2$	$R_{L_1} = 100m\Omega$
Irradiance Stage 2 $= 523.34W/m^2$	$R_{L_2} = 100m\Omega$
Irradiance Stage 3 $= 117.2482W/m^2$	$R_{L_3} = 100m\Omega$
Panel Array 1 Output voltage reference $= 543.5V$	$L_c = 80\mu H$
Panel Array 2 Output voltage reference $= 604.3V$	$R_{L_c} = 10m\Omega$
Panel Array 3 Output voltage reference $= 630.7V$	$C_c = 9\mu F$
$L_1 = 3.2mH$	$R_{C_c} = 8m\Omega$
$L_2 = 3.2mH$	Temp=25^oC
$L_3 = 3.2mH$	$A_g = 311V$

Table 4.8: Values used in simulation 4.7

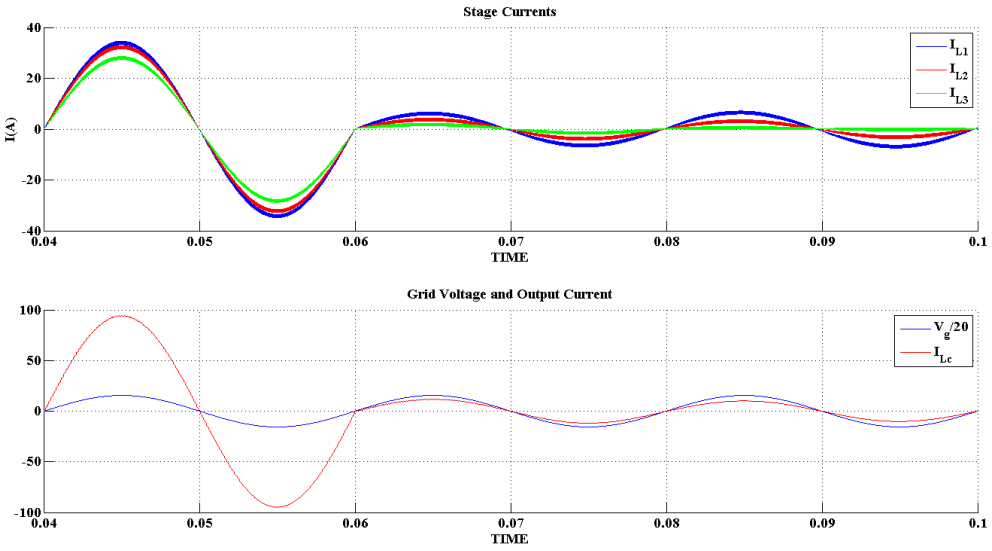


Figure 4.31: Currents and Grid Voltage. ZOOM at initial time

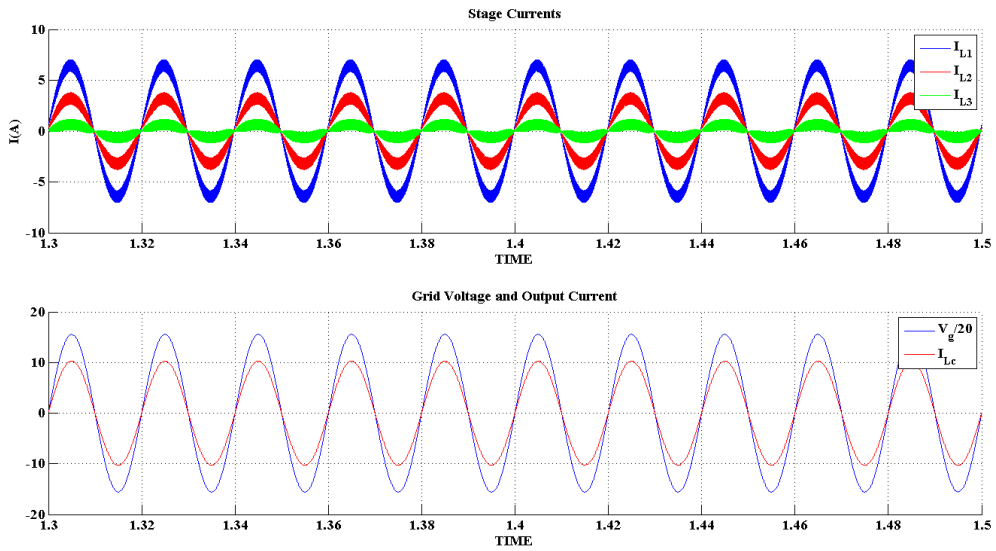


Figure 4.32: Currents and Grid Voltage. ZOOM at final time

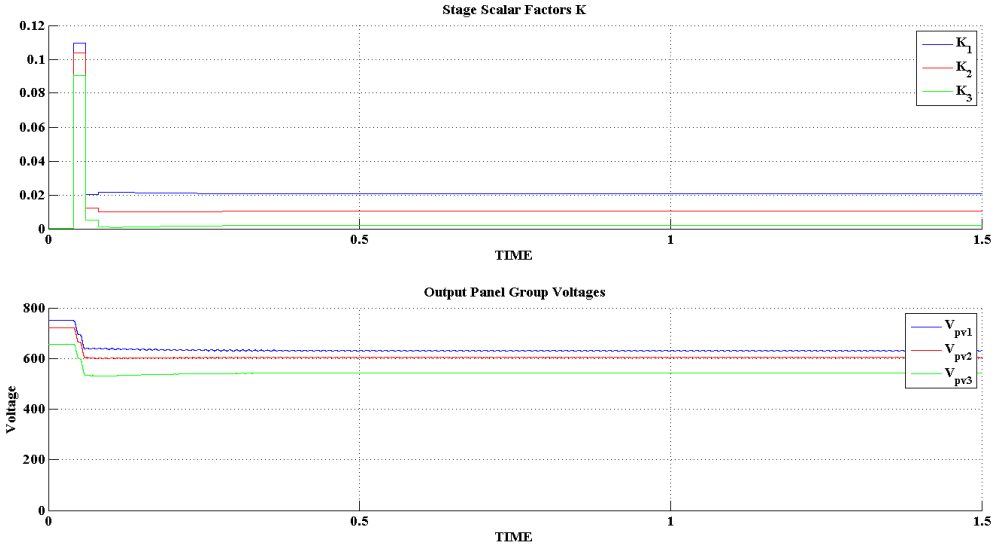


Figure 4.33: Scalar Factor values for each stage and Panel Array Output Voltages

Simulation 4.8. Real Nominal Duty with Phase Control over Real Plant with Tolerances

This simulation has been made to test the response of the system when the values of the components are estimated but not absolutely known. This is the same as simulation 4.6, but, this time, the values of the losses are included into the calculus. Table 4.9 shows the values used in the plant of the system. The voltage is not unbalanced. This is because, as commented, it is supposed to be properly and, if it is not, the performance of the system has already been tested.

Irradiance Stage 1 = $1000W/m^2$	$R_{L_1} = 110m\Omega$
Irradiance Stage 2 = $523.34W/m^2$	$R_{L_2} = 105m\Omega$
Irradiance Stage 3 = $117,2482W/m^2$	$R_{L_3} = 90m\Omega$
Panel Array 1 Output voltage reference = $543.5V$	$L_c = 96\mu H$
Panel Array 2 Output voltage reference = $604.3V$	$R_{L_c} = 12m\Omega$
Panel Array 3 Output voltage reference = $630.7V$	$C_c = 9\mu F$
$L_1 = 2.56mH$	$R_{C_c} = 7.2m\Omega$
$L_2 = 3mH$	Temp=25^oC
$L_3 = 3.84mH$	$A_g = 311V$

Table 4.9: Values used in simulation 4.8

Figure 4.34 shows the currents during the start-up time. The response showed is quite better than the presented in simulation 4.6. The offsets observed in the currents are lower. The settling time is very similar, as can be observed in figure 4.36, but the value of the control action is much more little when the losses are inserted in the calculus. For that reason, the injected current and the grid voltage are in phase in less time than the simulation 4.6. That is the main benefit of adding the losses in the calculus.

Figures 4.35 and 4.37 show that the system finally goes to the reference working point and is stable. That was expected having into account the results in previous simulations.

Finally,a comparative between the control action of different prediction levels for the value of the components and the losses is provided in figure 4.38. As can be seen, when the losses are predicted, the control action is smoother than for the other cases. And if the voltage grid is not properly sensed, then the control action must work harder than for the other cases.

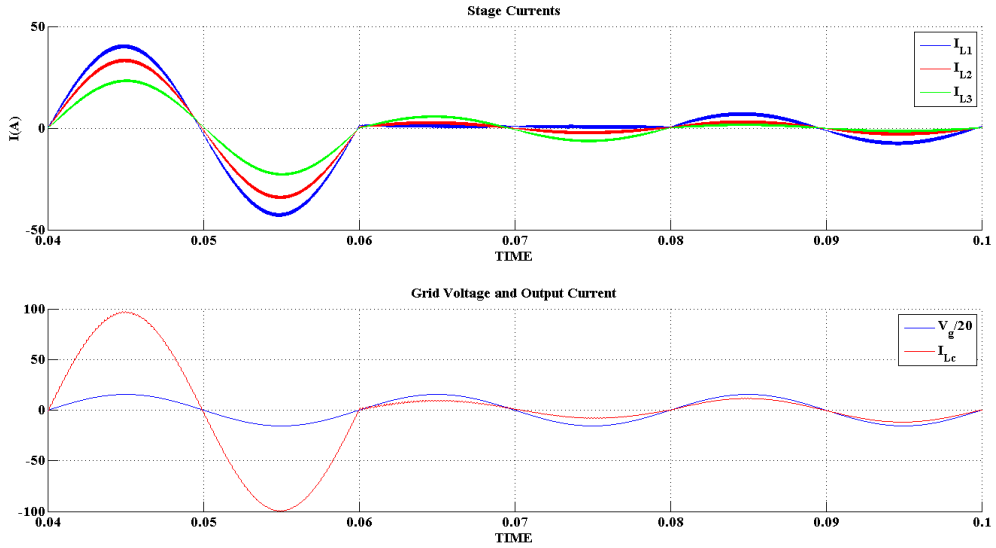


Figure 4.34: Currents and Grid Voltage. ZOOM at initial time

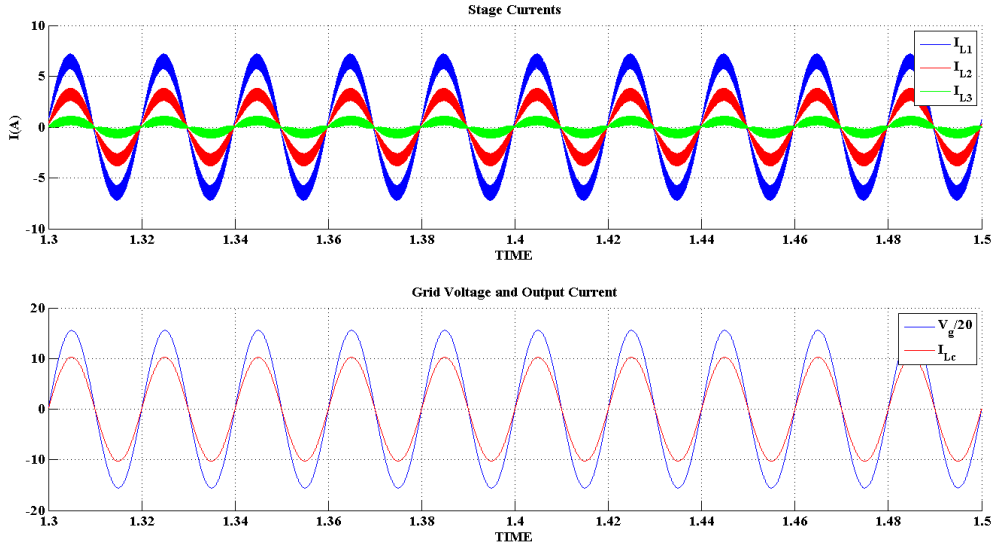


Figure 4.35: Currents and Grid Voltage. ZOOM at final time

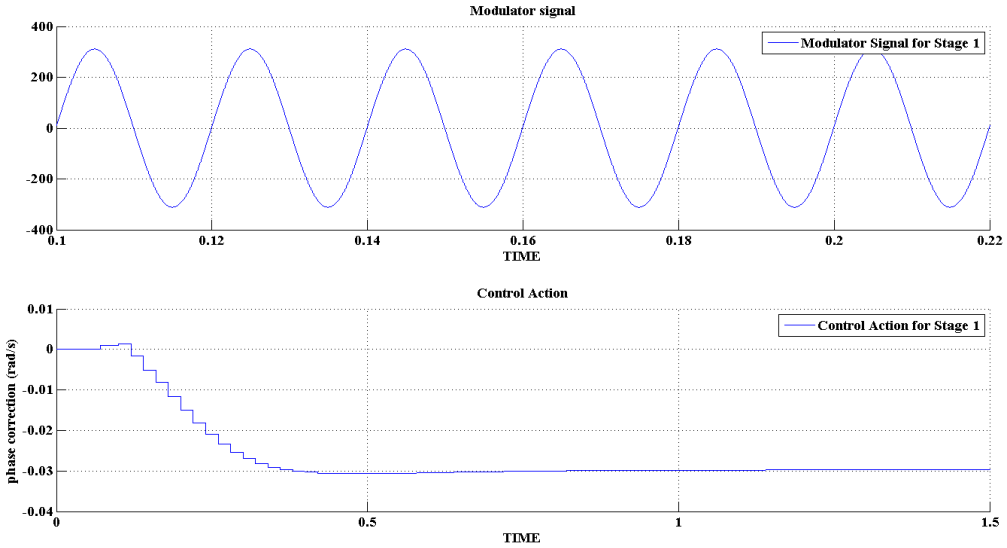


Figure 4.36: Modulation signal for Stage 1 and Control Action

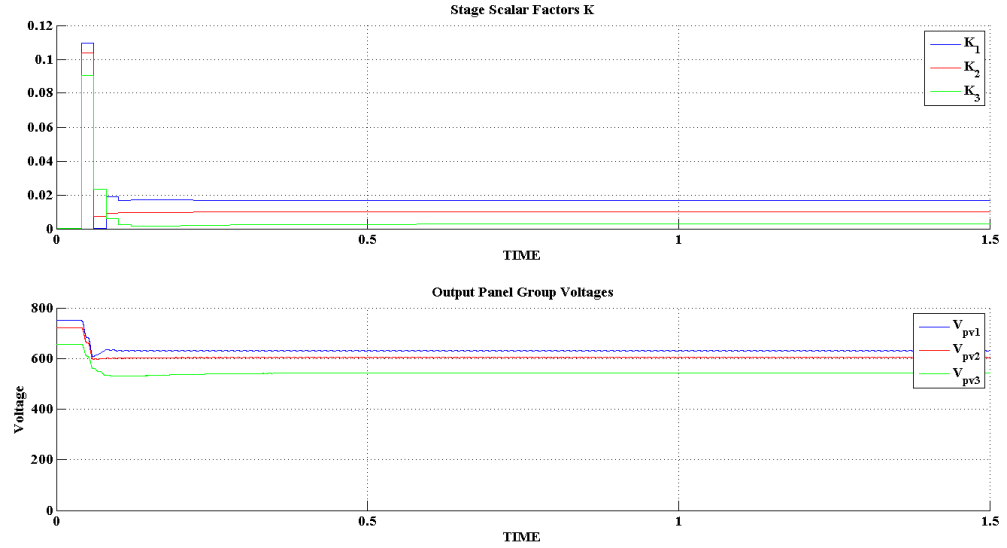


Figure 4.37: Scalar Factor values for each stage and Panel Array Output Voltages

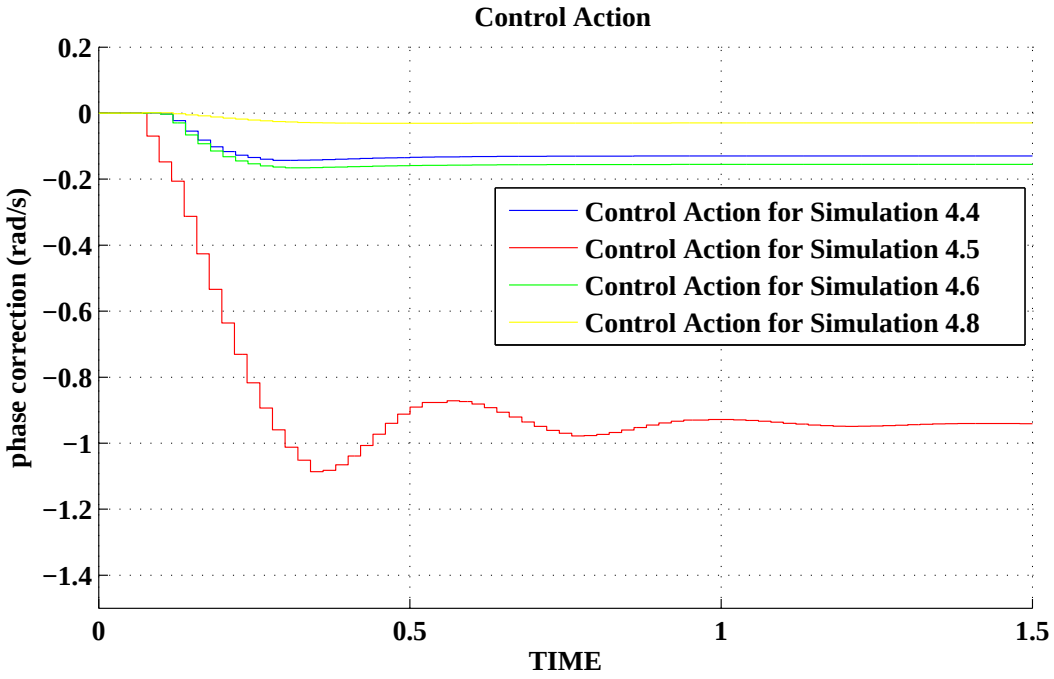


Figure 4.38: Control Action comparative for different simulations

Simulation 4.9. Irradiance Transient in Parallel Connected Inverters Topology

After presenting the studies for parallel inverters connected topology, the simulations that have been performed for the other topologies must be performed for this one. This simulation tests the response of the system in front of an abrupt irradiance transient. For this simulation, tolerances in the values of the components and the losses will not be applied. Table 4.10 shows the values used for the irradiance transient and the plant.

$L_1 = 3.2mH$	$R_{L_1} = 100m\Omega$
$L_2 = 3.2mH$	$R_{L_2} = 100m\Omega$
$L_3 = 3.2mH$	$R_{L_3} = 100m\Omega$
$L_c = 80\mu H$	$R_{L_c} = 10m\Omega$
$C_c = 9\mu F$	$R_{C_c} = 8m\Omega$
$A_g = 311V$	Temp=25^oC
$f_{sw} = 40kHz$	
Irradiance transients for all stages:	
$764.1678W/m^2$ $(750W)$	$0\ s < t \leq 1.3\ s$
$223.003W/m^2$ $(200W)$	$1.3\ s < t \leq 2.5\ s$
$764.1678W/m^2$ $(750W)$	$2.5\ s < t$
Panel Array Voltages references:	
$619.712V$	$0\ s < t \leq 1.3\ s$
$569.56V$	$1.3\ s < t \leq 2.5\ s$
$619.712V$	$2.5\ s < t$

Table 4.10: Values used in simulation 4.9

Figure 4.39 shows the stages currents, the output injected current and the grid voltage. As can be seen, the currents in all the stages are the same. This is because the system has not been unbalanced and the irradiance is the same for all the panel arrays. Here, the injected current is also in phase with the grid voltage including during the current transients.

Figure 4.40 shows the output voltages for all the stages. As the irradiance is the same and the transient is also the sme, the voltages follow the same reference all time. The difference between this simulation and the equivalent performed for the central and series topologies, is that the voltage transient is smoother here.

It has been seen that this control responds better than the control of the central and series topologies to an abrupt irradiance transient.

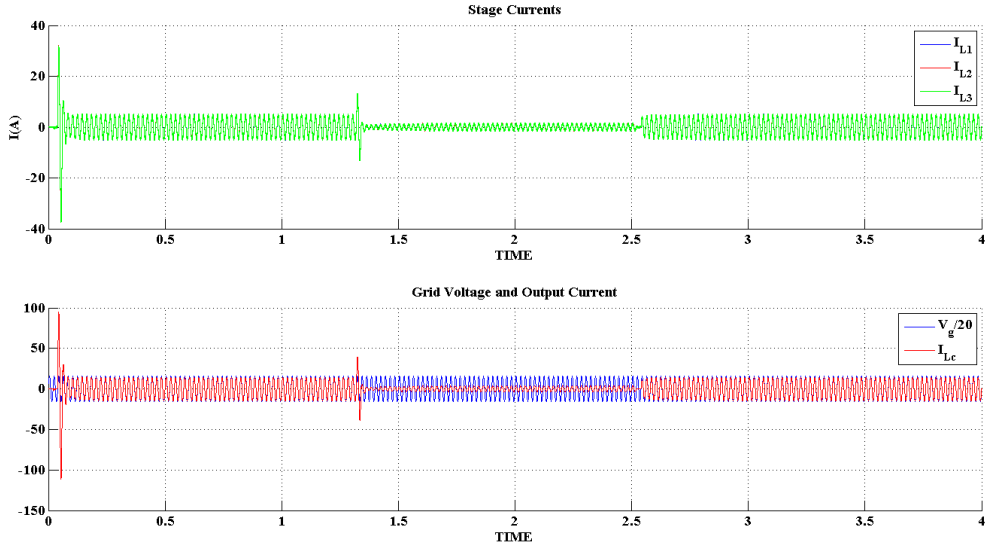


Figure 4.39: Currents and Grid Voltage

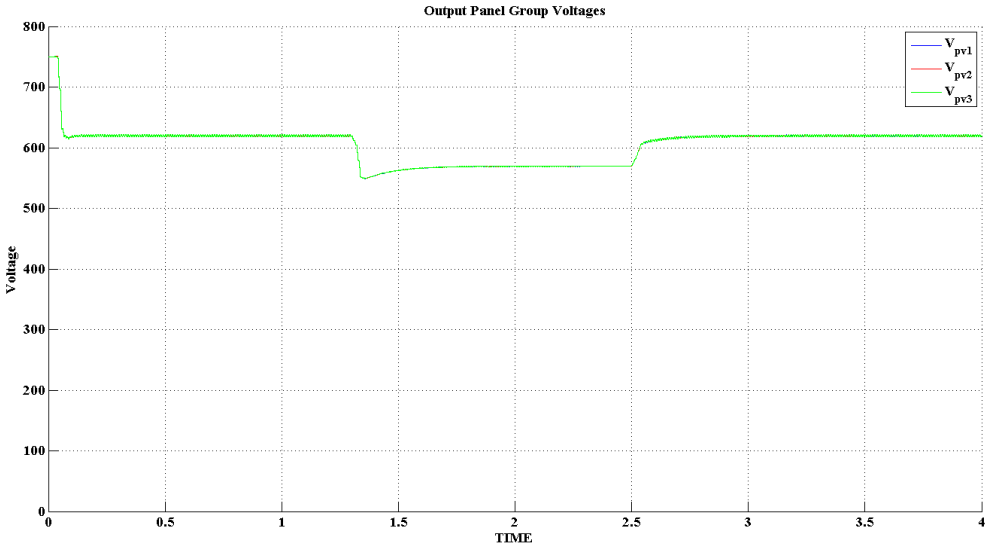


Figure 4.40: Panel Arrays Voltages

Simulation 4.10. MPPT Reference Abrupt Transient in Parallel Connected Inverters Topology

This simulation is performed to test the response of the system when an abrupt reference voltage transient occurs. Table 4.11 shows the values used for the simulation. The transient performed for each stage is different, so the values os the output voltages and the output currents will differ in this case.

Similarly to central and series topologies, figure 4.41 shows how the currents tend to their own reference value, as the voltage also do in figures 4.42 and 4.43. Voltages transition here is slower than for the central and series topologies, but finally all the values tend to their reference value.

$L_1 = 3.2mH$	$R_{L_1} = 100m\Omega$
$L_2 = 3.2mH$	$R_{L_2} = 100m\Omega$
$L_3 = 3.2mH$	$R_{L_3} = 100m\Omega$
$L_c = 80\mu H$	$R_{L_c} = 10m\Omega$
$C_c = 9\mu F$	$R_{C_c} = 8m\Omega$
$A_g = 311V$	Temp=25^oC
$f_{sw} = 40kHz$	Irradiance=$1000W/m^2$
Panel Array Voltages references. Stage 1:	
$630.969V$ $(1000W)$	$0\ s < t \leq 1.3\ s$
$727.288V$ $(500W)$	$1.3\ s < t \leq 2.5\ s$
$630.969V$ $(1000W)$	$2.5\ s < t$
Panel Array Voltages references. Stage 2:	
$630.969V$ $(1000W)$	$0\ s < t \leq 1.3\ s$
$737.984V$ $(300W)$	$1.3\ s < t \leq 2.5\ s$
$630.969V$ $(1000W)$	$2.5\ s < t$
Panel Array Voltages references. Stage 3:	
$630.969V$ $(1000W)$	$0\ s < t \leq 1.3\ s$
$742.384V$ $(200W)$	$1.3\ s < t \leq 2.5\ s$
$630.969V$ $(1000W)$	$2.5\ s < t$

Table 4.11: Values used in simulation 4.10

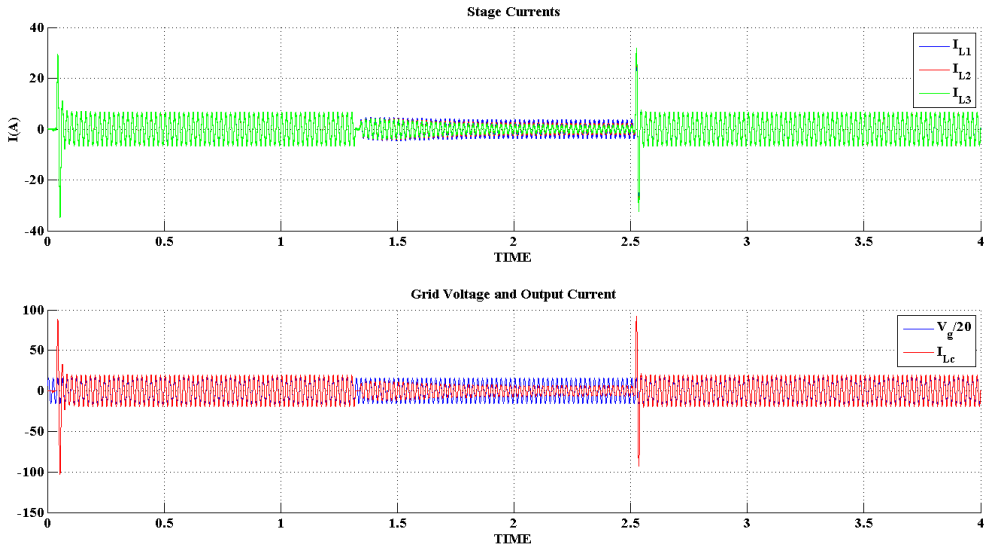


Figure 4.41: Currents and Grid Voltage

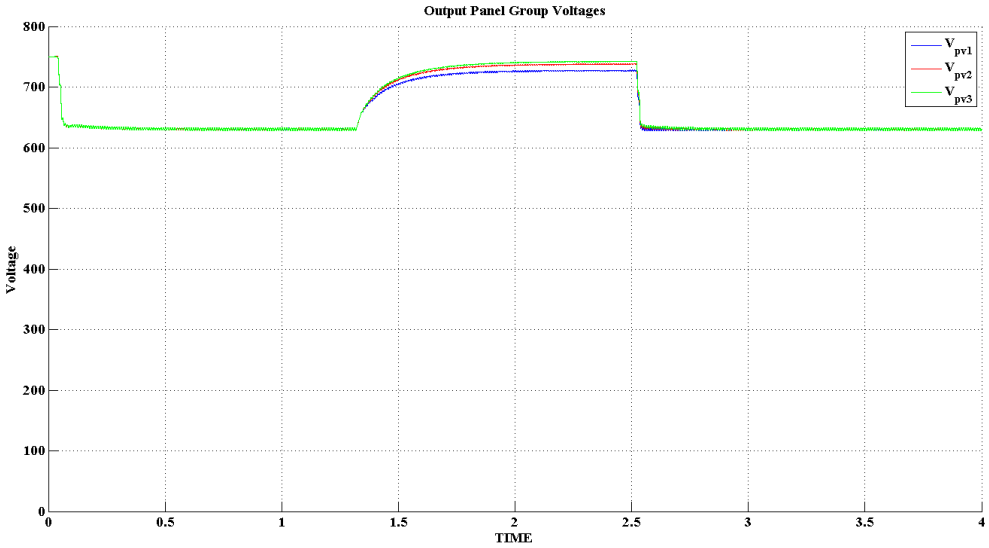


Figure 4.42: Panel Arrays Voltages

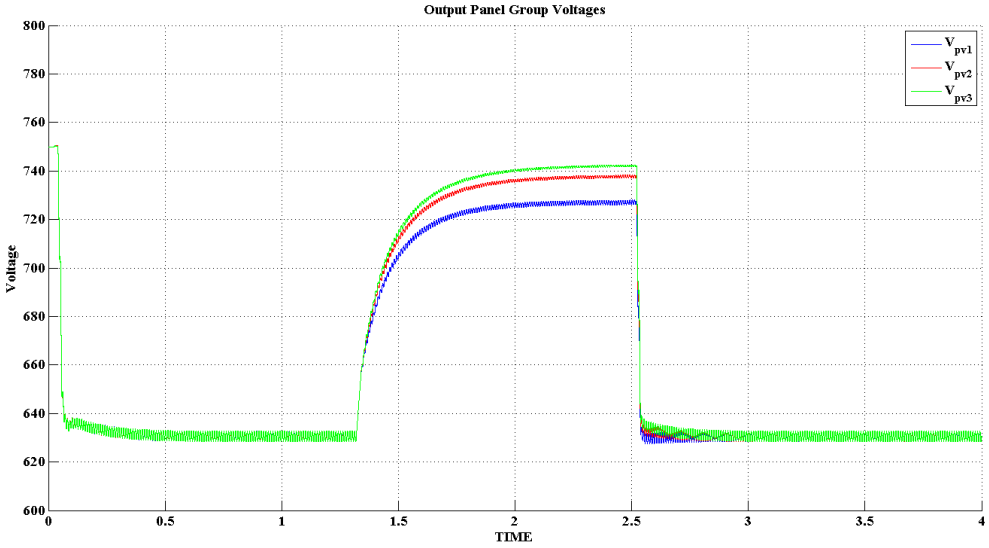


Figure 4.43: Panel Arrays Voltages. ZOOM

Simulation 4.11. MPPT Reference Tracking in Parallel Connected Inverter Topology

This simulation is in essence the same as the last one. It is performed to determine if the system is capable to respond properly to changes at the output voltage reference, like in simulation 4.10. These change will be smoother but with less time between them. Table 4.12 shows the values used to perform the simulation.

$L_1 = 3.2mH$	$R_{L_1} = 100m\Omega$
$L_2 = 3.2mH$	$R_{L_2} = 100m\Omega$
$L_3 = 3.2mH$	$R_{L_3} = 100m\Omega$
$L_c = 80\mu H$	$R_{L_c} = 10m\Omega$
$C_c = 9\mu F$	$R_{C_c} = 8m\Omega$
$A_g = 311V$	Temp=25^oC
$f_{sw} = 40kHz$	Irradiance=$1000W/m^2$
Panel Arrays Voltages references. All Stages:	
$630.969V$ $(1000W)$	$0\ s < t \leq 1.2\ s$
$707.168V$ $(750W)$	$1.2\ s < t \leq 1.8\ s$
$720.512V$ $(600W)$	$1.8\ s < t \leq 2.4\ s$
$727.288V$ $(500W)$	$2.4\ s < t \leq 3\ s$
$737.984V$ $(300W)$	$3\ s < t \leq 3.6\ s$
$742.384V$ $(200W)$	$3.6\ s < t$

Table 4.12: Values used in simulation 4.11

As for other topologies, figures 4.44 and 4.45 show how the currents of each stage, the injected current, and the output panel array voltages follow their own reference without any problem. Hence, it can be concluded that the parallel control has an acceptable response for these cases.

As the control in this topology depends on the values of the losses and the components, it seems to be obvious that applying tolerances to them would change the response of the system. However, as the system with tolerances has been tested before, it has been considered unnecessary to test in these last simulations.

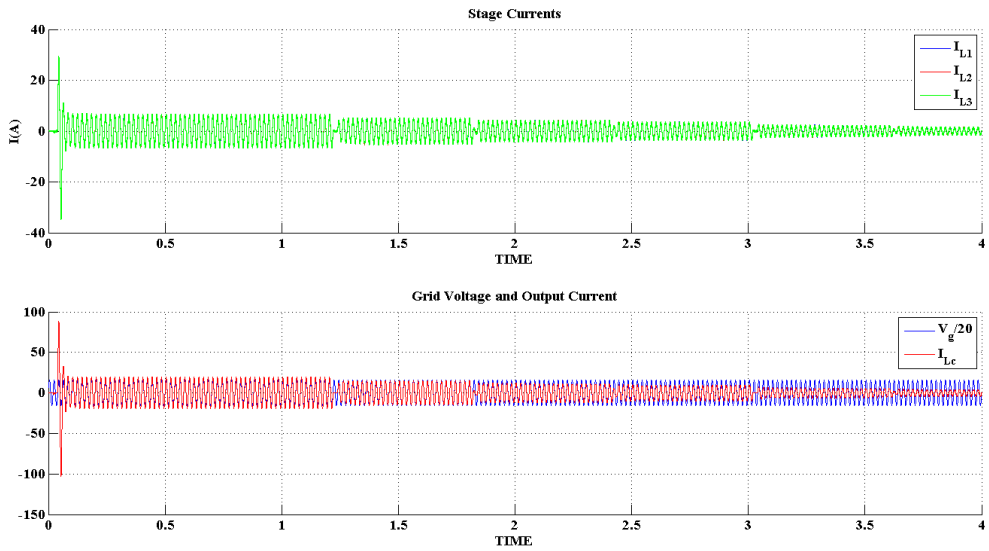


Figure 4.44: Currents and Grid Voltage

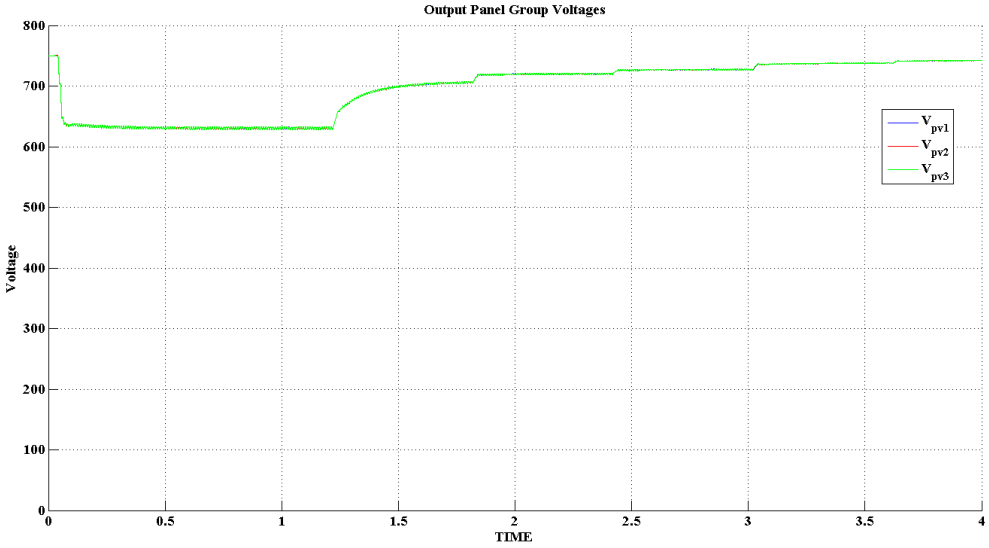


Figure 4.45: Panel Arrays Voltages

Chapter 5

Comparative between different topologies

After finding an acceptable performance for the parallel connected inverters topology, has been considered necessary to test what of the three topologies exposed in this thesis gives a better result in terms of efficiency.

5.1 Methodology

The comparative will be performed for different values of switching frequency and irradiance over the panel arrays. The values of different switching frequencies have been chosen from $20kHz$ to $100kHz$ with increments of $20kHz$. The values of irradiance are presented in tables 1.1, 1.2 and 1.3. In this case, differently from previous chapters simulations, the irradiances over the panel arrays will be the same for each array. The values of losses, inductors and capacitors for each topology are shown in table 5.1. As can be seen, the values coincide with the values proposed for a real plant, but without tolerances between them, this means that, for the case of the parallel connected inverters topology, the values of the components are exactly known when implementing the circuital analysis, so the phase differences between stages currents and the possible reactive power derived will be cancelled.

$L_1 = 3.2mH$	$R_{L_1} = 100m\Omega$
$L_c = 80\mu H$	$R_{L_c} = 10m\Omega$
$C_c = 9\mu F$	$R_{C_c} = 8m\Omega$
$A_g = 311V$	Temp=25^oC

(a) Values for Central Inverter and Series Connected Inverter topologies

$L_1 = 3.2mH$	$R_{L_1} = 100m\Omega$
$L_2 = 3.2mH$	$R_{L_2} = 100m\Omega$
$L_3 = 3.2mH$	$R_{L_3} = 100m\Omega$
$L_c = 80\mu H$	$R_{L_c} = 10m\Omega$
$C_c = 9\mu F$	$R_{C_c} = 8m\Omega$
$A_g = 311V$	Temp=25^oC

(b) Values for Parallel Connected Inverter topology

Table 5.1: Values of plant elements for different topologies

5.1.1 The Euro-efficiency

The different percentages of output power at each simulation are determined by the parameter known as euro-efficiency. The concept of euro-efficiency was created to facilitate a comparison of different inverters, and it is a standard for the european climate. A different irradiance of the panels will cause a different load working point for the panels, and, therefore, the efficiency will change. To calculate the euro-efficiency, the efficiencies at different output power points are weighted by the factors presented in equation 5.1.

$$\eta_{euro} = 0.03\eta_{5\%} + 0.06\eta_{10\%} + 0.13\eta_{20\%} + 0.1\eta_{30\%} + 0.48\eta_{50\%} + 0.2\eta_{100\%} \tag{5.1}$$

So the percentages of irradiance presented by equation 5.1 are the ones performed in the comparative for each topology.

5.1.2 The Transistor

The transistor used in the comparative for the bridges of each stage is the C2M0080120D from company CREE. It is a silicon carbide n-channel MOSFET. The advantages of the silicon carbide (SiC) over the normal silicon (Si) transistors are:

- Higher breakdown voltages, which leads to smaller devices. If the device is smaller, it means that the R_{ds} of the transistor will be also smaller. For this reason, the conduction losses of the device are reduced. This means a higher efficiency.
- Significantly reduced switching losses (minimal variation versus temperature) resulting in more compact designs (with smaller passive components). The miller capacitances of the MOSFET are reduced in respect of Si.
- Very high temperature handling capability, leading to simplified thermal management as well as improved system reliability.

So as maximum efficiency is desired, a SiC MOSFET has been selected. To perform a correct efficiency comparative, a transistor that could be used in all the topologies has been chosen, in order to have exactly the same parameters to be able to compare only in the terms elected (topology, frequency and irradiance). The most restrictive case of all topologies is the central inverter, because the transistors must be able to stand all the voltage ($V_{oc\ max} \simeq 750V$) and to deliver all the power. The parameter values of the MOSFET are available in its datasheet [18].

To simulate this transistor, the thermal module provided by PSIM software has been used. This module provides the possibility of simulating a non ideal transistor and its thermal behaviour. The losses can be included following the values provided by the datasheet. Figure 5.1 shows the thermal module for one transistor.

The outputs of the module are described as:

- **P-cond-Q** is the conduction loss of the transistor.
- **P-sw-Q** is the switching loss of the transistor.
- **P-cond-D** is the conduction loss of the internal diode.
- **P-sw-D** is the switching loss of the internal diode.

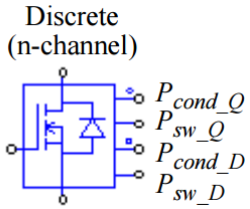


Figure 5.1: Thermal module symbol and outputs

5.1.2.1 Conduction losses

Despite the purpose of this thesis is not to deepening into the internal devices model, simplified models of MOSFET transistor and its intrinsic diode are shown in figures 5.2 and 5.3. The elements responsible of conduction losses are the internal resistance from drain to source of the transistor (R_{ds}) when the transistor is conducing, and the internal diode resistance (R_{dd}) and diode voltage fall (v_d) when the diode is conducing.

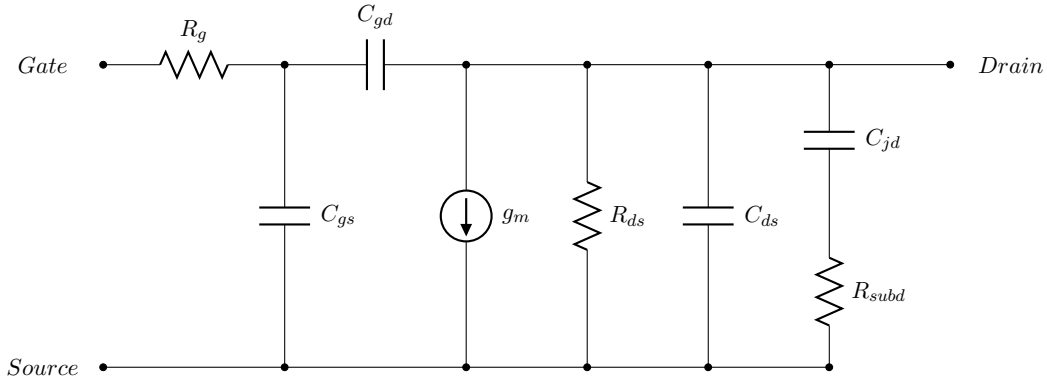


Figure 5.2: Simplified MOSFET Transistor Circuital Model

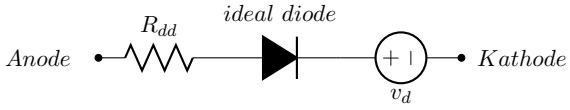


Figure 5.3: Simplified Diode Circuital Model

As both elements present a resistive opposition to current circulation, the losses will be quadratic with the current and can be calculated with the equation 5.2.

$$Conduction\ loss = R_{ds}I_{rms}^2 + R_{dd}I_{drms}^2 + I_{drms}v_d \tag{5.2}$$

Where I_{rms} is the current circulating through the transistor, and I_{drms} is the recirculating current through the intrinsic diode. If the transistors are working correctly, the intrinsic diode will never conduce, therefore, the only conduction losses will be those derived from R_{ds}. The value of $R_{ds} = 98m\Omega$ is taken from the datasheet [18]. This value is the maximum for the range of temperatures where the system will work, and it must be put into the thermal module model of PSIM.

5.1.2.2 Switching losses

Switching losses are those that the transistors develop during their transition between conduction and open circuit. The elements responsible of these losses are the intrinsic capacitors of the model shown in figure 5.2, C_{gd}, C_{gs} and C_{ds}. These values can be taken from the datasheet of the transistor, but they are not given by themselves. The values given are C_{oss}, C_{iss} and C_{rss}. The relation between these values and the capacitor of the transistor model are exposed in equation 5.3.

$$C_{oss} = C_{ds} + C_{gd} \qquad C_{iss} = C_{gs} + C_{gd} \qquad C_{rss} = C_{gd} \tag{5.3}$$

There are lots of ways to calculate the power dissipated during transitions in a MOSFET, depending on the topology of the converter or the application where the transistor is used. However, the most simple is shown in equation 5.4.

$$P_{sw} = (E_{on} + E_{off})f \tag{5.4}$$

Where E_{on} is the necessary energy to turn-on the MOSFET, and E_{off} is the energy necessary to turn-off it. This is the equation used for PSIM to calculate the losses. The values for E_{on} and E_{off} are provided by the datasheet of the MOSFET [18], but, however, this value depends on the voltage V_{ds} present in the MOSFET. The energy stored in a capacitor can be calculated by equation 5.5.

$$E_{cap} = \frac{1}{2}CV^2 \tag{5.5}$$

This equation could be used to make a simplified calculation of the energy necessary to turn-on and turn-off the transistor. Using C_{oss} and C_{iss} with their respective voltages V_{ds} and V_{gate}. In any case, whatever expression is used by PSIM, the values of the components provided by datasheet have been introduced, and the results can be compared because the formula will be the same for all the transistors. The important point here, is to have into account that switching losses depend directly from V_{ds} voltage, the capacitor values and and the switching frequency.

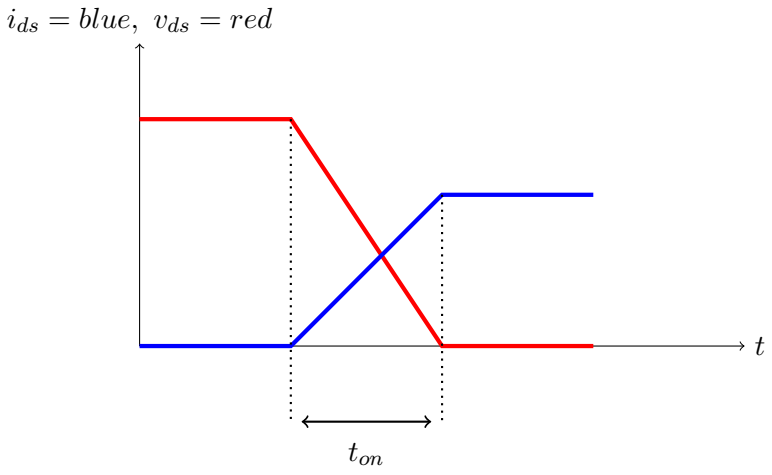


Figure 5.4: Switching loss in a MOSFET during turn-on time

Figure 5.4 shows the voltage from drain to source of the transistor (v_{ds}) and current through it (i_{ds}). The simplified waveforms during the turn-on time of a MOSFET are shown. It can be seen, that the losses depend also on the current that is circulating through the transistor, because during the time when the voltage transistor is not zero, the transistor is working in its ohmic zone, and therefore is dissipating power. The product $v_{ds} \cdot i_{ds}$ is the power dissipated

during the on-off or off-on transitions. In power transistors, this is the most important part of the switching losses.

5.1.2.3 Temperature

The thermal information is provided in terms of output currents. Therefore, the circuital representation of thermal resistances must be implemented, in order to extract the temperature information in terms of voltage. An example of the circuit for one transistor that has been implemented in this thesis is exposed in figure 5.5.

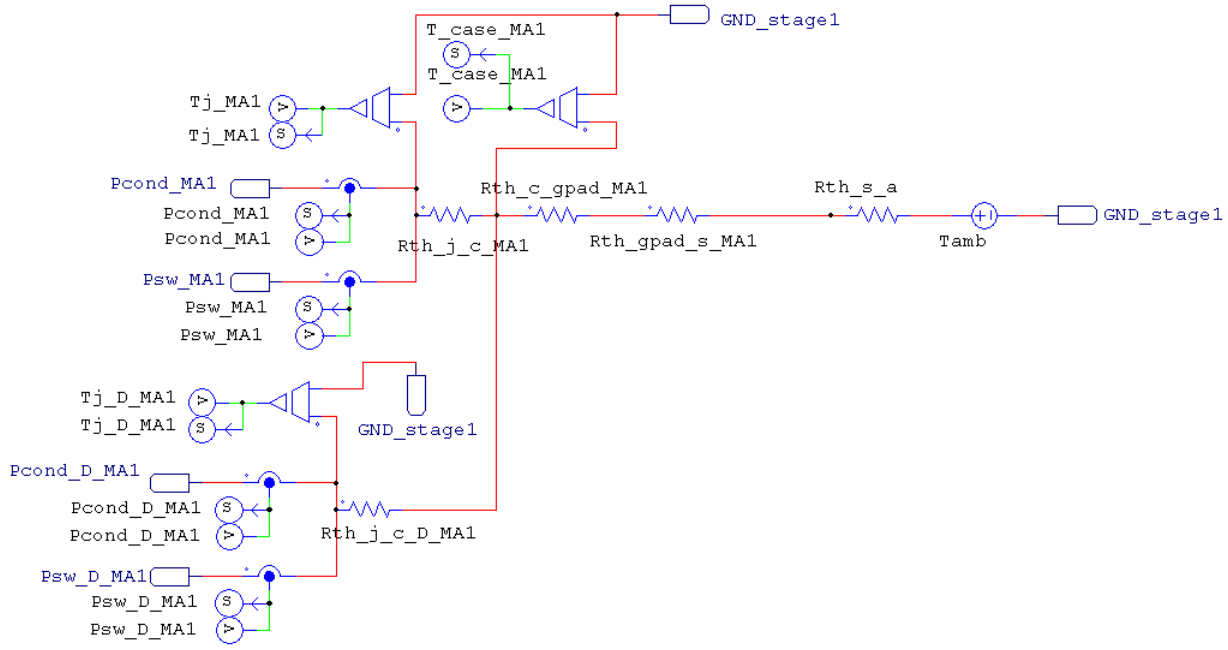


Figure 5.5: Thermal module symbol and outputs

The different thermal resistances that appear in figure are:

- **R-th-j-c** is the thermal resistance from junction to case for the transistor. This value is provided by the transistor datasheet. $R_{th\ j-c} = 0.65^{o}C/W$.
- **R-th-j-c-D** is the thermal resistance from junction to case for the intrinsic diode. This value is provided by the transistor datasheet. As it is the same device, the value is the same as for the transistor. $R_{th\ j-c.D} = 0.65^{o}C/W$.
- **R-th-c-gpad** is the thermal resistance from case device to gap pad insulator. Despite this value is not provided by the transistor datasheet, it can be found in an equivalent (CMF20120D) from the same family. The value is $R_{th\ c-gpad} = 0.25^{o}C/W$.
- **R-th-gpad-s** is the thermal resistance from insulator to the heating case. The model taken into account in this thesis is KU-KG38 [19]. The value of the thermal resistance can be taken from the datasheet. After applying the corresponding correction indicated in the datasheet, the value is rounded to $R_{th\ gpad-s} = 0.2^{o}C/W$.
- **R-th-s-a** is the thermal resistance from heating surface to ambient. This is the last dissipation step. The value can be taken from the curves of the datasheet [20] having into account that the fan is feed at $12V$. $R_{th\ s-a} = 0.68^{o}C/W$.

However, the main idea that must be taken is that all the results that are calculated in this thesis are dependant on the thermal model of the PSIM MOSFET.

5.2 Comparative Results

The results extracted from this comparative have been computed to show them graphically.

5.2.1 Conduction losses

Figures 5.6, 5.7 and 5.8 show, at the left side, the conduction losses for one of the MOSFETS that are working in the topology, and at the right side of this graph there are the total conduction losses for all the MOSFETS that work in the topology. Figure 5.9 shows a comparative of the total conduction losses for the three topologies.

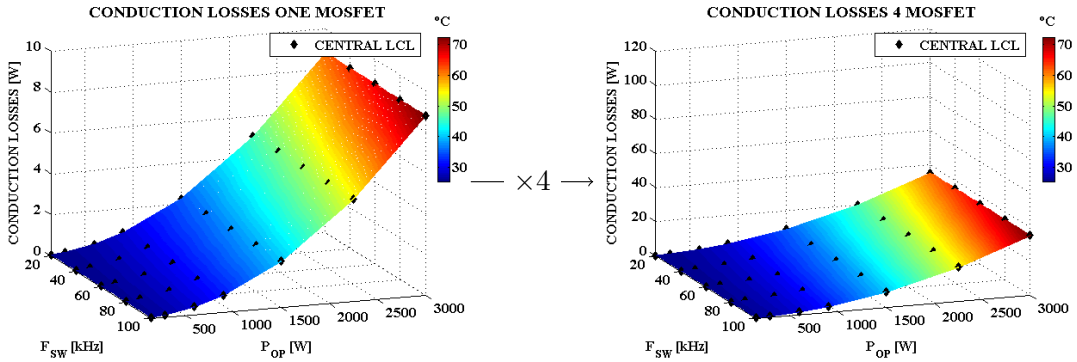


Figure 5.6: Conduction losses for central inverter topology

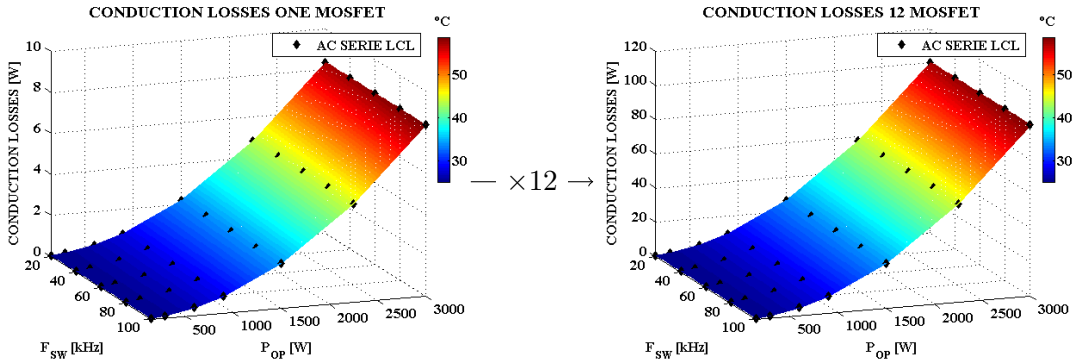


Figure 5.7: Conduction losses for series connected inverters topology

As can be seen, the conduction losses are quite significant. Especially for the case of the series connected inverter topology, where the losses are close to $100W$. The conduction losses depend on the current that flows through the transistors. In the central and series topologies, this current is the total extracted current, for that reason the losses in only one of the MOSFETS are very similar for both cases. However, the total conduction losses are lower for the case of the central topology because only uses four MOSFETS. Series connected inverter topology uses twelve MOSFETS, so the total losses are three times higher than for the central topology. For the case of the parallel connected inverter topology, the losses are lower because only the third

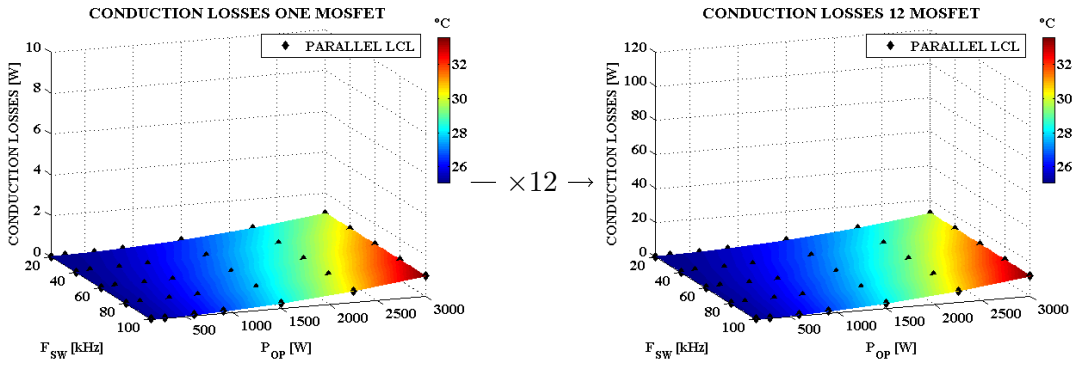


Figure 5.8: Conduction losses for parallel connected inverters topology

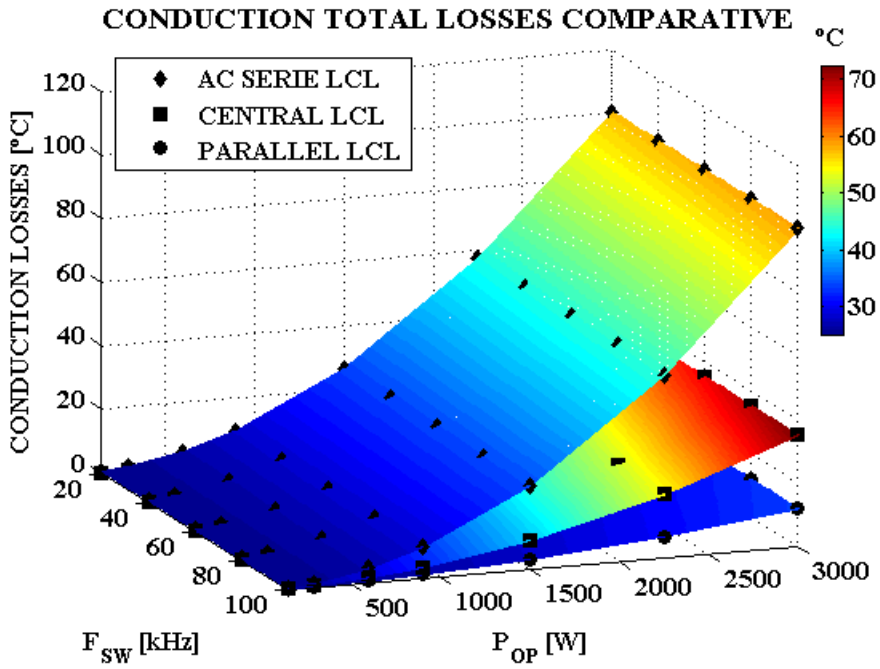


Figure 5.9: Total Conduction Losses Comparative

part of the current circulates for the transistors. Then, finally the parallel topology presents less conduction losses than the other topologies, as it can be seen in figure 5.9.

5.2.2 Switching losses

Figures 5.10, 5.11 and 5.12 show the switching losses for the three topologies. As in previous section, the losses are presented for one of the transistors and at side for all the transistors of the topology.

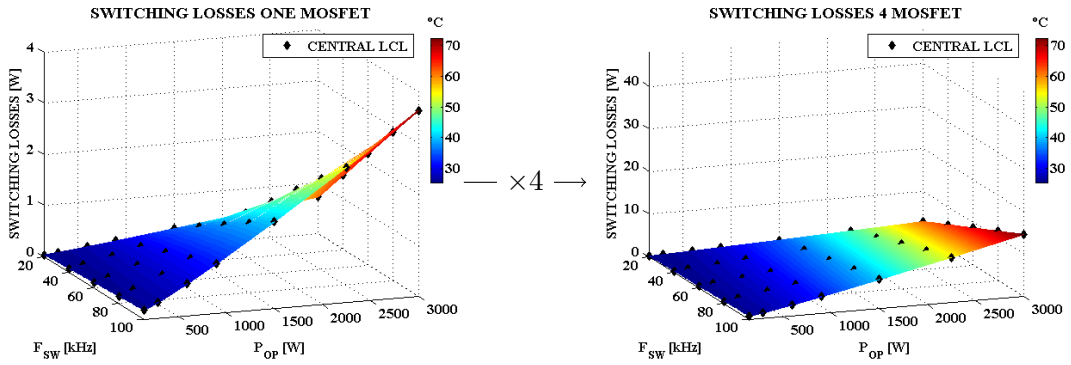


Figure 5.10: Switching losses for central inverter topology

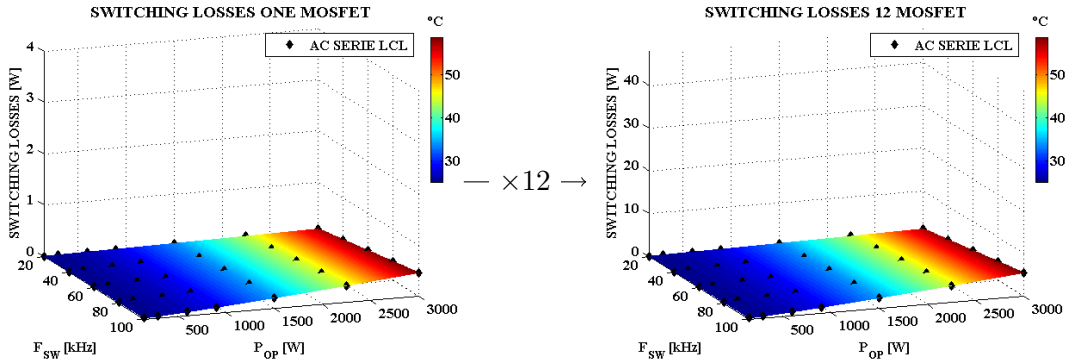


Figure 5.11: Switching losses for series connected inverters topology

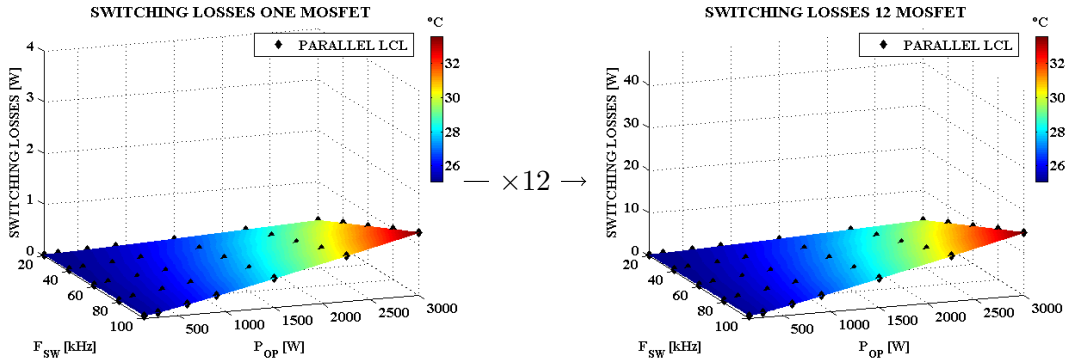


Figure 5.12: Switching losses for parallel connected inverters topology

As it can be seen, the switching losses are much lower than the conduction losses. This is because the silicon carbide transistors have the values of the parasitic capacitances very optimized, more than the channel resistance. Therefore, the conduction losses dominate over the switching losses. For the case of one single transistor, central inverter topology presents the higher losses, this is because the V_{ds} voltage is the maximum and all the current is circulating through them,

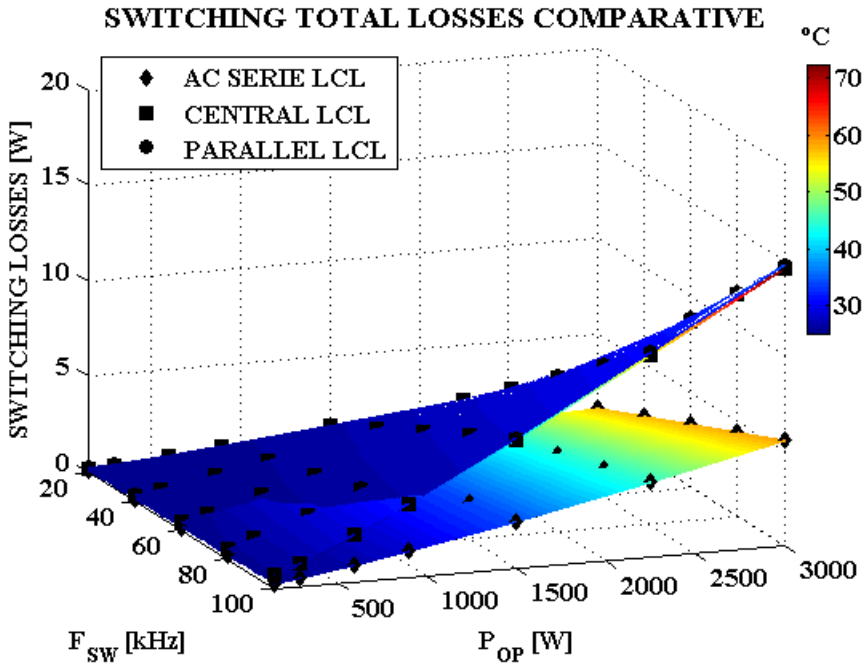


Figure 5.13: Total Switching Losses Comparative

therefore, during the transition time, the losses are the maximum that there could be. As these losses depend directly and quadraticly on the V_{ds} voltage over the transistors, the series connected inverter topology presents the smaller losses. For the case of the parallel connected inverters topology, despite the transistors work with the maximum V_{ds}, the current is divided by the number of stages, so during the transition time, the switching is not as hard as it is for the central inverter topology.

However, as the central inverter topology just uses four transistors, and the parallel uses twelve of them, the switching losses are finally similar, as can be seen in figure 5.13. For the case of switching losses, the series connected inverter topology is the most efficient. This is, thanks to the lower V_{ds} voltage, which leads to extremely low losses.

5.2.3 Junction Temperature

Despite the temperature of one of the MOSFETS for each topology has been exposed in all the previous figures, most accurate graphics are provided in 5.14 and 5.15.

This figures and previous ones, show that the colder transistors are the parallel connected inverter topology. The central inverter topology is the worst for that case, this is because all the current and the voltage affect the transistors, and the losses are distributed only between four transistors, and not twelve as in the other cases. For that reason, these transistors will work with more temperature stress than the others. The series connected inverters topology has an intermediate temperature between the temperatures of the other topologies, this is because the losses for one transistor are slightly less than for the central inverter topology, but the losses are distributed between twelve transistors.

However, the total temperature for all the topologies is not bad, the maximum temperature for one device is just near the 70^oC, and this is a good working temperature for a transistor.

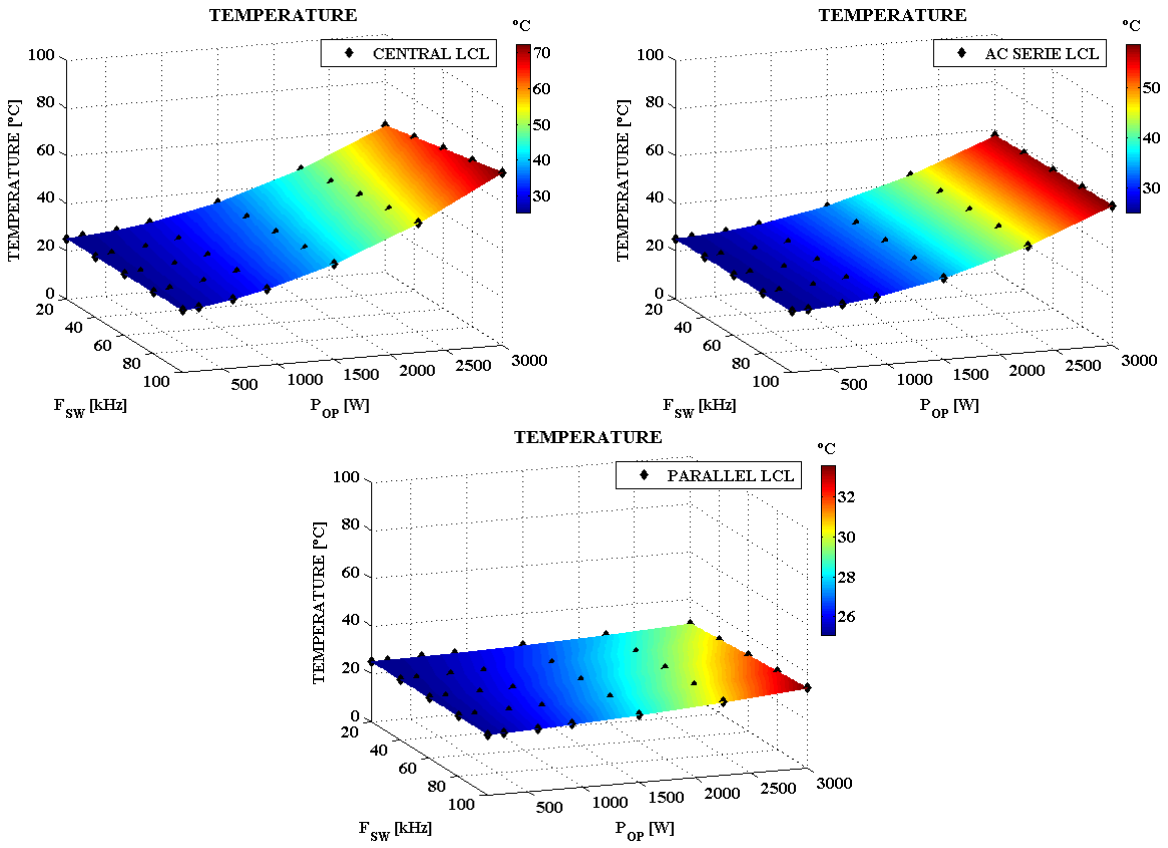


Figure 5.14: Temperature for one transitor for each topology

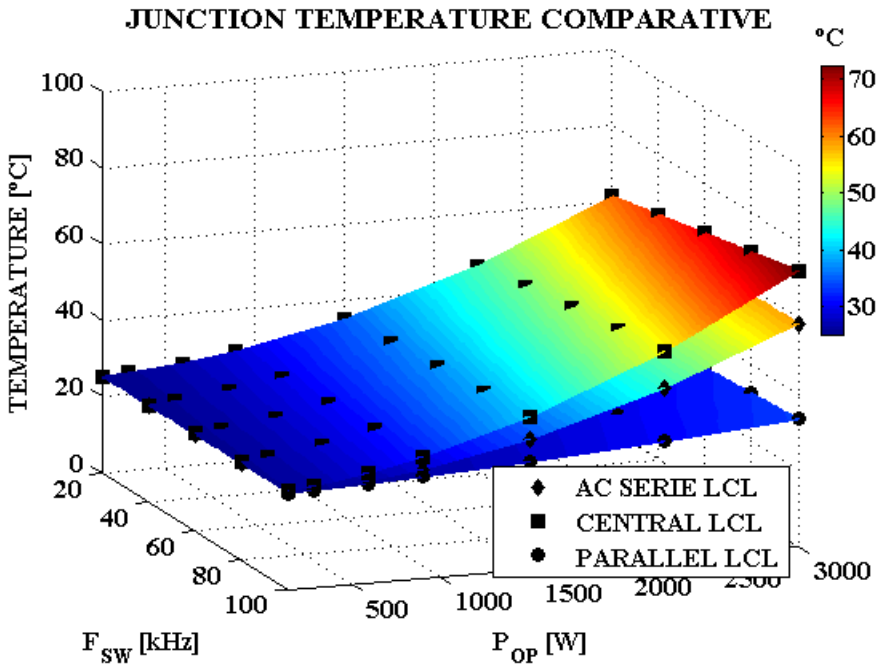


Figure 5.15: Comparative of temperature for one transistor

However, as said before, the absolute values of the simulations results are subject to the models

that PSIM uses, and can differ from the real results.

Finally, it must be said that the parallel topology had the advantage that its nominal duty generator "knew" exactly the values of the losses and the other components. This means that the possible reactive power that could be derived was completely cancelled for this comparative. That was a littler advantage it had, in terms of control.

5.2.4 Global Efficiency

The global efficiency of the system for the three topologies, is evaluated having into account the losses shown until now, and the losses in the inductors and capacitors. Figures 5.16 and 5.17 show the efficiency for each topology by separate and together.

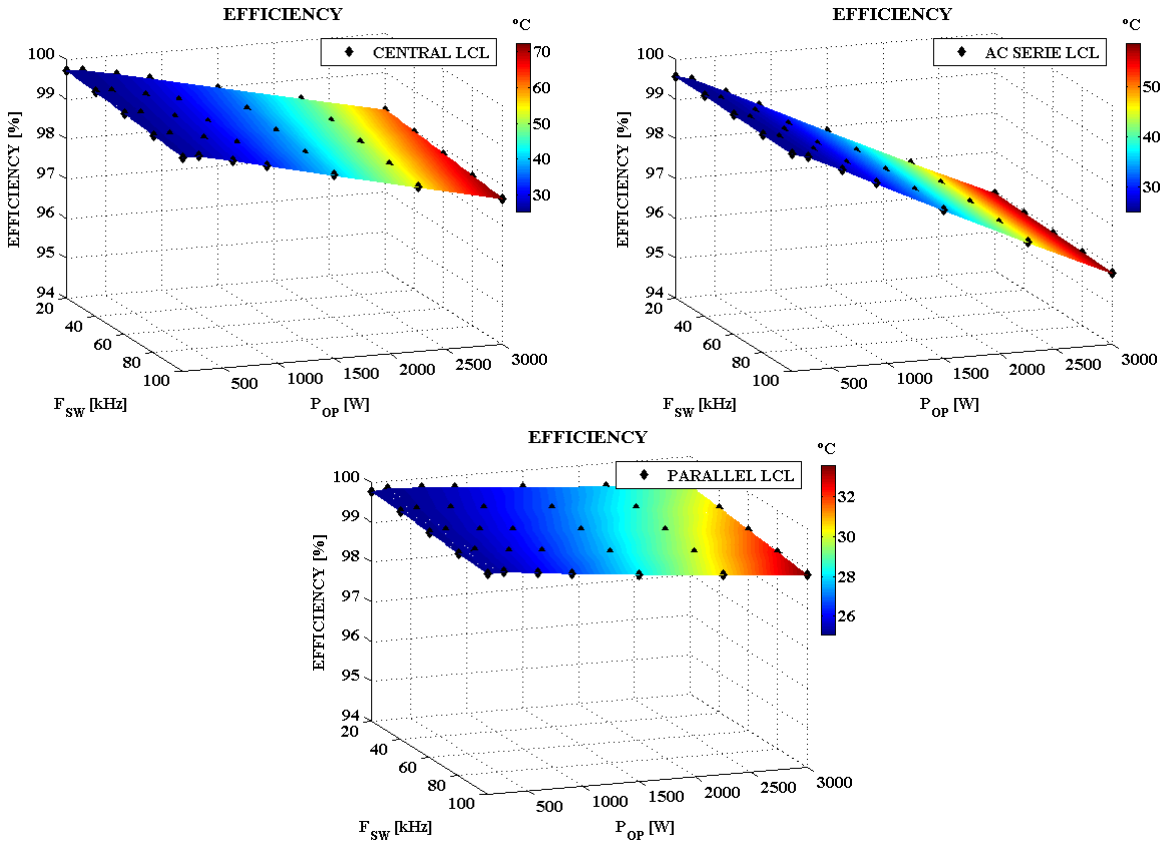


Figure 5.16: Global efficiency for each topology

As can be seen, the best efficiency is performed by the parallel connected inverters topology. This was an expected result having seen the switching and conduction losses results, and confirm that the conduction losses are the dominant losses. As the current augments quadraticly the conduction losses and in the parallel topology this current is divided by the number of stages (three in this case), the losses decrease significantly. This conduction losses for each MOSFET were similar for the central an series connected inverter topologies, as the current through them is the same and is the total output current (excepting the little LCL capacitor current), but, for the case of the series topology, the current circulates through twelve transistors, and it makes this the less efficient topology.

As the switching losses are not high, the efficiency does not fall a lot when augmenting the

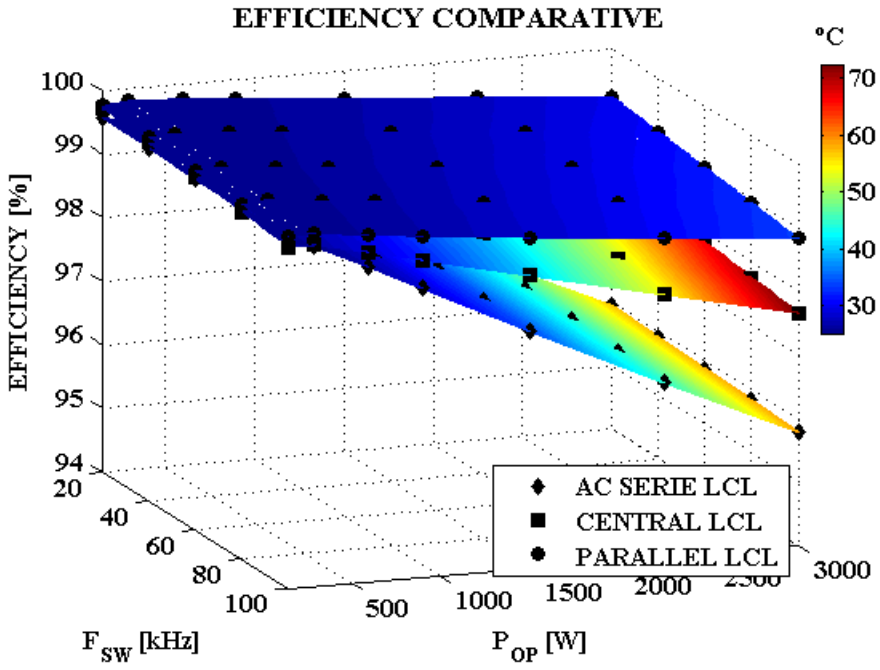


Figure 5.17: Global efficiency comparative

switching frequency. In the other hand, for more output power, the topologies where the conduction losses are higher, present a worse efficiency. For sure, the characteristics of silicon carbide MOSFETS have helped to dominance of the conduction losses. If the switching losses had a more important paper, the series topology would improve its efficiency in respect to the other topologies.

5.2.5 Euro-Efficiency

As exposed in section 5.1.1, the Euro-Efficiency is tested with the output power values shown in tables 1.1, 1.2 and 1.3 and through the equation 5.6 for each topology. The results of the previous simulations at different switching frequency have been used to calculate this parameter for each topology. The results are shown in figure 5.18.

$$\eta_{euro} = 0.03\eta_{5\%} + 0.06\eta_{10\%} + 0.13\eta_{20\%} + 0.1\eta_{30\%} + 0.48\eta_{50\%} + 0.2\eta_{100\%} \tag{5.6}$$

The euro-efficiency, similarly to the global efficiency, shows that the most efficient topology is the parallel connected inverters topology. However, the series inverter topology is the one which has the best evolution when augmenting the switching frequency. This coincides with the fact that this topology has the lower switching frequency losses. However, its Euro-efficiency is always lower than for the other topologies, which coincides with the results shown for the global efficiency.

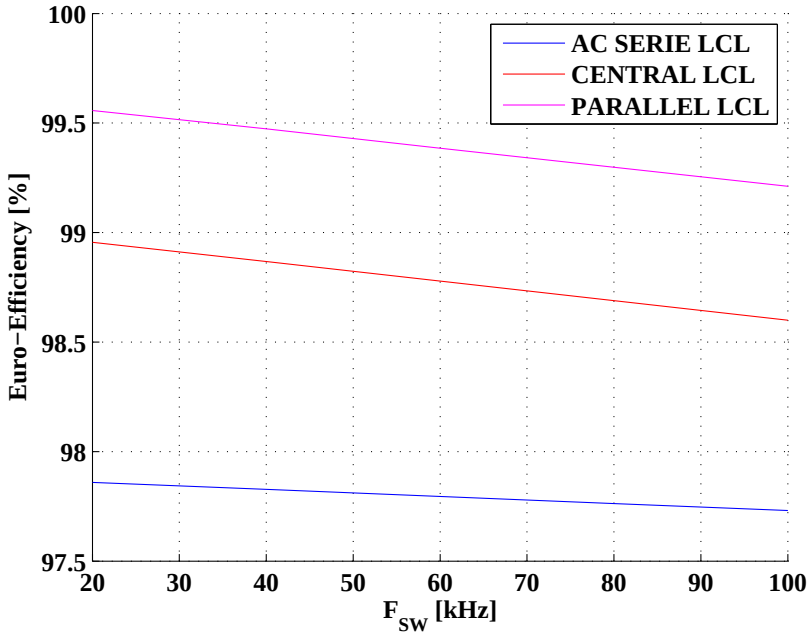


Figure 5.18: Euro-effiency performance comparative

5.2.6 Output Ripple

The evaluation of the output ripple is a must due to the importance of giving to the grid a clean power (free of undesired harmonics) in order not to create problems to other electronic equipments or machines connected to the same grid. Figure 5.19 shows the output ripple for all the topologies at maximum output power ($3000W$).

The amplitudes of the total output current differs because of the efficiency difference between them. The best ripple is presented by the series inverter topology. The modulation strategy applied in this topology helps to reduce it much better than the other ones. The phase shifting applied to the parallel connected inverter topology helps to reduce it, but it does not cancel it as could be expected. If the currents were continuous currents, then the phase shifting would cancel all the ripple if the stages currents were equal. But, in this case, the currents are sinusoidal, and therefore, the ripple is not cancelled at all, but it is reduced substantially. The worse ripple is for the central inverter topology, it was an expected result, as any modulation strategy can be applied on this topology.

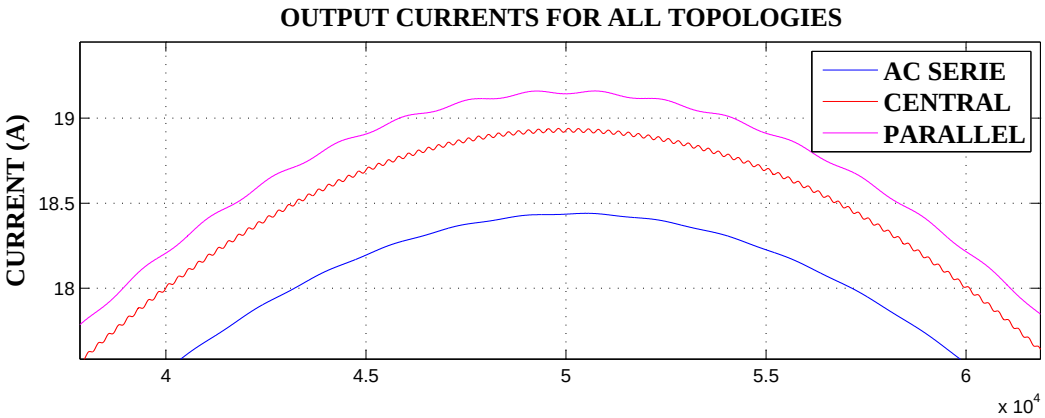


Figure 5.19: Output ripples for each topology

Chapter 6

Conclusions and future works

6.1 Conclusions

In this thesis, the subjects reviewed are:

- A little review about renewable energies and solar panel technology has been done.
- The control of the previously studied topologies (central and series inverter connection) has been redesigned to work under an LCL filter. The benefits of this filter have been proved. The harmonic content of the injected current much smaller than it was when a single inductor was used to connect the inverters to the grid.
- A dissertation about what is the best choice for the values of the stages inductors in the parallel connected inverters topology has been done. Techniques of phase shifting has been proposed in order to reduce the ripple in the injected current without using the too big value given by the theoretical calculation.
- The problems found for the proportional resonant control that was used in central and series inverter topology, have been corrected through a circuital analysis. This has allowed the implementation of a nominal duty generator in charge to generate the modulation signals for each phase.
- A new control has been developed for parallel connected inverters topology sharing the LCL filter. This control corrects the phase problems that the nominal duty generator presented. The amplitude of the currents is not directly controlled by this internal phase control, but it has been demonstrated that the external control is capable to do it, so the system gets stable conditions in any case. However, the complexity of the control and the computation requirements (great amount of trigonometric operations) make it undesirable.
- The main problem that the parallel topology presents, is the impossibility of controlling the stages currents without sensing them. This leads to a bad behaviour and a poor efficiency when the sensing of grid voltage has small variations (close to 1%). Thus, a very precise grid voltage sensing is required. This is not a suitable characteristic. However, if the grid voltage is properly sensed, the phase difference between stages currents can be minimized by inserting the losses estimation into the calculus, and, thanks to that, the behaviour of the system is acceptable.

- An efficiency and performance comparative has been implemented between the three topologies studied. The parallel connected inverters topology presented in this thesis has been the most efficient topology of the three tested. This justifies the investigation done over this topology and the LCL filter performance. Despite the control of this topology must be studied deeper as is not suitable at all, if the topology can work properly, better efficiencies can be achieved
- The parallel connected inverters topology proposed in this thesis requires more inductive components than the other ones. As these inductors are big, this leads to a more expensive system than for the other cases. However, it can be compensated because the MOSFETS had lower temperature than in the other topologies, and lower temperature means lower heatsink, which is another expensive component.

6.2 Future works

Following the studies exposed in this thesis thesis, the proposed future works are the next ones:

- The practical implementation of the parallel topology.
- In this thesis, the control of new inverter connection topology has been explored. Lots of problems were found at the time of reproducing the proportional-resonant control over the parallel connected inverters sharing the LCL filter. But, despite this, perhaps there is a way to make it work, so deepening on this control is a possibility.
- Consider the modifications of the topology when it is not connected to the grid and is only used to feed other load types.
- The mathematical explanation about the phase control for the parallel topology must be implemented.
- Consider the controllability of the different stages currents with the proposed control is another possibility.
- The performance of the parallel connected inverters topology and its control must be tested for different unpredictable problems that could appear. For example, voltage sags.

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