NOTICE: this is the author's version of a work that was accepted for publication in Microelectronic Engineering. Changes resulting from the publishing process, such as peer review, editing, corrections, structural formatting, and other quality control mechanisms may not be reflected in this document. Changes may have been made to this work since it was submitted for publication. A definitive version was subsequently published in Microelectronic Engineering, VOL 150, DOI 10.1016/j.mee.2015.11.006

Experimental and theoretical analysis of the electrical properties behavior with the temperature of organic thin-film transistors based on tetraphenyldibenzoperiflanthene deposited at different substrate temperatures

W.Boukhili[1, 2,*], M. Mahdouani[1], R. Bourguiga[1], J. Puigdollers[2]

[1]Laboratoire de Physique des Matériaux : Structure et Propriétés, Groupe Physique des Composants et Dispositifs Nanométriques, Faculté des Sciences de Bizerte, 7021 Jarzouna-Bizerte, Université de Carthage, Tunisia.

[2]Department d'Enginyeria Electronica, Universitat Politecnica de Catalunya, C/Jordi Girona, Modul C4, 08034 Barcelona, Spain.

ABSTRACT

A series of inverted-staggered (top contact) p-channel organic thin film transistors based on small molecule tetraphenyldibenzoperiflanthene (DBP) as an active layer have been fabricated by thermal evaporation at different substrate temperatures (300, 330, 360 and 390K). In this work, these devices have been electrically characterized at different temperatures from 300K to 370K in steps of 10K under vacuum. The influences of the temperature on the electrical performance of DBP-TFTs have been investigated in saturation regime. We found that the p-channel DBP-TFTs deposited at a substrate temperature (T_{sub}=390K) exhibited a better performance under an measurement temperature of 370K, where μ_{FET}, V_{th} and the ratio current were approximately 8.5x10^{-4} cm^{2}V^{-1}s^{-1}, -0.33V and 3x10^{6}, respectively. The field effect mobility of these types of devices is strongly dependent on temperature and follows the simple Arrhenius law. Additionally, the temperature-dependent electrical measurements performed on these devices reveal a thermally-activated behavior for each substrate temperature. This suggests that the charge transport in the examined devices occurs via hopping between localized states. The obtained results demonstrate well that the deposition conditions of organic active layer can improve well the device performance. Finally, an analytical model has been developed to reproduce the dependence of the total resistance and the current-voltage characteristics with the temperature and to understand the charge transport in the DBP-TFTs. The obtained data are in good agreement with the experimental results for all fabricated devices.

Keywords: DBP-OTFTs; Electrical parameters extraction; Thermally activated behavior; Analytical modeling.

* Corresponding author: wboukehili@yahoo.fr (Walid Boukhili).

1. Introduction

At present, the technologies of organic devices such as light-emitting diode (LED), organic photovoltaic cells (OPVCs) and organic thin-film transistors (OTFTs) have attracted widespread interest as a promising candidate to replace the conventional silicon technology. Among them, OTFTs have attracted a great deal of attention by the world industries and research organization due to their many advantages, including light-weight, low-cost production, mechanical flexibility and low temperature processing [1-3] allowing them to integrate within many technology applications such as sensors of temperature, pressure, gas and humidity, smart cards, flat panel displays and radio-frequency identification tags [4-8]. Roughly speaking, conjugated polymers and small-molecules are the most commonly used as active layers of OTFTs. Indeed, a best organic device performance has been obtained with materials belonging to the n or p-type small molecule category. For the p-type, the family of acenes is widely used as a hole transport material, among them the pentacene is a star molecule [9-12] showing high values of mobility and relatively good stability [9]. Particularly, the highest reported mobility in pentacene is about $3 cm^2 V^{-1} s^{-1}$ [12]. Alongside of the pentacene, other small-molecules (n or p-type) such as fullerene (C_{60}) [13], copper phthalocyanine (CuPc) [14-15] and N, N-ditridecylperylenediimide (PTCDI-$C_{13}H_{27}$) [16] are reported as a good candidates for the semiconductor layer in OTFTs devices. On the other hand, a numerous collection of donor organic materials have been developed and studied in the previous decade. In particular, tetraphenyldibenzoperiflanthene (DBP) has appeared as a promising electron-donor material for photovoltaic applications [17-20]. More recently, organic thin-film transistor based DBP (DBP-OTFTs) was fabricated in order to characterize the DBP the DBP thin-films [17]. In order to improve the performance of the OTFTs, several studies have focused on the effects induced by intrinsic factors such as humidity, illumination and temperature [16-24], as well as the nature of the dielectric layer and source-drain electrodes [25-26]. In order to understand the transport phenomena in the OTFTs, the behavior of the carrier mobility as function various gate voltages/carrier density and temperature has been widely studied [27-30].

In the present study, we report and analyze the results of an experimental study performed on the DBP-TFTs. Firstly, the electrical performance changes of the DBP-TFTs deposited at different substrate temperatures (T_{sub} = 300K, 330K, 360K and 390K) were examined in a wide range of temperature from 300K to 370K in steps of 10K, a detailed description of

current-voltage characteristics and electrical parameters of DBP-TFTs as a function temperature has been presented. Possible causes for the observed effects are discussed. Accordingly, the influences of temperature on various device performance metrics of the DBP-TFTs such as threshold voltage, trapped charge density, field effect mobility, contact resistance, current ratio, subthreshold slope, interface trap density and the turn-on voltage were systematically evaluated at V_D = -20 V for different substrate temperatures. Finally, in order to determine the charge transport mechanisms in these type of devices. From the measurement current-voltage characteristics of organic thin film transistors, we have modeled the total device resistance, as a function of the gate voltage and the temperature, based on a variable range and hopping (VRH) model. Furthermore, we have reproduced very well the current-voltage characteristics of organic thin film transistor based on small molecule tetraphenyldibenzoperiflanthene.

2. Experimental details

A schematic structure of the OTFTs processed in this study is given in fig. 1(a).

Fig. 1 (b) shows the chemical molecular structure of the small molecule tetraphenyldibenzoperiflanthene (DBP). The material was commercially available from Sigma Aldrich chemical with a purity of 98%, and it was used without any further purification process. All devices were built on highly doped n-type (n^+-Si) wafer substrate that simultaneously serves as a bottom-gate electrode. A 230 nm-thick layer of SiO_2 is grown on silicon by thermal oxidation, and used as a gate insulator layer. Thereafter, the tetraphenyldibenzoperiflanthene (DBP) thin film were deposited by thermal evaporation through a shadow mask with a base chamber pressure of $5x10^{-6}$ mbar. The deposition rate was $5Ås^{-1}$ and the total deposited thickness was 50nm, which are monitored by means of a surface profilometer (Veeco Dektak 150). The substrate temperature was varied in the range of 300K to 390K during the deposition of DBP active layers. The process is completed by the source and drain Au (80nm) electrodes, which were deposited by thermal evaporation on the DBP thin film for inverted staggered configuration (bottom gate top contact) using a shadow mask that defines a channel length (L) and width (W) of 80µm and 2000µm, respectively. All current–voltage characteristics of the fabricated OTFTs were performed in dark and vacuum (10^{-1}mbar) conditions by means of a parameter analyzer (model HP5156). The device temperature was varied from 300K to 370K in steps of 10K by means of an MMR Technologies controller (model K-20) [17].

3. Results and discussion

3.1. Influence of temperature on DBP-TFTs current-voltage characteristics

In this section, the temperature dependent current-voltage characteristics such as output and transfer characteristics of the DBP-TFTs deposited at different substrate temperatures (T_{sub}=300, 330, 360 and 390K) are presented.

3.1.1. Output characteristics

Fig. 2(a)-(d) show the output characteristics(drain current (I_D) versus drain voltage (V_D) curves) of the fabricated DBP-TFTs at different substrate temperatures (T_{sub}) (device A (T_{sub}=300K), device B (T_{sub}=330K), device C (T_{sub}=360K) and device D (T_{sub}=390K)) that were measured under vacuum by varying the drain voltage (V_D) from 0 to -20V in -0.2V increments for different gate voltages (V_G) of 0 to −40V with −8V increments. All the obtained output characteristics exhibit the expected behavior for a p-channel field effect transistor. As seen in fig. 2(a)-(d), at low drain voltage, the drain current follows ohm law; it is therefore proportional to both the gate and drain voltages. As the drain voltage increases, the voltage drops at drain decreases to a point at which it falls to zero. At this point, which occurs when the drain voltage approaches the gate voltage, there is a pinch off of the channel, and the channel current becomes independent of the drain bias. This regime is called saturation regime. From fig. 2(a)-(d), it's clear that I_D was improved by increasing the measurement and deposition temperatures.

3.1.2. Temperature dependent transfer characteristics

The transfer characteristics for the four fabricated DBP-TFTs (device A (T_{sub}=300K), device B (T_{sub}=330K), device C (T_{sub}=360K), device D (T_{sub}=390K)) are depicted in fig. 3(a)-(d) at a fixed drain voltage V_D= -20V in which the gate voltage (V_G) varied from 0 to -30V with a 0.3V increments, while sweeping the temperature from 300 to 370K in step of 10K. Fig. 3(a)-(d) shows that the drain current in the saturation regime (V_D= -20V) was significantly improved as the measurement temperature was increased from 300 K to 370K and as substrate temperature was increased from 300K to 390K.

Fig. 4 (a)-(d) shows the variation of the drain current as a function of 1000/T in the above threshold regime (V_G<V_{th}). As seen in fig. 4 (a)-(d), the drain current with temperature is showing Arrhenius-type dependence. For all devices (A, B, C and D), the Arrhenius-type

dependence at V_G = -28V has a slope around to 0.12eV (device A), 0.23eV (device B), 0.33eV (device C) and 0.57eV (device D).

3.2. Influence of temperature on DBP-TFTs electrical parameters

To analyze the temperature dependence of the fabricated device (A, B, C and D) electrical parameters in more detail, we determined all the electrical parameters of the BDP-TFTs depending on the temperature for each deposition temperature in the saturation regime (V_D= -20V).

3.2.1. Threshold voltage and trapped charge density

The threshold voltage (V_{th}) value of the studied DBP-TFTs at various temperatures was determined from the plot of square root of the drain current versus gate voltage ($|I_{D,sat}|^{1/2}$ vs. V_G) under V_D= -20V for each substrate temperature as shown fig. 5(a). From fig. 5(a), one can see that the threshold voltage is shifted to a smaller value (less negative) when the temperature is increased from room temperature (RT) to 370K. This shift in threshold voltage with temperature was attributed to the shallow trapped charge at the insulator/organic semiconductor interface [27, 31-32], which can be determined according to the equation below [21, 30]:

$$N_{trap.charge} = \frac{|V_{th}|Ci}{q} \quad (1)$$

where C_i is the insulator capacitance per unit area and q is the electronic charge.

The extracted values of $N_{trap.charge}$ are shown in fig. 5(b).

3.2.2. Field effect mobility versus temperature

Field effect mobility is the key device parameter affecting performance in any OTFTs. The temperature dependence of field effect mobility provides one of the most important indications about the charge transport behavior for an organic semiconductor.

At high constant drain voltage V_D= -20V (saturation regime), the slope of the square root of $|I_D|$versus V_G is used to extract the mobility according to the following equation:

$$\mu_{sat} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_D}}{\partial V_G}\right)^2 \quad (2)$$

The extracted field effect mobility is plotted in the Arrhenius plot versus the temperature at V_G =V_D= -20V for various substrate temperatures in fig. 6. The extracted mobility shows a thermally activated behavior for each substrate temperature in almost rang of the temperature (fig. 6). Among the treated devices, the obtained highest mobility is 8.5x10^{-4} cm^2V^{-1} s^{-1} under an temperature of 370K and a substrate temperature of 390K (device D), which is rather

similar to that reported in [19, 33] by comparing with mobility $3x10^{-6}$ cm^2 $V^{-1}s^{-1}$ of as-deposited device under a substrate temperature of 300K and treated at 300 K, as seen in fig. 6. It was found that the field effect mobility increased with increasing temperature. This increase of the mobility can be due to the enhanced carrier density and better crystalline quality of the conducting channel at high deposition temperature [34]. Indeed, this behavior can be due to the well ordered crystalline phase of the organic layer under high deposition and measurement temperatures [35]. From fig. 6, it's clear that the extracted field effect mobility of the DBP-TFTs clearly follows the simple Arrhenius relationship in which the activation energy expressed as $\mu_{FET} \propto \mu_0 exp(-E_a/k_B T)$ [36], with μ_0 being the specific mobility, E_a is the activation energy and k_B is the Boltzmann's constant. By fitting the data of fig. 6, the activation energy (E_a) can be determined to be 0.11eV for T_{sub}=300K, 0.22eV for T_{sub}=330K, 0.34eV for T_{sub}=360K and 0.54eV for T_{sub}=390K. The activation energy is substantially increased when the temperature is increased up to 360K. This behavior can be well explained by the fact that the charge carriers are trapped in localized states in the exponential tail of the density of state (DOS) and the thermal activation process in mobile states [17, 28, 37].

3.2.3. Contact resistance versus temperature

To discuss the dependence contact resistance of the DBP-TFTs with the temperature, we evaluated the total resistance of the fabricated devices from the linear region (V_D= -5V) in the output characteristics ($R_{tot} = [\frac{\partial V_D}{\partial I_D}]^{V_G}_{V_D \to 0}$) for high negative gate voltage (V_G= -40V) and the expression of the contact resistance of the DBP-TFT is given by [15, 38] :

$$R_c = R_{tot} - \frac{L}{WC_i \mu_{FET}(V_G - V_{th})} \quad (3)$$

where μ_{FET} is the field effect mobility.

Fig. 7 shows the obtained values of the contact resistance (R_c) versus the temperature for the four fabricated devices (device A, device B, device C and device D). We found that the contact resistance decreases with increasing temperature for each substrate temperature. The decrease behavior in the contact resistance can be due to the charge carrier transport near to the contact region, analogous to the thermally activated process of the mobility in the conductive channel. In other words, a very large number of traps distribute in the contact region and the carrier transport is more dominate via thermally activated hopping. The increase of the temperature can increase the hopping speed and thus the density of charge introduced in the conductive channel of the DBP-TFTs, which causes a decreased in contact resistance with increasing the temperature.

3.2.4. Thesubthreshold slope, interface trap density, turn-on voltage and ratio current I_{on}/ I_{off}

The subthreshold slope (SS) is a good indicator about the device switching speed, which can be estimated by [39]:

$$SS = \left[\frac{dlog(I_d)}{dV_g}\right]^{-1} \tag{3}$$

The subthreshold slope is clearly dependent on the temperature for the four devices (A, B, C and D), as seen in fig. 8 (a). Furthermore, SS is dependent on the trap density at the interface between the organic layer and gate insulator [40]. The influence of interface traps has a tendency more likely to reduce the diminution of SS with decreasing the temperature due to their augmentation of band edge. The interface quality of the gate insulator/organic layer plays also a critical role in the electrical performance of OTFTs. The interface trap density of the DBP-TFTs was determined by the following formula [24, 41]:

$$D_{it} = \left[\frac{SSlog(e)}{KT/q} - 1\right]\frac{C_i}{q} \tag{4}$$

where T is the temperature, k is Boltzmann's constant, q is the electronic charge.

The plots of D_{it} versus temperature for the DBP-TFTs are shown in fig. 8 (b). As seen in fig. 8 (b), the D_{it} values decreased with increasing of temperature for each fabricated device. For the current ratio and turn-on voltage parameters, we adapt the method used in [24] in order to determine the values of these two parameters versus temperature and for substrate temperature and they are shown in fig. 9 (a) and (b). It was found that the current ratio is improved with increasing the temperature. This increase in the current ratio is essentially due to the decrease in leakage current which directly related to the quality of morphology of the DBP thin films. Furthermore, we can see that the turn-on voltage becomes less negative with increasing the temperature (fig. 9 (b)). For high temperatures, it was found that the turn-on voltage is close to 0V. This behavior could be attributed to the a little intrinsic residual doping existing in the material [42].

4. Analytical modeling of the temperature dependence of the mobility, total resistance and the current-voltage characteristics of the DBP-TFTs

4.1. Modeling the temperature dependence of the field effect mobility in the DBP-TFTs

In order to analysis the charge transport mechanisms in OTFTs, a detailed examination of the field effect mobility dependent on the temperature was performed and suggests that the charge carriers transport in the conducting channel exhibiting a thermally activated behavior [27-28, 43-44]. In frame of the assumption used in [45-46], the developed expression of the field effect mobility is given by:

$$\mu_{FET}(T,T_0) = \mu_0\, A(T,T_0)\, \frac{C_i^{2\left(\frac{T_0}{T}-1\right)}}{\varepsilon_{DBP}^{\left(\frac{T_0}{T}-1\right)}} (V_{GS}-V_{th})^{2\left(\frac{T_0}{T}-1\right)} \tag{5}$$

ε_{DBP} is the dielectric constant of the organic semiconductor DBP, T_0 is the characteristic temperature, k_B is Boltzmann's constant and q is the electronic charge.

The function $A(T,T_0)$ is given by:

$$A(T,T_0) = \frac{qk_BTN_V\, exp\left[-\frac{E_{F0}-E_V}{kT}\right]}{\left[\pi qk_BTg_{d0}\exp\left(-\frac{E_{F0}-E_V}{kT_0}\right)\right]^{\frac{T_0}{T}}} \left[\frac{sin\left(\frac{\pi T}{T_0}\right)}{2k_BT_0}\right]^{\frac{T_0}{T}}$$

where g_{d0} is the density of localized states at the valence band, which described by an exponential type distribution, N_V is the valence band state density, and μ_0 istaken to be one (μ_0= 1 cm^2 V^{-1} s^{-1}) and used only for dimensional purposes.

4.2. Modeling of the total resistance of the DBP-TFTs

According to the variable range hopping model (VRH), the total device resistance is obtained from the inverse of the sheet conductance, and it can be expressed as [24, 47-51]:

$$R_{tot} = \frac{1}{g_{sh}} = \sqrt{\frac{\delta_0 N_t}{2\varepsilon_0\varepsilon_s K_B T_0}}\, \frac{q(T-2T_0)}{\sigma_0 K_B T}\, \frac{L}{W} \left[\left(\frac{V_G-V_{th}}{\frac{2(2\alpha)^3 B_C \varepsilon_0 \varepsilon_s K_B T_0}{c_i^2\left(\frac{T_0}{T}\right)^3 sin\left(\pi\frac{T_0}{T}\right)}}\right)^{\frac{2T_0}{T}-1} - 1\right]^{-1} \tag{6}$$

where σ_0 is the percolation prefactor of the conductivity,α is an effective overlap parameter that governs the tunneling process between two localized states, B_c is the critical number of bonds per site in the percolating network, for a three-dimensional amorphous system, $B_c \cong 2$ [49-50]. N_t is the number of states per unit volume and δ is the fraction of the localized states occupied by a carrier.

The set of parameters that gave a good agreement between the experimental data and those calculated by the equation (6) are listed in table 1. Fig. 10 (a)-(d) shows the good agreement between calculated and the experimental data of the total device resistance. The experimental

total resistance was determined from the linear regime of the output characteristics ($R_{tot} = [\frac{\partial V_D}{\partial I_D}]^{V_G}_{V_D \to 0}$) at high gate voltage.

4.3. Modeling of current-voltage characteristics

The modeling of the current-voltage characteristics (output and transfer characteristics) of the fabricated DBP-TFTs was performed using the following expression [24, 45-46]:

$$I_D = K\mu_{FET} \frac{(V_{GS}-V_{th})(1+\lambda V_D)}{[1+R_c K\mu_{FET}(V_{GS}-V_{th})]\left[1+\left[\frac{V_D}{\alpha_s(V_{GS}-V_{th})}\right]^m\right]^{\frac{1}{m}}} \quad (7)$$

Where$K = \frac{WC_i}{L}$, $\lambda$is the channel length modulation parameter,α_s is the saturation modulation parameter, and m is a control transition parameter from the linear to the saturation regime. The m parameter is also known as the knee shape parameter. The parameters λ, m and α_s are extracted by the used methods in [24]. The set of parameters that gave a best agreement between the experimental data and those calculated by the equation (7) are summarized in table 2. A very good agreement has been obtained between the calculated and experimental transfer characteristics I_D (V_G) at V_D= -20V (fig. 11(a)-(d)) and the output characteristics I_D (V_D) at V_G=-40V (fig.12) of the DBP-TFTs deposited at different temperatures. Comparing the measured transfer and output characteristics and those calculated by equation (7), we conclude that the model well correctly describes the electrical characteristics of DBP-TFTs.

5. Conclusions

The electrical proprieties of π -conjugated organic small molecule tetraphenyldibenzoperiflanthene based OTFTs which are deposited at different substrate temperatures have been studied as function temperature over the range of 300-370K. The electrical performances are strongly dependent on the temperature in the DBP- OTFTs. It can be noted that the device optimal parameters can be achieved with a high substrate temperatures (T_{sub}=370K and T_{sub}=390K). From the experimental results presented in this work, it can be concluded that the increase of the temperature could improve the electrical performance of the DBP-TFTs. From the extracted data of the field effect mobility, we found that the charge transport is thermally activated in this type of samples. Moreover, a analytical charge transport model able to reproduce accurately the dependence of the experimental data of the total resistance and current-voltage characteristics has been correctly applied for the DBP-TFTs. The modeled results show an excellent agreement with the experimental data in total resistance, transfer and output characteristics.

Acknowledgements
This work has been supported by the Spanish ministry of science under project ENE2014-56237-C4 and the Tunisian Ministry of Higher Education and Scientific, University of Carthage.

References

[1] C.L. Fan, P.C. Chiu, C.C. Lin, IEEE Electron Dev. Lett. 31 (2010) 1485.

[2] C.L. Fan, Y.Z. Lin, W.D. Lee, S.J. Wang, C.H. Huang, Org. Electron. 13 (2012) 2924.

[3] C.Y. Wei, F. Adriyanto, Y.J. Lin, Y.C. Li, T.J. Huang, D.W. Chou, Y.H. Wang, IEEE Electron Dev. Lett. 30 (2009) 1039.

[4] B. Crone, A. Dodabalapur, A. Gelperin, L. Torsi, H.E. Katz, A.J. Lovinger, Z. Bao, Appl. Phys. Lett. 78 (2001) 2229.

[5] M.C. Hamilton, J. Kanicki, IEEE J. Sel. Topics. Quantum Electron. 10 (2004) 840.

[6] H.E. Katz, Chem. Mater. 16 (2004) 4748.

[7] H. Nakanotani, S. Akiyama, D. Ohnishi, M. Moriwake, M. Yahiro, T. Yoshihara, S. Tobita, C. Adachi, Adv. Funct. Mater. 17 (2007) 2328.

[8] M. Berggren, D. Nilsson, N.D. Robinson, Nature Mater. 6 (2007) 3.

[9] S. J. Fakher, A.K. Hassan, M.F. Mabrook, Synth. Met. 191 (2014) 53–58.

[10] J. Puigdollers, C. Voz, I. Martin, M. Vetter, A. Orpella, R. Alcubilla, Synth. Met. 146 (2004) 355–358.

[11] M. Zhu, G. Liang, T. Cui, K. Varahramyan, Solid State Electron. 49 (2005) 884–888.

[12] H. Klauk, M. Halik, U. Zschieschang, G. Schmid, W. Radlik, Polymer gate dielectric pentacene TFTs and circuits on flexible substrates, International Electron Devices Meeting, San Francisco, CA, December 8–11, 2002. p. 557–60.

[13] J. Puigdollers, C. Voz, S. Cheylan, A. Orpella, M. Vetter, R. Alcubilla, Thin Solid Films 515 (2007) 7667–7670.

[14] J. Puigdollers, C. Voz, M. Fonrodona, S. Cheylan, M. Stella, J. Andreu, M. Vetter, R. Alcubilla, J. Non-Cryst. Solids 352 (2006) 1778–1782.

[15] W. Boukhili, M. Mahdouani, R. Bourguiga, J. Puigdollers, Superlattices Microstruct., 83 (2015) 224–236.

[16] J. Puigdollers, M. Della Pirriera, A. Marsal, A. Orpella, S. Cheylan, C. Voz, R. Alcubilla, Thin Solid Films 517 (2009) 6271–6274

[17] S. Galindo, M. Ahmadpour, L. G. Gerling, A. Marsal, C. Voz, R. Alcubilla, J. Puigdollers, Org. Electron. 15 (2014) 2553–2560.

[18] Y. Zheng, W. J. Potscavage, T. Komino, M. Hirade, J. Adachi, C. Adachi, Appl. Phys. Lett. 102 (14) (2013) 143304.

[19] X. Xiao, J. D. Zimmerman, B. E. Lassiter, K. J. Bergemann, S. R. Forrest, Appl. Phys. Lett. 102 (7) (2013) 073302.

[20] Z. Wang, D. Yokoyama, X. Wang, Energy 6 (1) (2013) 249–255.

[21] D.W. Chou , C.J. Huang , C.M. Su , C.F. Yang , W.R. Chen , T.H. Meen , Solid State Electron. 61 (2011) 76–80.

[22] B. Gunduz, Omar A. Al-Hartomy, Said A. Farha Al Said, Ahmed A. Al-Ghamdi, F. Yakuphanoglu, Synth. Met.179 (2013) 94– 115.

[23] C. Voz, A. Marsal, C. Moreno, J. Puigdollers, R. Alcubilla, Synth. Met. 161 (23–24) (2012) 2554–2557.

[24] W. Boukhili, M. Mahdouani, M. Erouel, J. Puigdollers, R. Bourguiga, Synth. Met. 199 (2015) 303–309.

[25] S. Zorai, S. Mansouri, R. Bourguiga, Superlattices Microstruct. 55 (2013) 211–221.

[26] J. W. Chang, W. L. Hsu, Ch. Y. Wu, T. F. Guo, T. Ch. Wen, Org. Electron. 11 (2010) 1613–1619.

[27] J. A. Letizia, J. Rivnay, A. Facchetti, M. A. Ratner, T. J. Marks, Adv. Funct. Mater. 20 (2010) 50-58.

[28] G. Horowitz, M. E. Hajlaoui, R. Hajlaoui, J. Appl. Phys. 87 (2000) 4456.

[29] M. C. J. M. Vissenberg, M. Matters, Phys. Rev. B 57 (1998) 12964.

[30] J. H. Schön, B. Batlogg, Appl. Phys. Lett. 74 (1999) 2.

[31] A. Bolognesi, M. Berliocchi, M. Manenti, A.D. Carlo, P. Lugli, K. Lmimouni, C. Dufour, IEEE Trans. Electron Dev. 51 (2004) 1997.

[32] R. J. Chesterfield, J. C. McKeen, C. R. Newman, P. C. Ewbank, D. A. da Silva, J. L. Bredas, L. L. Miller, K. R. Mann, C. D. Frisbie, J. Phys. Chem. B, 108 (2004) 19281.

[33] M. Hirade, C. Adachi, Appl. Phys. Lett. 99 (15) (2011) 153302.

[34] V. Podzorova, V. M. Pudalov, M. E. Gershenson, Appl. Phys. Lett. 82 (2003) 1739-1741.

[35] I. Kang, T.K. An, J. A. Hong, H. J. Yun, R. Kim, D.S. Chung, C.E. Park, Y.- H. Kim, S.-K. Kwon, Adv. Mater. 25 (2013) 524.

[36] L. Dunn, A. Dodabalapur, J. Appl. Phys. 107 (2010) 113714.

[37] A. Salleo, T. W. Chen, A. R. Völkel, Y. Wu, P. Liu, B. S. Ong, and R. A. Street Phys. Rev. B 70 (2004) 115311.

[38] D. Natali, M. Caironi, Adv. Mater. 24 (2012) 1357.

[39] L.A. Majewski, M. Grell, Synth. Met. 151 (2005) 175.

[40] C. Lee, D. Striakhilev, S. Tao, A. Nathan, IEEE Electron Device Lett. 26 (2005) 637.

[41] G. Horowitz, Adv. Funct. Mater. 13 (2003) 53.

[42] E. J. Meijer, C. Tanase, P. W. M. Blom, E. van Veenendaal, B. H. Huisman, D. M. de Leeuw, T. M. Klapwijk, Appl. Phys. Lett. 80 (2000) 3838-3840.

[43] G. W. Kang, K.M. Park, J.H. Song , C.H. Lee, D.H. Hwang, Current Applied Physics 5 (2005) 297–301.

[44] A. R. Brown, D. M. de Leeuw, E. E. Havinga, A. Pomp, Synth. Met. 68 (1994) 65.

[45] M. Estrada, I. Mejia, A. Cerdeira, J. Pallares, L.F. Marsal, B. Iniguez, Solid State Electron. 52 (2008) 787–794.

[46] M. Estrada, A. Cerdeira, I. Mejia, M. Avila, R. Picos, L.F. Marsal, J. Pallares, B. Iñiguez, Microelectronic Engineering 87 (2010) 2565–2570.

[47] S. Mansouri, S. Zorai, R. Bourguiga, Synth. Met. 162 (2012) 231– 235.

[48] M. C. J. M. Vissenberg, M. Matters, Phys. Rev. B 57 (1998) 12964.

[49] Ling Li, Hans Kosina, "An analytical model for organic thin film transistors", Conference on Electron Devices and Solid-State Circuits (EDSSC) Hong Kong, IEEE, (2005) 571-574.

[50] M. Sahimi, Applications of Percolation Theory, Taylor & Francis, London, 1994.

[51] G. Pike, C. Seager, Phys. Rev. B 10 (1974) 1421-1434.

T (K) / Parameters	300	310	320	330	340	350	360	370
$2T_0/T$	2.56	2.48	2.4	2.33	2.26	2.2	2.13	2.08
$g_{d0}(cm^{-3}\,eV^{-1})$	2.2×10^{23}	1×10^{23}	1.2×10^{23}	1.2×10^{23}	9.5×10^{22}	9×10^{22}	6.1×10^{22}	6.5×10^{22}
$\sigma_0(Sm^{-1})$	4.75×10^{5}	4.75×10^{5}	4.75×10^{5}	4.75×10^{5}	4.75×10^{5}	4.75×10^{5}	4.75×10^{5}	4.75×10^{5}
$\alpha^{-1}(\text{Å})$	3.1	3.2	2.9	3	2.8	2.8	2.7	2.85

Table.1.

Model parameters / Devices	m	$\lambda\ (V^{-1})$	α_s	$V_{th}(V)$	$R_c\ (\Omega)$
Device A (T_{sub}=300K)	1.65	4×10^{-3}	1.25×10^{-2}	-10	3×10^{8}
Device B (T_{sub}=330K)	1.4	1.25×10^{-3}	2×10^{-2}	-8	8×10^{7}
Device C (T_{sub}=360K)	1.72	4×10^{-2}	2×10^{-2}	-7.25	1.5×10^{7}
Device D (T_{sub}=390K)	1.7	0. 2	1×10^{-2}	-2.8	9×10^{6}

Table. 2

Figures caption:

Figure 1(a)-(b): (a) Schematic cross section of a DBP thin film transistor and **(b)** Molecular structure of tetraphenyldibenzoperiflanthene (DBP).

Figure 2 (a)-(b): Output characteristics curves of DBP-TFTs deposited at different substrate temperature (T_{sub}): **(a)** device A (T_{sub}=300K), **(b)** device B (T_{sub}=330K), **(c)** device C (T_{sub}=360K) and **(d)** device D (T_{sub}=390K).

Figure 3 (a)-(d): Transfer characteristics at different temperatures of DBP-TFTs: **(a)** device A (T_{sub}=300K), **(b)** device B (T_{sub}=330K), **(c)** device C (T_{sub}=360K) and **(d)** device D (T_{sub}=390K).

Figure 4 (a)-(d): Temperature dependence between 300K and 370K of the drain current in saturation regime: **(a)** device A (T_{sub}=300K), **(b)** device B (T_{sub}=330K), **(c)** device C (T_{sub}=360K) and **(d)** device D (T_{sub}=390K)

Figure 5 (a)-(b): (a) Temperature dependence of threshold voltage for the four DBP-TFTs (A, B, C and D) **(b)** Trapped charge density versus temperature for the four devices.

Figure 6: Field effect mobility versus temperature (in an Arrhenius plot) extracted at constant drain and gate voltages (V_D =V_G=-20V)in DBP-TFTs deposited at different substrate temperature.

Figure 7: Contact resistance versus temperature.

Figure 8 (a)-(b): Subthreshold slope **(a)** and the interface trap density **(b)** versus temperature for the fabricated DBP-TFTs

Figure 9 (a)-(b): Current ratio **(a)** and the turn-on voltage **(b)** versus temperature for the fabricated DBP-TFTs.

Figure 10: Experimental and modeled field effect mobility as a function temperature for the fabricated DBP-TFTs.

Figure 11: Compared between the modeled and the experimental total device resistance of the fabricated DBP-TFTs: **(a)** device A (T_{sub}=300K), **(b)** device B (T_{sub}=330K), **(c)** device C (T_{sub}=360K) and **(d)** device D (T_{sub}=390K).

Figure 12 (a)-(d): The good agreement between experimental (circle line) and that obtained from model (full line) output characteristics: **(a)** device A (T_{sub}=300K), **(b)** device B (T_{sub}=330K), **(c)** device C (T_{sub}=360K) and **(d)** device D (T_{sub}=390K) of the DBP-TFTs.

Figure 13: Comparison between the modeled and measured output characteristics at V_G = -40V for the DBP-TFTs deposited at different substrate temperatures.

Tables captions

Table 1. Parameter values that give a good agreement between the experimental field effect mobility and total resistance of the fabricated DBP-TFTs and those calculated by the used model.

Table 2. Parameter values that give a good agreement between the measured current-voltage characteristics and those obtained by the model.

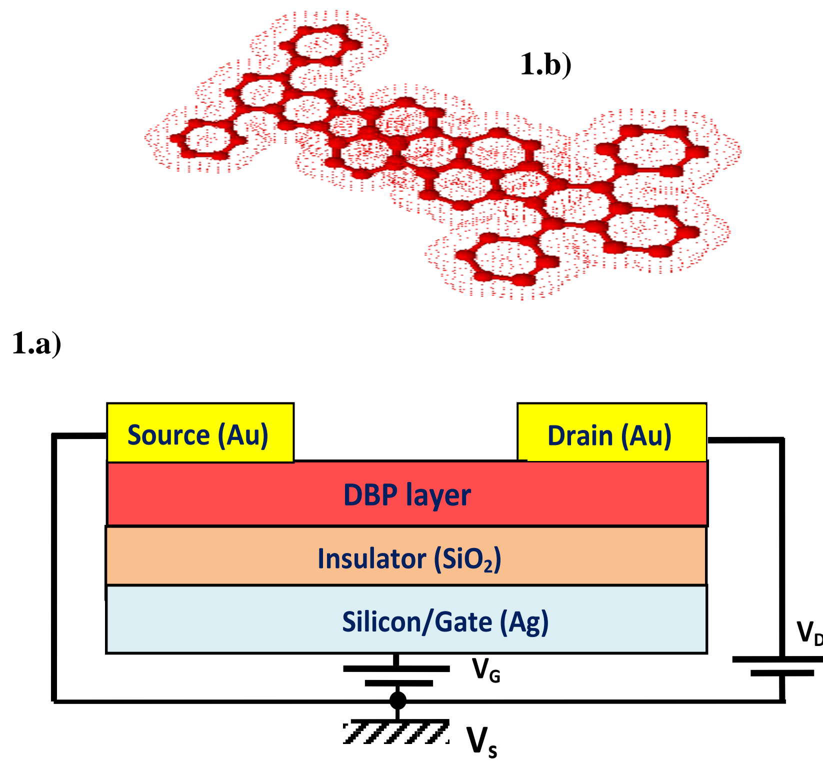


Figure 1 (a)-(b)

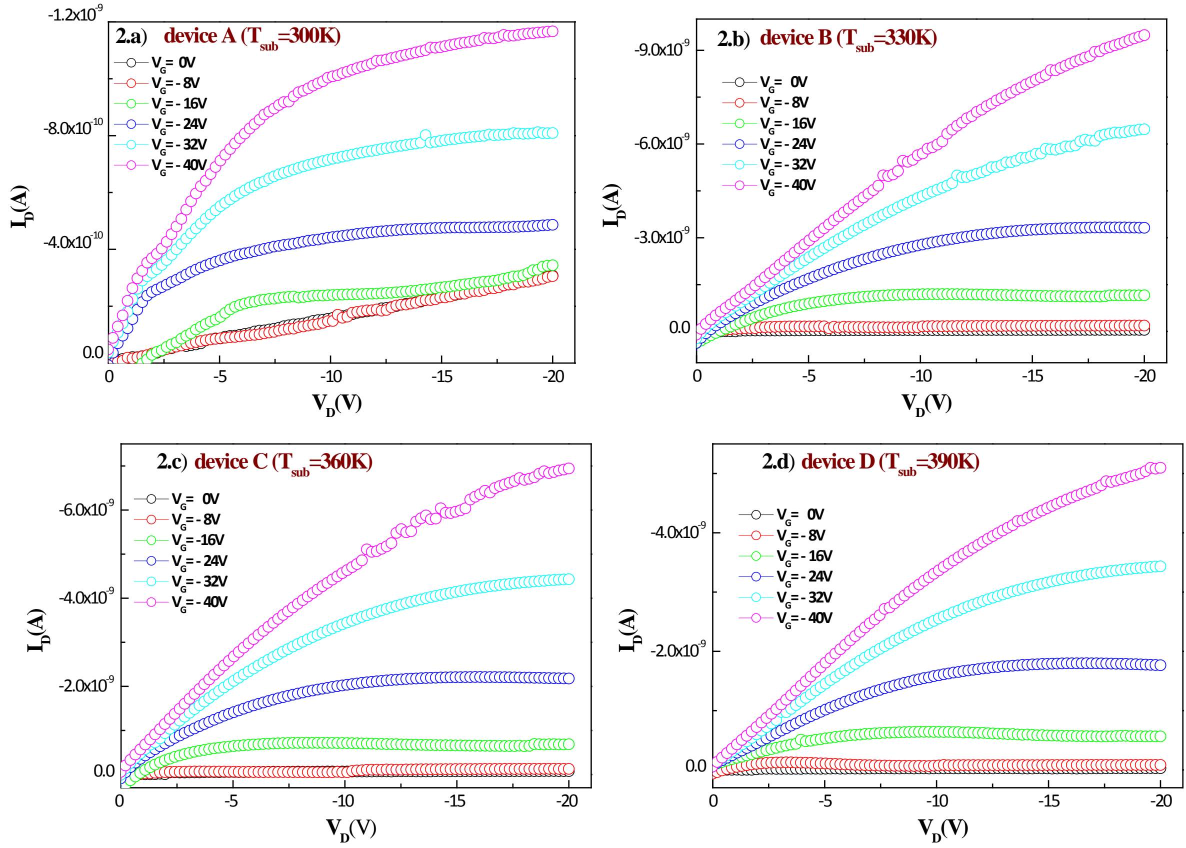


Figure 2 (a)-(d)

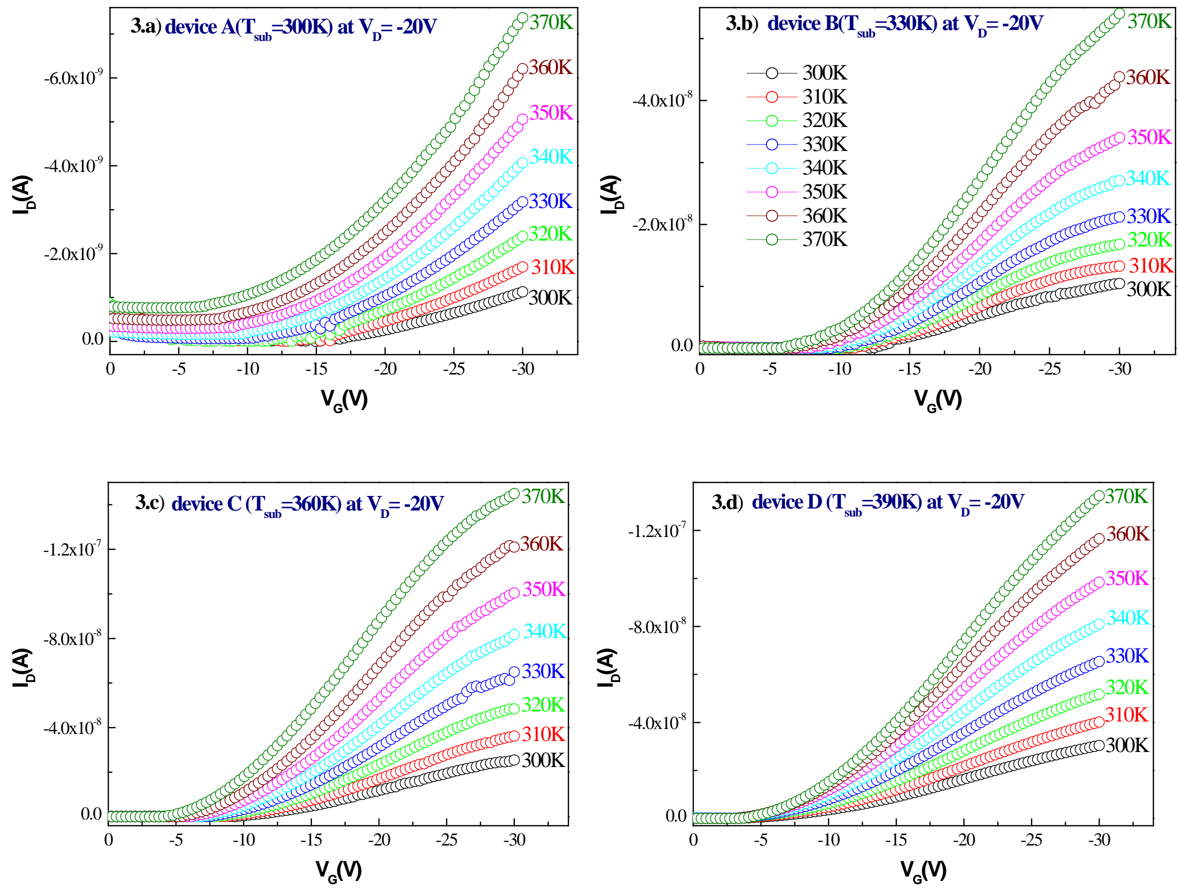


Figure 3 (a)-(d)

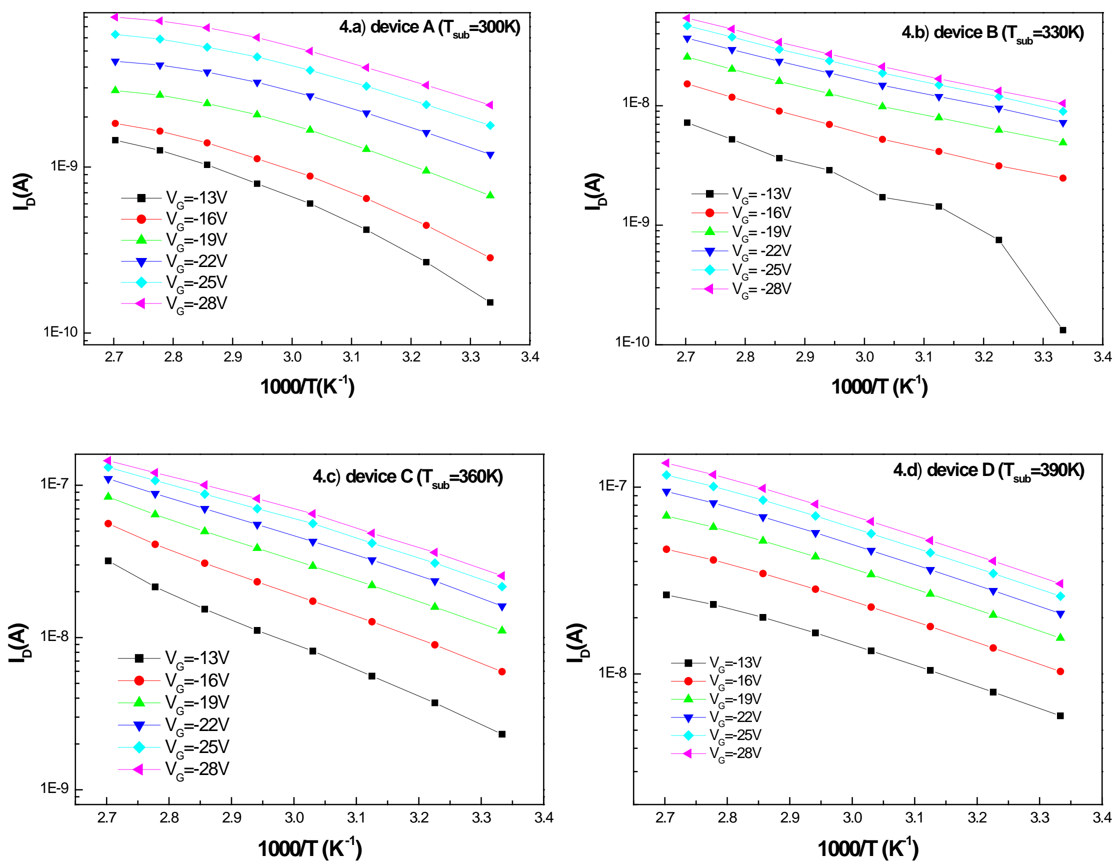
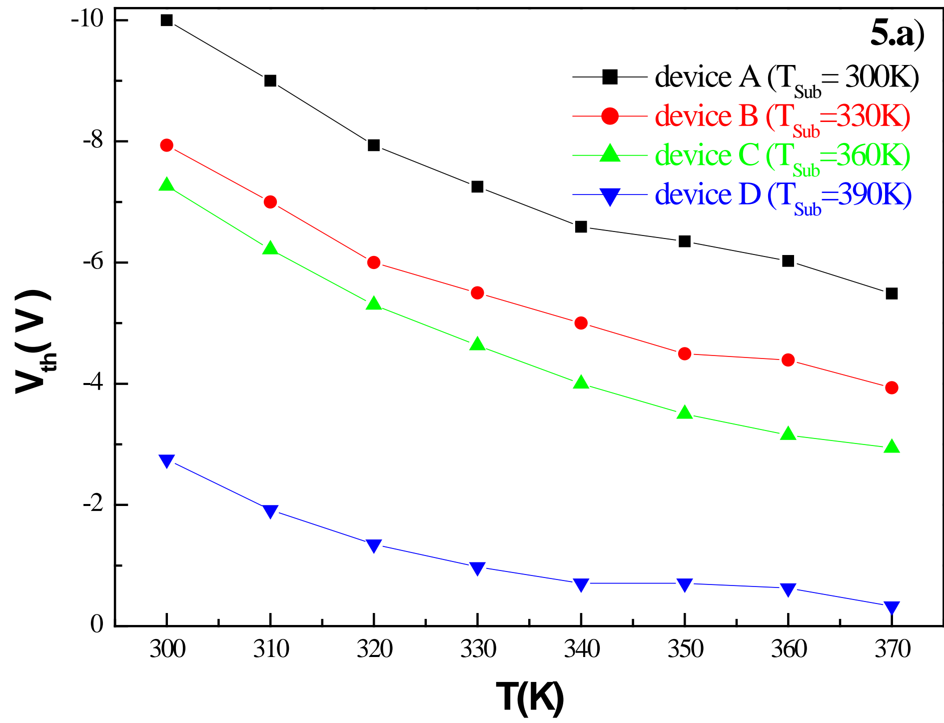


Figure 4. (a)-(d)



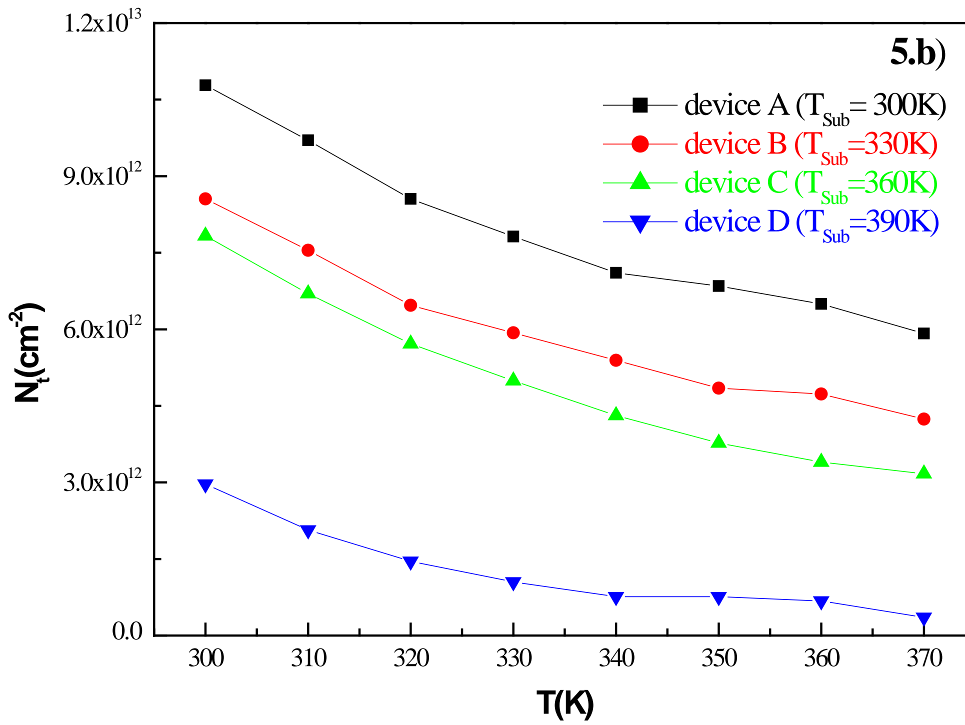


Figure 5 (a)-(b)

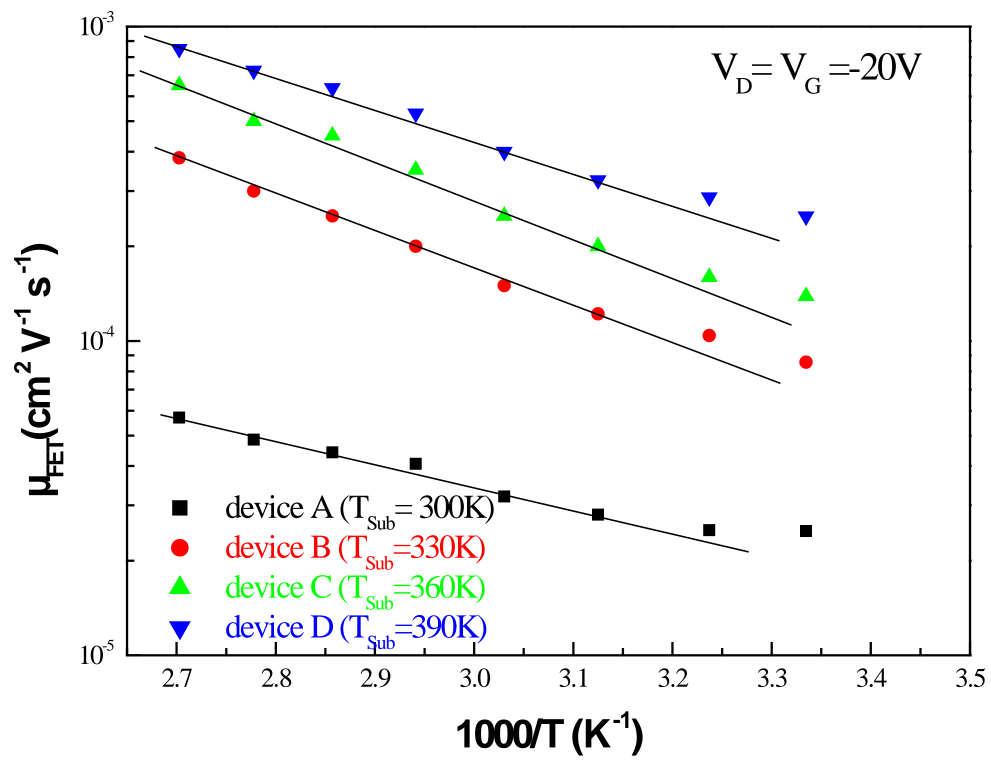


Figure 6

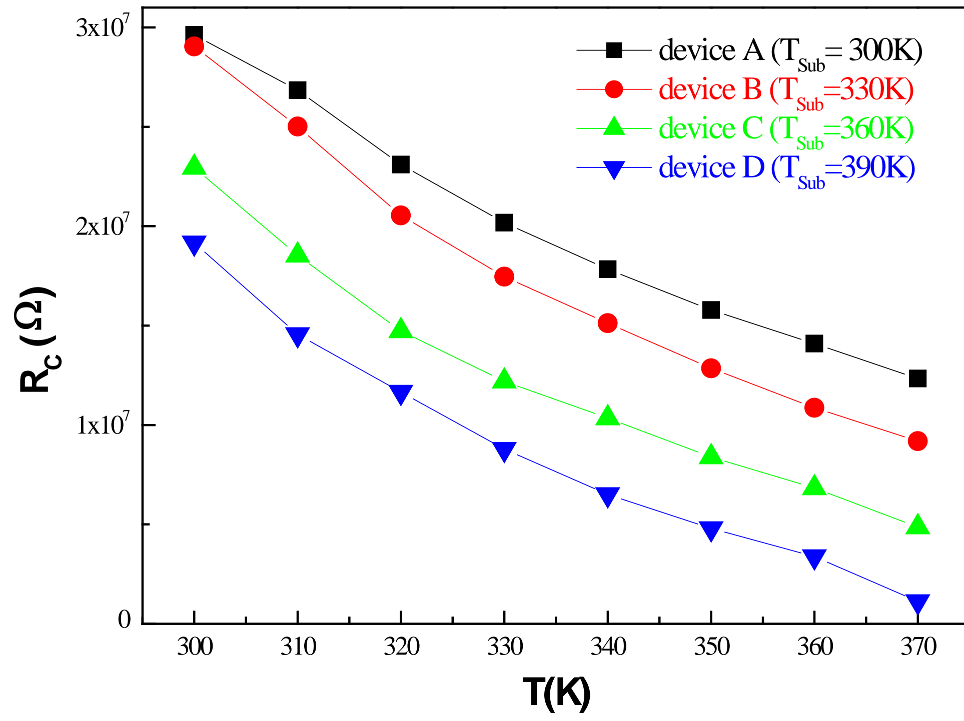
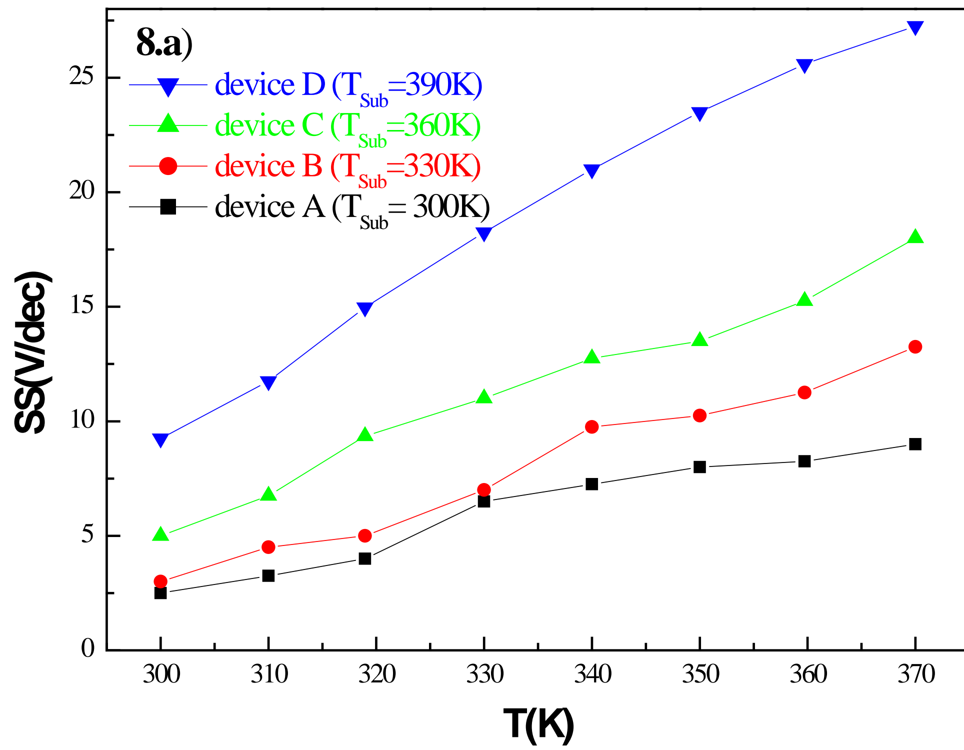


Figure 7



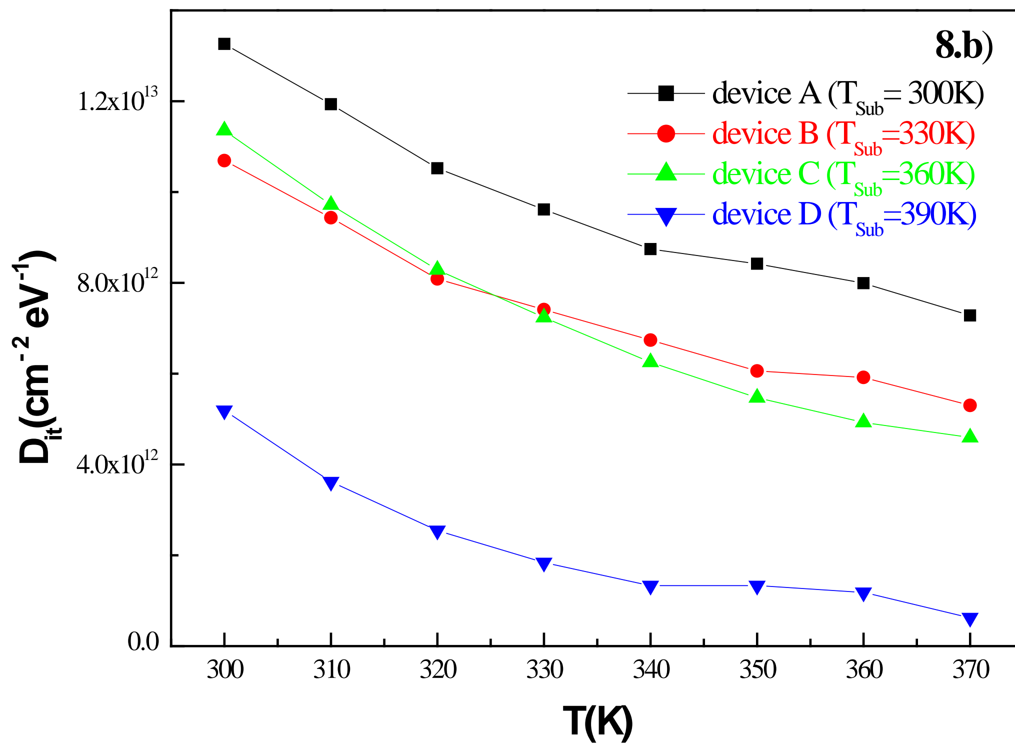
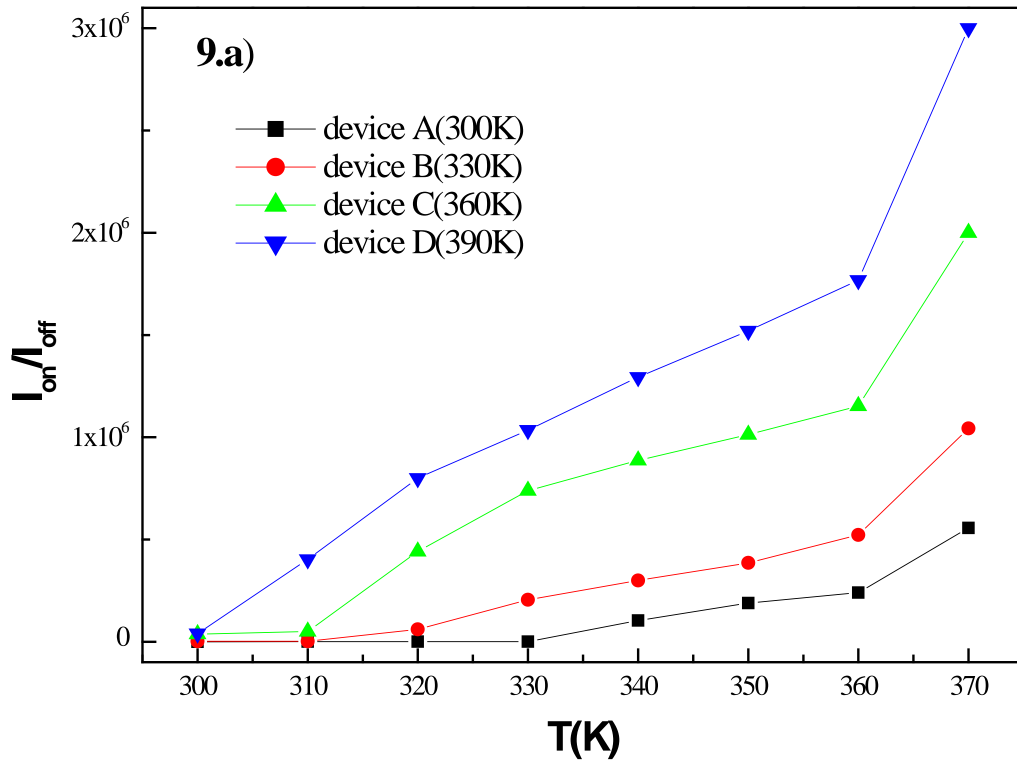


Figure 8 (a)- (b)



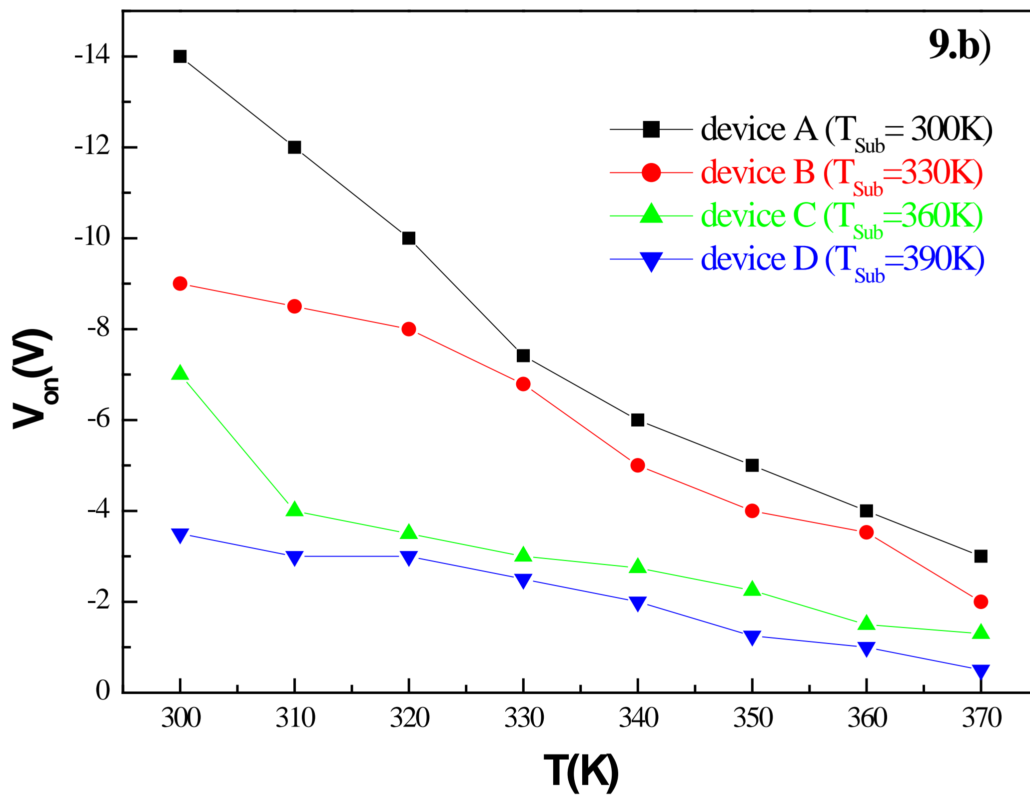
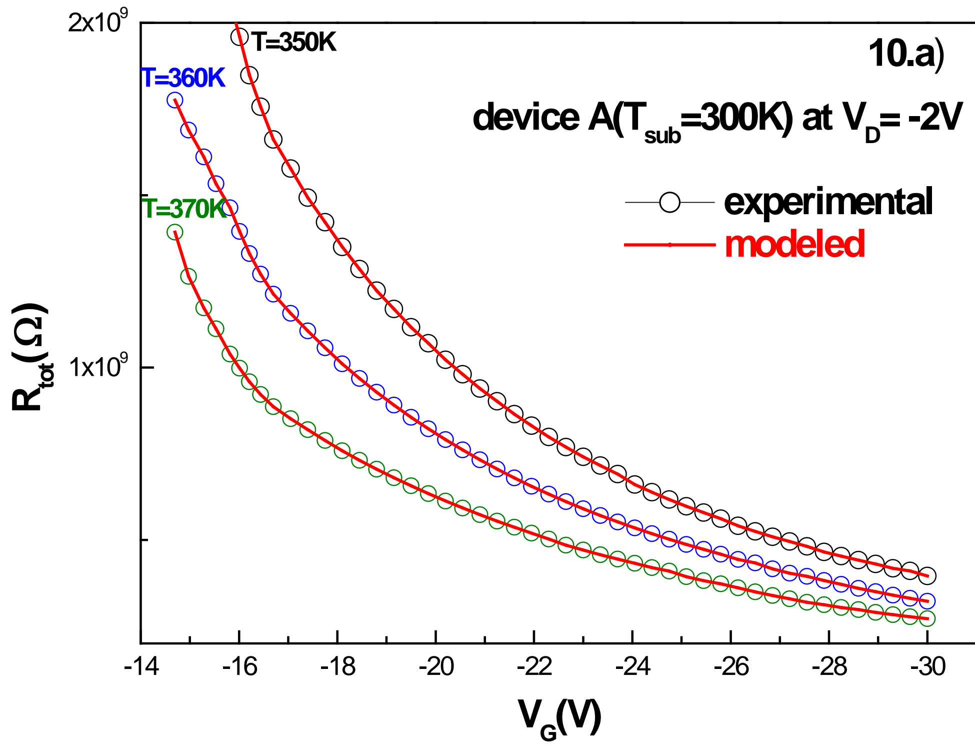


Figure 9 (a)- (b)



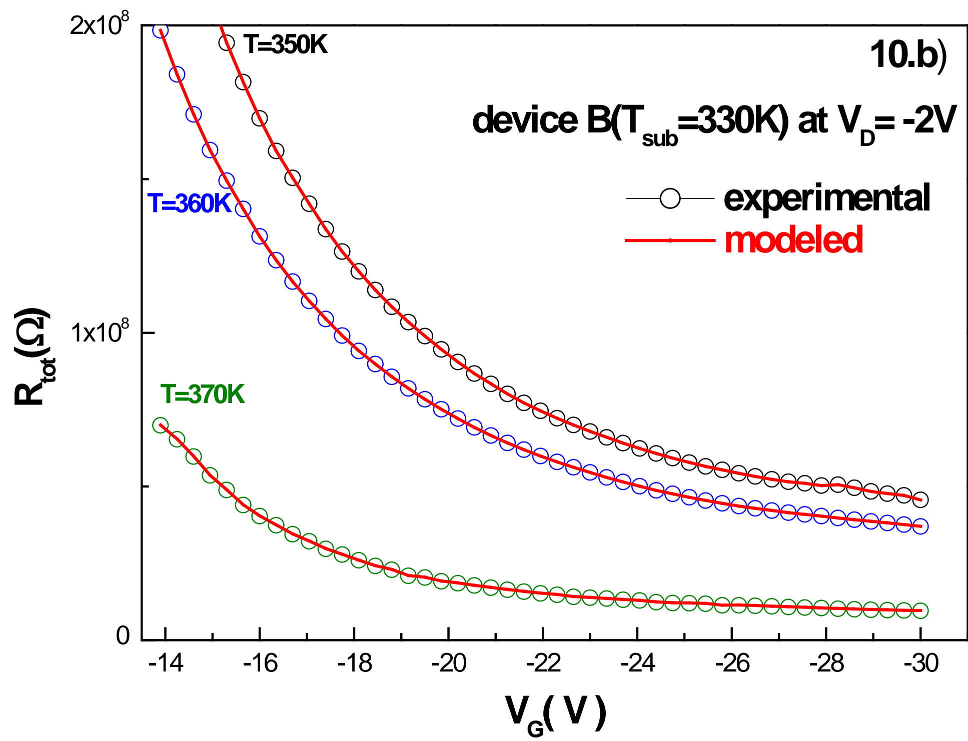
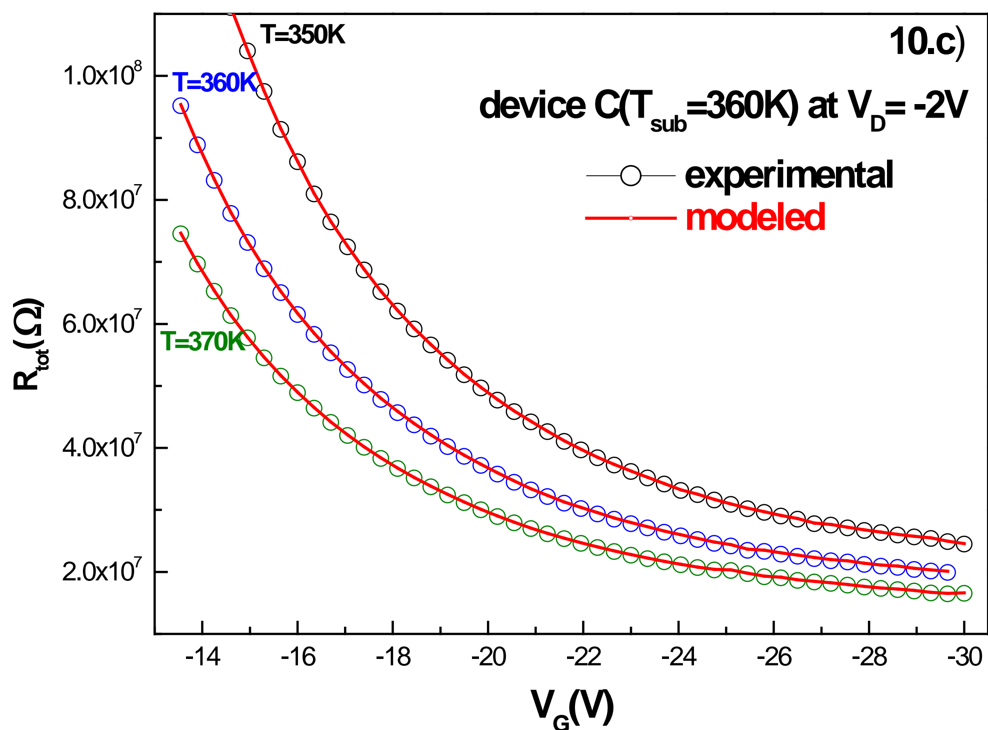


Figure 10 (a)-(b)



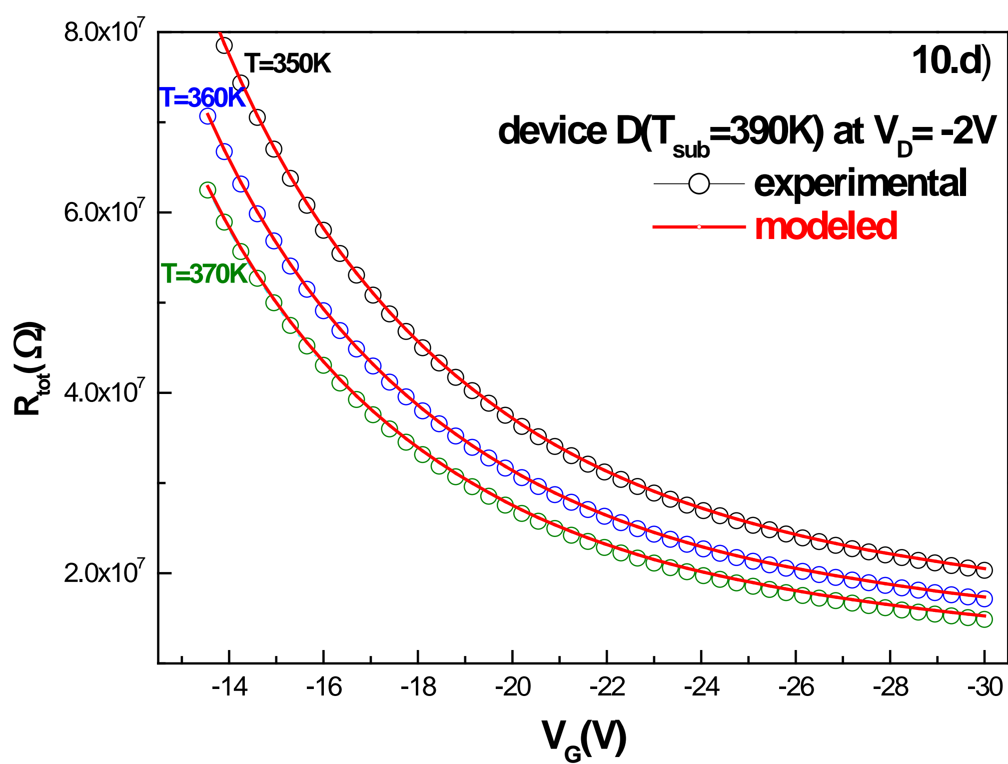
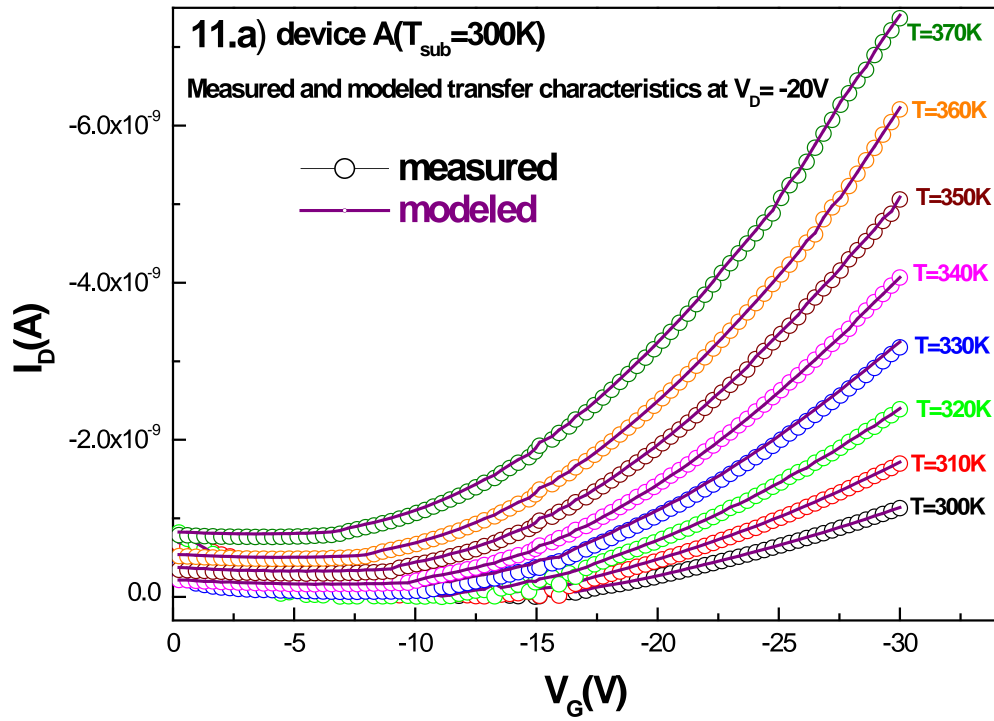


Figure 10 (c)-(d)



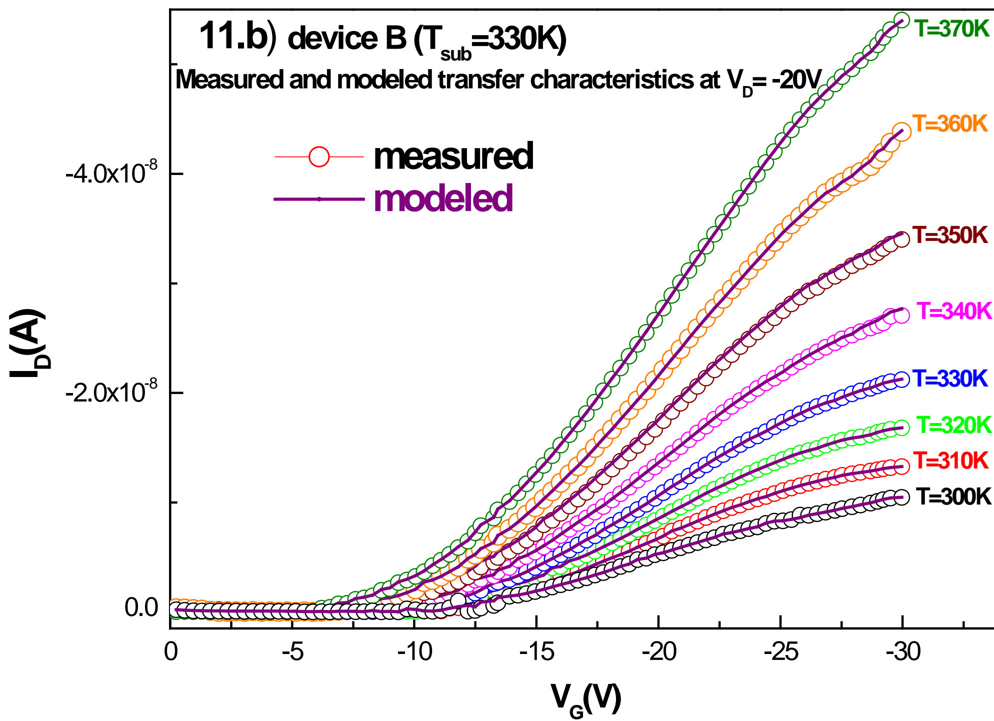
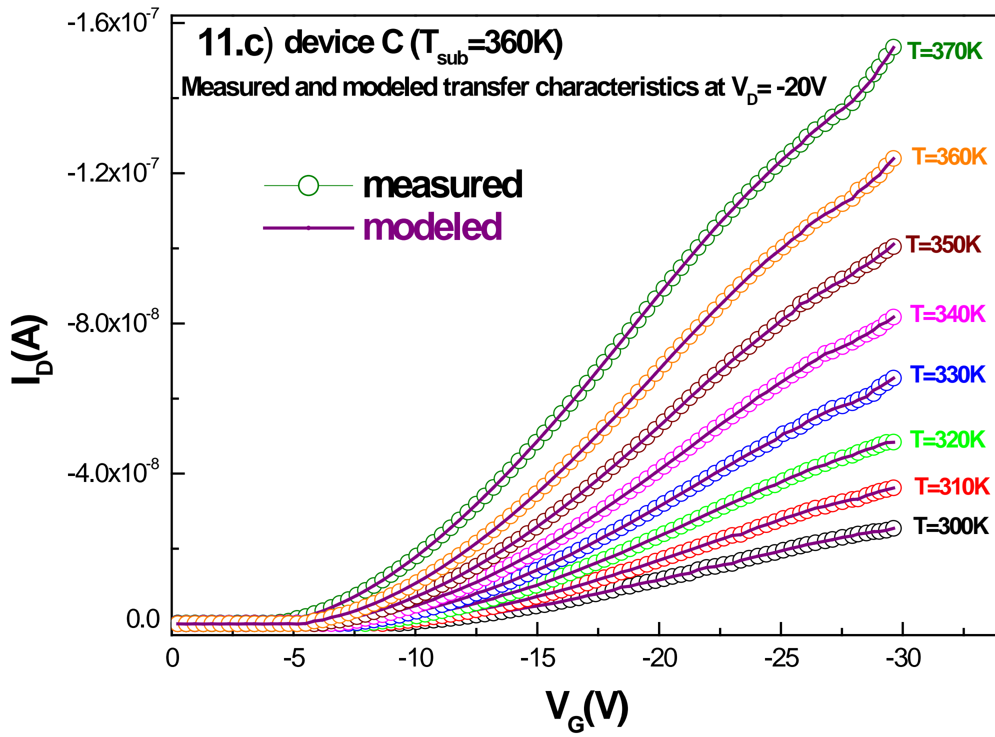


Figure 11 (a)-(b)



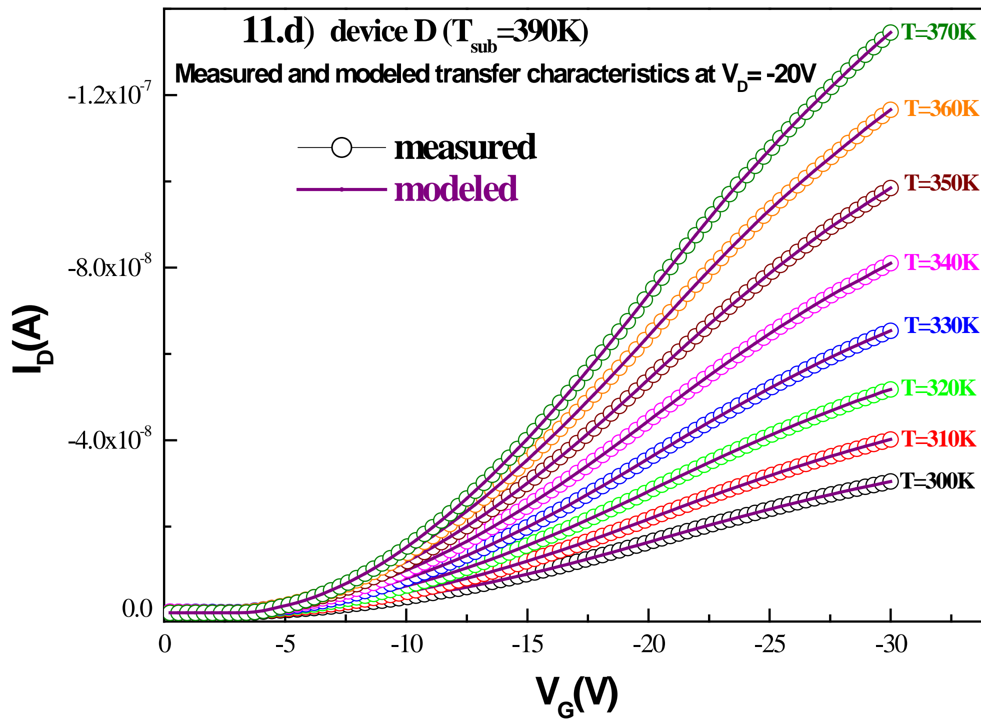


Figure 11 (c)-(d)

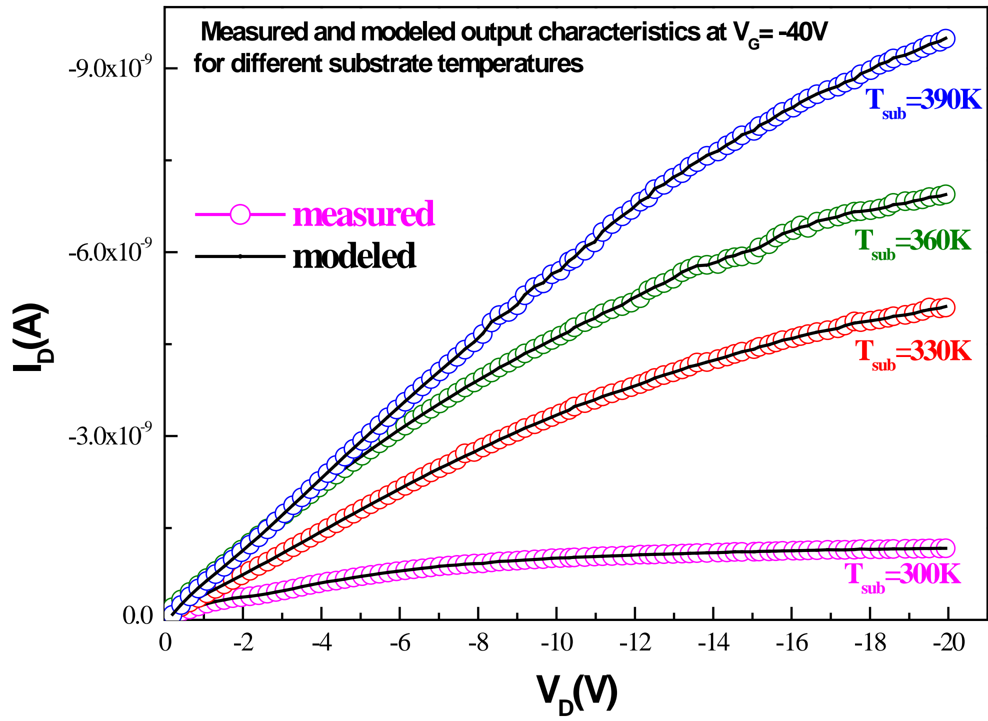


Figure 12