Design and Performance Comparison of a Superregenerative MPSK Transceiver

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***Abstract*—In this paper we present a superregenerative transceiver able to switch among BPSK, QPSK and 8PSK modulations. An HF-band proof-of-concept transceiver is implemented on an FPGA with a minimum of analog circuitry. The desire of making fair comparisons between BER figures rises a problem of clock frequency selection which is finally solved without consuming extra resources.**

I. Introduction

In the area of radio-frequency communications, the superregenerative (SR) receiver [1] is receiving renewed interest (e.g. [2], [3]) in applications where low-power and low-cost are the main driving forces. Recently [4], we presented a full QPSK SR transceiver, implemented on an FPGA. The receiver part was based on a SR receiver structure suitable for the QPSK detection approach proposed and experimentally confirmed in [5]. This approach takes advantage of the fact that an SR oscillator (SRO) generates RF pulses (SRO pulses) which preserve the phase information contained in the incoming signal. In this paper we propose and demonstrate a full MPSK SR transceiver which is implemented on an FPGA. This transceiver can also be switched among BPSK, QPSK and 8PSK. The transmitter is fully digital exploiting the fact that the targeted carrier frequency is well within the capabilities of even low-cost FPGA devices. Bit error rate (BER) measurements for different modulations validate this transceiver design. In order to compare these measurements with theoretical results it is necessary to appropriately choose the reference-clock frequency of the FPGA. The paper is structured as follows: In section II we present the MPSK transceiver. Section III describes the problem of choosing the right reference-clock frequency that allows the FPGA to generate all necessary signals. Section IV discuss BER measurements results, while section V presents some conclusions.

II. MPSK transceiver

An m-ary PSK (MPSK) modulated signal with a symbol rate $f_s = 1/T_s$ around a carrier f_c may be written as

$$x(t) = \sum_{n=-\infty}^{\infty} p_c(t - nT_s)\cos(2\pi f_c t + \phi_n) \qquad (1)$$

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with the phase corresponding to the n-th symbol given by $\phi_n = \{0, 2\pi/m, 2\times 2\pi/m, 3\times 2\pi/m, ..., (m-1)\times 2\pi/m\}$ and $p_c(t) = \Pi(t)$, i.e. a unit pulse. In the following we consider a differential PSK (DPSK) receiver to avoid the phase synchronization problem, although BER performance is better on non differential PSK modulations [6]. DPSK modulation requires differential encoding at the transmitter side, implemented on an FPGA with just a $\log_2 m$ bit adder.

We have extended the proof of concept superregenerative QPSK transceiver described in [4] to implement an MPSK transceiver that, by means of a digital signal, switches among BPSK, QPSK and 8PSK modulations. On the transmitter side the main impact of using an MPSK modulation is that the frequency needed to digitally synthesize the modulated signal is mf_c.

The main objective of this paper is to experimentally verify the performance of this transceiver for each value of *m*, obtaining the corresponding BER curves and comparing experimental results with the approximate theoretical references given in [6]. These are reproduced in Table I, where r_b is the bit rate (i.e. $r_b = f_s \log_2 m$), B_T is the bandwidth of the transmitted modulated signal,

$$Q(x) = \frac{1}{\sqrt{2\pi}}\int_x^{\infty} e^{\frac{-\lambda^2}{2}}\, d\lambda = \frac{1}{2}\text{erfc}\left(\frac{x}{\sqrt{2}}\right), \qquad (2)$$

and γ_b is the bit-energy to noise ratio.

Differences between these references and our measurements are due to a number of factors including receiver bandwidth, receiver noise figure and phase-quantization error.

The effect of receiver bandwidth and noise figure is straightforward to be accounted for, as they just scale the argument of BER functions in Table I, producing a translation of the BER curves, as will be seen in Fig. 6. Regarding the effects of phase quantization, some comments are needed.

The phase ϕ_n in (1) is inferred from the phase of the SRO pulse by subsampling, storing in a shift register a pattern of N 1-bit samples representing a single period of the SRO pulse. This pattern is compared with the one obtained from the previous SRO pulse and a decision on the observed phase differences is taken [5]. So, the absolute phase-quantization error q_ϕ between two consecutive pulses has a maximum $q_{\phi,\max} = \frac{2\pi}{N}$.

	$\mathbf{r_b/B_T}$	**BER**	$\boldsymbol{\gamma_b}$ **(dB)**
BPSK	1	$\frac{1}{2}e^{-\gamma_b}$	9.3
QPSK	2	$Q\left(\sqrt{8\gamma_b \sin^2 \frac{\pi}{8}}\right)$	10.7
8PSK	3	$\frac{2}{3}Q\left(\sqrt{12\gamma_b \sin^2 \frac{\pi}{16}}\right)$	14.6

TABLE I
DPSK MODULATIONS. GRAY-CODING THEORETICAL BER REFERENCES AND γ_b VALUE TO GET A BER OF 10^{-4}.

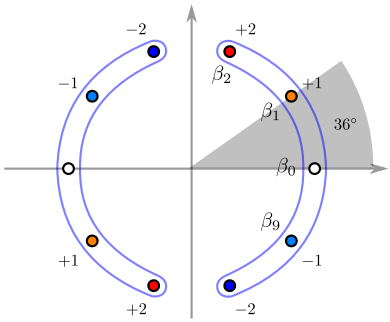

Fig. 1. BPSK constellation with N = 10.

The theoretical references in Table I are for a receiver with no phase-quantization error, i.e. $q_\phi = 0$. So, the minimum absolute noise difference (between two consecutive pulses) that produces a symbol error decision is $n^*_\phi = \frac{2\pi}{2m}$. On the contrary, the noise that produces a symbol error decision on our receiver is lower in q_ϕ, i.e $n_\phi = \frac{2\pi}{2m} - q_\phi$, with a minimum $n_{\phi,\text{min}} = \frac{2\pi}{2m} - q_{\phi,\text{max}} = \frac{2\pi}{2m} - \frac{2\pi}{N}$. Note that discretizing the samples with more than 1 bit could reduce q_ϕ and in the limit, with an infinite number of bits, $q_\phi = 0$ and $n_{\phi,\text{min}} = n^*_\phi$.

Considering the previous relations, if

$$\frac{N}{m} = \text{const.}, \tag{3}$$

then $n^*_\phi / n_{\phi,\text{min}}$ is constant and, assuming a linear relation between phase noise and amplitude noise (true for high signal to noise ratios), it is possible to say that the phase-quantization error is also equivalent to scaling the argument of BER functions in Table I, also producing a translation effect as the receiver bandwidth and noise figure.

On the receiver side the main impact of using an MPSK modulation is that the number of samples N used to subsample the SRO pulse must be increased when increasing m in order to fulfill (3).

Figures 1 to 3 show constellations for $m = \{2, 4, 8\}$ with the constant value of equation (3) equal to 5. So, the number of samples is $N = \{10, 20, 40\}$ and the phase in degrees between each sample is $\Delta_\theta = \frac{360°}{N} = \{36°, 18°, 9°\}$. The phase distance in degrees among symbols (white dots) is $\Delta_\phi = \{180°, 90°, 45°\}$.

III. REFERENCE-CLOCK FREQUENCY DESIGN

To prototype our MPSK SR transceiver we have implemented the transmitter and as many stages as possible of the receiver on an FPGA device.

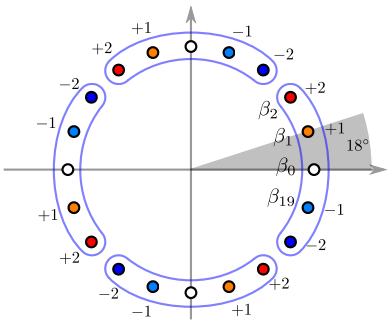

Fig. 2. QPSK constellation with N = 20.

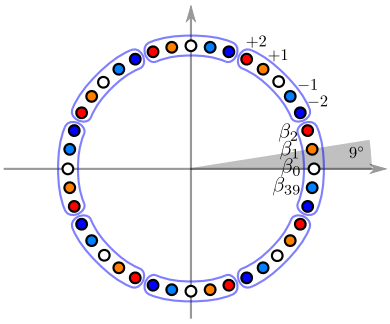

Fig. 3. 8PSK constellation with N = 40.

In order to create a synchronous and simple design the signals of these stages should be generated from a single reference clock of frequency f_{ref}. We have chosen f_{ref} equal to the higher of the signals that must be generated to avoid issues related to even higher clock frequencies. In our design this is the sampling signal of frequency f_{CLK} at which we sample the SRO pulse during a short period of time [5]. So, from now on $f_{ref} = f_{CLK}$.

Now we are going to focus our attention on the digital design of the sampling and decoding stages of the receiver. To fulfill (3) we have to be able to change N when changing the modulation type, i.e. m, but without changing f_c and f_s.

The following two design equations must be considered. The relation between the sampling frequency f_{CLK} and the SRO oscillation frequency f_0 (nominally equal to f_c), taking into account the number of samples N, is [5]

$$f_{CLK} = \left| \frac{N}{kN + 1} \right| f_0, \tag{4}$$

with k an integer. The relation between the sampling frequency f_{CLK} and the symbol frequency f_s should be

$$f_{CLK} = M f_s \tag{5}$$

with M an integer. Figure 4 (a) depicts a situation in which this condition is not fulfilled.

It must be pointed out that using the astable circuit showed in Fig. 5 we could generate f_{CLK} in a non digital way without fulfilling (5): by combining the values R and C, f_{CLK} could be adjusted without changing f_s. However, this kind of circuit does not take advantage of the available resources on the FPGA, adds complexity to the system, R and C need to be modified for each f_{CLK} and exhibits poor stability.

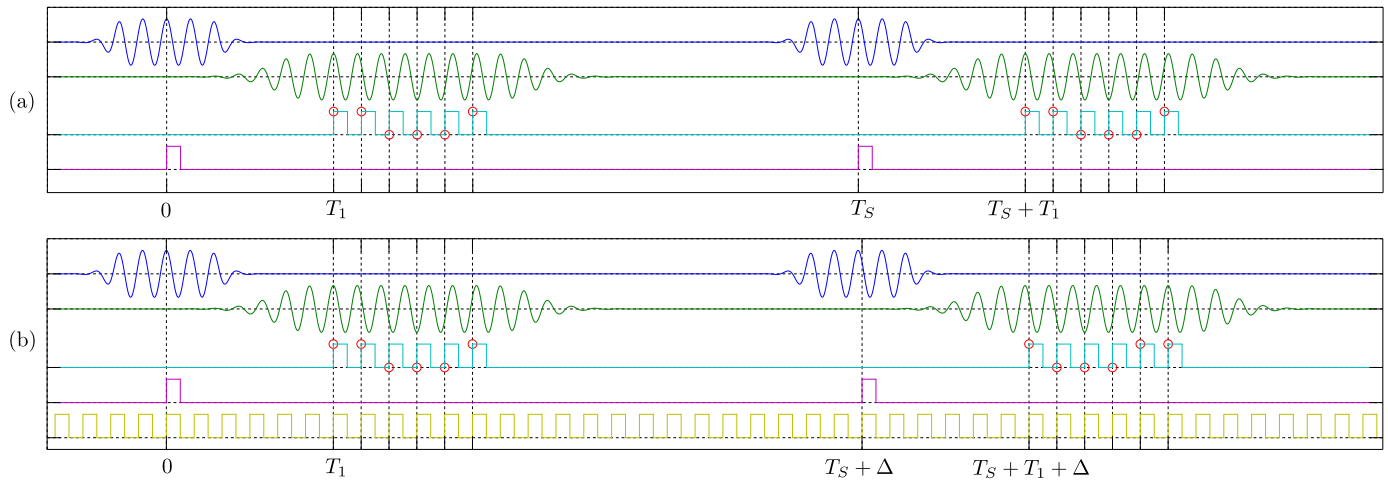

Fig. 4. Signals involved in the SR receiver. The phase of the RF input symbol (blue) at the rising edge of the symbol signal (magenta) is preserved in the generated SRO pulse (green). A sampling signal (cyan) is started at a fixed offset T_1 and $N = 6$ 1-bit samples (red circle) are taken. Figure (a) and (b) depicts this situation for two consecutive symbols exhibiting the same phase. In (a) the symbol signal (magenta) has period T_s and so, the pattern of 1-bit samples is the same on both SRO pulses, and the decision algorithm will conclude that the differential phase of the two consecutive symbols is also zero. In this example equation (5) is not fulfilled. On the contrary, in (b) the symbol signal has period $T'_s = T_s + \Delta$, with $\Delta = nT_0/N$ and $n = 1$, that fulfills equation (7), i.e. the period of the symbol signal T'_s is equal to $M = 25$ periods of the reference clock (yellow) or the sampling signal (as $f_{ref} = f_{CLK}$), with the effect that the second pattern is rotated to the left $n = 1$ samples. As this effect is known it can be easily corrected.

Assuming we prefer the digital design, we would like to, given a set of N values (one for each modulation), be able to find a set of k and M that, for a fixed f_0 and f_s, fulfill (4) and (5). Although we have one extra degree of freedom, f_{CLK}, in the general case we can not assure that both equations are fulfilled because of the integer nature of the unknowns, k and M, and because k is bounded by the finite duration of the SRO pulse.

As an example, lets take the values in [5] used in a QPSK modulation, i.e. f_0 = 26.25 MHz, f_s = 10 kHz and $N = 20$. To compare results among BPSK, QPSK and 8PSK modulations, according to 3 we should take $N_{BPSK} = 10$, $N_{QPSK} = 20$ and $N_{8PSK} = 40$. Solving (4) and (5) for the BPSK modulation with $k = 2$ gives $M = 1250$ and f_{CLK} = 12.5 MHz; for the QPSK modulation with $k = 1$ gives $M = 2500$ and f_{CLK} = 25 MHz; for the 8PSK modulation there is no integer k that gives an integer M, e.g $k = 1$, gives $M \simeq 2560.98$.

As we are forced to use an integer M, we should relax some of the previous restrictions. Relaxing (4) means loosing phase information that seems difficult to recover. This will result in some degradation in the performance of the system. In contrast, under certain conditions, (5) could be relaxed without loosing information. First, let us assume that the receiver can use a symbol frequency f'_s slightly different from f_s. Expressing it in terms of periods, we may write

$$T'_s = T_s + \Delta. \tag{6}$$

The relation between this new symbol frequency f'_s and f_{CLK} must be the same as in (5), i.e

$$f_{CLK} = M f'_s. \tag{7}$$

If Δ has the effect of delaying the initial sampling point exactly n samples, i.e.

$$\Delta = \frac{nT_o}{N} \tag{8}$$

with n an integer, the effect of this delay can be corrected later. Either we can recover the vector that would be obtained with a sampling period T_s by just rotating n times the obtained vector with a sampling period T'_s or, as the delay introduces a phase shift equal to n samples,

$$\phi_{shift} = \frac{\Delta}{T_0} 2\pi = n\frac{2\pi}{N} \tag{9}$$

it can be easily corrected modifying the phase-difference to symbol conversion table. Figure 4 (b) depicts a situation with $n = 1$ and $N = 6$ giving $\phi_{shift} = 60°$.

Of course, the initial sampling point is shifted Δ each symbol. This may be tolerated in packetized transmissions with limited packet lengths, and even in streaming transmissions where we can periodically jump back (or forward) a multiple of T_{CLK} when the accumulated shift approximates a multiple of T_{CLK}.

Now we have a new degree of freedom, i.e n, in addition to f_{CLK}. Therefore, our new goal is: given a set of N values,

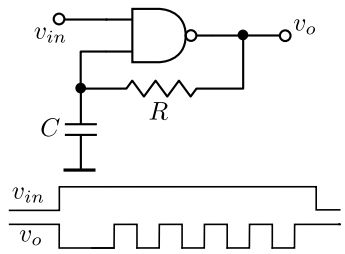

Fig. 5. Astable circuit to generate the sampling signal f_{CLK}.

be able to find a set of k, M and n that, for a fixed f_0 and f_s, fulfill (4), as before, and (6) to (8), instead of (5). A helpful derived relation is

$$M = \left| \frac{\frac{f_0}{f_s}N + n}{kN + 1} \right| \tag{10}$$

where small values of k and n can be tried in order to get an integer M.

With these relaxed restrictions we can tackle 8PSK modulation: taking $k = 1$ and $n = 1$ we get $M = 2561$ and $f_{CLK} \simeq 25.6098$ MHz. Now, the frequency f_s' of the symbol signal used at the receiver is slightly lower than f_s, the difference between its periods being $\simeq 952$ ps. Hence, according to (9), this delay introduces a phase shift equal to 9°.

IV. Experimental results

We have implemented two MPSK transceivers very similar to the QPSK transceiver described in [4]. The main difference is in the code used to program the FPGA on the DE0-Nano prototyping board [7] that allows switching among $m = \{2, 4, 8\}$. Moreover in the transmitter side we use a reference clock of frequency mf_c, and on the receiver side we have added an input matching stage. To test the BER performance of the receiver in operation we have used the test setup given in [5] with the parameters given in the example of Section III.

Theoretical curves are computed with an equivalent noise bandwidth $B_N^* = f_s = 10$ kHz for all modulations, while the actual noise bandwidth of our receiver is wider, $B_N = 58.1$ kHz [8]. So, instead of using

$$\gamma_b = \sqrt{\frac{E_b}{N_0}} \tag{11}$$

in Table I, we have used

$$\gamma_b = \sqrt{\frac{E_b}{N_0}\frac{B_N^*}{B_N}}. \tag{12}$$

This way, theoretical BER curves are moved to the right a value equal to

$$10 * \log_{10}\left(\frac{B_N}{B_N^*}\right) \simeq 7.64 \text{ dB} \tag{13}$$

to cancel the noise bandwidth difference, as is shown in Fig. 6. We have used

$$P_s = r_b E_b = r_b N_0 \gamma_b, \tag{14}$$

with $N_0 = k_B T$, being k_B the Boltzmann constant and $T = 298$ K, to relate the input power P_s in Fig. 6 with γ_b given in Table I.

Figure 6 shows an excellent agreement when comparing relative differences among the measured results with the relative differences among the theoretical results, while the remaining difference between theoretical and measured BER of $\simeq 4$ dB, with BER between 10^{-4} and 10^{-2}, is mainly due to the receiver noise figure and to a lesser extend to the phase-quantization error.

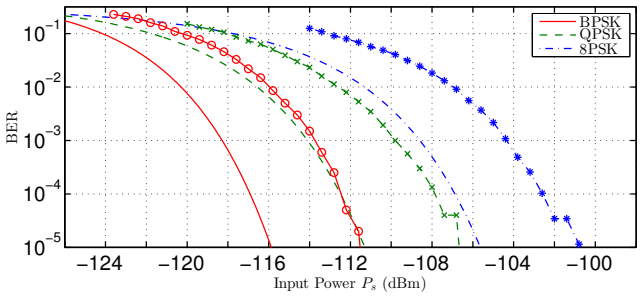

Fig. 6. Theoretical (without markers) and measured (with markers) BER curves. Theoretical curves have been translated to consider actual noise bandwidth.

V. Conclusion

The main result is that we have build the first MPSK SR transceiver able to switch among BPSK, QPSK and 8PSK modulations. The implementation is based on an FPGA, minimizing the use of analog circuitry. To be able to make a fair comparison between BER figures, a relation between the number of samples N used to determine the phase of the SRO pulse and the number of symbols m has to be fulfilled. This rises the problem of selecting a single reference clock frequency capable of generating the signals involved in the digital sampling and decoding stages. This is solved using a symbol signal period T_s' different than the symbol period T_s, producing a known phase shift that can be corrected without consuming extra resources. Excellent agreement between theoretical and measured BER results validate the transceiver. After correcting the bandwidth receiver, the remaining difference, $\simeq 4$ dB, is mainly attributed to the receiver noise figure which has not been optimized.

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