Analysis of Soft Error Rates for future technologies

Marc Riera Villanueva

Universitat Politècnica de Catalunya (UPC)
Facultat d'Informàtica de Barcelona (FIB)

Advisor: Ramon Canal
Co-Advisor/s: Jaume Abella and Antonio González
Departament d'Arquitectura de Computadors (DAC)

Date: 03/07/2015

Index

List of Figures

List of Tables

1. Summary

System reliability has become an important design aspect for computer systems due to the aggressive technology miniaturization. Errors are strongly related to the technology used to build the hardware and soft errors due to radiation. Therefore, this project is focused on describing and characterizing soft errors through current and future technologies. A methodology to characterize soft errors with different hardware components and technologies has been developed. Results at the technology layer show that current technology is in a dangerous point regarding the reliability aspect of the system while new technologies achieve a good improvement.

2. Introduction

Power consumption and performance are probably the most important design aspects in a computer system nowadays. However, the aggressive technology scaling introduces a large set of different sources of failure for hardware components [1]. Therefore, the reliability has become another important design aspect for computer systems. Unreliable hardware components affect computing systems at several levels. Errors are strongly related to the technology used to build the hardware blocks composing the system and are caused by effects such as physical fabrication defects, aging or degradation (e.g., NBTI), environmental stress (e.g., radiations), etc.

After a fault manifests in a given hardware block, it can be propagated through the different hardware structures composing the full system. Even if several faults can be masked during this propagation either at the technology or at the architectural level, some of them can possibly reach the software layer of a system by corrupting either data or instructions composing a software application, as shown in Figure 2.1. These errors can prevent the correct execution producing erroneous results if the computation is completed, or even prevent the execution of the application by causing exceptions, abnormal termination or lead to an application crash. This may have a serious impact on the overall reliability of the system.

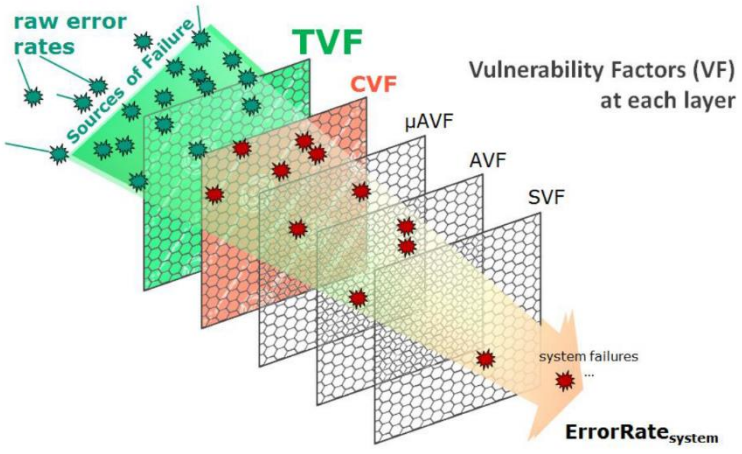


Figure 2.1: Error Propagation through different levels

This thesis analyses current and future technologies and describes the most common failure mechanisms. Radiation induced failures, more commonly called Soft Errors, have a huge impact on the reliability of new systems and its importance is increasing. Therefore, as soft errors are becoming a major concern in the industry, this project is focused on their characterization [2].

The most common and basic elements of hardware are simulated with different technology models to characterize their vulnerability to soft errors. A methodology to characterize soft errors is developed based on the literature. The first step is to find predictive models for the future technologies and develop SPICE circuits for the components that our analysis targets. The next step is to perform the SPICE simulations to test the reliability of these components with the different technologies and parameters like voltages or temperatures. Finally, the Soft Error Rate (SER) of each basic component can be computed, which can be used to compute the SER of more complex components like SRAM memories or logic blocs. Moreover, possible trends about SERs can be analyzed using the data obtained.

The document is organized in the following sections:

- **Introduction and Objectives:** Sets the background for the document.
- **Fundamentals and Related Work:** Describes the fundamentals and previous work done in the area of reliability for electronic devices.
- **Methodology:** Compares possible ways to compute the SER and describes the methodology used in this work.
- **Technology Review:** Review of the most promising future technologies.
- **SPICE Modeling:** Describes how the predictive technology models are done and how can be used to design SPICE circuits.
- **Analysis of Basic Components:** Gives a description and a summary of the data obtained for each component.

- **Trends in Soft Error Rates:** Gives some hints about future trends in soft errors comparing different technologies, elements and parameters.

- **Future Work and Conclusions:** Describes de work planned to do in near future and gives some final conclusions on the results obtained.

3. Objectives

The main objectives of this master thesis are:

- Studying the most promising future technologies
- Designing the SPICE circuits of the most common hardware elements including basic logic gates (AND, OR, NOT…), SRAM Cells and Registers
- Developing a methodology to characterize the Soft Error Rate of different hardware elements using different technologies
- Analyzing SER trends taking into account multiple parameters to compare

Consequently, the tasks conducted have been the following:

- Finding and testing the predictive models of the technologies selected
- Reviewing related work in the literature to find possible models to characterize the Soft Error Rate
- Analyzing the results of each component

4. Fundamentals and Related Work

This chapter introduces some initial concepts and gives a summary of the main failure mechanisms affecting electronic devices. Moreover, as the project is focused on analyzing soft errors, a complete description of radiation failures is included.

4.1. Faults, Errors and Failures

Faults, errors and failures are terms that are often confused but have different meanings [3]. A fault is a defect that may trigger an error, stay dormant or simply disappear. Faults in hardware structures could arise from defects, imperfections, or interactions with the external environment. Examples of faults include manufacturing defects in silicon chip or bit flips caused by cosmic ray strikes.

Faults are usually classified into three categories: permanent, intermittent and transient. Permanent faults remain for indefinite periods till corrective action is taken. Oxide wearout leading to a transistor malfunction is an example. Intermittent faults appear, disappear, and then reappear and are often early indicators of permanent faults. Finally, transient faults are those that appear and disappear in a very short period of time (typically one cycle). Bit flips or gate malfunctions due to a neutron strike are examples of transient faults. A fault in a particular system layer may not show up at the user level. This may be because the fault is being masked in an intermediate layer, a defective transistor may affect performance but not the correct operation, or because any of the layers may be designed to tolerate some faults.

Errors are the manifestation of faults and can be classified in the same way as faults. Faults could cause an error, but not all faults show up as errors. The final term, failure, is defined as a system malfunction that causes the system not to meet its correctness, performance, or other guarantees. Figure 4.1 summarizes this terms in the way of when they can arise.

Figure 4.1: Summary of fault, error and failure terms

Figure 4.2 shows the different types of SRAM failures, which can arise from manufacturing defects, process variations, alpha particles or neutron strikes, and are similar in logic gates.

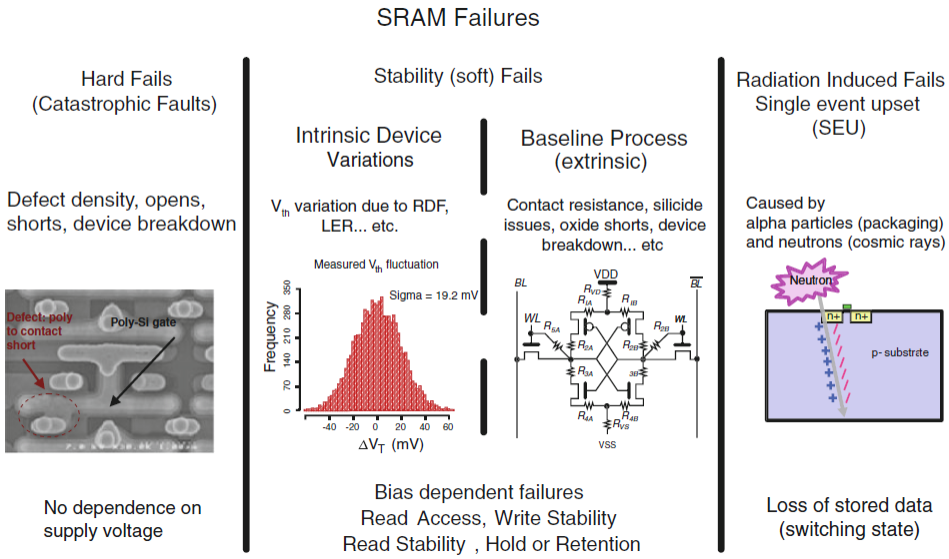


Figure 4.2: Different types of SRAM failures

4.2. Sources of Failure Summary

This project focuses in analyzing the soft errors produced by Radiation Induced Faults (RIF) and the next section has a detailed description of this type of errors. However, a previous study of different failure mechanisms has been done to know their effect on the reliability of the system. Table 4.1 summarizes the main types of failure mechanisms giving a brief description of each one [4][5][6].

Sources	Description
Random Dopant Fluctuations (**RDF**)	Process variation caused by the random fluctuation in the number of dopants in the channel gate and their placement, which results in threshold voltage (Vth) variations producing permanent failures.
Line Edge Roughness (**LER**)	Process variation caused by the change in the shape of the gate along the channel width direction, which results in Vth variations.

Random Telegraph Noise (**RTN**)	Random fluctuation in the device drain current due to the trapping and detrapping of channel carriers in the dielectric traps at the oxide interface, which causes Intermittent variations in the Vth.
Metal Stress Voiding (**MSV**)	Voids in metal lines due to different thermal expansion rates of metal lines and the passivation material they bond, causing permanent failures.
Electromigration (**EM**)	Voids in metal lines or interconnects caused by the electron flow and resulting in permanent failures.
Hot Carrier Injection (**HCI**)	Arises from impact ionization when electrons in the channel strike the silicon atoms around the drain-substrate interface. HCI results in a reduction of the maximum operating frequency of the chip.
Gate Oxide Wearout (**GOW**)	Sudden discontinuous increase in conductance causing a reduction in the current of the transistor, which may initially lead to intermittent faults but may eventually cause a permanent fault.
Negative/Positive Bias Temperature Instability (**NBTI/PBTI**)	Reduction in mobility of holes and shift in Vth when the device is under stress, like high temperatures, slowing down the transistor. NBTI affects pMOS transistors while PBTI affects nMOS transistors.
Radiation Induced Failures (**RIF**)	Can be produced by alpha particles from packaging and neutrons from the atmosphere producing transient failures.

Table 4.1: Summary of Failure Mechanisms

Most of the faults described in this summary can be taken care before a chip is shipped as most of them are related to process variations. Therefore, the most challenging failures to track are the ones related to aging and radiation. Since radiation failures have become more important in recent years and aging is already well known, this thesis only covers the analysis of radiation failures.

4.3. Radiation Induced Failures (RIF)

Radiation induced transient faults [4] can be produced due to different types of sources: alpha particles from packaging and neutrons from the atmosphere. Radiation faults are addressed with fault detection and error correction circuitry.

An alpha particle consists of two protons and two neutrons bound together into a particle. Alpha particles are emitted by radioactive nuclei, such as uranium or radium, in a process known as alpha decay. Alpha particles have kinetic energies of a few MeV, which is lower than those of neutrons that affect CMOS chips. Nevertheless, alpha particles can affect semiconductor devices because they deposit a dense track

of charge and create electron-hole pairs as they pass through the substrate. Alpha particles can arise from radioactive impurities used in chip packaging such in the solder balls or contamination of semiconductor processing materials. Alpha particles are already well known and can be reduced in different ways by changing the packaging of the chip. Therefore, we focused on computing the soft error rates due to neutrons.

The neutron is one of the subatomic particles that make up an atom. Atoms are considered the basic building blocks of matter and consist of three types of subatomic particles: protons, neutrons and electrons. A proton is positively charged, a neutron is neutral and an electron is negatively charged. An atom consists of an equal number of protons and electrons and hence it is neutral itself. The neutrons that cause soft errors arise when atoms break apart into protons, electrons and neutrons. Protons have a long half-life so can persist for long durations before decaying. They constitute the majority of the primary cosmic rays that bombard the earth's outer atmosphere. When these protons and associated particles hit atmospheric atoms, they create a shower of secondary particles named secondary cosmic rays. Untimely, the particles that hit the earth's surface are known as terrestrial cosmic rays.

Alpha particles and neutrons slightly differ in their interactions with silicon crystals. Charged alpha particles interact directly with electrons. In contrast, neutrons interact with silicon via inelastic or elastic collisions. Inelastic collisions cause the incoming neutrons to lose their identity and create secondary particles, whereas elastic collisions preserve the identity. Inelastic collisions cause the majority of the soft errors due to neutrons.

Neutrons do not directly cause a transient fault because they do not directly create electron hole-hole pairs in silicon crystals (as alpha particles). Instead, these particles collide with the nuclei in the semiconductor resulting in the emission of secondary nuclear fragments. These fragments could consist of particles such as pions, protons, neutrons, deuteron, tritons, alpha particles and others. These

secondary fragments can cause ionization tracks that can produce a sufficient number of electron-hole pairs to cause transient faults in the device.

The charge accumulation needs to cross a certain threshold before an SRAM cell, for example, will flip the charge stored in the cell. This minimum charge necessary to cause a circuit malfunction is termed as the critical charge of the circuit represented as Qcrit. Typically, Qcrit is estimated in circuit models by injecting different current pulses till the circuit malfunctions. Hazucha and Svensson [7] proposed the following model to predict neutron induced Soft Error Rate (SER):

$$Circuit\ SER = Constant\ x\ Flux\ x\ Area\ x\ e^{-\frac{Qcrit}{Qcoll}}$$

Constant is a constant parameter dependent on the process technology and circuit design style, *Flux* is the flux of neutrons at the specific location, *Area* is the area of the circuit sensitive to soft errors, and *Qcoll* is the charge collection efficiency, which is the ratio of collected and generated charge per unit volume. *Qcoll* depends strongly on doping and *Vcc* (operating voltage) and is directly related to the stopping power, so the greater is the stopping power, the greater is *Qcoll*. *Qcoll* can be derived empirically using either accelerated neutron tests or device physics models, whereas *Qcrit* is derived using circuit simulators. Figure 4.3 shows a diagram illustrating the effects of soft errors.

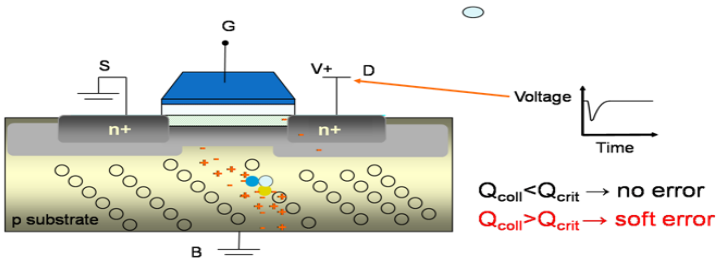


Figure 4.3: Diagram of soft errors effects

With every process generation, the area of a given circuit shrinks, so this should reduce the effective SER from one process generation to the next. However, Qcrit also decreases because the voltage of the circuit decreases across process generations. Therefore, for some elements like latches and logic, this effect appears

to cancel each other out, resulting in a constant SER across generations. However, if Qcrit is sufficiently low, such in SRAM devices, then the impact of the area begins to dominate. This is referred as saturation effect, where the SER decreases with process generations. However, the circuit is highly vulnerable to soft errors in the saturation region. In the extreme case, as Qcrit approaches to zero, almost any amount of charge produced by alpha or neutron strikes will result in a transient fault.

When a charge produced by an alpha particle or neutron strike is sufficient to overwhelm a circuit, then it may malfunction. At the gate or cell level, this malfunction appears as a bit flip. For storage devices, when a bit residing in a storage cell flips, a transient fault is said to have occurred. For logic devices, a change in the value of the input node feeding a gate or output node coming out of a gate does not necessarily mean a transient fault has occurred. Only when this fault propagates to a forward latch or storage cell does one say a transient fault has occurred.

4.4. Environmental Considerations

Environmental factors can impact the characteristics or behavior of a source of failure. Table 4.2 shows different environmental factors and describes how these factors impact on the different types of errors. In our simulations, these environmental factors will also be taken into account using different voltages and temperatures, and later analyzing the SER in different locations and altitudes.

Factors	Transient errors	Intermittent errors	Permanent errors
Temperature	Increased leakage	Device degradation (e.g. NBTI effects) and thermal stress	Device degradation (e.g. Electromigration) and thermal stress (e.g. Wear Out)
Humidity/Dust Acid/Salt	Not Affected	Not Affected	Corrosion/shorting on contacts
Vibration/Pressure Gravity	Not Affected	May cause intermittent failures depending on the strength	Mechanical stress and contact/solder breaks
EMC/EMI Radiation/Altitude	Increased interferences	May cause intermittent failures for unshielded components	Oxide failure or metal melt and device degradation effects

Table 4.2: Environmental factors and their effects on different types of errors

4.5. Previous Analysis

Ziegler and Lanford [11] demonstrated on 1979 that cosmic rays creating energetic neutrons also could cause soft errors. Indeed, in modern devices, cosmic rays are the predominant cause of soft errors. They analyzed SRAM memories with experimental tests and developed they own method to characterize soft errors, the BGR method. From that point, many researchers have studied the effect of neutron strikes in electronic devices. One of the most important studies is the one from Hazucha and Svensson [15]. They analyzed a 65nm SRAM with experimental tests and then propose a model to characterize soft errors through different technologies, which is the model used in this work.

Many studies focus on characterizing the soft error rates of individual components such as latches [41], flip flops [42] or SRAM cells [43], using Hazucha's model or experimental tests. Some of these studies also provide alternative designs of these components to improve their resistance to radiation. In addition, there have been some studies analyzing all the basic components including combinatorial logic [25]. Nevertheless, most of them are done for bulk planar technologies up to 22nm, but there are also some recent studies on new technologies such as FinFET [44], SOI [22] and III-V HEMT [45].

Our work provides the soft error characterization of all the basic components that can be found in any electronic device. Moreover, we provide data for the most recent technologies, materials and technology nodes. In addition, we also provide data for different environmental setups. To the best of our knowledge, in the literature there is not a study comparing SERs for all those recent technologies on the same ground. Works analyzing specific technologies build upon different assumption and methodologies, thus limiting the conclusions that can be extracted when comparing different technologies. Therefore, our work settles the same assumptions and methodologies for the different technologies compared so as high confidence can be had on the conclusions obtained.

5. Methodology

This chapter describes the methodology used to compute Soft Error Rates (SER) for different hardware blocks and technologies. First of all, we do an evaluation of the most important models and methods to compute the SER. Then, we justify our decision of developing our own methodology based on some of these models. Finally, our own methodology and the tools needed are described. Before entering in the methodology, some general considerations are made below.

As described in chapter 4, for an alpha particle or a neutron to cause a soft error, the strike must flip the state of a bit. Whether the bit flip eventually affects the final outcome of a program depends on whether the error propagates without being masked, and whether there is some error detection and correction scheme. Architecturally, the error detection and correction mechanisms create two categories of errors: Silent Data Corruption (SDC) and Detected Unrecoverable Error (DUE) [4].

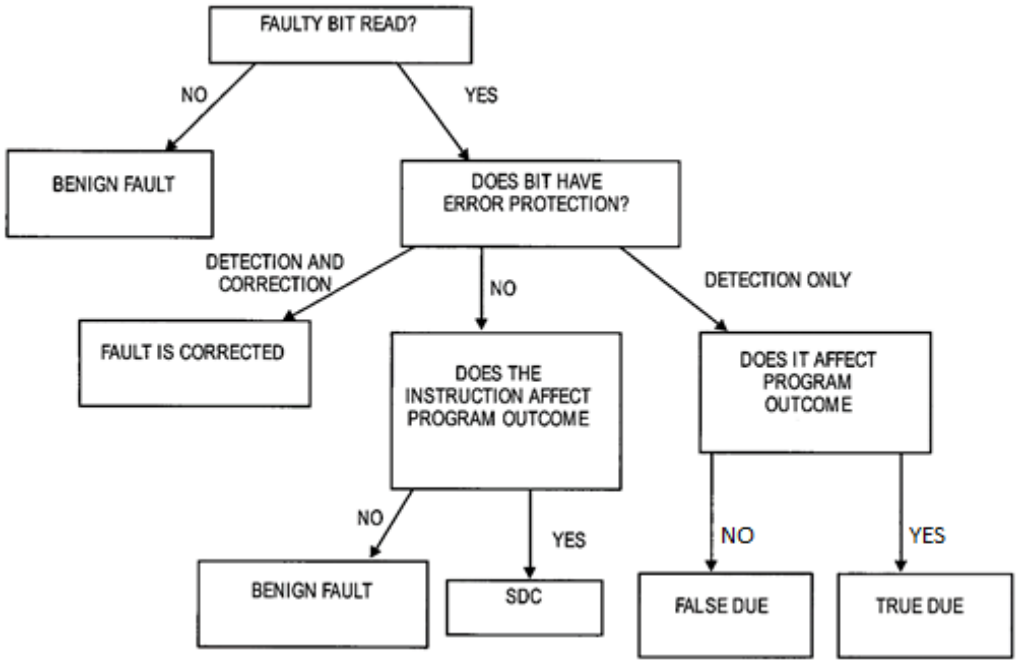


Figure 5.1: SDC and DUE Scheme

Figure 5.1 shows the different outcomes of a bit flip. The most insidious form of error is SDC since a fault induces the system to generate erroneous outputs. SDC rates can be expressed as either Failure in Time (FIT) or Mean Time to Failure (MTTF). FIT rates are the number of failures in one billion (10^9) device-hours of operation while MTTF describes the expected time to failure for a non-repairable system.

To avoid SDC, designers use basic error detection mechanisms, such as parity. The ability to detect a fault but not correct it avoids generating incorrect outputs, but prevents from finalizing the task. Therefore, simple error detection does not reduce the overall error rate but provides fail-stop behavior and avoids data corruption. Errors in this category are called DUE, and can also be quantified using FIT and MTTF. DUE events are further divided according to whether the detected fault would have affected the final outcome of the execution or not, calling them true and false DUE respectively. In following sections, SERs are expressed in FIT rates.

5.1. Modeling Circuit Level Soft Error Rates (SER)

Computing the SER of a microprocessor requires the analysis of two areas: the raw SER of the circuits comprising the chip (technology vulnerability) and the corresponding derating factors [4]. Computing the raw SER of a circuit element is generally done in a two-step process: first one must compute the critical charge (Qcrit) that the charge released by a neutron strike must overcome to cause a malfunction. Thereafter, the Qcrit must be mapped to a corresponding SER for the circuit element. The general procedure to compute the SER applies to memory elements, latches and logic gates.

Once the raw SER is computed, it needs be derated by a variety of vulnerability factors. For example, if a latch is not vulnerable 50% of the time, then the raw SER needs to be multiplied by 0.5 to compute the derated SER. Later in this chapter, a description of such vulnerability factors and masking effects and how are they taken into account in our results is included.

5.2. Critical Charge (Qcrit)

An alpha particle or a neutron strike typically manifests itself as a transient disturbance that would usually last less than 100 picoseconds. If this charge disturbance is smaller than the noise margin, the circuit will continue to operate correctly. Otherwise, the disturbed voltage may invert the logic state.

Figure 5.2 shows an SRAM cell made of a pair of cross-coupled inverters. When the wordline is low, the cell holds data in the inverters and the bitlines are decoupled. If a particle strike causes one of the sensitive nodes to transition, then the disturbance may propagate through the inverter and cause a transient disturbance on the second sensitive node. This will cause the second node to propagate the incorrect value, thereby causing both nodes to flip. This results in flipping the state of the bit held in the SRAM cell. Other circuit elements, such as register files, latches and logic gates, are affected in similar ways by particle strikes.

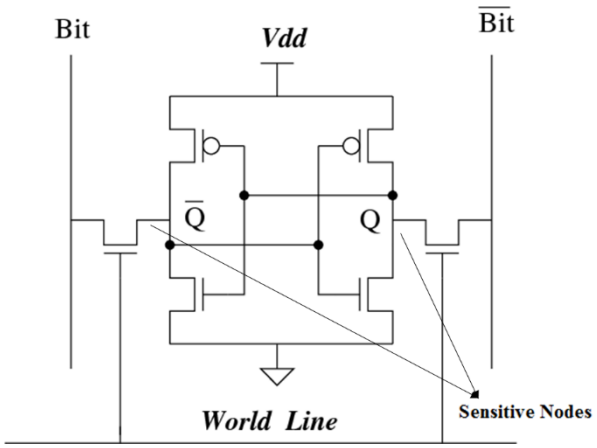


Figure 5.2: A transistor-level diagram of an SRAM cell

Critical charge (Qcrit) [4] is defined as the minimum charge that must be deposited by a particle strike to cause a circuit malfunction. Qcrit is usually computed using integrated circuit simulators, such as SPICE, by injecting current pulses into the sensitive nodes of a circuit as can be seen in Figure 5.3.

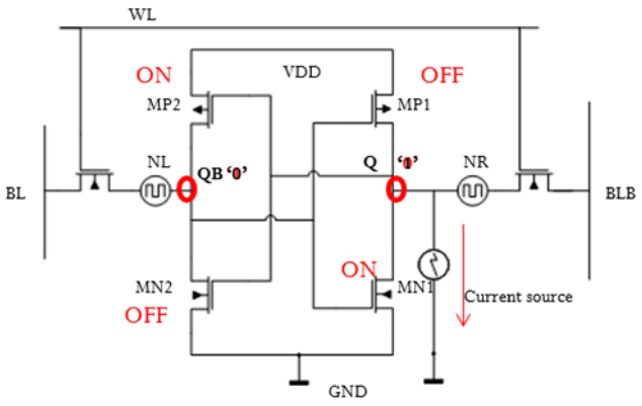


Figure 5.3: Current pulse injected in a 6T SRAM Cell sensitive node

The current pulses represent the current generated from electron-hole pairs created by a neutron strike. The smallest charge corresponding to an injected current pulse that inverts the state of a circuit element is the Qcrit of the circuit. However, there are many factors that impact the critical charge [8]. Because *charge = capacitance x voltage*, Qcrit depends on the supply voltage. Qcrit is also weakly dependent on temperature and strongly dependent on the shape of the current pulse injected.

The pulses in general have a rapid rise followed by a slow decay, and are characterized by their time constants. A circuit which recovers quickly from a disturbance may have a lower Qcrit for a spike of current than for a slower pulse. A high number of current models have been proposed in the literature [9] over the years and they are used to characterize Qcrit by performing SPICE simulations. The most common pulses are:

- **Roche Model**: Qcrit can be found by integrating an exponentially decaying current ($I_0.exp(-\tau)$) with small time constants which are less than 20ps.

- **Diffusion Model**: Qcrit can be found with a diffusion collection model where t_{max} represents the instant when the maximum value of the current is reached, and can be represented by the following equation:

$$I(t) = I_{max}\,[exp(t_{max}/t)]^{3/2}\,[exp(-3t_{max}/2t)]$$

- **Freeman Model**: Current is defined in terms of total charge deposited (Q) by the ion and a single timing parameter τ by the following equation:

$$I(t) = (2/\sqrt{\pi}).(Q/\tau).(\sqrt{(t/\tau)}).exp(-t/\tau)$$

- **Double Exponential Model**: The most commonly used model by the community is a double exponential pulse with two timing parameters representing the rising and falling time constants of the exponentials. The following equation is used:

$$I(t) = (Q/(\tau f - \tau r)\,[exp(-t/\tau f) - exp(-t/\tau r)]$$

Figure 5.4 shows a plot with an example of each of these current pulses. The current pulse rise and fall times strongly affect the characterization of Qcrit, to the point where each pulse model results in its own Qcrit value.

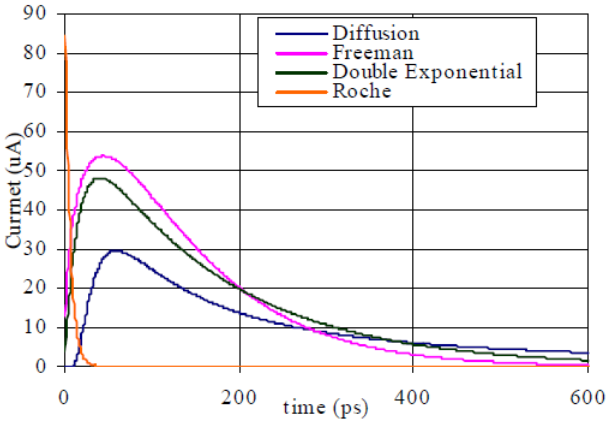


Figure 5.4: Current Pulse Profiles

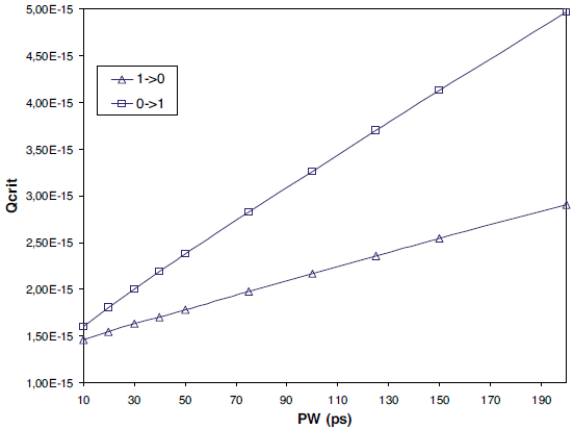


Figure 5.5: Pulse Width dependence of Qcrit

Another factor that strongly affects the value of Qcrit is the pulse width, as can be seen in Figure 5.5, which determines the range of the integral from where Qcrit is computed [10]. Some empirical approximations have been used in the literature to select values for these parameters. However, there is not a unique way to make the computation of Qcrit. Therefore, multiple voltages, temperatures, types of current pulses and parameters for these pulses can be tested. Section 5.6 describes how we compute the Qcrit and which parameters are used.

5.3. Mapping Qcrit to SER

Once Qcrit is computed for a specific circuit element, it needs to be mapped into a SER expressed in FIT. This mapping can be derived by combining physics-based models and experimental data. There are different models and methods to do this mapping. Three of these models are especially relevant as the rest are based on them by adding extensions or adjusting parameters, and there is also the option to use model simulations [4]. These models and methods are described below:

- **Hazucha and Svensson Model**: One can start from an equation such as the one proposed by Hazucha and Svensson [7]:

$$Circuit\ SER = Constant\ x\ Flux\ x\ Area\ x\ e^{-\frac{Qcrit}{Qcoll}}$$

  Flux is the neutron flux experienced by the circuit, *Area* is the effective diffusion area, and Qcoll is the collection efficiency. The parameters of the equation (e.g., *Constant*, *Qcoll*) can be derived empirically using accelerated tests. Such empirical mapping is a popular method to compute the SER of CMOS circuits. However, the equation must be calibrated for each new technology generation.

- **Burst Generation Rate (BGR) Method**: The BGR method proposed by Ziegler and Lanford [11] is based on two key parameters: the sensitive volume (SV) and neutron-induced recoil energy (E-recoil). An upset is said to occur if the burst of charge generated by neutron-silicon interactions within the SV of a device is greater than *Qcrit*. E-recoil is expressed as:

$$E - recoil = Qcrit\ x\ 22.5,$$

  Then, the upset rate is computed as:

$$Upset\ rate = Qcoll\ x\ SV\ x \int_{E-neutron} \left(BGR(E - neutron, E - recoil) \frac{dN}{dE} \right) dE$$

Where *dN/dE* is the differential neutron flux, *E-neutron* is the neutron energy, the BGR function is the energy deposited in silicon by neutron interactions, and *Qcoll* is the collection efficiency. Empirical heavy ion testing is used to obtain and tabulate the BGR values and the integration is performed numerically using the experimental BGR data.

- **Neutron Cross-Section (NCS) Method**: To compute the device upset rate using the BGR method, one must compute the SV of the device, which is often difficult to compute. Instead, the NCS method proposed by Taber and Normand [12] tries to avoid using the SV parameter (as well as Qcrit), by directly correlating the neutron environment parameters, such as flux and energy, with the device upset rate. NCS expresses the upset rate as:

$$Upset\ rate = \int_{E-neutron} (\sigma \frac{dN}{dE}) dE$$

This equation replaces Qcoll, SV and the BGR function, with a single variable σ denoting the neutron cross section. The neutron cross section is defined as the probability that a neutron with energy *E-neutron* will interact and produce an upset. These probabilities are generated for specific device types using accelerated neutron tests.

- **Simulation Models**: Murley and Srinivasan had proposed modeling the charge collection phenomenon simulating neutron strikes from first principles [13]. In cases where simulations result in a collected charge greater than Qcrit, the circuit is assumed to malfunction. This gives the probability of an upset given a certain neutron flux, and can be easily converted into FIT rate. However, this methodology requires detailed knowledge of the process technology and how that can interact with neutrons.

The soft error models must be calibrated and validated with measurements. Because soft errors typically occur once in several years in a single chip, the occurrence of errors needs to be accelerated to measure them in a short period of time. This can be accomplished either by collecting data from numerous chips and computers or by increasing the flux of the generated alpha particles and neutrons. For neutrons, the accelerated neutron tests can be performed in particle accelerators. Thus, soft errors can be captured easily by exposing the test chips to a neutron beam.

All these models have advantages and disadvantages, Table 5.1 summarizes them:

Model	Pros	Cons
Hazucha and Svensson	• Qcrit and Area can be easily computed • Popular and widely used in the literature	• Constant and Qcoll derived empirically
Burst Generation Rate (BGR)	• Qcrit can be easily computed	• Qcoll and BGR require empirical tests • SV difficult to compute without good knowledge of the chip's layout
Neutron Cross-Section (NCS)	• Sensitive Volume not required	• Requires experimental tests • Probabilities for specific devices • Qcrit not used
Simulation Models	• Once the probability of an upset is obtained it can be easily converted into FIT	• Requires detailed knowledge of the technology and its interaction with neutrons

Table 5.1: Pros and Cons of each model

In our methodology, the Hazucha and Svensson model is used because is the most common in SER studies [14][25] and has been validated with experimental data [7][15]. Moreover, most of the required parameters can be computed with the tools and resources that we have. Qcrit can be obtained with SPICE simulations and the Area can be easily computed since the dimensions of the transistors are specified. Moreover, we can deal with the parameters derived empirically scaling them as is described later in this chapter. The other methods require detailed knowledge in fields that are out of our specialization and tools that are out of our possibilities.

5.4. Neutron Flux

The reference neutron flux commonly used in the SER computation is from New York City at sea level. However, neutron flux depends on the location and is mainly affected by two parameters: Altitude and Vertical Cutoff [16]. Neutron flux increases exponentially with the altitude while the vertical cutoff is a parameter of the magnetic field of the earth which depends on the coordinates as can be seen in Figure 5.6. The earth magnetic field maximum is in the poles while the minimum is in the equator. Therefore, the neutron flux decreases when approaching the equator and increases in the poles. The neutron flux also depends on the solar activity.

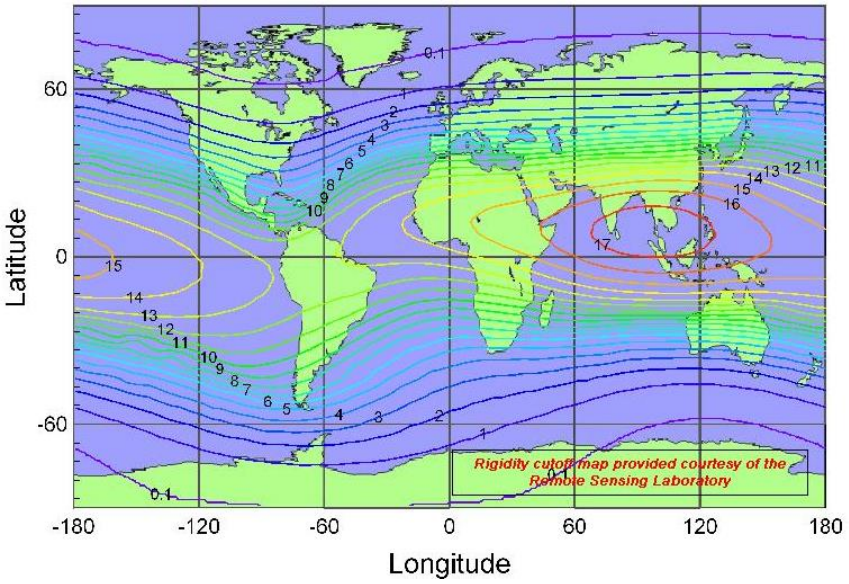


Figure 5.6: Vertical Cutoff Map

There are two main ways to compute the flux considering the location. First one involves using the methodology described in Annex A of the JEDEC standard [17]. Alternatively, one can use the online calculator from [18] which is compatible with the JEDEC standard and outputs the flux relative to the flux from NYC. The second method involves the use of a model tested and corrected with empirical data which has been proposed by Gordon, et al. [19], and has the following high level form:

$$F = F_{ref}\ x\ F_{alt}(d)\ x\ F_{BSYD}(Rc,\ d,\ I)$$

Where F_{ref} is the flux at a reference location (i.e.: Flux of New York City at sea level), F_{alt} is the function describing the dependence on altitude, F_{BSYD} is the function describing the dependence on geomagnetic location and solar activity, d is the atmospheric depth, Rc is the vertical cutoff and I is the relative count rate of a neutron monitor measuring solar modulation. Both ways are equally good and can be used to obtain a relative flux that can be directly multiplied by the SER computed with the reference flux. Table 5.2 shows the flux in some locations of the United States:

Locations	Altitude (m)	Cutoff (GV)	Relative Flux	Total Flux
Fremont Pass, CO	3450	2,94	12,58	0,07
Leadville, CO	3150	2,97	9,56	0,05
Mt. Wash., NH	1905	1,58	4,70	0,027
Yorktown Hts., NY	167	2	1,20	0,007
Houston, TX	14	4,68	0,91	0,005

Table 5.2: Neutron Flux in USA Locations

Total flux has been obtained experimentally by Gordon, et al. and then fitted to their model [19]. Table 5.3 shows the neutron flux of different coordinates and altitudes:

Coordinates	Altitude (m)	Cutoff (GV)	Relative Flux	Total Flux
19N, 127W	20300	12	217,07	1,28
54N, 117W	20000	0,8	1495,42	10,2
56N, 121W	16200	0,7	1070,18	10
38N, 122W	11900	4,5	301,16	3,4
37N, 76W	0	2,7	0,99	0,0122

Table 5.3: Neutron flux at high altitudes

In this case, total flux has been obtained by measurements aboard an ER-2 high-altitude airplane [20]. The flux observed increases between 200x-1500x, and the effect of the vertical cutoff can be observed as the first location has a big cutoff and the flux is reduced around 7x compared with the second location which is at a similar altitude but has a low cutoff. In section 9.5, some examples of relative fluxes for different locations are given using the online calculator, including a SER example.

5.5. Time Vulnerability Factor and Masking Effects

Once the raw SER of a circuit is computed, it must be derated by the appropriate vulnerability factors to compute the circuit-level SER [4]. Timing Vulnerability factor (TVF) is the fraction of time a circuit is vulnerable to upsets. An SRAM cell usually has a TVF of 100% because any strike during a clock cycle can change the value stored in the SRAM cell. However, flip-flops and latches are clocked elements and have a TVF less than 100%.

Figure 5.7 shows a latch and its corresponding timing diagram. When the clock transitions from high to low the data at input D is latched. During the low phase of the clock, the latch is in the hold mode, maintaining the value at the output Q. The storage nodes of the latch are vulnerable to soft errors when the latch is holding data at the low phase of the clock. When the clock phase is high, the latch is in transparent mode driving data to the next stage, and is able to recover from a particle strike. Consequently, latches TVF is roughly 50% (half of the clock).

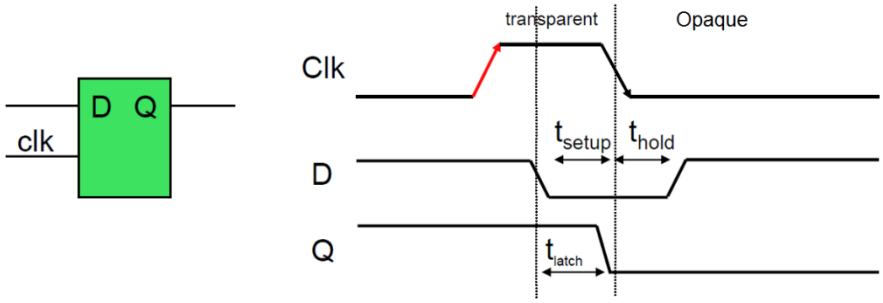


Figure 5.7: Latch Timing Diagram

In modern microprocessors, latches start to driven data during the hold mode so upsets must occur early in the low clock phase for the signal to propagate to the next element. Hence, TVF is usually smaller than 50% and also depends on different components, besides propagation delay, such as setup time, clock rise and fall time.

Logic gates are the building blocks of modern silicon chips. A malfunction due to a particle strike in one logic gate must reach and be captured in the forward memory element for the malfunction to cause an error. Otherwise, the effects are masked.

Thus, evaluating the SER of a logic gate consists of evaluating the Qcrit of each gate, mapping the Qcrit to the appropriate SER and evaluating if the fault introduced in the gate will be masked or reach the forward latch.

In today's microprocessors, more than 90% of the radiation induced faults in logic gates can be masked. Nevertheless, faults in logic gates cannot be ignored for three main reasons. First, modern microprocessors are composed of tens to hundreds of millions of logic gates. Second, the masking effects decrease with new technology generations. Third, it is more difficult to protect logic gates compared to SRAM cells because ECCs are difficult to implement for logic blocks. There are three kinds of masking commonly observed in logic blocks:

- **Logical Masking**: A strike can be logically masked if it affects a portion of the circuit that does not logically affect the final outcome of the circuit.
- **Electrical Masking**: A strike can be electrically masked if the pulse created by the strike attenuates before it reaches the forward latch.
- **Latch-Window Masking**: A strike can also be masked if the resulting pulse does not reach the forward latch at the clock transition where the latch captures its input value.

To accurately compute the SER of logic blocks, it is essential to model each of these masking effects. Electrical masking and latch-window masking can be taken into account at the technology layer, but for logical masking is required to know the function of the circuit and occurs one layer above. Consequently, we are still working in the integration of all these effects which are planned to be in future work.

5.6. Evaluation Framework and Tools

After considering the main models to compute the raw SER and their parameters, we defined our methodology which follows the workflow of Figure 5.8. As we target an exhaustive design space characterization, we wrote a python script for each component that is analyzed. Each script defines a collection of loops to simulate an element with a variety of configuration parameters, such as temperatures and voltages, and different technology models. In the inner loop, a function call is made. This function defines another loop to iterate the current injected with the pulse until a flip or glitch is detected measuring the stored value (SRAM) or the output (Logic Gates). An example of one script is shown in the following pseudocode:

Pseudocode of the Script:

```
For each Technology Do
      For each Voltage Do
            For each Temperature Do
                  For each Current Pulse Do
                        For each Input or Stored value Do
                              For each Sensitive Node Do
                                    Current=0;
                                    Flipped=0;
                                    While not flipped {
                                          Increase Current Injected;
                                          Generate SPICE Files;
                                          Simulate Element in HSPICE;
                                          Read Simulation Results;
                                          If Flip Detected {
                                                Flipped=1;
                                                Write Results in a CSV;
                                          }
                                          Clean Simulation Files;
                                    }
```

To make the SPICE simulations, HSPICE [21] which is a commercial circuit simulator from Synopsis, is invoked in a subprocess. The charge generated from a pulse that causes a malfunction is stored and defined as the Qcrit of that element in a specific state. Finally, for each Qcrit, a raw SER is computed using the model in [7] and stored into an Excel file, including the parameters that define the state.

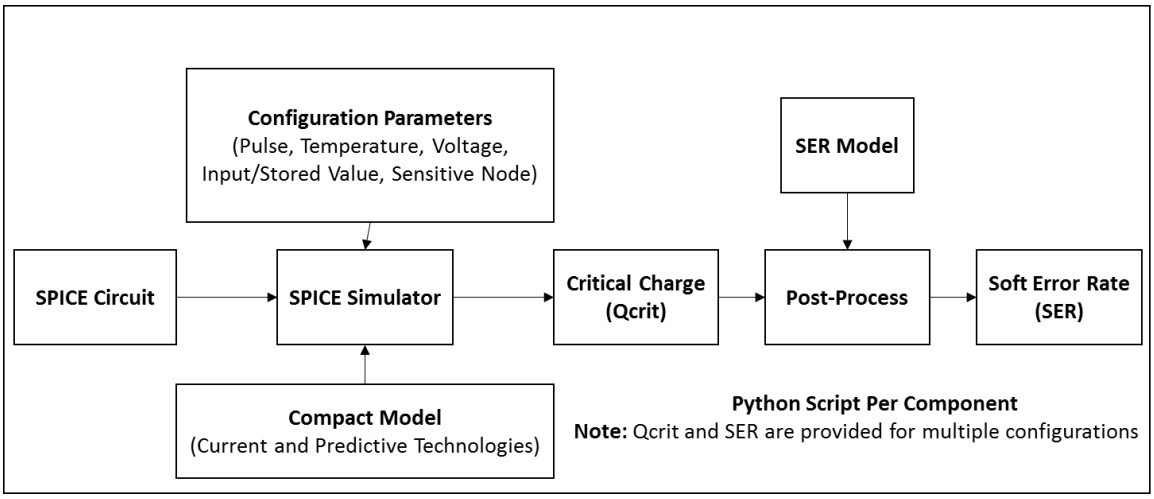


Figure 5.8: Workflow schema

As it has already been commented, there are many factors that affect the Qcrit. Because of that, we decided to test a variety of parameters and compute a Qcrit for each combination. Voltage ranges from 0.7V to 1.2V which can be used to distinguish between high performance and low power processors. Temperatures tested include 25, 50, 75 and 100 C^o which can be used to map idle, typical and extreme conditions. Stored values 0 and 1 have been tested for SRAM cells, and for logic gates all the input combinations have been analyzed. Moreover, each element may have more than one sensitive node so all nodes are considered.

A double exponential pulse is used since HSPICE only has this type. The shape of the current pulse also strongly affects Qcrit. For that reason, multiple rise time constants used in the literature (2ps, 16ps, 33ps and 90ps) have been tested but maintaining a falling time constant of 200ps [9][10]. Pulse width also has a strong effect on Qcrit affecting the integral range. Looking at the literature, there is not a clear way to define the pulse width so we decided to define it from the start of the

pulse until the pulse decreases an 80% of its maximum which represents the spike of the pulse. Then, Qcrit is computed by doing the integral of the current pulse in that range as can be graphically seen in Figure 5.9.

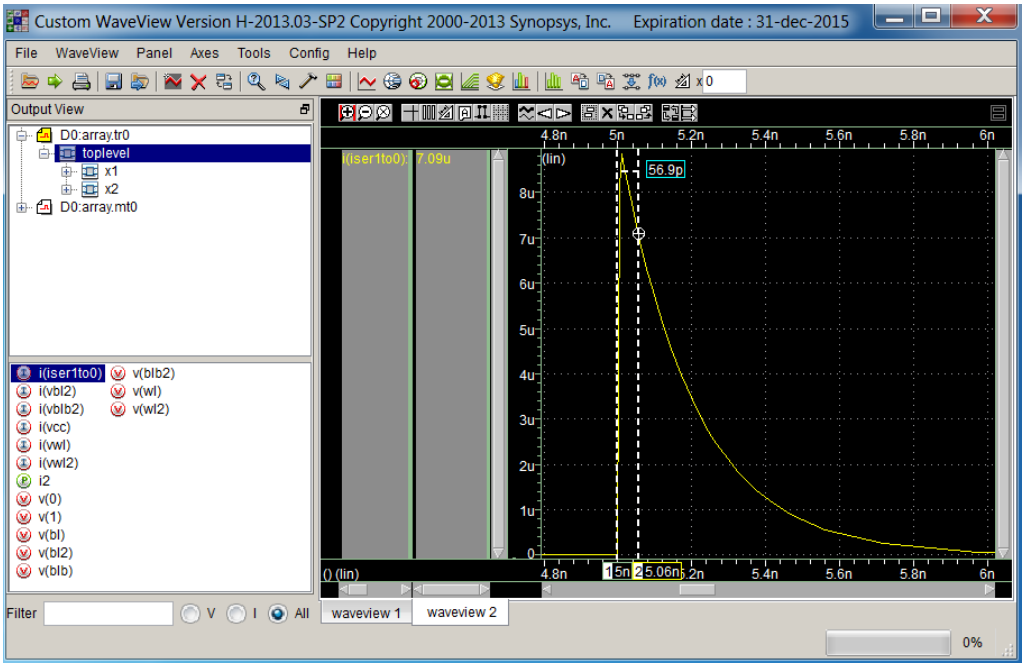


Figure 5.9: Qcrit Measurement

SER is computed using the Hazucha and Svensson model [7]:

$$SER_{raw}\ \alpha\ Constant\ x\ Flux\ x\ Area\ x\ e^{-\frac{Qcrit}{Qs}}$$

The area sensitive to neutron strikes is the drain area of the transistors which is defined in the SPICE circuits, so it can be easily obtained. The constant is a technology independent parameter which was computed by Hazucha and Svensson and has a value of $2.2*10^{-5}$. The exponential part of the formula is the technology vulnerability factor (TVF). If the charge collected (Qcoll) by a particle is greater than Qcrit a soft error is produced. Charge Collection Efficiency (Qs) is the mean of Qcoll in a range of energy particles and a parameter dependent of the technology which is usually computed experimentally. However, Qs scales approximately linear with the Length Gate (Lg), so Qs has been scaled down with a linear regression from experimental data [7] for CMOS technology. In the case of newer technologies, a

study of how Qcoll changes has been done, and an approximate technology factor has been extracted from previous works [22][23][24].

We can also combine the previous formula with the neutron flux model from Gordon to compute the neutron flux dependent of the location:

$$F = F_{ref}\ x\ F_{alt}(d)\ x\ F_{BSYD}(Rc,\ d,\ I)$$

Concluding this chapter, multiple SER values are obtained for each state, which is represented by the combination of parameters. However, the SER of the circuit or element is the sum of the SER from all sensitive nodes [25]. Therefore, SERs from different sensitive nodes but same conditions are summed. For example, a 6T SRAM cell has two sensitive nodes which are symmetric. Therefore, the SER of the cell can be computed as the sum of the SER of one node storing a 1 and the SER of the other node storing a 0. Then, depending on the element, SERs are derated by a timing factor, such as the latch where a factor of 50% is applied. Finally, a weighted average can be done with the SERs of different states to give a unique SER for the element. This is the case of logic gates where the SER can be averaged by the SERs of the different inputs, but still there will always be multiple SERs for the different voltages, temperatures and current pulses.

6. Technology Review

Planar Complementary Metal-Oxide Semiconductor (CMOS) technology is still being used and will stay here for a long time. Planar CMOS has been scaled down during many generations but physical limitations and reliability problems are starting to be a serious challenge for lower technology nodes. There are several technologies that are strong candidates to be used in a near future. In this chapter, the current and most promising technologies are reviewed.

6.1. Planar CMOS

Planar CMOS on Bulk-Si is the usual name to identify planar MOSFETs built in bulk silicon CMOS processes. As any other transistor, they can be thought as an ideal switch. When it is active the two terminals are connected and thus current flows through the switch, when it is inactive, the two terminals are not connected. This communication in a switch translates in the device to an active channel through which charge carriers, electrons or holes, flow from the source to the drain. The conductivity of the channel is a function of the potential applied across the gate and the source terminals.

The transistor terminals are: Source (S), through which the carriers enter the channel; Drain (D), through which the carriers leave the channel; Gate (G), the terminal that modulates the channel conductivity; and Body (B), the terminal that can slightly modulate the channel conductivity. Figure 6.1 shows a schematic of the planar CMOS transistor. Further details can be found in [36].

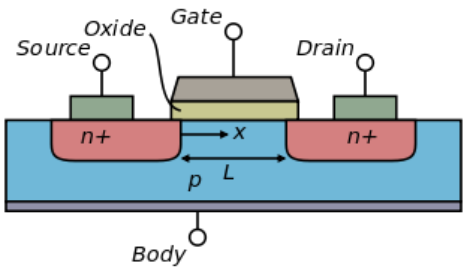


Figure 6.1: Planar CMOS transistor

6.2. FinFET

FinFETs emerged in high-end microprocessors in the last years. Figure 6.2 shows the basic structure of a FinFET. In contrast to the planar CMOS, the channel is surrounded by the gate on three sides, and not on just one side, with a thin silicon "fin". This configuration allows for better channel control and, thus, better "on-off" behavior (i.e., higher currents for when on, and lower currents –leakage- when off). The thickness of the fin is the major challenge for FinFET fabrication as it determines the effective length of the channel. Further details can be found in [37].

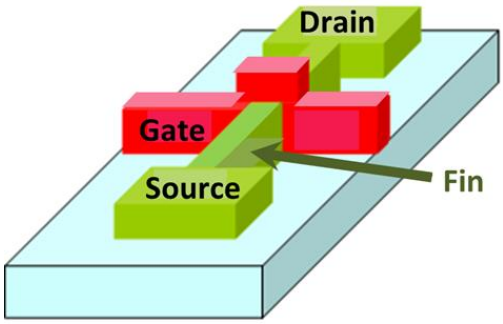


Figure 6.2: FinFET structure

6.3. Silicon on Insulator (SOI)

Silicon-On-Insulator (SOI) refers to the use of layered silicon-insulator-silicon substrate instead of the conventional silicon substrate. With SOI wafers, transistors are formed in thin layers of silicon that are isolated from the main body of the wafer by a layer of electrical insulator, usually silicon dioxide. Isolating the active transistor from the rest of the silicon substrate reduces the electrical current leakage that would otherwise degrade the performance of the transistor. Since the area of electrically active silicon is limited to the immediate region around the transistor, switching speeds are increased and sensitivity to soft errors is reduced [22].

Types of SOI-CMOS transistors are characterized by the thickness of the Si-SOI layer. For partially-depleted SOI-CMOS, the device Si layer is thicker than the depletion layer under the channel, in the range of 100 to 200 nm. As CMOS gates are scaled down, CMOS devices will be formed in thin Si layers, which are fully-

depleted in the channel region between the source and the drain junctions. For fully-depleted CMOS, the Si device layer is of the order of 50 nm and shrinking towards 10 nm, also known as the "nano-SOI" regime. Fully-depleted CMOS devices will take advantage of the ability of advanced SOI fabrication processes to provide wafers capable of forming dual-gate transistors, with control gates both above and below the thin channel. Figure 6.3 shows the predicted evolution of SOI devices together with their expected physical design. Further details can be found in [26].

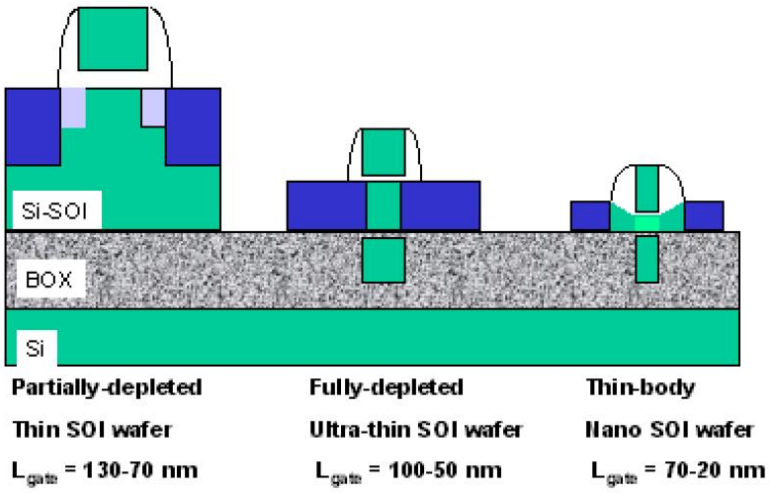


Figure 6.3: Different types of SOI devices

6.4. III-V HEMT

New device engineering is indispensable in overcoming difficulties of advanced CMOS and realizing high performance circuits under 10 nm. In this scenario, the channel materials with high mobility and low effective mass are preferable. Strong attention was recently paid to Ge and III-V semiconductor channels. Because of extremely high mobility and low effective mass of Ge and III-V semiconductors, these materials are suitable for high performance CMOS applications.

Transistors using these materials must be fabricated on Si substrates in order to utilize Si CMOS platform, meaning the necessity of the co-integration of III-V/Ge on Si, which is often called heterogeneous integration. Also, those channels must be ultrathin body structures such as ultrathin films, fin structures or nano-wire

structures, because of their better control of short channel effects. The gate stacks composed of high-K gate insulators and metal gates are regarded as mandatory for scaled CMOS. Figure 6.4 shows an experimental design of a III-V HEMT transistor. Further details can be found in [27].

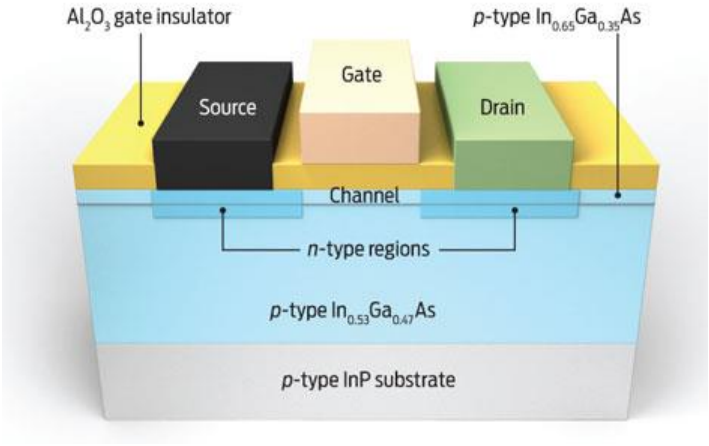


Figure 6.4: III-V HEMT experimental transistor design

6.5. Technology Roadmap

Chapter 6 identifies those technologies that are more likely to be important in the development of future systems and therefore to focus the research activities and resources to these technologies. Figure 6.5 shows the expected technology roadmap based on the ITRS predictions [33].

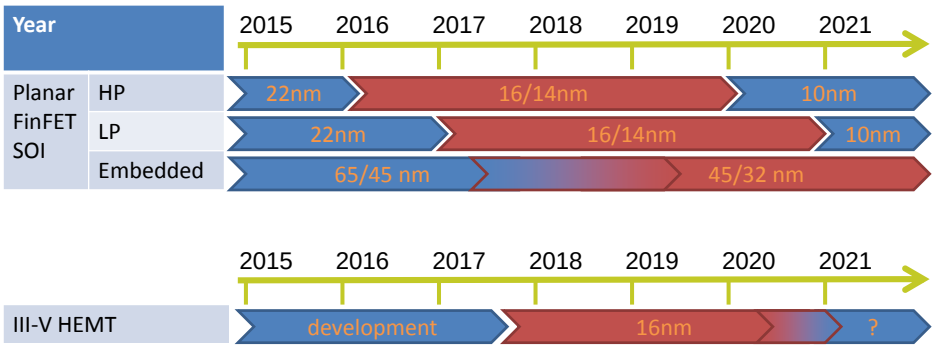


Figure 6.5: Technology Roadmap

7. SPICE Modeling and Circuit Design

This chapter is divided into two sections. First section describes the models for future technologies, and comments which are the main models and which models are used for our simulations. The second section gives the general guidelines about circuit design in SPICE using the predictive technology models, and describes the components analyzed in this project.

7.1. Predictive Models

Transistors are simple devices with a complicated physical behavior. Transistor models are used for almost all modern electronic design work. Circuit simulators such as SPICE use models to predict the behavior of a design and ensure the reliability of the circuit. Most design work is related to integrated circuit designs which have a very large tooling cost and there is a large economic incentive to get the design working without any iterations. Complete and accurate models allow a large percentage of designs to work the first time. Transistors are modeled using compact models with predicted parameters [28][29]. Compact models include effects of the transistor layout such as width, length, current-voltage characteristics, parasitic capacitances, resistances, time delays and temperature effects, among other physical effects.

The models used in SPICE are a hybrid of physical and empirical models. Physical models are based on the physical phenomena within a transistor, while empirical models are based on fitting measured data. Such models are incomplete unless they include specification of how parameter values are to be extracted for a specific technology node. In SPICE, these parameters are specified in the model card of each technology. To attempt standardization of model parameters used in different simulators, an industry working group was formed, the Compact Model Council (CMC) [30], to choose, maintain and promote the use of standard models. One of their main goals is to predict how circuits using the next generation of devices should

work, to identify which direction the technology should take, and have models ready beforehand.

In the area of predictive modeling, the most important models are the BSIM (Berkeley Short-channel IGFET Model) Group [31] and the Arizona State University (ASU) PTM [32] based on BSIM, which were developed for Planar CMOS technology nodes up to 7nm. BSIM was developed by empirically extracting model parameters from early stage silicon data while ASU PTM improved the methodology by taking into account significant physical correlations among model parameters. Both groups also developed PTM models for multi-gate transistors, mainly FinFETs, for sub-20nm technology nodes. Moreover, the Berkley group have also developed some SOI models.

All the predicted models are developed based on the scaling theory of planar CMOS and multi-gate devices, physical models and the International Technology Roadmap for Semiconductors (ITRS) projections [33], which recollects data of the industry and makes projections about the future technologies.

We use the ASU PTM models for Planar and FinFET technologies since they include the model cards of the most recent technology nodes, which can be directly used to simulate in SPICE. For SOI technology, we tried the Berkley model (BSIM-SOI) but as the model cards are not included the results were not accurate. Then, we found an alternative model, the UTSOI model from the *Laboratoire d'électronique des technologies de l'information* (CEA-Leti) [34], which has a model card of planar SOI with values for 20/22nm. In spite of having all these models, we could not find predictive models for SOI FinFET and III-V HEMT.

7.2. Circuit Design

In Table 7.1 there is the list of all the hardware components, technologies and technology nodes to be analyzed. The technologies in red are still not available as there are no public technology models for them, and efforts are being made to find

these models for future work. All the components have been modeled and analyzed with SPICE. For this purpose, we developed a description of the necessary circuits at transistor level and use the appropriate predictive technology model (PTM) of the technology node to be analyzed.

Technology (CMOS)	Technology Nodes
Bulk Planar (ASU PTM Models)	22nm and 16nm (Bulk Planar)
Bulk FinFET (ASU PTM Models)	20nm and 14nm (Bulk FinFET)
SOI Planar (UTSOI Model)	22nm (SOI Planar)
SOI FinFET (Future Work)	N/A
III-V HEMT (Future Work)	N/A

X

Circuits
SRAM Cells 6T/8T/10T
Flip Flop - D
Latch
Logic Gates (AND, OR, NOT…)

Table 7.1: Hardware elements and Technologies analyzed

SPICE (Simulation Program with Integrated Circuit Emphasis) is an electronic circuit simulator used in integrated circuits design to check the integrity of the circuit and predict its behavior. To simulate in SPICE, one needs to describe the base components with transistors, then the circuit netlist and finally select which type of simulation will be performed (e.g. transient, montecarlo) [35]. We use HSPICE, a commercial version of SPICE, to make transient simulations of the components listed to compute their Qcrit under different conditions. Annex A shows a simulation example code in HSPICE of a 6T SRAM Cell with its circuit description.

CMOS technology provides two types of transistors: an n-type transistor (NMOS) and a p-type transistor (PMOS). These are also defined in the circuit description and their symbols are shown in Figure 7.1. Further details can be found in [36].

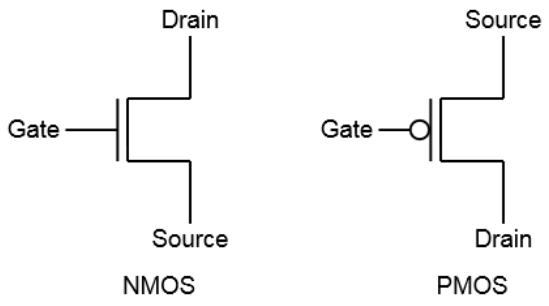


Figure 7.1: NMOS and PMOS Symbols

Transistors of each component need their size to be specified in the SPICE circuit description. Transistors sizing depends on the technology used. In the case of Planar CMOS, the sizing means to specify the length and the width of the transistor in lambdas or nanometers. Examples of most of the circuits can be found in the literature with the sizes in lambdas [36]. In a similar way, the transistors for FinFETs are sized in terms of number of fins which determines the effective width of a FinFET transistor [37].

7.2.1 SRAM Cells

SRAM is a type of memory widely used in current CPUs. For example, it is used in cache memories and register files of processors. SRAMs are made of arrays of cells, each one storing a bit of memory. There are different types of cells depending on the number of transistors used to make the cell, being 6T, 8T and 10T the most common ones. They are depicted in Figure 7.2, Figure 7.3 and Figure 7.4, respectively.

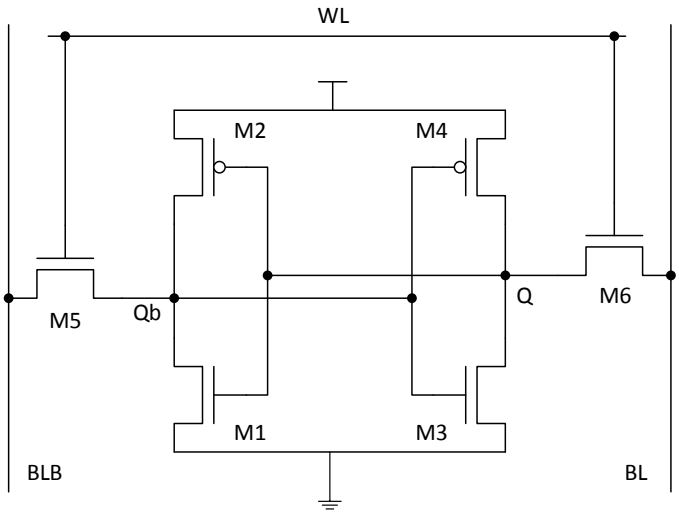


Figure 7.2: Scheme of a 6T Cell

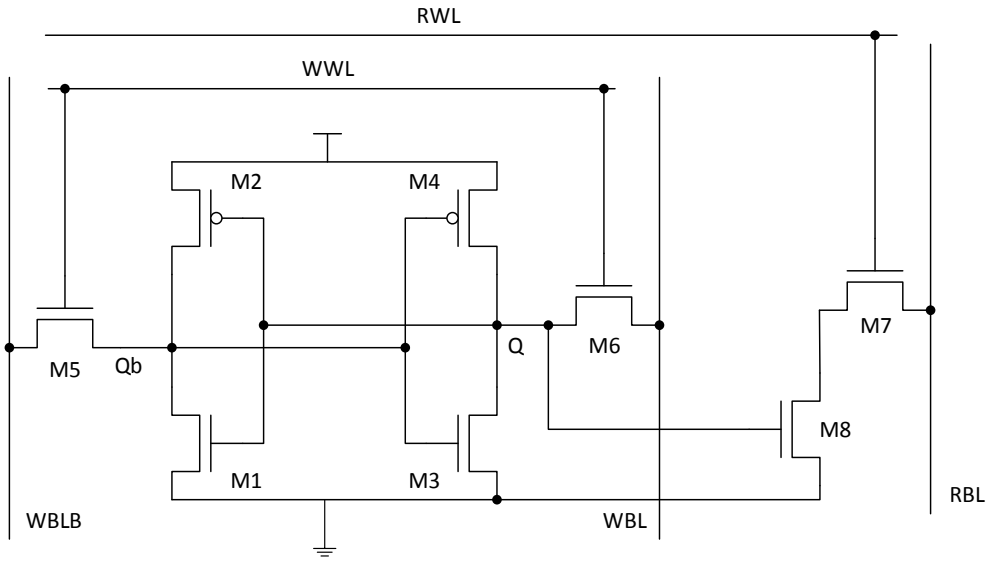


Figure 7.3: Scheme of an 8T Cell

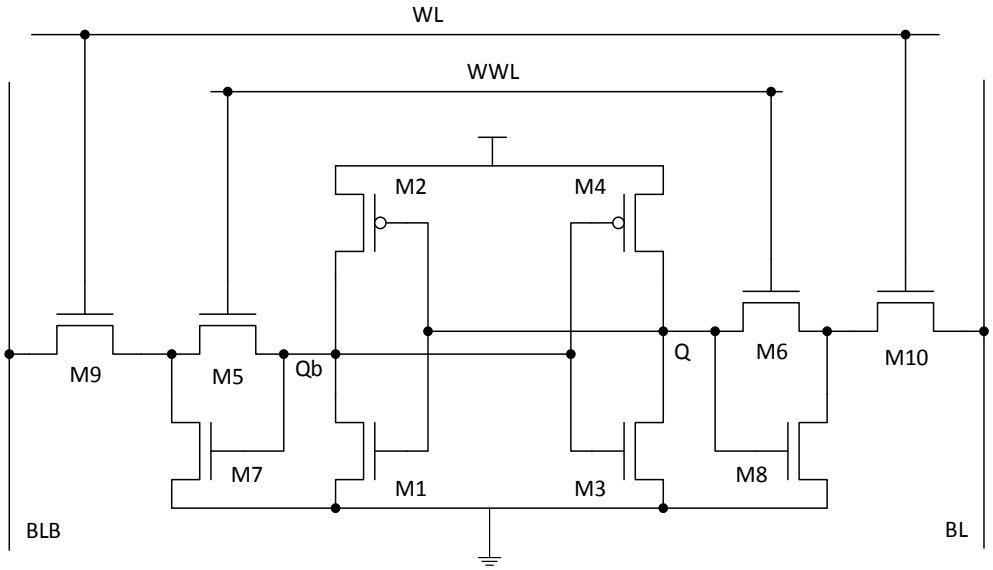


Figure 7.4: Scheme of a 10T Cell

Choosing the 6T cell as example, this cell has a pair of inverters (M1-M4) and two access transistors M5 and M6. This cell needs a careful transistor design as the strength (i.e. Width/Length ratio) of the transistors is crucial to write new values in the cell (Q and Qb) and, at the same time, perform read operations without losing the content. The nMOS transistors in the cross-coupled inverters must be the strongest. The access transistors are of intermediate strengths and the pMOS transistors must be weak. Therefore, for bulk and SOI planar, we have made the

nMOS transistors in the inverters (Width/Length) 8/2λ, access transistors 4/2λ and pMOS transistors 3/3λ, which are typical lambda values [36]. In the case of FinFETs, we use 2 fins for M1 and M3 and 1 for the rest of transistors, which are values obtained from the literature [38].

The 8T and 10T cells have as base the 6T cell, but in the case of the 8T, it adds more transistors to decouple the reading from the writing; and, in the case of the 10T, it adds more transistors to be more robust. Transistors of these cells are sized to conserve the same strength of the 6T cell.

7.2.2 Latch and Flip Flop

Latches are the most basic sequential logic elements. Their output values depend not only in the current inputs but also in the previous ones. Therefore, latches are used to store data like state information. Figure 7.5 shows the scheme of the latch used in our simulations being the Flip flop composed of two of this latches.

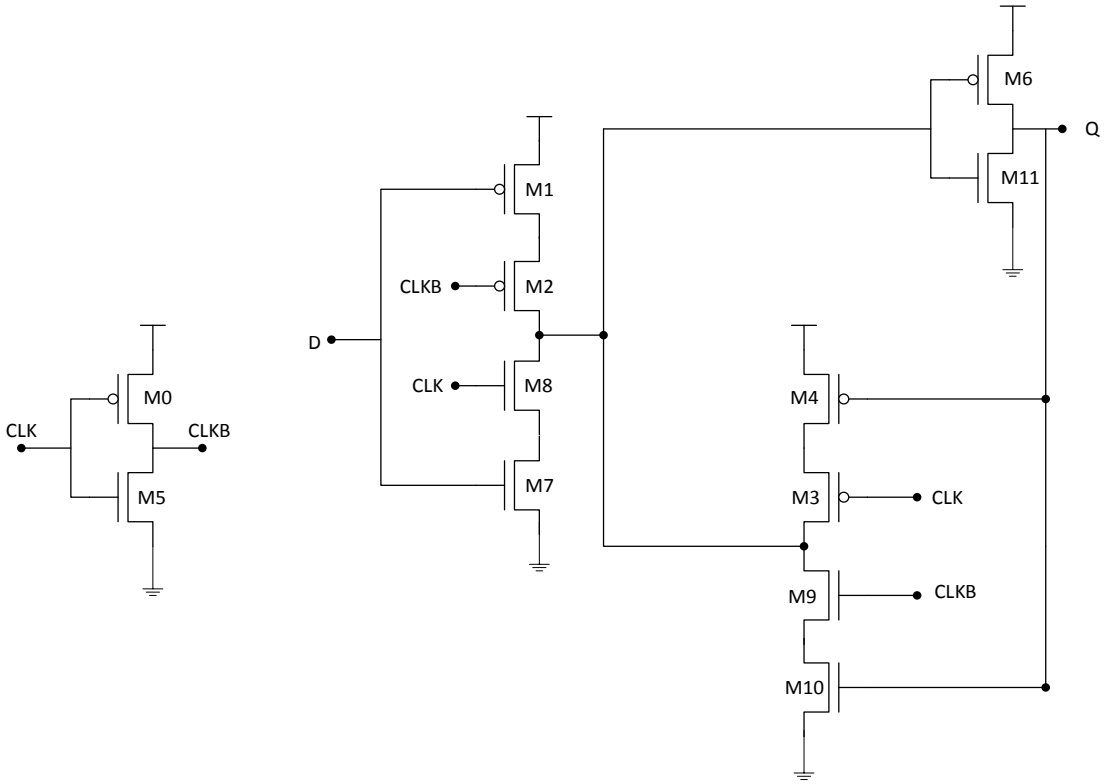


Figure 7.5: Scheme of a Latch

Latches and Flip flops are sized similarly to SRAM cells. For our latch, the first logic structure is a combination of a latch and an inverter that forms a tristate buffer. To be able to transfer new data into this latch, the first tristate buffer must be stronger as compared to the feedback inverter and the second tristate buffer [39]. Therefore, we start from minimum sizes (2/2λ or 1 fin) and then increase following this principle for each technology.

7.2.3 Logic Gates

Logic gates are the basis of any electronic device being the most common the NAND, NOR and NOT, which are depicted in Figure 7.6 with four inputs. Further details on how to implement other common gates and functions can be found in [36].

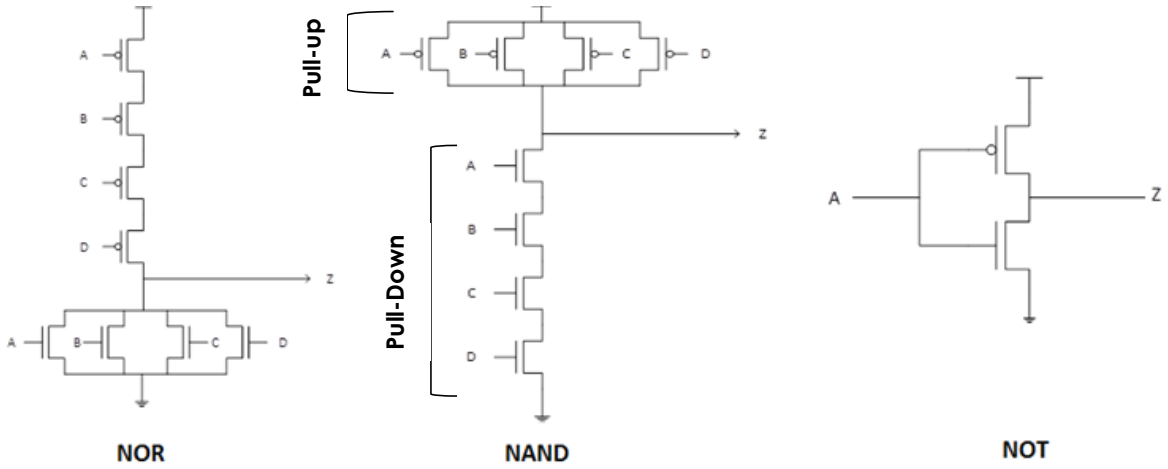


Figure 7.6: NAND, NOR and NOT Schemes

Logic gates are sized to have minimum size but being symmetric so that the delays to commute from 0 to 1 and back are equal or at least similar. This symmetry is achieved by matching the strength (Rs=Width/Length) of the pull down and pull up to 1 Rs. In the case of bulk planar, the PMOS transistors from the pull up have a lower strength (2x-3x) than the NMOS transistors from the pull down. Therefore, to make the gate symmetric, the PMOS transistors are sized with a higher width to increase their strength. PMOS and NMOS transistors of FinFET and SOI technologies have a similar strength relation, which has been tested with SPICE.

8. Analysis of Basic Components

As has been already described, to obtain the Soft Error Rate (SER) of a component, the critical charge (Qcrit) is required. Qcrit is obtained doing simulations with HSPICE by inserting a current pulse in the sensitive nodes of the component, where the current pulse represents the charge produced by the impact of a neutron strike. This chapter describes how the SER has been computed for each component and it summarizes some of the results obtained.

8.1. Analysis of SRAM Cells

To obtain the Qcrit of the SRAM cell, current pulses are inserted in the storage node Q since the other node (Qb) is symmetric. The values of Qcrit obtained for the 6T SRAM cell have been summarized in Table 8.1, showing the maximum, the minimum and the average Qcrit from all the environmental parameters (i.e. voltage, temperature, stored value and pulse time). The latest technology nodes have usually lower critical charge than their predecessors. However, recent technologies, such as FinFETs and SOI improve this aspect and have a higher Qcrit.

6T SRAM Cell			
Technology	**Minimum Qcrit (fC)**	**Maximum Qcrit (fC)**	**Average Qcrit (fC)**
22nm Bulk Planar	0,07	35,89	5,79
22nm SOI Planar	0,53	43,97	9,70
20nm Bulk FinFET	1,94	120,10	21,00
16nm Bulk Planar	0,03	22,79	3,64
14nm Bulk FinFET	2,74	104,00	30,09

Table 8.1: Qcrit values of a 6T SRAM Cell

A Soft Error Rate (SER) is computed from each Qcrit. Then, as the total SER of the element is the sum of the SER from all sensitive nodes, in the case of SRAM cells, SERs from the same environment (voltage, temperature and pulse) but different stored values (0 and 1) are added. That is because the cell has two sensitive nodes and each one always will store the inverse of the other node. Moreover, we could

also weight SER values depending on the state of the cell (i.e. holding, reading and writing), but as most of the time cells are holding a value, only the holding mode is considered. Table 8.2 shows the total SER of the 6T and 8T cells build with different technologies, and simulated with typical environmental parameters (1V, 50ºC) and the pulse of 2ps which is the worst case.

SRAM Cells with Typical Conditions		
Technology	**6T Total SER (FIT)**	**8T Total SER (FIT)**
22nm Bulk Planar	2,04E-05	1,99E-05
22nm SOI Planar	1,17E-06	1,17E-06
20nm Bulk FinFET	2,04E-07	1,85E-07
16nm Bulk Planar	1,09E-05	1,07E-05
14nm Bulk FinFET	5,59E-09	3,57E-09

Table 8.2: 6T and 8T SERs

Both cells have similar SER values, and similar values are obtained with the 10T cell, as the core of all the cells is the 6T and they all have the same sensitive nodes. The highest SERs are with bulk planar and the lowest with bulk FinFET, which corresponds with the highest and lowest Qcrit values. In the case of bulk planar, the 16nm node has lower SERs than the 22nm node. That is because the reduction in the area has more effect when the Qcrit values are already very low, overcoming the reduction of Qcrit.

8.2. Analysis of a Latch

The methodology used to compute the Qcrit of the latch is similar to the methodology used for SRAM cells. A current pulse is injected in the sensitive nodes of the latch, which in our design are the intermediate node and the output node. The latch can be in two modes, transparent which is when the latch transfers the input value to the output or holding the value, being 50% of the time each one. Only the hold mode is considered on the following results since in transparent mode the flipped value is usually rewritten and can be only propagated if the flip happens in a very specific moment (setup time). Table 8.3 shows the Qcrit values obtained for the latch,

showing the maximum, the minimum and the average Qcrit for all the combinations of parameters. Results are similar to those of SRAM cells, being FinFET and SOI technologies more robust by having a higher Qcrit.

Latch			
Technology	**Minimum Qcrit (fC)**	**Maximum Qcrit (fC)**	**Average Qcrit (fC)**
22nm Bulk Planar	0,54	16,79	4,27
22nm SOI Planar	0,39	63,39	4,26
20nm Bulk FinFET	1,90	39,05	12,49
16nm Bulk Planar	0,36	8,19	2,40
14nm Bulk FinFET	2,71	117,40	21,88

Table 8.3: Latch Qcrit values

Similarly to SRAM cells, SERs from both sensitive nodes are added for each environmental setup (i.e. Temp, V…). Then, SERs of different inputs (0 and 1) are weighted considering equal probabilities. Finally, since we are only considering the holding mode, we are assuming that 50% of the time the latch is not sensitive to particle strikes, so we apply a 0.5x derating factor to the SERs. Table 8.4 shows the total SERs of a latch build with different technologies, and simulated with typical environmental parameters (1V, 50^{o}C) and the pulse of 2ps which is the worst case.

Latch	
Technology	**Total SER (FIT)**
22nm Bulk Planar	5,97E-06
22nm SOI Planar	4,59E-07
20nm Bulk FinFET	1,02E-07
16nm Bulk Planar	2,58E-06
14nm Bulk FinFET	2,49E-09

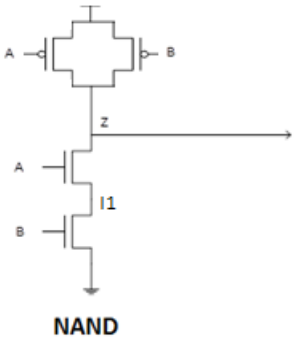
Table 8.4: Latch SERs

The critical charges of the latch are similar to ones of the SRAM cells. However, since the SERs of the latch are derated by a time vulnerability factor of 50%, the final results are lower. The technology comparison is still the same, being SOI and

FinFET more robust to soft errors. Flip flop results are similar since it is composed of two latches being each one vulnerable 50% of the time.

8.3. Analysis of Logic Gates

Logic gate SER analysis is done by injecting the current pulses in the internal nodes that are sensitive to neutron strikes, which depends on the inputs and gate type. Understating that a particle strike activates an off transistor, we can analyze which nodes are sensitive to particle strikes and inject the current pulse in these nodes. Choosing a NAND of 2 inputs as example, we obtained Figure 8.1, which shows which nodes are sensitive for each combination of inputs. This analysis is done for each gate to simulate the strikes only in the sensitive nodes.



NAND

NAND2 Sensitivity to Stikes			
Input Value (AB)	**Output Value (Z)**	**Z Node**	**I1 Node**
00	1	No	No
01	1	Yes	No
10	1	No	Yes
11	0	Yes	No

Figure 8.1: NAND2 Sensitivity Analysis

Qcrit values for the NAND2 are shown in Table 8.5.

NAND2			
Technology	**Minimum Qcrit (fC)**	**Maximum Qcrit (fC)**	**Average Qcrit (fC)**
22nm Bulk Planar	0,73	63,39	15,78
22nm SOI Planar	0,68	153,00	21,65
20nm Bulk FinFET	3,33	214,40	50,07
16nm Bulk Planar	0,59	87,05	16,35
14nm Bulk FinFET	4,51	314,80	75,42

Table 8.5: NAND2 Qcrit values

A SER is computed for each input combination by adding the SERs of all the sensitive nodes. Then, the SERs of each input combination are weighted by the probability of the input to occur, but for now, equal probabilities are considered. SER results for the NAND2 are shown in Table 8.6.

NAND2	
Technology	**Total SER (FIT)**
22nm Bulk Planar	1,78E-06
22nm SOI Planar	5,33E-08
20nm Bulk FinFET	1,35E-09
16nm Bulk Planar	7,75E-07
14nm Bulk FinFET	2,02E-12

Table 8.6: NAND2 SERs

SER values of logic gates are even lower than SRAM cells and latches. That is because analyzing each combination of inputs, a gate usually has one or even none sensitive nodes to strikes. In contrast, the SRAM cells and the latch always have two sensitive nodes. Therefore, when the average is done the total SER of the gate is reduced and lower than in other components.

9. Trends in Soft Error Rates

In previous chapter we have analyzed some of the components giving some clues on which technologies are more robust to radiation. This chapter provides more data and plots to show different trends. In section 9.1, there is a global comparison between the technologies and components described. Sections 9.2 and 9.3 show the impact of increasing the voltage and the temperature, respectively. Section 9.4 compares the SERs of a logic gate using different fanouts. Finally, section 9.5 shows SERs in different locations and the impact of the neutron flux.

9.1. Technology Trend

Gathering the results of the previous chapter we can compare the SERs of different components and technologies. These results are plotted in Figure 9.1, where each color represents a technology and each group of bars a component.

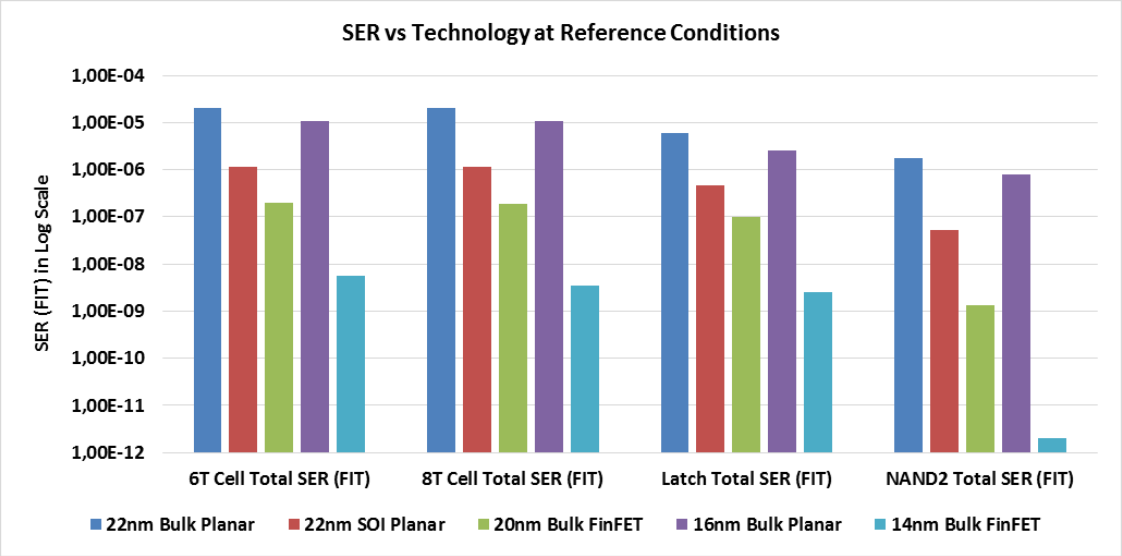


Figure 9.1: Technology Comparison

SERs are in logarithmic scale and looking at the bars of a component, such as the 6T cell, the higher SERs are from bulk planar and the lower are from bulk FinFET with SOI planar in the middle. Therefore, the most vulnerable technology is the bulk

planar while bulk FinFET and SOI planar can reduce SERs up to 100x, which makes sense since the sensitive area and the collected charge are bigger in bulk planar.

Between components, both memory cells have similar results, the latch is a bit more reliable as it is vulnerable 50% of the time and the NAND2 has the lower SERs. Typical logic gates (NAND, NOR and NOT) usually have less sensitive nodes to strikes for each input combination, resulting in a total SER lower than in other components.

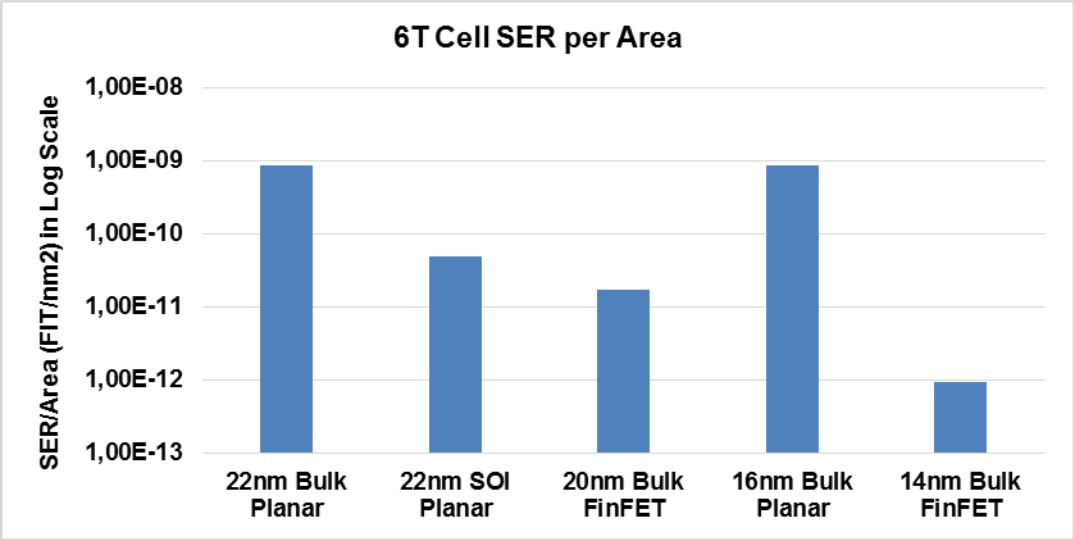


Figure 9.2: SER/Area of a 6T SRAM Cell

In addition, in bulk technology, lower nodes have lower SERs which may seem contradictory as in lower nodes Qcrit is usually reduced. However, the reduction in area has a stronger effect when the critical charge is already very low. Therefore, if we look at the SER/Area in Figure 9.2, both nodes of bulk planar are quite similar, being slightly higher the node of 16nm. Thus, if we put more elements the total SER of a 16nm chip will increase. As an example, if we consider an SRAM chip with constant die area of 1.5 cm^2, the approximately SER of the 16nm chip would be 129544 FIT and 127671 FIT for the 22nm chip. In the case of FinFETs, our results show that the critical charge of the 14nm node is lower than the one with 20nm. Therefore, adding the lower critical charge, the reduction in the sensitive area and the reduction in the collection efficiency, results in much lower SER values.

9.2. Voltage Trend

Table 9.1 compares the soft error rates of a 6T SRAM cell though increasing voltages and different technologies.

Technology	6T SRAM Cell Total SER (FIT)					
	(0,7V|50C)	(0,8V|50C)	(0,9V|50C)	(1V|50C)	(1,1V|50C)	(1,2V|50C)
22nm Bulk Planar	2,50E-05	2,33E-05	2,18E-05	2,04E-05	1,91E-05	1,79E-05
22nm SOI Planar	3,95E-06	2,74E-06	1,88E-06	1,17E-06	8,76E-07	6,12E-07
20nm Bulk FinFET	6,92E-07	4,65E-07	3,13E-07	2,04E-07	1,44E-07	9,91E-08
16nm Bulk Planar	1,33E-05	1,24E-05	1,17E-05	1,09E-05	1,03E-05	9,64E-06
14nm Bulk FinFET	9,70E-08	3,97E-08	1,48E-08	5,59E-09	2,18E-09	1,36E-09

Table 9.1: Voltage comparison

Figure 9.3 shows the plot of these results in logarithmic scale where lower values are better. SERs increase with lower voltages since the critical charge becomes smaller. Therefore, it is easier to flip the value and the variation may be as high as 70x as can be seen with the red lines of the plot.

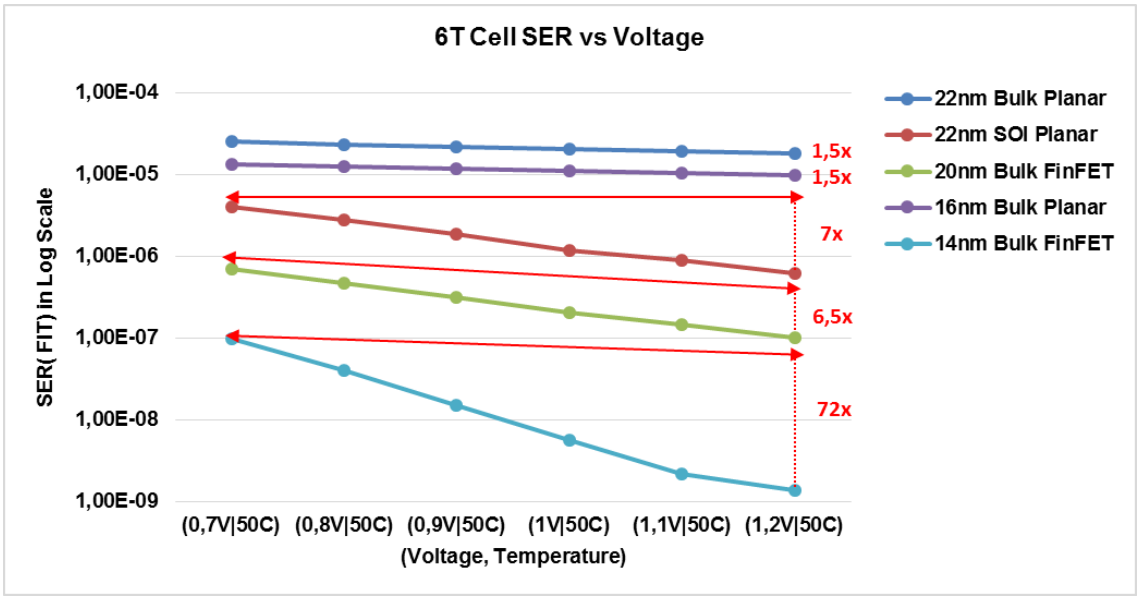


Figure 9.3: Voltage Comparison Plot

9.3. Temperature Trend

Table 9.2 compares the soft error rates of a 6T SRAM cell though increasing temperatures and different technologies.

Technology	6T SRAM Cell Total SER (FIT)			
	(1V|25C)	(1V|50C)	(1V|75C)	(1V|100C)
22nm Bulk Planar	1,88E-05	2,04E-05	2,17E-05	2,27E-05
22nm SOI Planar	1,18E-06	1,17E-06	1,38E-06	1,47E-06
20nm Bulk FinFET	2,09E-07	2,04E-07	2,17E-07	2,20E-07
16nm Bulk Planar	9,97E-06	1,09E-05	1,17E-05	1,23E-05
14nm Bulk FinFET	5,04E-09	5,59E-09	6,79E-09	5,56E-09

Table 9.2: Temperature Comparison

Figure 9.4 shows the plot of these results in logarithmic scale where lower values are better. SER increases with higher temperatures since the critical charge becomes smaller. Even if seems that the variation is low it can be greater than 20% as can be seen with the red lines of the plot, but still has a low effect compared with the voltage variation. In the case of FinFET technology, the models used don't model the temperature accurately [40] so the variations are very low and slightly oscillating.

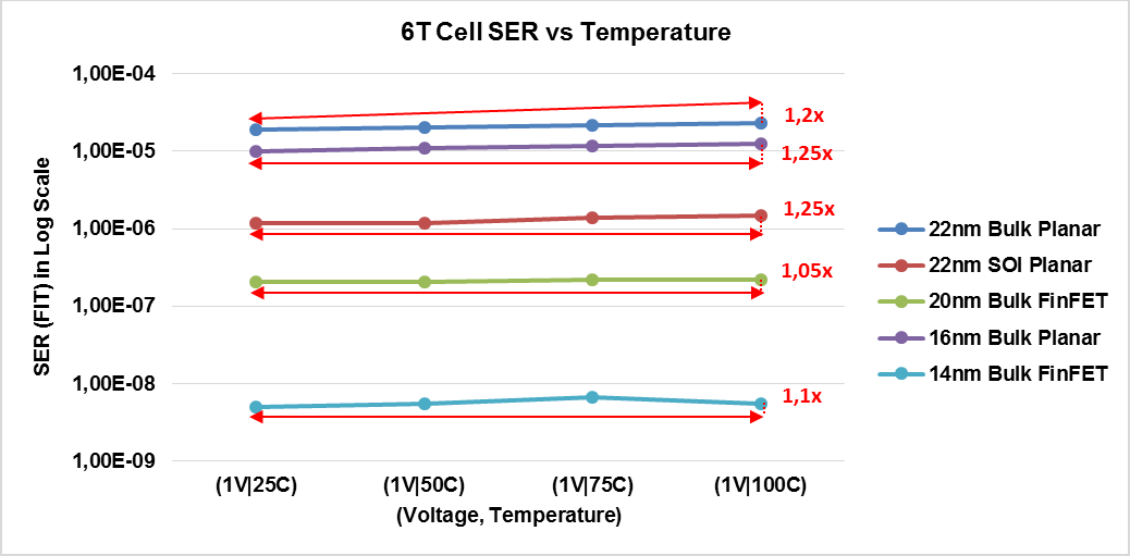


Figure 9.4: Temperature Comparison Plot

9.4. Fanout Trend

Table 9.3 compares the soft error rates of the logic gate NOT build in 22nm bulk planar technology with different fanouts.

NOT (22nm Bulk Planar)	
Fanout	**Total SER (FIT)**
1	2,55E-06
2	2,46E-06
3	2,40E-06
4	2,34E-06
5	2,29E-06
6	2,24E-06
7	2,19E-06
8	2,13E-06
9	2,09E-06
10	2,05E-06

Table 9.3: Fanout and Current Pulse Comparison

In Figure 9.5 SERs are slightly reduced with higher fanouts as there is more capacity in the output and the critical charge increases, with a variation that can be up to 1.5x.

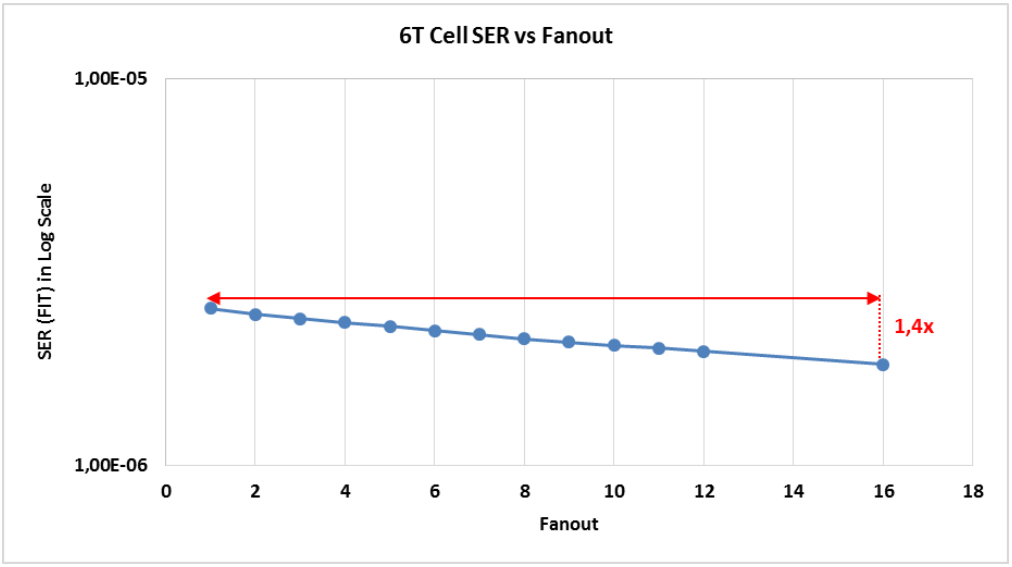


Figure 9.5: Fanouts Comparison Plot

9.5. Location Trend

Table 9.4 shows neutron fluxes of different European locations relatives to the reference flux from New York City at sea level.

Reference Flux = 0,00565 neutrons/cm2*s (NYC, SL)				**Note:** Flux At Medium Solar Modulation					
				Neutron Flux Relative to the Reference Flux					
Location	**Coordinates (Grades)**	**Vertical Cutoff (GV)**	**Mean Altitude (m)**	**Sea Level**	**Base Altitude**	**2000m**	**4000m**	**8000m**	**12000m**
Turin	45N, 7E	5	239	0,87	1,07	4,29	15,56	98,62	296,19
Barcelona	41N, 2E	6	12	0,8	0,81	3,78	13,25	79,41	228,2
Athens	37N, 23E	8	170	0,72	0,83	3,27	11,06	62,78	172,64
Västerås (Sweden)	59N, 16E	1	17	1,01	1,03	5,38	21,06	153,56	527,47
Berlin	52N, 13E	2	34	0,97	1	5,01	19,07	131,78	428,58
London	51N, 0W	3	24	0,97	0,99	4,99	18,96	130,7	424,01
Moscow	55N, 37E	2	150	0,99	1,13	5,18	19,96	141,23	469,94

Table 9.4: Relative Fluxes of different locations

Figure 9.6 shows the relative fluxes plotted. The higher neutron fluxes are located in Västerås as is closest to the pole while the lower is in Athens which is near the equator. These relative fluxes have been computed using the online calculator [18], which uses the JEDEC standard, with a medium solar activity (50%).

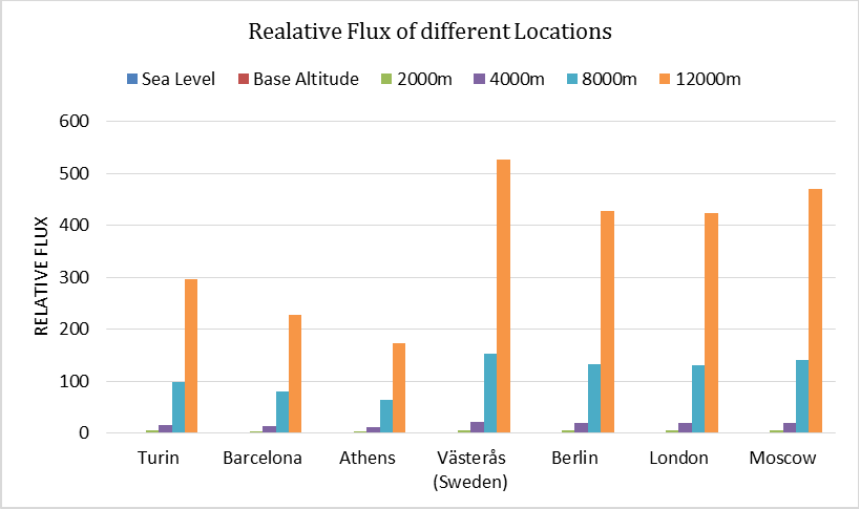


Figure 9.6: Relative Neutron Fluxes

The relative fluxes can be multiplied directly by the Soft Error Rates (SER) obtained with the reference flux to obtain the SER of the desired location. We have computed the SERs of a 6T SRAM cell at different locations and altitudes as is shown in Figure 9.7.

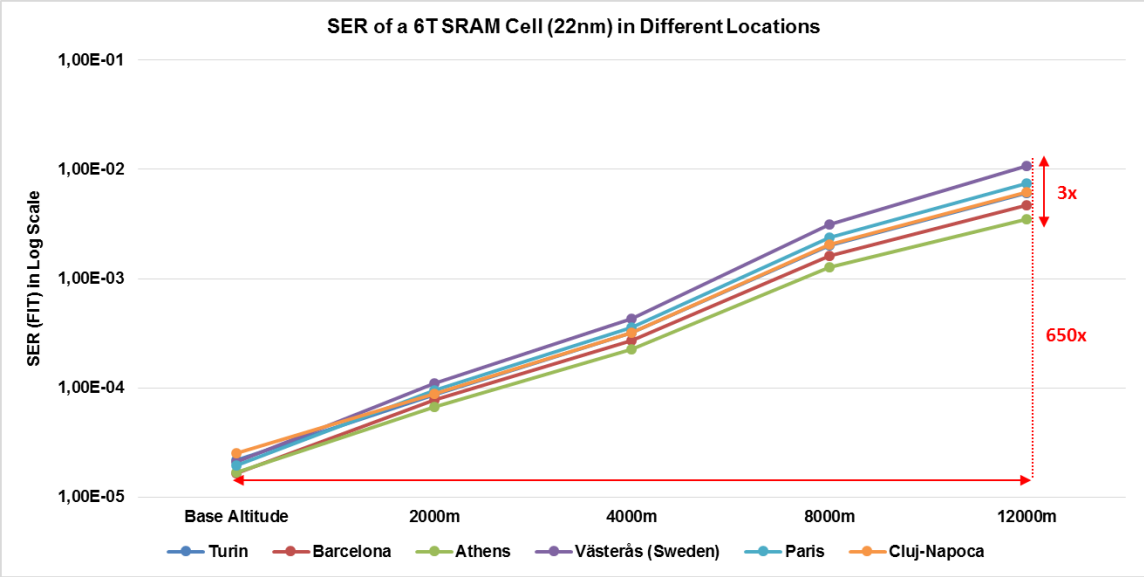


Figure 9.7: SERs depending on the Location and Altitude

The difference between cities is due the influence of the magnetic field of the earth, where cities near the equator have lower SERs. Moreover, there is an exponential increase of the SER when varying the altitude that can be as high as 650x.

9.6. Discussion

In chapter 9 we have reviewed the major trends in soft error rates. Voltage and location are the operating conditions that have been proved to have an important impact in the reliability of a chip. Nowadays, the power consumption is the main focus of attention and consequently the voltage is reduced for lower power consumption. However, reliability is becoming an important parameter so it should be taken into account when deciding the voltage used in a processor. There is already a tradeoff between the power consumption and the performance, but the reliability should also be included. Location has the greatest impact in SERs,

especially when varying the altitude. Therefore, it is important to take location into account when developing electronic devices for airplanes.

Finally, the most important trend has been seen in the technology comparison. According to the results, bulk FinFET is the most robust technology from the ones analyzed. Moreover, lower technology nodes of FinFET are even more robust to radiation induced failures. SOI planar also shows good results, and maybe the combination of both, SOI FinFET, could be the best option for reducing SERs in the future.

10. Future Work

This chapter describes the work that is planned to do in a near future. Our main objective is to characterize soft errors of the most promising technologies. However, as have been already commented, we are still missing technology models for III-V HEMT and SOI FinFET. Therefore, our main priority is to find models for these technologies, in order to be able to simulate them and do the corresponding analysis.

Section 5.5 describes the effects that may mask some of the soft errors. The time vulnerability factor is already being considered in the analysis of the latch and flip flop. Moreover, we plan to add the electrical derating and the latch window masking to our study of the logic gates, since they can be computed at the technology layer. We are still discussing how to add these effects, but we already have some intuitions on this. The latch window masking could be computed by measuring the delays of the gates to know if the glitch will arrive to the latch. On the other hand, the electrical derating could be measured by computing the difference between output pulses in a chain of logic gates.

Finally, we are also studding an effect called Multi Cell Upset (MBU). MBU consists in flipping the stored value of multiple SRAM cells from one single strike. MBU effect occurs when the charge cloud produced from one strike in a cell is large enough to affect the cells that are near. MBU becomes worst when technology shrinks since elements are closer. Therefore, we are studding MBU to give the probabilities of this effect to occur in function of the distance between cells. Moreover, we want to analyze if MBU affects also logic gates.

11. Conclusions

The work has been focused on the characterization of soft errors due neutron strikes, which have been the major reliability concern of the industry in the last years and are also expected to be in the near future. In this master thesis, technologies being used or expected to be used in the near future have been reviewed. In addition, different possible source of failures that may be critical for these technologies have been described.

Looking at the results, it is obvious that as bulk planar technology scales down Qcrit is lower so the elements may become more vulnerable to soft errors. However, the scaled area and collection efficiency overcomes the reduction of Qcrit making the SER almost constant or even a bit lower. Nevertheless, taking into account the increase in the number of elements integrated in a chip when the technology scales down, the SER increases and becomes an important issue for the reliability of the device.

On the other hand, newer technologies, such as multi-gate FinFETs, and newer materials, such as SOI, are more resistant to radiation effects. In addition, we have showed that environmental parameters, such as temperature and voltage, and the location, may have a huge impact on the soft error rates. Specially the altitude, which may increase the SERs up to 650x. In conclusion, this study suggests that newer technologies can reduce soft error rates up to 100x whereas planar CMOS is becoming more vulnerable due to the scaling down of its components and the increased number of elements.

12. Bibliography

[1] S. Borkar, et al., "Design and Reliability Challenges in Nanometer Technologies", IEEE DAC, pp. 75-75, 2004

[2] R. Baumann, "Soft Errors in Advanced Computer Systems", IEEE Design & Test of Computers, vol. 22, no. 3, pp. 258-266, May/June, 2005

[3] D. J. Sorin, "Fault Tolerant Computer Architecture", Morgan & Claypool Publishers, 2009

[4] S. Mukherjee. "Architecture Design for Soft Errors", Morgan Kaufmann, 2008

[5] M. H. Abu-Rahma, M. Anis. "Variability in Nanometer Technologies and Impact on SRAM", Springer New York, 2013

[6] Shrikanth, "Reliability In The Face of Variability in Nanometer Embedded Memories", UPC Thesis, March, 2014

[7] P. Hazucha and C. Svensson, "Impact of CMOS Technology Scaling on the Atmospheric Neutron Soft Error Rate", IEEE Transactions on Nuclear Science, Vol. 47, No. 6, pp.2586-2594, December 2000

[8] T. Heijmen, D. Giot and P. Roche, "Factors that impact the critical charge of memory elements", IEEE International On-Line Testing Symposium, 2006

[9] R. Naseer, S. DasGupta. "Critical Charge Characterization for Soft Error Rate Modeling in 90nm SRAM", IEEE, 2007

[10] S. Bota, G. Torrens, et al., "Critical Charge Characterization in 6-T SRAMs During Read Mode", IEEE, 2009

[11] J. F. Ziegler and W. A. Lanford, "Effect of cosmic rays on computer memories", Science, Volume 206, Issue 4420, pp. 776-788, 1979

[12] A. Taber and E. Normand, "Single Event Upset in Avionics", IEEE Transactions on Nuclear Science, Vol. 40, No. 2, April 1993

[13] P. C. Murley and G. R. Srinivasan, "Soft-error Monte Carlo modeling program, SEMM", IBM, 1996

[14] P. Shivakumar and M. Kistler, "Modeling the Effect of Technology Trends on the Soft Error Rate of Combinational Logic", International Conference on Dependable Systems and Networks, 2002

[15] P. Hazucha, C. Svensson, and S. A. Wender, "Cosmic ray soft error rate characterization of a standard 0.6 µm CMOS process," IEEE J. Solid-State Circuits, Oct. 2000

[16] J. F. Ziegler, "Terrestrial cosmic rays", IBM journal of research and development, 1996

[17] JEDEC Standard, "Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices", JESD89A, 2006

[18] Neutron Flux Calculator (SEUTEST), http://www.seutest.com/cgi-bin/FluxCalculator.cgi

[19] M. S. Gordon, P. Goldhagen, et al., "Measurement of the Flux and Energy Spectrum of Cosmic-Ray Induced Neutrons on the Ground", IEEE Transactions on Nuclear Science, Vol. 51, No. 6, December 2004

[20] P. Goldhagen, et al., "Measurement of the energy spectrum of cosmic-ray induced neutrons aboard an ER-2 high-altitude airplane", Nuclear Instruments and Methods in Physics Research, 2002

[21] Synopsys HSPICE, https://www.synopsys.com/tools/Verification/AMSVerification/CircuitSimulation/HSPICE/Pages/default.aspx

[22] E. H. Cannon, et al., "SRAM SER IN 90,130 AND 180 NM BULK AND SOI TECHNOLOGIES", IEEE, 2004

[23] D.R. Ball, et al., "Comparing Single Event Upset Sensitivity of Bulk vs. SOI Based FinFET SRAM Cells using TCAD Simulations", IEEE, 2010

[24] Yi-Pin Fang and Anthony S. Oates, "Neutron-Induced Charge Collection Simulation of Bulk FinFET SRAMs Compared With Conventional Planar SRAMs", IEEE Transactions On Device And Materials Reliability, 2011

[25] Tino Heijmen, "Analytical semi-empirical model for SER sensitivity estimation of deep-submicron CMOS circuits", IEEE International On-Line Testing Symposium, 2005

[26] K. Bernstein, N. J. Rohrer, "SOI Circuit Design Concepts", IBM Microelectronics, Springer, 2007

[27] S. Oktyabrsky, P. D. Ye, "Fundamentals of III-V Semiconductor MOSFETs", Springer, 2010

[28] Y. Cao, "Predictive Technology Model for Robust Nanoelectronic Design", Integrated Circuits and Systems, Springer, 2011

[29] D. Lu, "PhD Dissertation: Compact Models for Future Generation CMOS", Electrical Engineering and Computer Sciences University of California at Berkeley, 2011

[30] Compact Model Council (CMC), https://www.si2.org/cmc_index.php

[31] BSIM, http://www-device.eecs.berkeley.edu/bsim/

[32] Arizona State University (ASU) PTM, http://ptm.asu.edu/

[33] International Technology Roadmap for Semiconductors (ITRS) projections, http://www.itrs.net/

[34] Leti UTSOI Model, http://www-leti.cea.fr/en/How-to-collaborate/Focus-on-Technologies/UTSOI

[35] SPICE Simulation Fundamentals, National Instruments, http://www.ni.com/white-paper/5413/en/#toc4

[36] Neil H. E. Weste, David Money Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", Addison Wesley Publication, 2010

[37] P. Mishra, A. Muttreja, N. K. Jha, "FinFET Circuit Design", Springer Science, 2011

[38] Z. Jaksic and R. Canal, "Enhancing 6T SRAM Cell Stability by Back Gate Biasing Techniques for 10nm SOI FinFETs under Process and Environmental Variations", 19th International Conference "Mixed Design of Integrated Circuits and Systems", May 24-26, 2012

[39] S. A. Tawfik, V. Kursun, "Characterization of New Static Independent-Gate-Biased FinFET Latches and Flip-Flops under Process Variations", 9th International Symposium on Quality Electronic Design, IEEE, 2008

[40] S. Sinha, G. Yeric, et. al., "Exploring Sub-20nm FinFET Design with Predictive Technology Models", ACM, 2012

[41] S. Lin, Y. Kim and F. Lombardi, "Soft-Error Hardening Designs of Nanoscale CMOS Latches", VLSI Test Symposium, 2009

[42] T. Heijmen, P. Roche, et. al., "A Comprehensive Study on the Soft-Error Rate of Flip-Flops From 90-nm Production Libraries", IEEE Transactions On Device and Materials Reliability, 2007

[43] E. Ibe, et. al., "Impact of Scaling on Neutron-Induced Soft Error in SRAMs From a 250 nm to a 22 nm Design Rule", IEEE Transactions On Electronic Devices, 2010

[44] F. Wang, et. al., "Dependability Analysis of Nano-scale FinFET circuits", IEEE Proceedings of the Emerging VLSI Technologies and Architectures, 2006

[45] H. Liu, et. al., "Technology Assessment of Si and III-V FinFETs and III-V Tunnel FETs from Soft Error Rate Perspective", IEEE, 2012

13. Acronyms

The following table shows a list of the most important acronyms used and their meaning:

Acronym	Definition
CMOS	Complementary Metallic Oxide Semiconductor
FinFET	Fin-Shaped Field Effect Transistor
SOI	Silicon On Insulator
RIF	Radiation Induced Faults
SEU	Single Event Upset
SER	Soft Error Rate
Qcrit	Critical charge
FIT	Failure In Time
MTTF	Mean Time to Failure
SDC	Silent Data Corruption
DUE	Detected Unrecoverable Error
TVF	Time Vulnerability Factor
PTM	Predictive Technology Model
ITRS	International Technology Roadmap for Semiconductors
MCU	Multi Cell Upset

Annex A. SPICE Example

```
* Import technology model
.INCLUDE PTM_PLN_22nm_HP.pm

* Parameters
.PARAM VDD=0.8V
.PARAM L1=22n
.PARAM L2=33n
.PARAM W1=88n
.PARAM W2=44n
.PARAM W3=33n
.PARAM N='6*11n'

* Current Pulse Parameters
.PARAM I1=0A I2=10.00uA TD1=5N TD2='5N+5*TAU1' TAU1=2P TAU2=200P

* 6T SRAM cell Design (Lambda=11nm, N=6 lambdas, Area=W*N, P=2*(W+N))
M1 qb q 0 0 nmos L=L1 W=W1 AD='W1*N' AS='W1*N' PD='2*(W1+N)' PS='2*(W1+N)'
M2 qb q 1 1 pmos L=L2 W=W3 AD='W3*N' AS='W3*N' PD='2*(W3+N)' PS='2*(W3+N)'

M3 q qb 0 0 nmos L=L1 W=W1 AD='W1*N' AS='W1*N' PD='2*(W1+N)' PS='2*(W1+N)'
M4 q qb 1 1 pmos L=L2 W=W3 AD='W3*N' AS='W3*N' PD='2*(W3+N)' PS='2*(W3+N)'

M5 blb wl qb 0 nmos L=L1 W=W2 AD='W2*N' AS='W2*N' PD='2*(W2+N)' PS='2*(W2+N)'
M6 bl wl q 0 nmos L=L1 W=W2 AD='W2*N' AS='W2*N' PD='2*(W2+N)' PS='2*(W2+N)'

* VDD to GND V
VCC 1 0 DC VDD

* Input waves
VWL wl 0 PWL(0ns 0)
.IC V(bl) = 0V
.IC V(blb) = 0V

* Current Pulse
ISER1TO0 q 0 EXP(I1 I2 TD1 TAU1 TD2 TAU2)

* Precharged Values: Initial Memory Stare
.IC V(q) = VDD
.IC V(qb) = 0V

* Loop to test the current that makes flip
.TRAN 1ps 16ns

* Measurements
.MEASURE TRAN MAXVAL MAX I(ISER1TO0) FROM=0ns TO=16ns
.MEASURE TRAN PulseTime TRIG AT=5ns TARG I(ISER1TO0) val=MAXVAL*0.8 td=5ns fall=1
.MEASURE TRAN FLIP WHEN V(q)=0.01V TD=4ns
.MEASURE TRAN Qcrit INTEG I(ISER1TO0) FROM=2ns TO='5ns+PulseTime'

.END
```