Diagnosis of Full Open Defects in Interconnect Lines with Fan-out

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***Abstract* — The development of accurate diagnosis methodologies is important to solve process problems and achieve fast yield improvement. As open defects are common in CMOS technologies, accurate diagnosis of open defects becomes a key factor. Widely used interconnect full open diagnosis procedures are based on the assumption that neighbouring lines determine the voltage of the defective line. However, this assumption decreases the diagnosis efficiency for opens in interconnect lines with fan-out, when the influence of transistor capacitances becomes important. This work presents a diagnosis methodology for interconnect full open defects where the impact of transistor parasitic capacitances is included. The methodology is able to properly diagnose interconnect opens with fan-out even in the presence of Byzantine behaviour. Diagnosis results for real defective devices from different technology nodes are presented.**

I. INTRODUCTION

FAILURES associated with open defects are common in CMOS technologies. Among open defects, interconnect opens have received significant research effort since they have become more frequent with technology shrinking due to the replacement of aluminum by copper in metal interconnections [1] together with the increasing number of vias/contacts [2]. In the presence of an interconnect full open defect, the affected line is disconnected from its driver, becoming electrically floating. The voltage of the floating line depends strongly on the circuitry surrounding the defective line, on the capacitances of the driven gates and on the initial trapped charge, as reported in previous works [3]-[11]. The logic response of the defective circuit due to an interconnect full open depends also on the logic input threshold voltages of the downstream gates for each particular test pattern. If the floating line voltage is higher than the logic input threshold of the downstream gate, it will be interpreted as logic one, otherwise as logic zero. In general, gates have different logic thresholds. Hence, if an intermediate voltage is generated in a floating line with fan-out, some of the downstream gates may interpret such voltage as logic 0 and other gates as logic 1. This behaviour is known as the Byzantine effect [12].

The diagnosis of interconnect open defects is important for solving process problems and for achieving fast yield improvement. Initial research in this field was based on logic information [13]-[14]. Subsequently, some works included layout information to improve diagnosis resolution [15]-[19]. Most of the existing diagnosis methodologies for interconnect opens relies on the assumption that the behaviour of the floating line is dominated by the neighbouring coupling capacitances. However, the effectiveness of these techniques decreases when the floating line is short or when the floating line has large fan-out. Research effort to overcome this problem considering physical information is found in [18]. Nevertheless, the Byzantine problem is not considered.

In this work, the impact of the downstream gates is included to improve the existing diagnosis techniques. The paper is organised as follows. Section II presents the floating line behaviour due to an interconnect full open defect. Section III focuses on the prediction of floating lines. In Section IV, the diagnosis methodology is proposed. Real cases proving the feasibility of the proposed methodology are presented in Section V. In the last Section, the conclusions of the work are presented.

II. INTERCONNECT OPEN DEFECT BEHAVIOUR

According to the charge conservation law, once the initial charge is trapped in an isolated line, the total charge does not change and is redistributed among the connected capacitors. Thereby, in the presence of an interconnect full open defect generating a floating line voltage V_{FN}, given a pattern (P) setting the rest of the circuit to a known state, the charge stored in the capacitors connected to neighboring structures ($Q_N(P,V_{FN})$) plus the charge stored in the parasitic capacitors of the transistors ($Q_{TR}(P,V_{FN})$) driven by the floating line must be equal to the constant trapped charged (Q_o) accumulated during the fabrication process, as indicated in eq (1).

$$Q_N(P,V_{FN}) + Q_{TR}(P,V_{FN}) = Q_o \quad (1)$$

Both $Q_N(P,V_{FN})$ and $Q_{TR}(P,V_{FN})$ are pattern (P) dependent and also depend on the floating node voltage (V_{FN}).

In general, drivers managing neighboring lines can be assumed electrically strong so that the corresponding parasitic capacitances are ideally tied to V_{DD} or *GND*. Therefore, $Q_N(P,V_{FN})$ can be expressed by the charge portion accumulated in the capacitors where the corresponding neighbors are tied to V_{DD} plus the portion accumulated in the capacitors where the neighbors are set to GND, as expressed in eq (2):

$$C_{up}(P)\cdot(V_{FN} - V_{DD}) + C_{down}(P)\cdot V_{FN} + Q_{TR}(P,V_{FN}) = Q_o \quad (2)$$

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where $C_{up}(P)$ and $C_{down}(P)$ are the parasitic capacitances from neighbors tied to V_{DD} and *GND*, respectively. Notice that these capacitances are pattern dependent, although their sum ($C_{up}(P) + C_{down}(P)$) remains constant. By isolating the voltage of the floating node from eq (2) yields eq (3):

$$V_{FN} = \frac{V_{DD}C_{up}(P) - Q_{TR}(P,V_{FN}) + Q_o}{C_{up}(P) + C_{down}(P)} \quad (3)$$

For long lines, the influence of $Q_{TR}(P,V_{FN})$ is small and can be neglected. For that reason, most diagnosis methodologies assumed that the floating line voltage is mainly determined by the ratio between the neighboring capacitances tied to V_{DD} and the total neighboring capacitances ($C_{up}(P)/(C_{up}(P)+C_{down}(P))$) plus the constant influence of the trapped charge. In case of fan-out, the influence of transistor capacitances ($Q_{TR}(P,V_{FN})$) may not be negligible and must be included in the prediction of the floating node voltage. However, $Q_{TR}(P,V_{FN})$ depends in turn on V_{FN}. An iterative procedure is required then to predict V_{FN} in a similar way as an electrical simulator does. However, this process is time consuming and the diagnosis procedure would be inefficient. Instead, we propose to focus the effort to compute $Q_{TR}(P,V_{FN})$ bounds, which in turn are used to predict V_{FN} bounds, instead of predicting the exact V_{FN} value. This proposal is shown in the next section.

III. Voltage Bound Prediction of the Floating Node

This section describes the prediction of the floating node behaviour based on voltage bounds. For ease of understanding, we consider first the case where the floating line drives a single gate. Subsequently, the methodology is generalized to the case with fan-out.

A. Single gate

Without loss of generality, consider a four input gate from a CMOS digital library where one of the inputs is floating due to an interconnect open defect. The gate transfer function related to the floating node voltage (V_{FN}) is illustrated in Figure 1a. Furthermore, it is known that the charge accumulated in the gate terminals of a CMOS gate pair of transistors due to transistor parasitic capacitances is an increasing function of the gate voltage. The charge stored in the transistor parasitic capacitances related to *FN* is depicted in Figure 1b for every combination of the three other inputs (*ABC*) of the gate. Every group of input combinations in Figure 1b showed equivalent results for the charge accumulated in the transistor parasitic capacitances. Notice how for every input combination the charge monotonically increases with V_{FN}.

A monotonic function is easily bounded in the working range. In fact, it is possible to limit the value of $Q_{TR}(P,V_{FN})$ according to the logic interpretation of V_{FN} made by the downstream gate. If the floating node voltage is interpreted as logic 0 (V_{FN0}) for a given pattern P_0, the maximum $Q_{TR}(P_0,V_{FN})$ value is obtained when V_{FN} is equal to V_{ILmax} (see Figure 1a and 1b). Symmetrically, if the floating node voltage is interpreted as logic 1 (V_{FN1}) for a given pattern P_1, the minimum $Q_{TR}(P_1,V_{FN})$ value is obtained when V_{FN} is equal to V_{IHmin} (see Figure 1a and 1b). To include such charge bounds to the prediction of the floating node voltage, the following inequalities are derived:

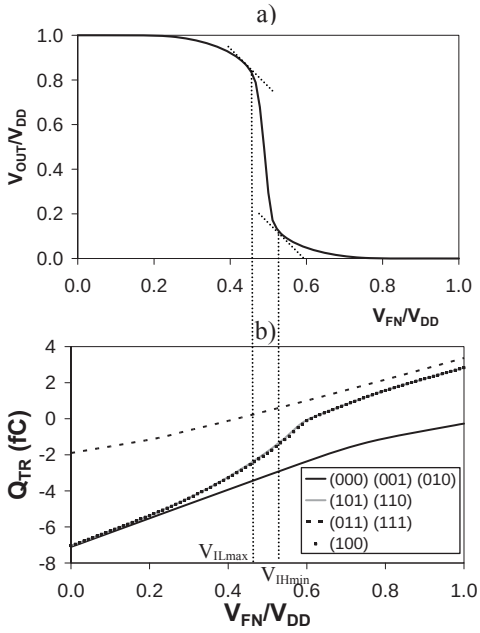

Figure 1: CMOS gate a) V_{OUT} vs V_{FN} b) Q_{TR} stored in the transistor pair driven by *FN* as a function of V_{FN} and the inputs combinations (ABC).

$$V_{FN0} > \frac{V_{DD}C_{up}(P_i) - Q_{TR}(P_i,V_{LTH}) + Q_o}{C_T} = B_0(P_i) \quad (4)$$

$$V_{FN1} < \frac{V_{DD}C_{up}(P_j) - Q_{TR}(P_j,V_{LTH}) + Q_o}{C_T} = B_1(P_j) \quad (5)$$

where $B_0(P_i)$ ($B_1(P_j)$) is a lower (upper) bound of V_{FN0} (V_{FN1}) when it has been interpreted as logic 0 (1). For every pattern exciting the defective line, a voltage bound is predicted, depending on the logic interpretation of V_{FN}. Thereby, for a pattern set PS, denoting as PS_0 (PS_1) the patterns setting the floating node to a voltage interpreted as logic 0 (1), the bound predictions are consistent with the observed behavior of the floating node as long as the maximum $B_0(P_i)$ value is lower than the minimum $B_1(P_j)$ value, hence:

$$\max_{P_0 \in PS_0} B_0(P_i) < \min_{P_1 \in PS_1} B_1(P_j) \quad (6)$$

Note that the result of the bound comparison is not modified by discarding the constant influence of the trapped charge.

B. Fan-out

In case of fan-out, the difference related to the single gate case lies in situations where the floating node is set to an intermediate voltage, which can be interpreted differently by the downstream gates. This may lead to inconsistencies when applying eq. (6). To avoid the non-desired implication of the Byzantine behavior, the voltage bounds reported in eq. (4) and (5) must be predicted separately for every downstream gate. To simplify the exposition, let us consider the case where the floating node is driving two gates. For a given pattern *P*, let us

assume that gate G_1 interprets V_{FN} as logic 0 whereas G_2 as logic 1. In this situation, for G_1 a lower bound ($B_0(P_0,G_1)$) is predicted while for G_2 an upper bound ($B_1(P_1,G_2)$) is predicted. In a general case, for every gate (G_m) driven by the floating node, the maximum value of max($B_0(P_0)$) must be lower than the minimum value of min($B_1(P_1)$).

$$\max_{P_0 \in PS_0} B_0(P_0, G_m) < \min_{P_1 \in PS_1} B_1(P_1, G_m) \quad (7)$$

The proposed method requires a dictionary of $Q_{TR}(P)$ vs. V_{FN} for every excitation of each gate of the technology.

IV. Diagnosis of Interconnec Full Open Defects

For an accurately diagnosis of interconnect opens, we consider any possible open location along the defective line using the full open segment (FOS) model [17]. This model divides the defective line into different segments according to the topology of the line itself and of the surrounding lines. An illustrative example is shown in Figure 2. The defective line has four neighbors and is driving an inverter. Labels *Mi* indicate the metal layer of the corresponding portion of the tracks. Segment breaks (*Seg_i*) are generated by a change in the layout of the neighborhood. The coupling capacitance per unit length is constant within a segment. Hence, each segment consists of the target line and zero to two neighboring lines. In the example, nine segments have been obtained.

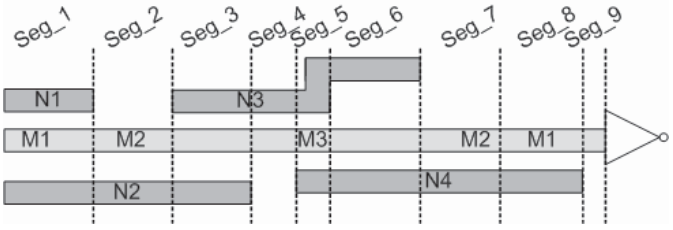

Figure 2: Example of segment division based on the FOS model [17].

With the previous segment division proposal, every segment has at the most two coupling capacitances, every of which tied either to V_{DD} or to ground, depending on the neighboring line state. Assuming that the open is located at the end of segment *k*, the terms included in the bound predictions consist of the contribution of the next segments after the open. This contribution is a constant figure determined by $C_{up}(P)$ and $C_{down}(P)$ for a given pattern (P). Since it is a linear dependence, it is sufficient to calculate the values at the beginning and at the end of the segment and perform an interpolation for the rest of positions. Hence, we determine the contribution of the neighboring lines assuming an open at the end of segment k, for a given test pattern (P), and include it on the prediction of the voltage bounds as follows:

$$B_0(P_0, G_m, k) = \frac{V_{DD}\sum_{n=k+1}^{N} C_{up\_n}(P_0) - Q_{TR}(P_0, V_{IL\max}) + Q_o}{\sum_{n=k+1}^{N} C_{up\_n}(P_0) + \sum_{n=k+1}^{N} C_{down\_n}(P_0)} \quad (8)$$

$$B_1(P_1, G_m, k) = \frac{V_{DD}\sum_{n=k+1}^{N} C_{up\_n}(P_1) - Q_{TR}(P_1, V_{IH\min}) + Q_o}{\sum_{n=k+1}^{N} C_{up\_n}(P_1) + \sum_{n=k+1}^{N} C_{down\_n}(P_1)} \quad (9)$$

With this information, we can predict the voltage bounds for every segment division of the target line and compare max($B_0(P_0,G_m,k)$) with min($B_1(P_1,G_m,k)$). Segments with consistent results for every downstream gate are the possible open locations, as described by the following expression:

$$\max_{P_0 \in PS_0} B_0(P_0, G_m, k) < \min_{P_1 \in PS_1} B_1(P_1, G_m, k) \quad (10)$$

For the application of the proposed diagnosis methodology, a set of lines suspected to contain an open, e.g. determined with a fault localization tool, and the fail results of a voltage test obtained on a standard ATE tester are required. The information given by the voltage test indicates, for each test pattern, whether the voltage of the target floating line has been interpreted as logic 1 or as logic 0. As an example, assume that there is a line suspected to be affected by an open. The open fault is excited by four test patterns {P_A, P_B, P_C, P_D}. From test results we know that the downstream gate G_1 has interpreted the voltage of the floating line as logic 1 for P_A and P_C and as logic 0 for P_B and P_D. Therefore, for every segment (open location) upper bounds are predicted for P_A and P_C (denoted by $B_1(P_A,G_1,k)$) and $B_1(P_C,G_1,k)$, respectively) and lower bounds for P_B and P_D ($B_0(P_B,G_1,k)$ and $B_0(P_D,G_1,k)$). Figure 3 illustrates the bound predictions for the whole set of segments assuming an open located at any position of the target line. Lower bounds are plotted in dotted black and upper bounds in dotted grey. To explain the observed logic results we need to determine a location in which *max*($B_0(P_0,G_1,k)$) (solid black) is lower than *min*($B_1(P_1,G_1,k)$) (solid grey). The open locations fulfilling this requirement are locations between segments 5 and 6 (grey shaded area).

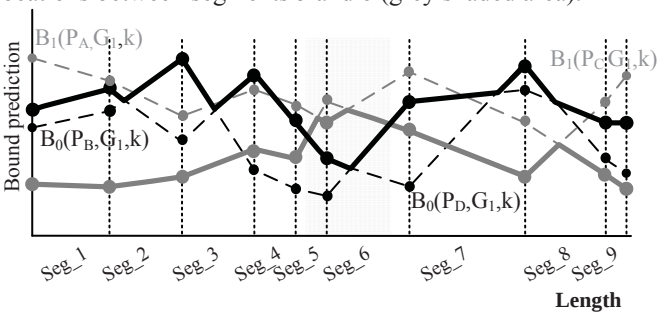

Figure 3 Bound prediction for four test patterns (P_A, P_B, P_C, P_D). Lower (upper) bounds are drawn in dotted black (grey). *max*$B_0(P_0,G_1)$ (*min*$B_1(P_1,G_1)$) is drawn in solid black (grey)-

V. Experimental Work

In this section, two real case studies are presented where the application of the proposed methodology is decisive for the proper diagnosis of an open defect. The first case belongs to a 0.18 µm technology while the second to a 65 nm technology.

A. Case study 1

The first case corresponds to a defective device from an

industrial test design fabricated in a CMOS 0.18 µm technology from NXP Semiconductors. This device did not pass the logic test. Subsequently, a logic diagnosis tool was used as a first step to interpret the failing information. The tool reported, as the most probable explanation for the failing behavior, four failing branches of the same net, as indicated in Figure 4a. This net has large fan-out driving a high number of gates. The layout information reports that the four branches have a common stem, illustrated in Figure 4b. Therefore, a possible explanation of the failing behavior could be an interconnect open at some point of the stem. However, the stem is still more than 100 µm long. Applying the proposed diagnosis methodology we want to confirm (or discard) the existence of the open and determine its exact location on the stem (if confirmed). As it is a huge net, for ease of understanding, the results are focused only on the last part of the net, i.e., from the stem driving the four gates to the input of one of the gates. The bound prediction results are reported in Figure 5 for every downstream gate. Black lines correspond to the maximum value of the lower bound ($maxB_0(P_0,G_m,k)$) whereas grey lines to the minimum value of the upper bound ($minB_1(P_1,G_m,k)$). For every gate, the range of locations accomplishing expression (10) is surrounded by a dotted square. G_4 does not add any information because V_{FN} was interpreted as logic 1 for all the patterns. Notice that G_2 reports the most restrictive range of locations with consistent results. Thus, the probable range of open locations is around 70-120 µm. (grey shaded area). The stem driving the four nets is around 120 µm. Therefore, we are discarding more than half the possible locations of the defect.

The proposed methodology has corroborated the presence of an open defect and minimized the range of its possible locations. However, if we had applied the approach without the inclusion of transistor parasitic capacitances, the results obtained would have been the ones shown in Figure 6. Solid (grey) black line represents the maximum (minimum) V_{FN} prediction for patterns where V_{FN} has been interpreted as logic 0 (1). To corroborate the presence of an open defect, the black line must be above the grey one. Notice how this is not accomplished for any of the downstream gates (except for G_4 which doesn't add information). Hence, using this methodology we would have lead to the wrong conclusion that the failing behavior of the device was not explained by an interconnect open defect in the target net.

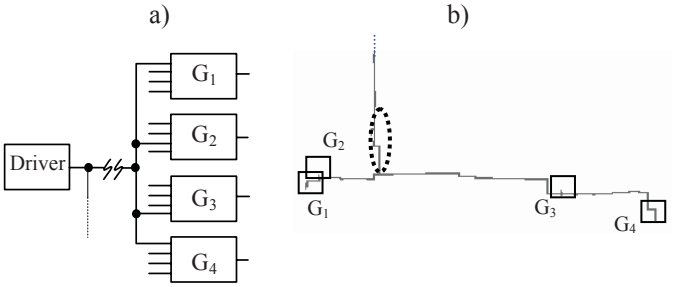

Figure 4: Defective device from a 0.18 µm technology a) Schematic of the target net b) Layout of the stem of the target net driving the four gates. Stem in dotted black.

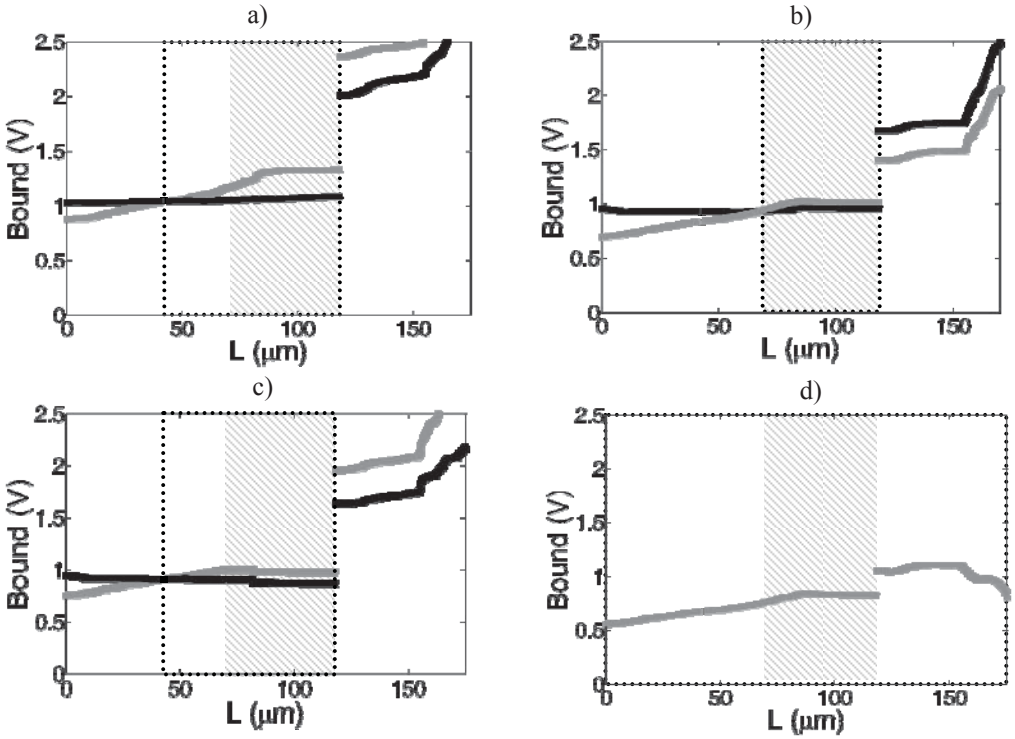

Figure 5: Bound prediction for a defective device from a 0.18 µm technology. $maxB_0(P,G_m,k)$ $(minB_1(P,G_m,k))$ in solid black (grey). The dotted squares limit the locations where $maxB_0(P_0,G_m,k) < minB_1(P_1,G_m,k)$ is accomplished for every specific gate independently. The grey shaded area represents the possible open locations, i.e. open locations where $maxB_0(P_0,G_m,k) < minB_1(P_1,G_m,k)$ is accomplished for all the gates. Results for a) G_1 b) G_2 c) G_3 d) G_4.

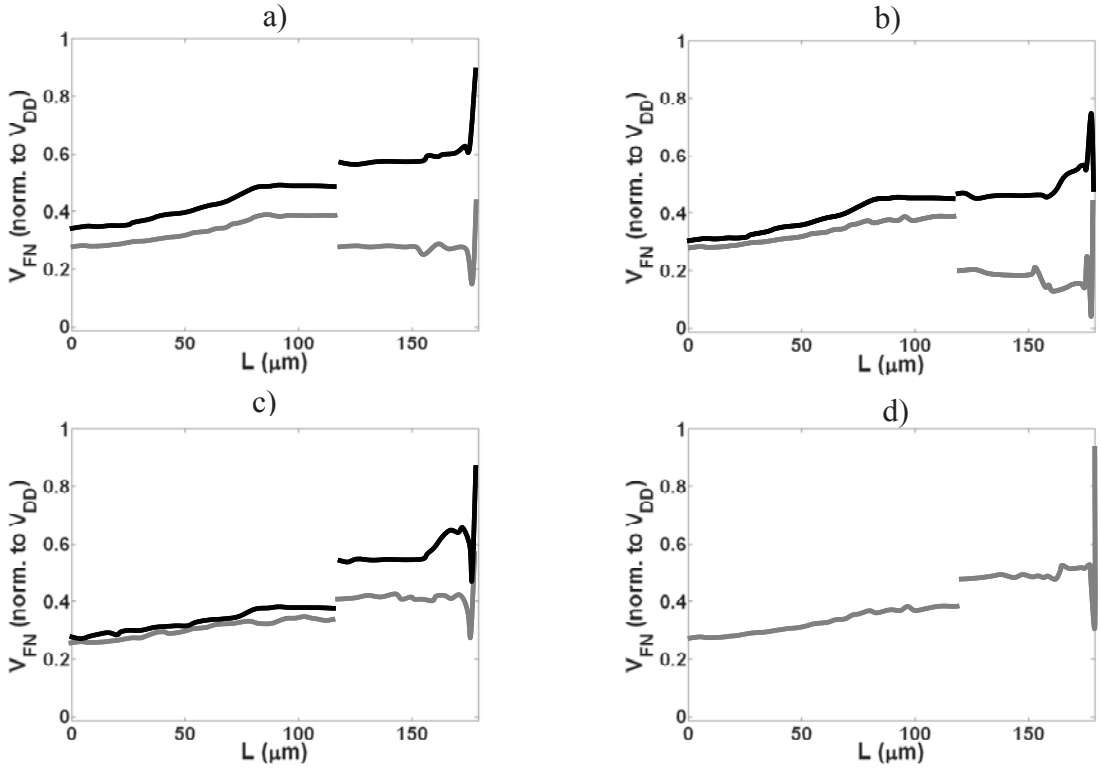

Figure 6: Voltage prediction for a defective device from a 0.18 µm technology. Solid black line (grey) corresponds to the maximum (minimum) voltage prediction for the patterns where V_{FN} has been interpreted as logic 0 (1). Results for a) G_1 b) G_2 c) G_3 d) G_4.

A. *Case study 2*

The second case study refers to a test design fabricated in a CMOS065-SOI 65 nm technology from STMicroelectronics. The design comprises random logic where a set of open defects have been intentionally injected. The target case is a full open defect located in an interconnect line of 100µm long. The defective interconnect line is cross-coupled with ten neighbors and is driving an inverter and a 2-input NOR gate, as shown in Figure 7.

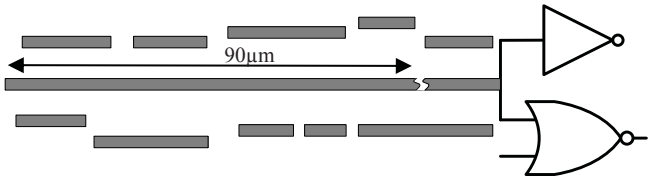

Figure 7: Layout information for a floating line from a 65nm technology device.

A logic test has been applied where the patterns have generated different neighbor excitations to the floating line. The bound prediction results are illustrated in Figure 9. The results showed consistent behavior for a short range of possible locations of a few µm long (located around 90µm far from the driver), which in fact, include the real location of the open. Similar to the previous case, if we had neglected the transistor parasitic capacitances, we would have lead to the wrong conclusions that an open can not explain the faulty behaviour. These results are illustrated in Figure 8. Notice that, although there are locations where the results are consistent for the NOR gate, there is not a consistent open location for the inverter results since the voltage predictions for the patterns setting a logic 1 are not higher (although very close) than the predictions for the patterns setting a logic 0.

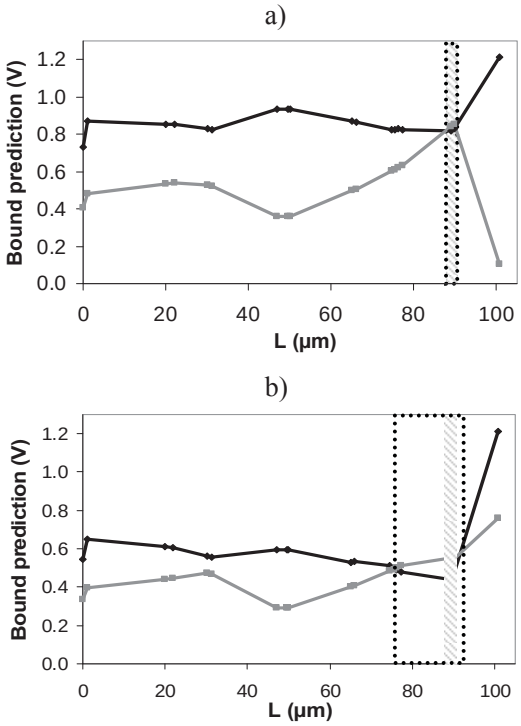

Figure 8: Bound prediction for a defective device from a 65 nm technology. $maxB_0(P,G_m,k)$ $(minB_1(P,G_m,k))$ in solid black (grey). The dotted squares limit the locations where $maxB_0(PS_0,G_m,k) < minB_1(PS_1,G_m,k)$ is accomplished for every specific gate independently. The grey shaded area represents the possible open locations. Results for a) Inverter b) 2-input NOR gate.

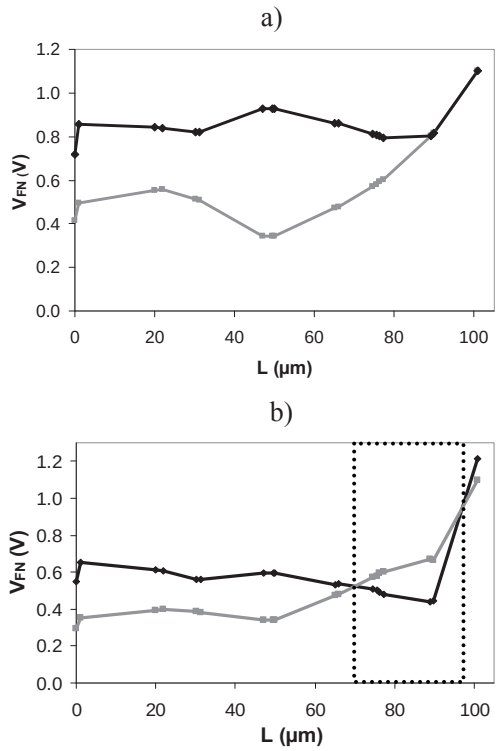

Figure 9: Voltage prediction for a defective device from a 65 nm technology. Solid black line (grey) corresponds to the maximum (minimum) voltage prediction for the patterns where V_{FN} has been interpreted as logic 0 (1). Results for a) Inverter b) 2-input NOR gate.

VI. Conclusion

The development of accurate diagnosis methodologies is important to solve process problems and yield improvement. For the diagnosis of interconnect open defects, the majority of diagnosis methodologies are based on the assumption that neighbouring lines determine the voltage of the floating node. However, this assumption is not valid in case of interconnect lines with fan-out, where transistor parasitic capacitances also influence the behaviour of the floating line.

This work presents a diagnosis methodology for interconnect full open defects where the impact of transistor parasitic capacitances are included. For that purpose, voltage bounds are predicted instead of predicting the exact voltage value of the floating line. The methodology is able to properly diagnose interconnect opens with fan-out even in the presence of Byzantine behaviour. Results for real defective devices from two different technology nodes have been presented. The inclusion of the impact of transistor capacitances in the diagnosis methodology has been determinant to properly diagnose the open defects.

Acknowledgment

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