High-Performance Control of a Single-Phase Shunt Active Filter

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***Abstract*—Shunt active power filters are devices, connected in parallel with nonlinear and reactive loads, which are in charge of compensating these characteristics in order to assure the quality of the distribution network. This paper analyzes the dynamics of a dc bus split-capacitor boost converter used as an active filter and proposes a control system which guarantees the desired closed-loop performance (unity power factor and load-current harmonics and reactive-power compensation). The proposed controller is hierarchically decomposed into two control loops, one in charge of shaping the network current and the other in charge of assuring the power balance. Unlike previous works that appeared in the literature, both control loops are analytically tuned. This paper describes the analytical design of the controller and presents some experimental results that show the good performance of the closed-loop system.**

***Index Terms*—Active power filters, current harmonics compensation, digital-control implementation, reactive-power compensation, repetitive control.**

I. Introduction

ACTIVE FILTERS are devices which allow the coexistence of nonlinear loads and good energy quality in distribution networks. A principal effort in the design and control of these devices has been developed in the past years. One research line deals with topologies and architectures [1], [2]. Several types of topologies have been proposed including parallel (shunt active filters), serial, and hybrid serial–parallel connections. Aside from the architecture, the underlying basic operation principle has also been a research topic. Passive, active (using switching converters), and mixed passive-active devices have been proposed [1]. Converter-based active filters may use a voltage or a current dc bus [3]. Most common architectures correspond to converter systems based on a voltage dc bus connected in parallel with the load. Usually, a passive filter connected in series with the converter is added to compensate switching ripple.

Another important research line related with active filters is their control, where many approaches have been proposed [4]–[9]. Most of them are based on two hierarchical control loops, an inner one in charge of assuring the desired current and an outer one in charge of determining the required shape as well as the appropriate power balance and converter operating point. The current control loop needs to be fast and precise. To assure this objective, several approaches have been proposed: hysteresis-based control [10]–[12], deadbeat controllers [13], Park transformation combined with linear controllers [14], and methods based on the application of the internal model principle [9], [15], [16]. For the outer control loop, many approaches have been proposed: genetic algorithms [17], [18], neural networks [13], Fourier series analysis [12], Lyapunov functions [19], or proportional–integral (PI) controllers to determine the amplitude of the network sinusoidal current or to cover the active-filter losses. Using a PI controller is the most common approach by far but, since the plant is nonlinear, this PI controller is usually experimentally tuned. When tuning this outer loop, generally, a time-scale decomposition is assumed, i.e., the outer loop is designed presuming the inner one is in steady state, see [9] for a deeper analysis.

This paper presents a new controller for a single-phase shunt active filter that uses the traditional two-control-loop decomposition. The current controller is composed of a feedforward action to obtain a very fast transient response and a feedback control law in charge of assuring closed-loop stability and a very good harmonic correction performance. The feedback control law is based on the use of a repetitive odd-harmonic controller [20]. The outer control law is based on the exact computation of the sinusoidal current network amplitude, and in order to improve robustness, this computation is combined with a feedback control law with an analytically tuned PI controller based on the average (at the line frequency) of the energy stored in the capacitors. The most relevant contribution of this work in comparison to [15] is the combined use of feedforward and feedback actions in the overall controller. The effect of the feedforward action is to enhance the convergence to the steady state, i.e., to reach the steady-state faster. This allows one to reduce the problems introduced by the two-loop structure and yields very good experimental results, both in transient and steady state.

This paper is organized as follows. Section II introduces the problem, the load description, the control objectives, and the model of the system. Section III shows the multiloop controller design with the underlying theoretical aspects and the zero-dynamics analysis. Section IV describes the experimental setup and gives some implementation issues. Section V presents some selected experimental results that show the good behavior of the whole system. Finally, Section VI summarizes the results of the work.

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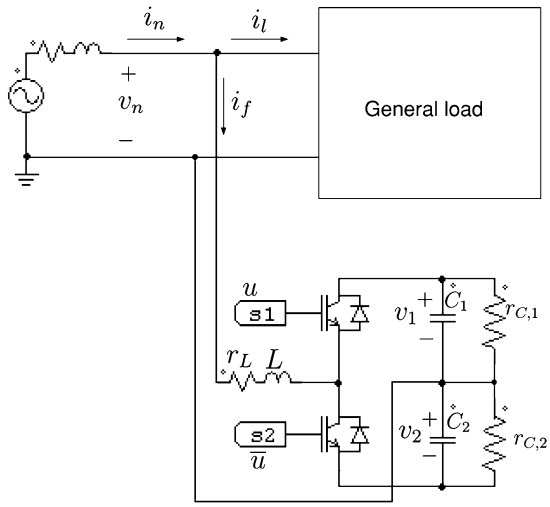

Fig. 1. Single-phase shunt filter connected to the network-load system.

II. Problem Formulation

A. Physical Model of the Boost Converter

Fig. 1 shows the system architecture. A load is connected to the power source, and in parallel, an active filter is applied in order to fulfill the desired behavior, i.e., to guarantee a unity power factor (PF) in the network port. A boost converter with the ac neutral wire connected directly to the midpoint of the dc bus is used as the active filter. The averaged (at the switching frequency) model of the boost converter is given by

$$L\frac{di_f}{dt} = -r_L i_f - v_1 d - v_2(d-1) + v_n \tag{1}$$

$$C_1\frac{dv_1}{dt} = -\frac{v_1}{r_{C,1}} + i_f d \tag{2}$$

$$C_2\frac{dv_2}{dt} = -\frac{v_2}{r_{C,2}} + i_f(d-1) \tag{3}$$

where d is the duty ratio, i_f is the inductor current, and v_1 and v_2 are the dc capacitor voltages, respectively; $v_n = V_n\sqrt{2}\sin(\omega_n t)$ is the voltage source that represents the ac line source; L is the converter inductor, r_L is the inductor parasitic resistance, C_1 and C_2 are the converter capacitors, and $r_{C,1}$ and $r_{C,2}$ are the parasitic resistances of the capacitors. The control variable d takes its value in the closed real interval [0, 1] and represents the averaged value of the pulsewidth-modulated (PWM) control signal injected to the actual system.

Assumption 1: Due to the nature of the voltage source, the load current, in steady state, is usually a periodic signal with only odd harmonics in its Fourier series expansion; therefore, it can be written as

$$i_l = \sum_{n=0}^{\infty} a_n \sin\left(\omega_n(2n+1)t\right) + b_n \cos\left(\omega_n(2n+1)t\right) \tag{4}$$

where a_n and $b_n \in \mathbb{R}$ are the real Fourier series coefficients of the load current. Note that it is assumed that there is no dc current in the load current as it is usual in ac distribution systems.

B. Control Objectives

Roughly speaking, the control objectives are the following.

1) The active-filter goal is to assure that the load is seen as a resistive one. This goal can be stated as $i_n^* = I_d^* \sin(\omega_n t)$, i.e., the source current must have a sinusoidal shape in phase with the network voltage[1]. The accomplishment of this objective will assure unity PF in the network terminals.
2) In order to assure a correct converter operation, it is necessary to maintain the dc bus voltage inside a certain range. As it will be formally proved in Section III-C, it is not possible to keep the dc bus voltage constant while fulfilling the previous control objective. Instead, the average value of the dc bus voltage is desired to be constant[2], i.e., $\langle v_1 + v_2\rangle_0^* = v_d$, where v_i, $i = 1, 2$, must fulfill the boost condition $(v_i > \sqrt{2}V_n)$. It is also desirable that this voltage would be almost equally distributed among both capacitors $(v_1 \approx v_2)$.

These two objectives define a nonstandard control problem. The second one is a regulation objective for the mean value of $v_1 + v_2$, but the first one is not a tracking specification because only a shape and not a signal is defined, i.e., I_d^* is not known *a priori*, and it must take the adequate value to maintain the power balance of the whole system. This special form of problem specifications implies the particular structure of the controller loops described in the next section.

C. Rewriting the Equations

Proposition 1: Let us assume that $C = C_1 = C_2$ and $r_C = r_{C,1} = r_{C,2}$. Then, using the diffeomorphism $\alpha = v_1 d + v_2(d-1)$, $i_f = i_f$, $E_C = (1)/(2)(C_1 v_1^2 + C_2 v_2^2)$, and $D = C_1 v_1 - C_2 v_2$, system (2) and (3) results in

$$L\frac{di_f}{dt} = -r_L i_f + v_n - \alpha \tag{5}$$

$$\frac{dE_c}{dt} = -\frac{2E_c}{r_C C} + i_f \alpha \tag{6}$$

$$\frac{dD}{dt} = -\frac{1}{r_C C} D + i_f. \tag{7}$$

Remark 1: E_C corresponds to the energy stored in the converter capacitors and D to the charge unbalance between them.

Remark 2: Equations (5) and (7) are linear and decoupled with respect to state variable E_c.

This new system, (5)–(7), needs a controller to fulfill the desired performance. This controller is designed using a two-level approach: first, a current controller which forces the sine wave shape for the network current and, second, an outer control loop to accomplish the appropriate active power balance for the whole system which computes the amplitude of the sinusoidal reference for the previous loop. This active power balance is achieved if the average energy stored in the active-filter capacitors is equal to a reference value E_c^d.

The full control scheme for the system is shown in Fig. 2. The specific controller designs will be presented in Sections III-A and III-B. It is worth to remark that (7) results in a forced first-

[1] x^* represents the steady-state value of signal $x(t)$.

[2] $\langle x\rangle_0$ means the dc value, or mean value, of the signal $x(t)$.

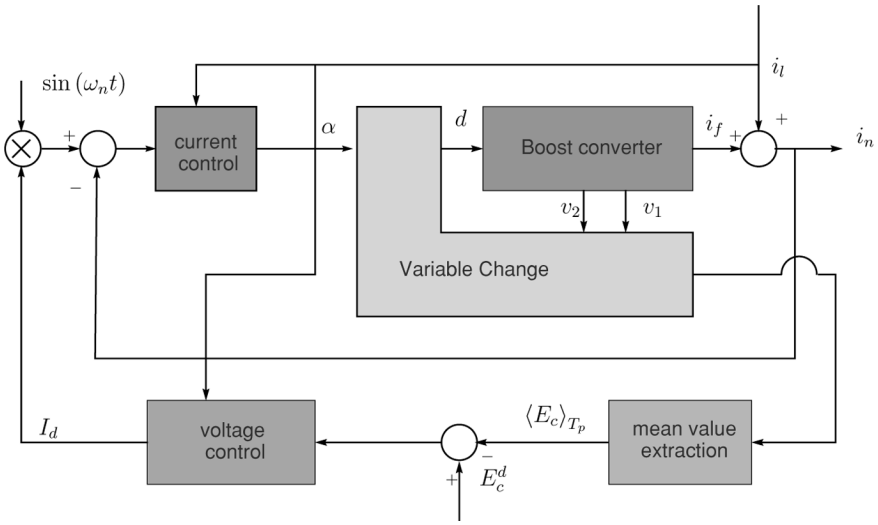

Fig. 2. Block diagram of the controller showing (inner) the current control loop and (outer) the voltage (or energy) control loop.

order linear system. The corresponding zero dynamics is studied in Section III-C.

III. Control Design

A. Current Loop

Taking benefit from the fact that (5) is linear, a linear controller is designed to force a sinusoidal shape in the network current (see Fig. 2). This controller consists of two parts:

1) a feedforward controller which fixes the desired steady state

$$i_n = I_d(t)\sin(\omega_n t). \tag{8}$$

2) a feedback controller which compensates uncertainties and assures closed-loop stability.

Proposition 2: The control action

$$\alpha_{\text{ff}} = v_n + L\frac{di_l}{dt} + r_L i_l - r_L I_d(t)\sin(\omega_n t) - L\omega_n I_d(t)\cos(\omega_n t) - L\frac{dI_d(t)}{dt}\sin(\omega_n t) \tag{9}$$

forces the current network to be $I_d(t)\sin(\omega_n t)$ in steady state.

Proof: By construction, the following equations are always fulfilled:

$$i_n = i_f + i_l \tag{10}$$

$$\frac{di_n}{dt} = \frac{di_f}{dt} + \frac{di_l}{dt}. \tag{11}$$

Then, from (5) and (11)

$$\frac{di_n}{dt} = -\frac{r_L i_n}{L} - \frac{\alpha}{L} + \frac{v_n}{L} + \frac{di_l}{dt} + \frac{r_L i_l}{L}. \tag{12}$$

Forcing $i_n = I_d\sin(\omega_n t)$ and isolating α, (9) is obtained. ■

Remark 3: Equation (9) defines the nominal control action which will keep the system in the desired trajectory; therefore, it will be used as a feedforward action. It is worth noticing that it can be statically computed in each time instant from measured data. Clearly, this action must be combined with a feedback path in order to overcome model uncertainties, disturbances, and measurement noise.

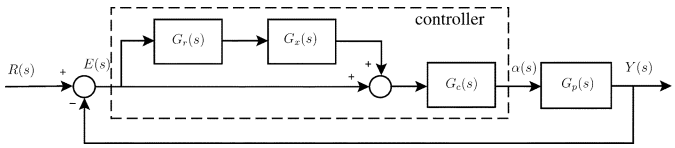

Fig. 3. Repetitive control current loop.

Remark 4: As the signal to be tracked and rejected in this system is periodic, it is convenient to design a controller which allows one to track and reject this type of signals. Moreover, as it has been shown in Section III-A, this signal will be periodic but containing only odd harmonics. A technique which has been proved particularly good for this type of signals is repetitive control [21] and, in particular, odd-harmonic repetitive control [20].

Repetitive controllers are usually implemented in a "plug-in" fashion, i.e., the repetitive compensator is used to augment an existing nominal controller $G_c(s)$ (Fig. 3). This nominal compensator is designed to stabilize the plant $G_p(s)$ and provides disturbance attenuation across a broad frequency spectrum. The controller is composed of the internal model (Fig. 4) and a linear system $G_x(s)$ which is designed to ensure closed-loop stability. In this scheme, (5) corresponds to plant

$$G_p(s) = \frac{Y(s)}{\alpha(s)} = \frac{-1/r_L}{\frac{L}{r_L}s + 1}. \tag{13}$$

Odd-harmonic repetitive control uses an internal model (Fig. 4) which introduces infinite gain at a certain frequency and all its odd harmonics. This internal model is based on to feedback a pure delay of $T_p/2$ seconds, with T_p being the fundamental period of the periodic signal to be tracked or rejected.

In practical implementations, a low-pass filter $H(s)$ is placed in the internal model loop in order to reduce gain at those frequencies where system behavior is not properly modeled (Fig. 4). It is important to emphasize that the low-pass filter

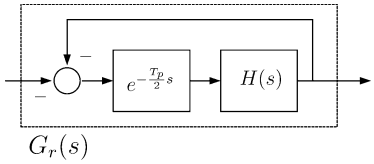

Fig. 4. Odd-harmonic repetitive control-loop internal model.

$H(s)$ reduces the repetitive loop gain to finite values for all the frequencies, giving it a general low-pass shape.

Proposition 3 ([20]): The closed-loop system of Fig. 3 is stable if the following conditions are fulfilled.

1) The closed-loop system without the repetitive controller is stable, i.e., $G_o(s) = (G_c(s)G_p(s))/(1 + G_c(s)G_p(s))$ is stable.
2) $||H(s)||_\infty < 1$.
3) $||1 - G_o(s)G_x(s)||_\infty < 1$, where $G_x(s)$ is a design filter to be chosen.

Remark 5 ([20]): These conditions hold by a proper design of $G_c(s)$ and $G_x(s)$. Namely,

Condition 1) It is advisable to design the controller $G_c(s)$ with a high-enough robustness margin.

Condition 2) There is no problem with the causality of $H(s)$ because it is series connected with the delay $e^{-(T_p)/(2s)}$ and the repetitive loop will be implemented as a whole.

Condition 3) A trivial structure which is often used is [22]: $G_x(s) = k_r(G_o(s))^{-1}$. This structure can only be used if $G_o(s)$ is a minimum-phase transfer function. Otherwise, other techniques should be applied in order to avoid closed-right-hand-side (RHS) plane zero–pole cancellations [22]. Moreover, as stated before, there is no problem with the causality of $G_x(s)$. As argued in [23], k_r must be designed looking for a tradeoff between robustness and transient response.

This repetitive controller defines the feedback law

$$\alpha_{\rm fb} = G_c(s)\left(1+G_x(s)\left(\frac{-{\rm e}^{-\frac{T_p}{2}s}H(s)}{1+{\rm e}^{-\frac{T_p}{2}s}H(s)}\right)\right)(I_{n,{\rm ref}}(s) - I_n(s)). \tag{14}$$

Proposition 4: Under the combined action of the feedforward and the feedback control action ($\alpha = \alpha_{\rm fb} + \alpha_{\rm ff}$), the network current will tend to

$$\lim_{t\to\infty} i_n(t) = I_d(t)\sin(\omega_n t). \tag{15}$$

B. Energy Shaping (Voltage Loop)

As the source voltage is $v_n = V_n\sqrt{2}\sin(\omega_n t)$, the network current which guarantees a PF of one is $I_d^*\sin(\omega_n t)$. Hence, the desired power flow seen from the network is

$$p_l(t) + p_f(t) = p_n(t) \triangleq v_n(t)i_n(t) = I_d^*\sqrt{2}V_n\sin^2(\omega_n t) \tag{16}$$

where $p_l(t)$ and $p_f(t)$ stand for the instantaneous power consumed from the load and the active filter, respectively (see Fig. 1). This desired power flow is obtained once the network current has been shaped by the inner loop, i.e., the inner loop has reached the steady state.

A complementary active-filter goal is to consume no power, except for its operating losses. Therefore, as it is not possible to demand $p_f(t) \approx 0\ \forall t$, the following relationship is desired:

$$\int_{t-T_p}^{t} p_f \approx 0. \tag{17}$$

From the power-flow point of view, the active filter redistributes the power flow within one period so that (16) and (17) hold. Hence, the total energy stored in the converter (E_T) should not suffer variations within a period, i.e.,

$$\int_{t-T_p}^{t} \dot{E}_T = 0. \tag{18}$$

The stored energy in the converter can be decomposed into the energy stored in the inductors $(E_L = (1/2)L(i_f)^2)$ and the energy stored in the capacitors $(E_c = (1/2)C_1v_1^2 + (1/2)C_2v_2^2)$. Aside from this, some energy is lost in the parasitic resistors of the inductors, capacitors, and switches.

Noting that $i_f \approx I_d^*\sin(\omega_n t) - i_l$ is an odd-harmonic periodic signal and dismissing the parasitic resistance of the inductors, it can be easily proven that, independent of the load currents, the steady-state variation of energy in the inductors in one period is zero. Thus

$$\int_{t-T_p}^{t} \dot{E}_T = \int_{t-T_p}^{t} \dot{E}_c. \tag{19}$$

Proposition 5: The averaged evolution of E_T in one period (T_p) in steady state with $r_L \approx 0$ is[3]

$$\begin{aligned}\frac{d}{dt}\langle E_T(t)\rangle_{T_p} &= \frac{d}{dt}\langle E_c(t)\rangle_{T_p} \\ &= \frac{V_n\,(I_d^* - a_0^*)}{\sqrt{2}} - \frac{2}{r_{C_1}}\langle E_c(t)\rangle_{T_p}.\end{aligned} \tag{20}$$

Proof: As previously mentioned, in steady state, the averaged evolution of E_T and E_c are the same. It is important to note that

$$\frac{d}{dt}\langle E_c(t)\rangle_{T_p} = \frac{d}{dt}\int_{t-T_p}^{t} E_c(t)dt = \int_{t-T_p}^{t}\frac{dE_c(t)}{dt}dt.$$

The evolution of E_c is described by (6); its averaged behavior in one period (T_p) can be obtained by

$$\begin{aligned}\int_{t-T_p}^{t}\frac{dE_c}{dt}dt &= \int_{t-T_p}^{t}\left(-\frac{2E_c}{r_C C} + i_f\alpha\right)dt \\ &= -\frac{2}{r_C C}\langle E_c(t)\rangle_{T_p} + \int_{t-T_p}^{t} i_f(t)\alpha(t)dt.\end{aligned}$$

[3] $\langle f(t)\rangle_{T_p} = (1/T_p)\int_{t-T_p}^{t} f(\tau)d\tau$.

From (4), (5), (8), and (10) and presuming steady state, it can be established that

$$\int_{t-T_p}^{t} i_f(t)\alpha(t)dt = \frac{\sqrt{2}V_n\pi\left(I_d^* - a_0^*\right)}{\omega_n} - \frac{r_L\pi}{\omega_n} \times \left(\left(I_d^* - a_0^*\right)^2 + \left(b_0^*\right)^2 + \sum_{j=1}^{\infty}\left(\left(a_j^*\right)^2 + \left(b_j^*\right)^2\right)\right)$$

where the term proportional to r_L represent the losses in the inductor parasitic resistor. Then, assuming $r_L \approx 0$

$$\frac{d}{dt}\left\langle E_c(t)\right\rangle_{T_p} = -\frac{2}{r_C C}\left\langle E_c(t)\right\rangle_{T_p} + \frac{\sqrt{2}V_n\pi\left(I_d^* - a_0^*\right)}{\omega_n}. \quad (21)$$

■

Remark 6: The value of $a_0(t)$ corresponds to the active part of the fundamental component of i_l (the load current). This value can be obtained from the analysis of the load current as

$$a_0(t) = 2\left\langle i_l(t)\sin(\omega_n t)\right\rangle_{T_p}. \quad (22)$$

Remark 7: Note that (20) in Proposition 5 describes the desired averaged behavior of the capacitor energy dynamics in (6). Alternatively, these results can be obtained by applying averaging theory [24] as in [25] and [26].

In Section III.A, a current control loop is built with feedforward and feedback actions. The feedforward action makes the convergence of the current loop to the reference very fast[4]; therefore, it can be considered in steady state after a short initial transient. The feedback action guarantees that the system does not leave the reference trajectory once it is reached.

In this context, the system complete dynamics can be decomposed into a fast dynamics corresponding to the current equations and a slow dynamics corresponding to the energy dynamics. This type of decomposition corresponds to a kind of two-time-scale decomposition [9], [27].

In our case, (20) represents the capacitor energy evolution under the assumption that the current loop is in steady state and that $I_d(t)$ is an almost constant value. Therefore, in order to make this equation represent the behavior of the slow dynamics, it is necessary to design an energy controller with a small bandwidth to obtain an $I_d(t)$ as constant as possible (i.e., the energy controller should have a slow dynamics compared to the current one).

Choosing

$$\begin{aligned} I_d(t) &= I_d^{\text{ff}}(t) + I_d^{\text{fb}}(t) \\ &= a_0(t) + k_i\int_0^t \left(E_c^d - \left\langle E_c(t)\right\rangle_{T_p}\right)d\tau \\ &\quad + k_p\left(E_c^d - \left\langle E_c(t)\right\rangle_{T_p}\right). \end{aligned} \quad (23)$$

[4]It is important to note that, in this type of circuit, the feedforward action is very efficient due to the fact that the circuit structure and parameters are very well known.

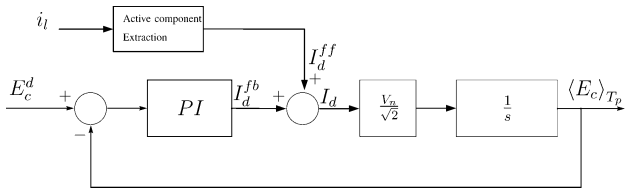

Fig. 5. Simplified 50-Hz model with PI controller.

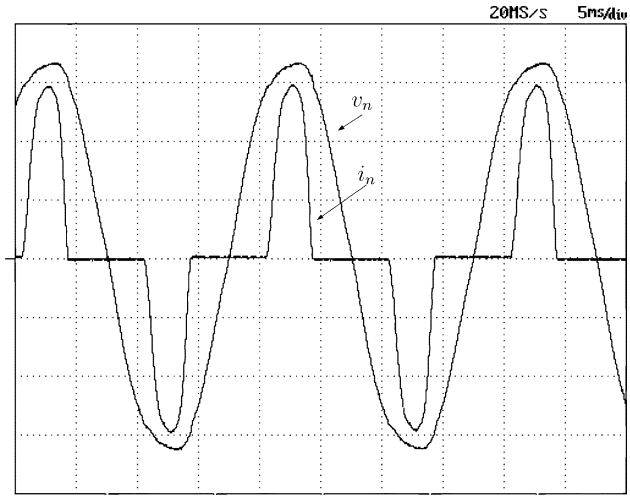

Fig. 6. Nonlinear load: Voltage and current (92 and 19.2 A/div, respectively).

(20) will converge to $\left\langle E_c(t)\right\rangle_{T_p} = E_c^d$ and$(d/dt)\left\langle E_c(t)\right\rangle_{T_p} \approx 0$ once the steady state is reached (Fig. 5).

This control law has the following structure:

1) A feedforward term $I_d^{\text{ff}}(t) = a_0(t)$. This feedforward term assures the energy balance in the ideal case ($r_L = 0$ and $r_C = 0$) and takes into account i_l characteristics. Hence, changes in i_l are immediately taken into account. This feedforward term constitutes the major term of I_d, and it will be constant unless the load current changes. In case of load-current change, this term will contribute to avoid significant variations in $\left\langle E_c(t)\right\rangle_{T_p}$. Note that this term makes (21) independent of the load current and does not interfere with the time-scale decomposition.
2) A feedback term which is in charge of compensating dissipative effects and the system uncertainties, the contribution of this term will be small compared to the feedforward one. Thus, a classical PI controller will regulate $\left\langle E_c(t)\right\rangle_{T_p}$ to the desired value E_c^d without steady-state error, i.e., the losses in the inductor and capacitor parasitic resistances can be considered as an additive complex-dynamics disturbance in the voltage closed-loop system. However, as the experimental results will show, it is not worth taking these losses into account in the design of the voltage loop.

   It is important to note that, in order to strengthen the time-scale decomposition, k_i and k_p should be chosen to obtain a slow changing $I_d(t)$.

Although the active-filter topology is different, in [26], a similar PI controller designed in an averaged framework is proposed. However, in order to implement it, in [26], an instantaneous version of the controller is obtained from the averaged one. Unlike this approach, in this paper, the PI controller works

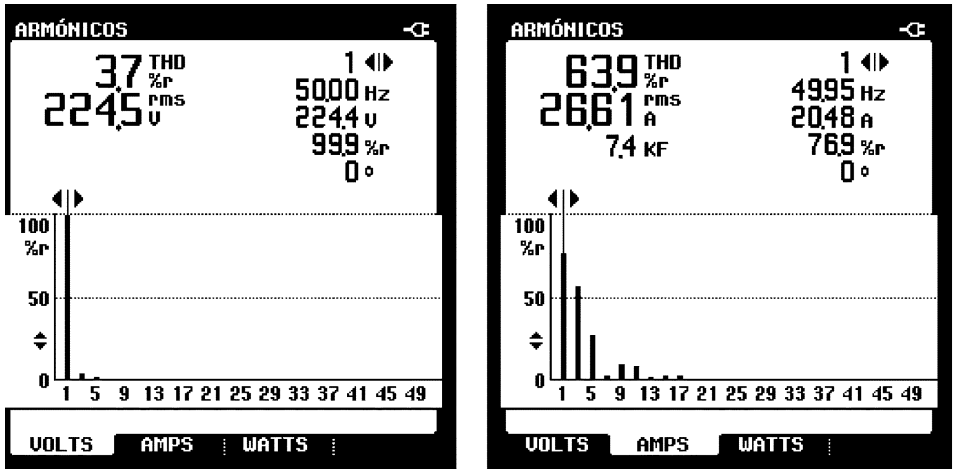

Fig. 7. Nonlinear load: Voltage and load current (rms and THD).

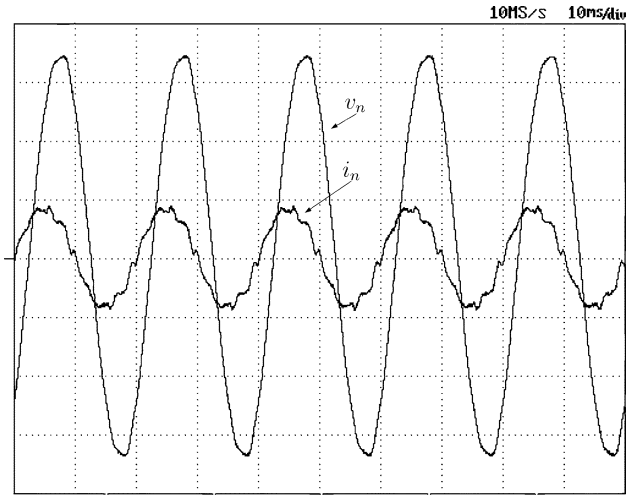

Fig. 8. Linear load: Voltage and current (92 and 19.2 A/div, respectively).

directly on the averaged variables that are continuously computed from the acquired physical data, giving a simpler framework and a more straightforward implementation.

C. Zero Dynamics

In the previous sections, the evolution of (5) and (6) has been analyzed, and the controller was designed. In order to complete the study, this section analyzes the dynamics of (7) that represents the charge unbalance of the dc bus. Ideally, no unbalance is desired, i.e., $D(t) \approx 0$.

Proposition 6: In steady state, the unbalance evolves as

$$D^*(t) = \frac{I_d^*}{\varsigma_0}\sin(\omega_n t + \delta_0) - \sum_{n=0}^{\infty}\frac{a_n^*}{\varsigma_n}\sin\left(\omega_n(2n+1)t + \delta_n\right) + \frac{b_n^*}{\varsigma_n}\cos\left(\omega_n(2n+1)t + \delta_n\right) \quad (24)$$

where $\varsigma_n = \sqrt{\gamma^2 + ((2n+1)\omega_n)^2}$ and $\delta_n \triangleq -\tan^{-1}(((2n+1)\omega_n)/\gamma)$ with $\gamma \triangleq 1/(r_C)$.

Proof: Equation (7) is a first-order linear differential equation with an exogenous input $i_f \approx I_d\sin(\omega_n t) - i_l$; therefore, it can be written in input–output form as

$$\frac{D(s)}{i_f(s)} = \frac{1}{s+\gamma}. \quad (25)$$

Note that $\gamma > 0$; therefore, the system is stable.

As, in steady state, the input is a periodic signal, the output will also be a periodic signal. Combining the definition of (4) and the solution of the system (25) in a steady-state forced periodic regime, (24) is obtained. ■

Proposition 7:

$$\|D\|_\infty < \frac{1}{\gamma}\|i_f\|_\infty. \quad (26)$$

Proof: Straightforward from previous proposition. ■

Although this equation may be too conservative, it gives an approximate idea about the bounds over D. As ς_n increases with the frequency and assuming that, as usual, higher harmonics have lower amplitudes than near fundamental ones, the contribution of these harmonics to the evolution of $D^*(t)$ may be neglected in most cases.

Remark 8: As a conclusion, D^* presents an intrinsic oscillatory behavior with zero mean value. As $D = C_1v_1 - C_2v_2 \approx C(v_1 - v_2)$, this implies a voltage unbalance proportional to the inverse of the capacitance; therefore, increasing the capacitance will reduce their amplitude.

Proposition 8: E_c^* is an even-harmonic periodic signal obtained by filtering $i_f^*\alpha^*$ with $1/(s+2\gamma)$.

Proof: The evolution of the energy stored in the capacitors (E_c) is described by (6). This equation corresponds to a stable linear system with an exogenous input. This input is $i_f\alpha$, where i_f^* and α^* are odd-harmonic signals. As a consequence $i_f^*\alpha^*$ will be an even-harmonic periodic signal. ■

Remark 9: The voltage loop (Section III.B) will assure that the dc component of these intrinsic oscillations will be regulated to the desired value (E_C^d). As a conclusion, E_C^* presents an intrinsic oscillatory behavior with a mean value which can be regulated by the energy control loop.

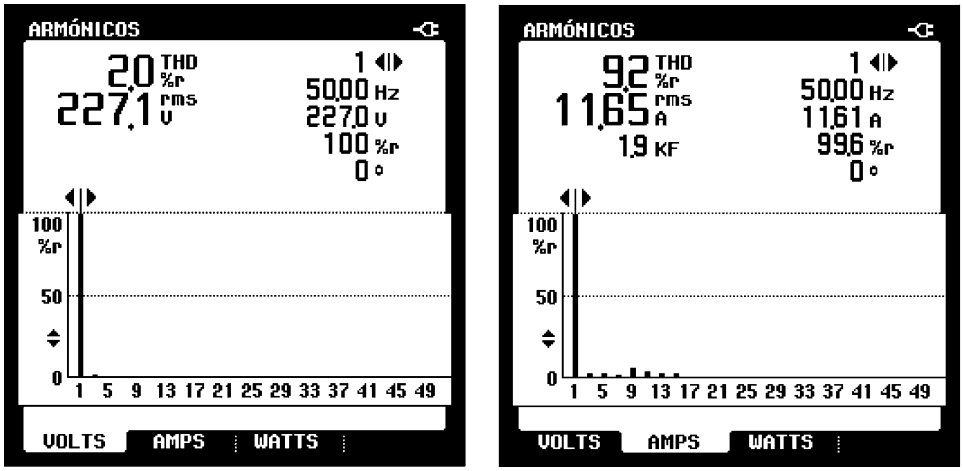

Fig. 9. Linear load (resistive–capacitive): Voltage and load current (rms and THD).

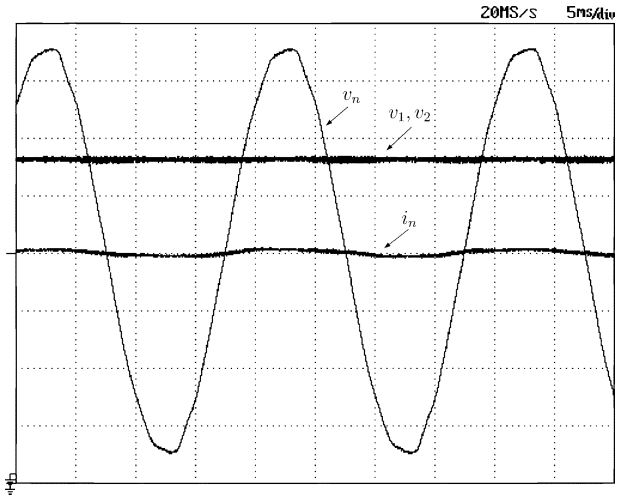

Fig. 10. Active filter with no load: Network voltage v_n, network current i_n, and semibus dc voltages v_1 and v_2 (92 V/div, 19.2 A/div, and 74.5 V/div, respectively).

Proposition 9: The energy intrinsic oscillations can be bounded in the following way:

$$\begin{aligned}\left\|E_c^*-E_c^d\right\|_\infty &< \frac{1}{2\gamma}\Bigg(\frac{\left(r_L-\sqrt{r_L^2+\omega_n^2L^2}\right)}{2}(I_d^*)^2 \\ &\quad + L_l\|i_l\|_\infty\left\|\frac{di_l}{dt}\right\|_\infty + r_L\|i_l\|_\infty^2 \\ &\quad + \left(L\left\|\frac{di_l}{dt}\right\|_\infty + V_n + L\omega_n\|i_l\|_\infty + 2r_L\|i_l\|_\infty\right) \\ &\quad \times I_d^*V_n\|i_l\|_\infty\Bigg).\end{aligned}$$

Proof: From (5)

$$\left\|E_c^*-E_c^d\right\|_\infty < \frac{1}{2\gamma}\left\|i_f^*\alpha^*\right\|_\infty. \tag{27}$$

Assuming steady-state current, $\alpha^* = \alpha_{\text{ff}}$; hence, an analytic expression for $i_f^*\alpha^*$ can be obtained. This expression can be bounded in terms of I_d^*, $\|i_l\|_\infty$, and $\|\frac{di_l}{dt}\|_\infty$. ■

Remark 10: As I_d^* can be approximated by the load-current active component ($I_d^* \approx a_0$), the amplitude of the oscillations can be bounded if the load current is known. This bound may be useful to design the dc bus active-filter capacitance. Similar results for other shunt active-filter topologies have been previously stated in [28].

IV. Experimental Setup and Implementation Issues

A. Experimental Setup

The experimental setup used to test the designed controller has the following parts.

1) Active filter: half-bridge boost converter (split-capacitor dc bus) with insulated-gate bipolar transistor (IGBT) switches (nominal current of 100 A) and the following parameters: $r_L = 0.3\ \Omega$, $L = 0.8$ mH, $C_1 = C_2 = 9900\ \mu$F, and $r_{C_1} = r_{C_2} = 8200\ \Omega$. The switching frequency of the converter is 20 kHz, and a synchronous (regular) centered-pulse single-update-mode pulsewidth modulation strategy is used to map the controller's output to the IGBT gate signals.
2) Rectifier (nonlinear load): full-wave diode rectifier with a filter capacitor $C = 4500\ \mu$F. The active power with the nominal dc resistor is $P = 4.56$ kW, and its reactive power is approximately zero. Fig. 6 shows the shape of the ac mains voltage and current, and Fig. 7 shows the harmonic content of the voltage and the current for the rectifier with the nominal dc resistor. It is worth to remark that the total harmonic distortion[5] (THD) of this current is about 63.9%, and its maximum derivative is about 70 kA/s.
3) Linear load: resistive–capacitive load with active power $P = 1.85$ kW, reactive power $Q = 1.85$ kVA, apparent power $S = 2.62$ kVA, $\cos\phi = 0.71$, and $PF = 0.69$. Fig. 8 shows the shape of the ac mains voltage and current,

[5]In this paper, the THD figures and the harmonic content are always taken with respect to the rms value of the signals ($\text{THD} \in [0, 100]$) and they have been obtained using a Power Quality Analyzer Fluke 43 instrument.

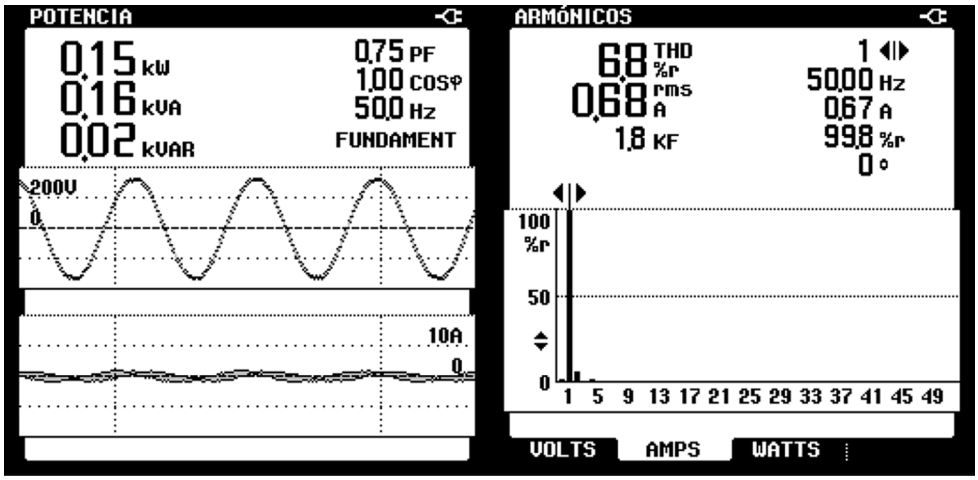

Fig. 11. Active filter with no load: RMS and THD values of network current $i_n(t)$ and $\cos\phi$ and PF.

and Fig. 9 shows the harmonic content of the voltage and the current for this RC load.

4) Analog circuitry of feedback channels. The ac mains voltage, the ac mains current, and the dc bus voltages are sensed with a voltage transformer, a hall-effect sensor, and two isolation amplifiers, respectively. All the signals from the sensors pass through the corresponding gain conditioning stages to adapt their values to the A/D converter input, taking advantage of their full dynamic range. In addition, all the feedback channels include a first-order low-pass filter with unity dc gain and 4.3-kHz cutoff frequency[6].
5) Control hardware and DSP implementation. The control board has been internally developed and is based on an ADSP-21161 floating-point DSP processor with an ADSP-21990 fixed-point mixed-signal DSP processor that acts as coprocessor, both from Analog Devices. The ADSP-21161 and the ADSP-21990 communicate with each other using a high-speed synchronous serial channel in direct-memory-access (DMA) mode. The ADSP-21990 deals with the PWM generation and the A/D conversions with its eight integrated 14-bit high-speed A/D channels.
6) The nominal voltage of the ac mains is $V_n = 230$V rms, and its nominal frequency is 50 Hz.

B. Implementation Issues

As previously stated, the controller has been implemented on a DSP-based hardware; therefore, all the controllers are implemented in a digital framework. The IGBT switching frequency is technologically limited to 20 kHz; therefore, this frequency has been selected as the sampling one. In the following points, several topics, including the discretization procedure and the controller implementation, are discussed.

1) The sampling rate of the A/D channels and the current loop is $F_s = 20$ kHz, the same as the switching frequency of the active filter. Because the sampling rate of the ac mains voltage and current is the same as the converter switching frequency, some aliasing problems can arise. In particular, the switching ripple appears, usually, as a dc component on the discrete-time side (after A/D conversion). This fact has proved particularly critical in ac mains voltage sensing because this signal is used as the carrier signal in the controller. To solve this problem, the sampled ac voltage is passed through a parametric equalizer filter that includes a zero in $z = 1$ to reject, in steady state, the dc component of the signal. In the ac mains current, the problem is not so important because the open-loop dc gain of the current loop is low, and then, the current loop is hardly affected by the fictitious current dc component.
2) The controller and its related code (communications, alarms supervision, data collection routines, etc.) are coded in C programming language without an underlying real-time operating system. Only a few of the lowest level procedures are coded in assembler for efficiency reasons.

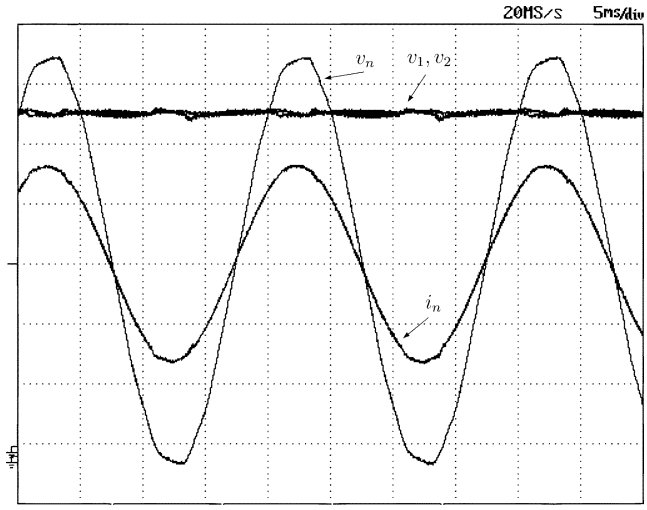

Fig. 12. Active filter with the nonlinear load: Network voltage v_n, network current i_n, and semibus dc voltages v_1 and v_2 (92 V/div, 19.2 A/div, and 74.5 V/div, respectively).

[6]The oscilloscope screens in the figures of this section and the following show the voltages and currents after the corresponding analog low-pass filters.

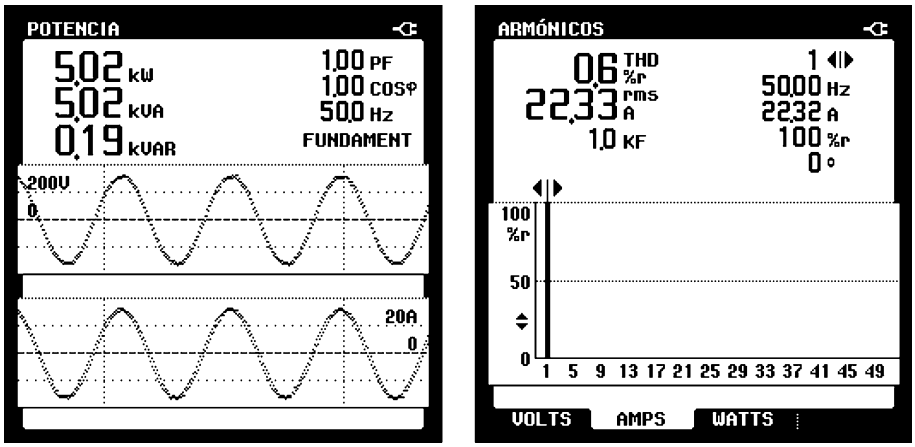

Fig. 13. Active filter with the nonlinear load: RMS and THD values of network current i_n and P, Q, $\cos\phi$, and PF.

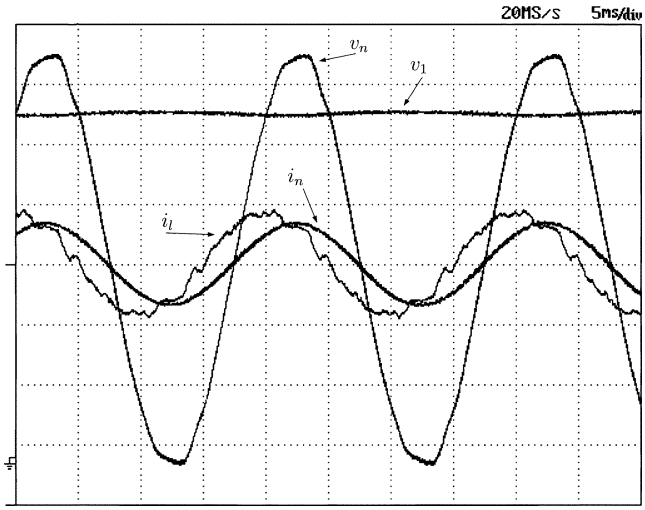

Fig. 14. Active filter with the linear load: Network voltage v_n, network current i_n, load current i_l, and semibus dc voltage v_1 (92 V/div, 19.2 A/div, 19.2 A/div, and 74.5 V/div, respectively).

The available computing power of the floating-point DSP processor allows the controller operations to be calculated in about one third of the sampling period.

3) The inner current loop controller $G_c(s)$ has been designed as a first-order lag controller, specifically $G_c(s) = -(0.0135s+73.55)/(s+1996)$, and its main objective is to improve the closed-loop gain margin. The designed $G_c(s)$ gives a closed-loop transfer function $G_o(s)$ which is minimum phase; therefore, there is no problem in choosing $G_x(s) = k_r(G_o(s))^{-1}$. The assigned value for k_r is 0.5, and the selected low-pass finite-impulse-response filter is $H(s) = (1/4)e^{T_s s} + (1/2) + (1/4)e^{-T_s s}$. The whole controller has been discretized using the bilinear approximation method. Note that $1/T_s$ is an integer multiple of $1/T_p$, i.e., $(T_p/T_s) = 400$; this particular fact allows the easy implementation of the pure delay as a discrete-time delay.
4) Combining (20) and (23), the closed-loop transfer function $G_E(s)$ with input $E_c^d(t)$ and output $\langle E_c(t)\rangle_{T_p}$ is

$$G_E(s) = \frac{k_i + k_p s}{\frac{\sqrt{2}}{V_n}s^2 + \left(k_p + \frac{4}{V_n\sqrt{2}r_C}\right)s + k_i}. \tag{28}$$

This transfer function is used to design the closed-loop time response. The closed-loop system has two poles and one zero. In this paper, one of the two poles has been selected to cancel the zero (both placed in $s = -(1/4100)$ rad/s), and the other pole is in $s = -22$ rad/s, giving $k_p = 0.1$ and $k_i = 0.02 \cdot 10^{-3}$. This pole–zero configuration corresponds to a tradeoff between stability and settling time. As the PI controller is digitally implemented, it has been discretized using the bilinear approximation method with a 20-kHz sampling frequency.

5) In order to compute the value of a_0 and $\langle E_c(t)\rangle_{T_p}$, the continuous-time integrals have been substituted by a discrete-time comb filter with transfer function

$$F(z) = \frac{Y(z)}{U(z)} = \frac{2T_s}{T_p}\frac{1 - z^{-\frac{T_p}{T_s}}}{1 - z^{-1}} \tag{29}$$

where $(T_p/T_s) = 400$.

6) The inner loop feedforward term, (9), implies the knowledge of di_l/dt. Unfortunately, it is difficult to directly measure this information. As the only measured variable is i_l, the filter $Ls + r_L$ should be implemented but this filter is noncausal. In order to obtain a causal behavior and to reduce the noise problem caused by the derivative term, it has been completed with a low-pass term giving $H_d(s) = (Ls+r_L)/(T_s s+1)$. This filter has also been digitally implemented using the bilinear approximation method with sampling time T_s.
7) Additionally, the inner loop feedforward term (9) needs $dI_d(t)/dt$. This value can be obtained directly from (23). To compute the operator $d\langle\cdot\rangle_{T_p}/dt$, the digital comb filter $J(z) = (2T_s/T_p)(1 - z^{-(T_p/T_s)})$ is used.

V. Experimental Results

This section shows some of the experimental results obtained for the active-filter operation with the designed control system. The results are presented by means of oscilloscope and power analyzer screen dumps of the ac mains electrical variables and, when it is necessary, the active-filter semibus dc voltages.

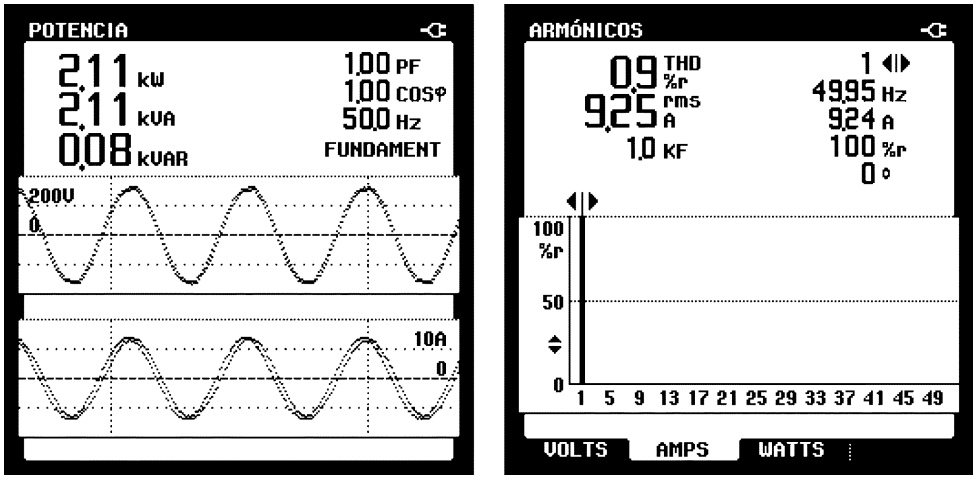

Fig. 15. Active filter with the linear load: RMS and THD values of network current i_n and P, Q, $\cos\phi$, and PF.

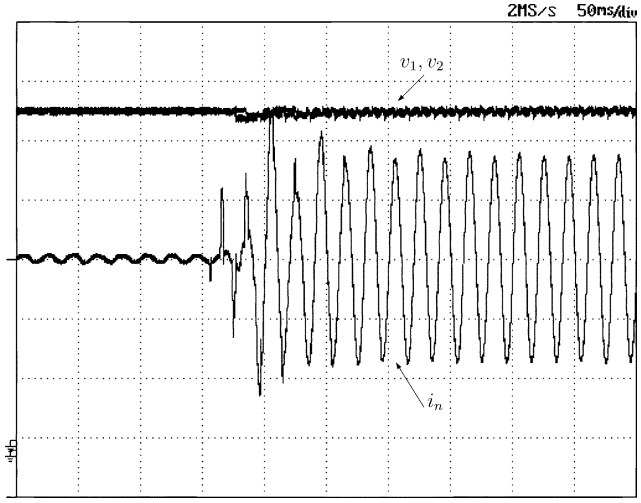

Fig. 16. Network current i_n and semibus dc voltages v_1 and v_2: From no load to full nonlinear load (19.2 A/div and 74.5 V/div, respectively).

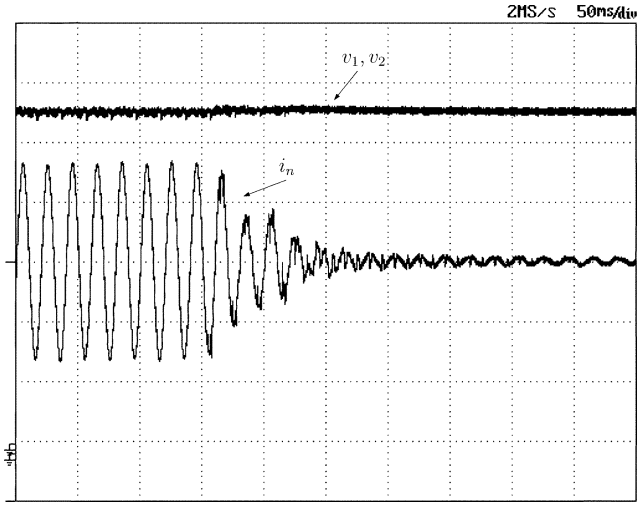

Fig. 17. Network current i_n and semibus dc voltages v_1 and v_2: From full nonlinear load to no load (19.2 A/div and 74.5 V/div, respectively).

Apart from the selected experiments collected in this section, a lot of numerical simulations, including mainly capacitive or inductive loads, have been carried out, showing the same good performance as it will be shown in the following. Furthermore, it is worth noting that several numerical simulations including loads that work as generators at some time periods[7] (thus imposing a negative active power flow to the source) have been carried out without problems. The voltage loop of the overall controller assures the active power balance, and after a transient, in steady state, the input to the AM modulator is negative, giving a current reference shifted π rad from the network voltage that the current loop tracks without difficulty.

Although the energy shaping loop is closed using the energy, the measured physical variables are the capacitor voltages v_1 and v_2, which are the meaningful electrical variables of the actual system. For this reason, these are the variables shown in the experimental plots. Note that these variables are directly related with D and E_c.

A. Active-Filter Operation With No Load

This section presents some results of the no-load operation of the active filter. Fig. 10 shows the network voltage and current and the semibus dc voltages. The rms value of the current is about 0.68 A, and its THD value is 6.8%. Then, the resulting active power consumed by the filter to cover its losses without compensating any load is about 0.15 kW. It is worth to note that the fundamental component of the current is in phase with the voltage ($\cos\phi = 1$), see Fig. 11. Therefore, almost no reactive power is consumed by the filter. The low figure of the PF is owed to the high value of the switching ripple with respect to the fundamental component of the current.

B. Active-Filter Operation With the Nonlinear Load

In this experiment, the diode rectifier described in Section IV.A is connected to the network. This nonlinear load does not have reactive power at the fundamental frequency; however, the active filter must work to compensate all the generated higher order current harmonics. Fig. 12 shows the current that appears with a good sinusoidal shape and is in phase with the grid voltage. This figure also shows the values

[7]This problem was established as a hard one by Depenbrock and Staudt [29].

of each semibus of the active-filter dc bus. As it can be seen in Fig. 13, the THD of the current is very low (0.6%), and the PF is 1.

C. Active-Filter Operation With the Linear Load

In this case, the capacitive–resistive load described in Section IV.A is used. Fig. 14 shows i_n, i_l, v_n, and v_1 (semibus dc voltage). As it can be seen, the mains current is a sinusoidal signal in phase with the network voltage.

Fig. 15 shows some details about i_n and the power characteristics at the network port. It can be observed that the current THD is 0.9% which is a very low value, thus confirming the sinusoidal shape of the current. Additionally, the PF and $\cos\phi$ are 1.

D. Active-Filter Transient Response

This section presents the results for the following experiments: 1) the full nonlinear load is connected to the network with the active filter in operation (Fig. 16) and 2) the full nonlinear load is disconnected from the network with the active filter in operation (Fig. 17).

In each case, the overshoot in the semibus dc voltages is almost imperceptible. Therefore, there is no problem with the maximum load variations expected in the system.

VI. Conclusion

The paper shows the design and implementation of a controller for a single-phase shunt active filter. The controller consists of an inner current control loop and an outer dc bus voltage control loop. The current reference for the inner control loop is built by passing the output of the voltage controller through an AM modulator that uses as a carrier a filtered version of the network voltage. Both the inner and outer controllers are based on the combination of feedforward and feedback control laws. This controller architecture allows one to obtain an almost perfect response both in transient and steady-state operation.

The inner current control loop that, as the experimental results show, perfectly shapes the network current is designed using a repetitive control approach. The high-gain loop injected by the repetitive controller at the fundamental and the harmonic frequencies of the network frequency plus the feedforward action guarantee the good tracking of the reference current and rejection of the high-order harmonics of the load current. Moreover, the feedforward path allows one to obtain the desired sinusoidal shape for the current quickly, in just one cycle, which is a clear improvement from previous controllers and permits one to assume that the network current is always a sinusoidal signal; therefore, a nice model for the dc bus voltage can be stated. This model is used to analytically design and tune a controller for the outer control loop which is in charge of assuring the power balance of the whole system. It is worth to remark that the combined effect of feedforward and feedback paths in this loop keeps the dc bus voltage mean value almost unchanged even in front of large transients.

As a conclusion, the proposed control scheme constitutes a step forward in the active-filter control area. Both the transient and steady-state behaviors are very good in the network current shape and active-filter semibus dc voltages.

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