AIRBORNE BISTATIC SAR RECEIVER WITH THE CAPABILITY OF USE DIFFERENT OPPORTUNITY TRANSMITTERS.

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ABSTRACT

This paper describes the design and construction of a bistatic SAR receiver suitable for airborne applications, using orbital SAR systems *(ENVISAT, ERS-2, RADARSAT, TerraSAR-X* among others) as opportunity transmitters. The challenge of this design is to reduce the required data throughput of the recorded data. This is achieved storing data only in the time intervals when scattered signal from the target area appears. The task of detecting this time intervals is performed in real time using a matched filter of the signal received directly from the SAR transmitter.

***Index Terms*—**SAR, bistatic radar, Programmable Logic Devices.

1. INTRODUCTION

In the last decades, Synthetic Aperture Radar (SAR) has developed into a standard tool for Earth Observation. While monostatic SAR can be considered a mature field, bistatic and multistatic configurations are opening new research lines, exploring the potential benefits of new geometries and exposing different scattering mechanisms. In this context, the Remote Sensing Laboratory (RSLab) at the Universitat Politècnica de Catalunya has developed a dual channel C-band bistatic receiver that uses the SAR systems onboard the ENVISAT and ERS-2 satellites as sources of opportunity, named SABRINA (SAR Bistatic Receiver for INterferometric Applications)[1]. This ground based system down converts the C-band signal to video band using a *home-grown* RF front end and samples the signal using an off-the-shelf PXI-based high speed digitizer.

Bistatic systems that use sources of opportunity have to overcome a series of synchronization challenges. One of these is the lack of an explicit PRF synchronism mechanism. The current SABRINA prototype addresses this lack of synchronism by acquiring continuously during a temporal window around the expected overpass time of the transmitter (which for ERS-2 and ENVISAT can be determined with less than 0.5 second error). PRF synchronism is recovered during post processing from one of the two channels, which is used to acquire a direct, line of sight, signal. For ERS-2 and ENVISAT's 16 MHz bandwidth signals this results in a sustained throughput of 40MS/s per channel that, restricted by the on-board memory of the digitizer, limits the acquisition length to approximately 8 seconds, which is more than required. However, new systems like RADARSAT-2, TerraSAR-X or the future Sentinel-1 will transmit signals with much larger bandwidth, requiring sampling rates above 200 MS/s, in which case the current acquisition strategy will not be feasible. Moreover, the development of the next SABRINA prototype aims at an Unmanned Airborne Vehicle (UAV) based system that will eliminate some of the geometric limitations associated to a ground based systems. Thus a new compact and light weight receiver needs to be developed that can sample and store high bandwidth bistatic signals in an efficient way.

This paper presents the design and construction of a bistatic SAR receiver suitable for UAV and able to meet the throughput requirements previously discussed. This is achieved saving the data obtained selecting the intervals of time where the information of the scattering of the target area appears. To accomplish this task it is necessary to implement a system which continuously synchronizes the receiver with the PRF of the SAR transmitted signal. Synchronism is recovered by matched-filtering the acquired signal in real-time, using a high density Programmable Logic Device (PLD) to parallelize the required signal processing.

Section 2 of this paper describes the architecture of the proposed SAR bistatic receiver, explaining each of its constitutive components. Then, Sections 3 and 4 describe the main subsystems, the RF front End and the acquisition system. Finally, conclusions are exposed in section 5.

2. SYSTEM DESCRIPTION

A general block diagram of the bistatic receiver is shown in Figure 1. This diagram describes the SAR receiver that is designed to be carried by an UAV.
The system has a set of antennas to receive the SAR signals. One antenna receives the direct path signal needed for synchronization, while the others receive the scattered signal in a polarimetric or interferometric configuration.

The RF Front-ends takes the RF signals and down-converts them to video-band after filtering and amplifying. A dual C- and X-band receiver will allow the reception of the signals transmitted by the aforementioned C-band SAR systems and TerraSAR-X.

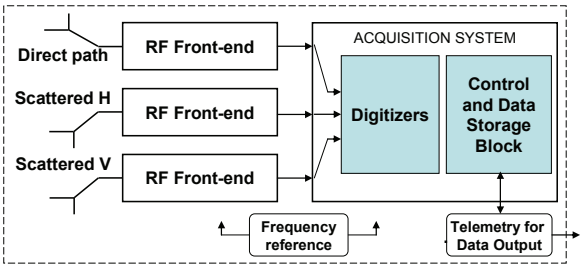

Figure 1. Simplified architectural diagram of SABRINA.

The final block of the receiver is the acquisition system that contains the digitizers and a Control and Data Storage block. This unit stores the received data in a non volatile memory. This acquisition system will be integrated at a Printed Circuit Board (PCB) level using ultra high density PLDs.

The data throughput required for the acquisition system storing in a continuous time basis three channels is given by:

$$\text{Throughput} = \text{Fs} \times \text{Nbits} \times 3 \quad (1)$$

In this way the Dthr required to store ENVISAT signals will be 1.44 Gbits/s. Then having the maximum ground range of interest (R_{gnd_max}) the length of segment (τ_{acq}) that are required to be stored is calculated as follows:

$$\tau_{acq} = \tau_{chirp} + \frac{\sin\theta + 1}{c} \times R_{gnd\_max} \quad (2)$$

Where τ_{chirp} is the duration of the chirp pulse, θ the incidence angle and c the speed of light. Then, the duty cycle of the adquisition, that is the percentage of lowering of the throughput can be calculated:

$$\text{Dutty\_cicle} = \tau_{acq} \times PRF \quad (3)$$

As an example, the duty cycle for storing ENVISAT data for a maximum ground range of 10Kms will be 0.12, and the required throughput lowered to 173Mbits/s.

3. RF FRONT END AND FREQUENCY REFERENCE BLOCK

The RF front-end implements three receive channels, taking the local oscillator signals from the frequency reference block. Figure 2 shows the double conversion superheterodyne architecture of each receiver channel. The receiver is divided in two blocks: a band dependent tunable RF module and a common IF module.

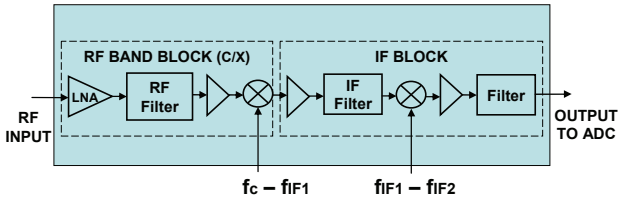

Figure 2. Receiver Channel Diagram.

The RF module consists of a LNA amplifier, a broadband image-reject filter, a second gain block and a frequency mixer that takes the received signal to f_{IF1}.

A first version of the RF module was constructed, implementing a C band Front-End.[3] This consist of a LNA, a home designed C-band coupled lines filter and a commercial RF amplifier. This module is capable of receive signals in a range of frequencies, allowing the module to receive signals from different opportunity transmitters. The characteristics and frequency ranges of operation of this module are summarized in table 1.

The local oscillators required for down conversion and sampling are derived from an Ultra Stable Oven Controlled Crystal Oscillator (OCXO). [2]

The IF module has a similar architecture to the RF module, with the addition of a final anti-aliasing filter. The IF frequency, f_{IF1}, has been set to 1409 MHz, to benefit from existing commercially available components at that frequency. The characteristics of the IF module are in table 2, and its hardware implementation is shown in figure 3. To avoid the calibration problems associated to phase and quadrature demodulation, the signal is shifted to a second IF frequency, $f_{IF2}=f_s \cdot 1.25$, selected so that it is aliased to a quarter of the sampling frequency.

Fc	LO =	Gain	BW	NF

(GHz)	Fc-Fif1 (GHz)	(dB)	(MHz)	(dB)
5.300 -5.4	3.891-3.991	21	568	3

Table 1. Parameters of C-band module.

Fif1 (MHz)	Fs (MHz)	Fif2 (MHz)	Gain (dB)	BWFif1 (Mhz)	NF
1409	40	50	17	109	3.4

Table 2. Parameters of IF converter block.

Figure 3. Photography of the SABRINA IF block.

4. ACQUISITION SYSTEM.

The acquisition system is divided in two main blocks, the digitizer block and the Control and Data storage Block

The digitizer contains a set of commercial A/D converters, digital buffers and the circuitry needed to implement them. In the digitizer each received channel is sampled with 12 bit of resolution at a rate of 40MS/s. However the system is capable of handling higher data rates.

The sampled signals are sent to the Control and Data storage Block. This block is implemented using a high density PLD, and a set of commercial non volatile massive data storage devices to save the received data. Also, it implements algorithms to synchronize the receiver with the SAR transmitted signals. A diagram of this block is shown in figure 4.

Frames of data received from the ADC are saved in a temporary FIFO memory. Also at the same time the PRF synchronism recovery block detects the time instants at which the chirp pulses are received using the direct path and send this information to the storage controller.

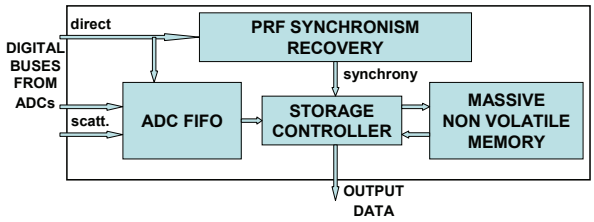

Figure 4. Control and Data Storage Block.

The storage controller, having the synchrony information determines which of the data stored in the FIFO is relevant and need to be recorded in the massive non volatile memory. This is a critical step required to reduce the throughput to the mass-storage device to a feasible rate.

The time when data is recorded is started by the reception of the direct path chirp, and ends after some time that depends on the maximum range of interest. The effective swath of the bistatic sensor is typically much smaller than that of the associated orbital SAR system. Therefore relatively small intervals of the sampled signals are needed to be recorded, and in this way a lower data throughput is achieved. In this way the system intelligently selects the length of the sampled data that contains signal scattered off the target area. This enables the use of flash memory devices of high capacity (4GB in an integrated circuit and more) and connected in parallel. This kind of memories could not be used if the data were been recorded in a continuous time basis.

- **PRF SYNCHRONISM RECOVERY BLOCK**

The PRF synchronism recovery is implemented applying a matched filter in real time to the direct path signal and detecting the peaks of power in its output. The matched filter is performed with the FFT algorithm, which is implemented in hardware in the PLD taking advantage of its velocity, logic density and size of its internal memory. A functional diagram of this block is exposed in Figure 5.

The FFT and IFFT blocks run concurrently inside the PLD. This device also instantiate internally RAM modules to handle the intermediate results and ROM modules to store the coefficients of the matched filter in the frequency domain.

For the computation of the FFT and IFFT the PLD works with a clock rate that is 2.5 times the sampling rate, allowing a continuous processing of all the input data [4],[5].

The length of the transforms is 8192; the length of the frame to be processed is 7153, and the length of the filter in time for ENVISAT is 1040 samples. Both transforms are implemented with a fixed integer representation of 16 bits, so the input data of 12 bits are appended to a 16 bit representation. After processing the IFFT, the final output of the processing is obtained of adding the overlapping sections of 2 consecutive processing pages that in the ENVISAT case is 1039 samples [4].

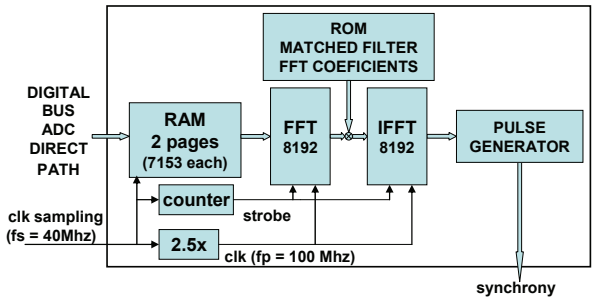

Figure 5. Functional Description of the PRF Synchronism Recovery block.

The detection of one peak is done frame by frame detecting the maximum output of the filter in a frame if it surpasses a threshold level. This threshold level varies adaptively depending on the power average of the filter output.

An acquisition system prototype is being constructed using a development tools, specifically using a development board with the FPGA Virtex 4 SX35. Also an ADC evaluation board is used. Currently, the PRF pulses generated can be used to trigger the PXI-based digitizer used in the ground based receiver. A plot of the input chirp and the generated trigger signal which is used by the PXI digitizer is shown in Figure 6.
The test signal is a pulsed chirp with duration of 26 microseconds, a bandwidth of 15.32 MHz, and a PRF of 1652.42Hz, emulating an ENVISAT signal, centered at an IF of 10MHz. In this case the trigger is predicted and will be activated just before the beginning of the next chirp, and the duration of the stored data depends on the settings of the PXI acquisition system.

7. CONCLUSIONS

The efficiency of the acquisition system for bistatic measures can be improved by saving the data just in the segments where relevant information of the scattered channels appears. During the design and construction of the SABRINA airborne bistatic receiver. The real time pulse compression was implemented in order to detect the PRF synchrony using a development environment.

The ability to reduce the throughput will be more decisive when working with system with SAR transmitters with higher bandwidths as in the case of the RADARSAT and TerraSAR-X systems.

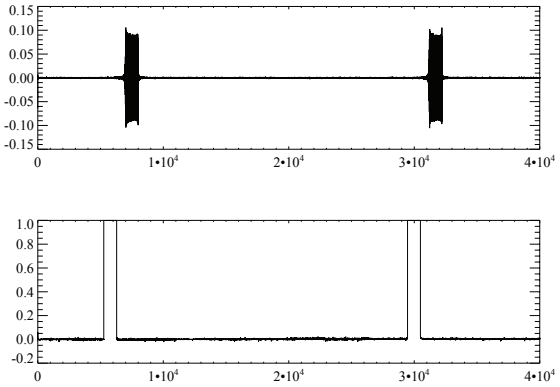

Figure 6. Input chirp signal and predicted PRF synchrony signal.

7. REFERENCES

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