A BPSK Superregenerative Receiver. Preliminary Results

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***Abstract*—This paper describes a bit-synchronous superregenerative receiver suitable for BPSK demodulation. The output of the superregenerative oscillator (SRO), which reproduces the phase information of the input signal, is directly sampled by a *D* flip flop clocked by a signal derived from the quench waveform. Analytical background on the response of the SRO to a BPSK modulated input is presented. A PSpice macromodel of the receiver is also provided, allowing simulation in the linear and logarithmic modes of operation. Simulation results confirm the feasibility of the described approach. Finally, a proof-of-concept superregenerative receiver, capable of receiving a BPSK modulated carrier at 27 MHz with preliminary experimental results is presented. The measured sensitivity of this receiver is –99.5 dBm for a bit error rate of 10^{-3}.**

I. INTRODUCTION

Superregenerative receivers are an attractive alternative for low-power wireless data links because of its reduced complexity, which is easily translated into low cost and low power consumption. Since its introduction in 1920 [1] this receiver has been successively refined. In the traditional approach, aimed at detecting OOK (on-off keying) modulated signals, a quench signal of considerably higher frequency than the actual data rate is used to effectively oversample the incoming RF signal. This generates RF pulses in the core of the receiver, the so-called superregenerative oscillator (SRO), whose envelope is dependent on the input RF amplitude in the vicinity of certain sensitivity windows, which are controlled by the quench signal. These RF pulses are detected by a rectifier circuit and low-pass filtered before a final comparator makes the decision on the received bit. In this approach, the equivalent bandwidth of the receiver turns out to be much larger than the bandwidth of the transmitted signal. As a consequence, the required input signal-to-noise ratio is higher than the one that is required for other kinds of receiver, such as the superheterodine receiver.

To overcome this drawback, a bit-synchronous quench signal may be used to generate a single oscillation pulse for each received bit [2]. In this approach, the envelope of the generated RF pulse is also dependent on the amplitude of the incoming RF signal. Again, envelope detection is used but the bit decision is done after each quench cycle instead of low-pass averaging the output of several quench cycles. In this approach, the sensitivity function of the receiver may operate as a matched filter, optimizing the noise performance of the receiver. Based on this idea, the receiver has also been used to detect direct-sequence spread-spectrum signals, where the quench signal is synchronous to the chip rate [3].

While it is known that the signal generated in the SRO preserves input phase information [4], [5] there has only been one known implementation [4] of a superregenerative receiver able to detect a BPSK modulated signal. In [4], the SRO is built around a transmission line oscillator where the transmission line supports two modes of oscillation depending on a control signal. In the first mode of oscillation, the generated signal has no dc component and is an exponentially growing oscillation whose phase is coherent with the phase of the received signal. At a given instant, the circuit topology is switched to generate the second oscillation mode which is characterized by producing a waveform consisting in the sum of *a*) a similar waveform whose frequency is twice the frequency of the first mode and *b*) an exponentially growing low frequency component whose amplitude is proportional to the cosine of the generated signal phase in the first topology at the moment of switching. Low-pass filtering the generated signals allows retrieving a dc component whose sign is used to decide the received bit in a BPSK modulation.

In this paper we make use of a SRO to demodulate BPSK signals using an alternative approach. Essentially, we make use of a conventional SRO to generate RF pulses where the input phase information is preserved. Once the generated signal achieves sufficient amplitude, the SRO signal, with the addition of the proper dc bias, is sampled by a conventional *D* flip-flop which, at the same time, decides the received bit. Taking this approach, the oscillator topology does not necessarily have to rely on a transmission (or delay) line, which may not be the best choice for all frequencies. Also, in this configuration, the active element does not have to be able to sustain oscillation at twice the input RF frequency, which may be cumbersome and power consuming. Finally, there is

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no need for the low-pass filter and the final comparator, since the flip-flop directly provides the decided bit.

The paper is organized as follows. Section II describes the underlying principle. Section III presents simulation results of the SRO while experimental results are presented in section IV. Concluding remarks are presented in section V.

II. Principle of Operation

Consider a SRO which is controlled by a quench signal that induces circuit instability at t=0. In the linear mode of operation, the output of this oscillator to an incoming RF pulse expressed as

$$v(t) = Vp_c(t)\cos(\omega t + \phi) \tag{1}$$

where $p_c(t)$ is the normalized impulse response of the pulse shaping filter of the transmitter, may be written as [5]

$$v_O(t) = VK|H(\omega)|p(t)\cos(\omega_O t + \phi + \arg(H(\omega))). \tag{2}$$

In the context of this paper, K may be considered an amplification constant, $H(\omega)$ is a bandpass function, $p(t)$ is a pulse, normalized to achieve $\max\{p(t)\}$=1 and ω_O is the natural oscillation frequency of the SRO. The reader is referred to [5] for an exact description of these terms and the influence that the quench shape has on them.

From (2), it turns out that the phase information ϕ is preserved in the output waveform of the SRO.

Next, consider a phase modulated input signal, expressed as

$$v(t) = V\sum_{m=-\infty}^{\infty} p_c(t-mT)\cos(\omega t + \phi_m). \tag{3}$$

The output of the SRO to this signal is given by

$$v_O(t) = VK|H(\omega)|\times \sum_{m=-\infty}^{\infty} p(t-mT)\cos(\omega_O(t-mT) + m\omega T + \phi_m + \arg(H(\omega))). \tag{4}$$

If the phase changes in the transmitted signal happen at instants that are integer multiples of the transmitter carrier period, i.e.

$$\omega T = 2N\pi, \tag{5}$$

equation (4) may be rewritten as

$$v_O(t) = VK|H(\omega)|\times \sum_{m=-\infty}^{\infty} p(t-mT)\cos(\omega_O(t-mT) + \phi_m + \arg(H(\omega))). \tag{6}$$

where it is clear that phase information is preserved.

In a BPSK transmission, ϕ_m is allowed to take only the values 0, π. Hence, the resulting modulation, sometimes called Phase-Reversal Keying (PRK), may also be viewed as a bipolar ASK transmission. In this case, since the SRO behaves as a linear (and variant) system, it is obvious that a sign reversal in the input signal causes a sign reversal in the output.

III. Superregenerative BPSK Receiver

From the previous results it follows that sampling $v_O(t)$ at any fixed offset τ from the start of each instability cycle produces a signal whose sign changes as ϕ_m changes. Obviously, there are certain optimum sampling points coinciding with the relative maxima or minima of $v_O(t)$.

To demonstrate this behavior, a PSpice macromodel of the SRO has been built (Fig. 1) and simulated. The lower block in Fig. 1 implements the time-varying conductance of the SRO, providing $G_a(t)$=$VCx(t)$ ($G_a(t)$ defined in [5]) while the soft

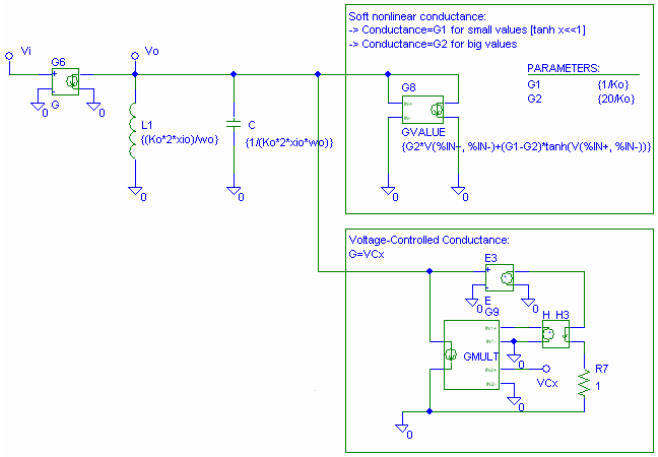

Figure 1. PSpice macromodel of the SRO.

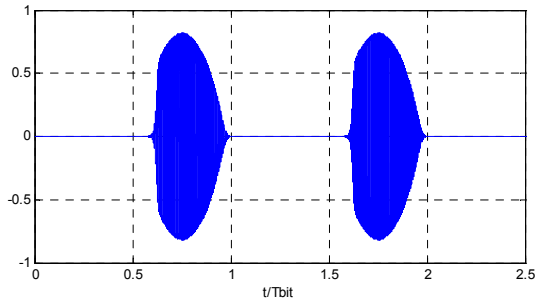

Figure 2. PSpice simulation showing the SRO waveform, $v_o(t)$, in the logarithmic mode of operation

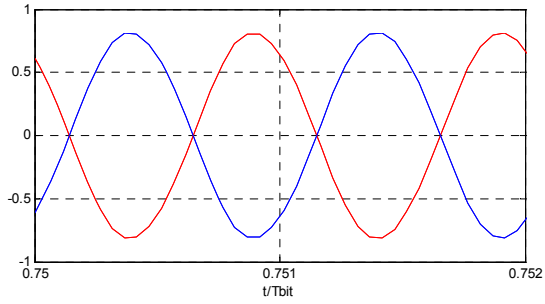

Figure 3. PSpice simulation. Detail of the SRO waveforms when transmitting "1" or "0".

nonlinearity (upper block in Fig. 1) limits the oscillator amplitude and allows to simulate the logarithmic mode of the SRO. The parameters *Ko*, *xio* and *wo* are, respectively, K_O, ξ_O and ω_O in [5].

A sketch of the simulated waveforms with PSpice is depicted in Fig. 2 and Fig. 3. Figure 2 depicts the SRO output operating in logarithmic mode during two bit periods while Fig. 3 shows a detail of the superimposed waveforms obtained when transmitting a "1" and a "0". From this, it is clear that phase information is also preserved despite operation in the logarithmic mode.

Note that, since, in general, there is no absolute phase reference, a differentially encoded BPSK modulation (DBPSK) should be used where, for instance, ϕ_m=0 if the *m*-th bit is equal to the previous one and ϕ_m=π otherwise.

IV. Experimental Results

A. Proof-of-concept implementation

To test the proposed idea in practice, a prototype superregenerative receiver at 27 MHz was designed, powered at 3 V (Fig. 4) and built from BFR93A transistors. It consists of a preamplifier, a SRO and a *D* flip-flop. The preamplifier is in a cascode configuration, which provides sufficient signal gain (around 20dB), presents suitable loading to the SRO and is able to provide sufficient (on the order of 40 dB) reverse attenuation. Some improvement is still to be expected by a proper input matching section.

The SRO is essentially a common-base Colpitts oscillator where the transistor is controlled by a quench sinusoidal signal with adjustable offset and amplitude. Oscillation frequency is controlled by *L* (560 nH), *C1* (56 pF) and *C2* (100 pF).

Sampling is achieved by a 74LV74A flip-flop, which is able to operate at clock frequencies well over 100 MHz. The SRO dc level is shifted appropriately for the *D* input to be able to detect signals. The SRO amplitude may be controlled by the quench signal to achieve sufficient amplitude, eventually operating clearly in the logarithmic mode. We have noted that the documented input signal levels for a 3 V supply (V_{ILow}=0.8 V and V_{IHigh}=2 V) may be reduced in practice. We have found that a 200 mVpp signal is sufficient to drive the *D* input.

B. Response to a BPSK modulation

We programmed an Agilent ESG-D 4431B generator to generate a BPSK modulated signal around 27.5 MHz. The data rate was set to 10 kbit/s and a rectangular pulse-forming filter was used. First, the ability of the SRO to generate pulses conserving phase information was tested. Figures 5 and 6 show the SRO output for input levels of –90 dBm and –100 dBm, respectively. These traces were obtained with 10 s persistence. While they can not be considered true eye-diagrams, these figures clearly show that phase information is preserved and suggest that the receiver might be able to perform reasonably well down to about –100 dBm.

It should be pointed out that these results were obtained in the logarithmic mode of operation. In this mode of operation, the overall circuit behavior is much more insensitive to variations in the quench signal than when operating in the linear mode. This is an advantage in front of superregenerative receivers designed for ASK detection, which are usually designed to operate near the linear mode because of the increased distance between the envelope of the SRO waveforms corresponding to a logical "0" or a logical "1".

C. Measured Bit Error Rate

Next, we investigated the behavior of the simple data recovery approach depicted in Fig. 4. The clock signal for the *D* flip flop is generated from the sinusoidal quench signal, which is squared by a comparator and delayed τ seconds to effectively sample the SRO signal at a relative maximum or minimum. To investigate the true sensitivity that may be achieved with the current receiver design, we set up a bit error rate (BER) test making use of a PN9 bit pattern. A graph of the measured BER as a function of the input signal power is given in Fig. 7. From this, it follows that the receiver sensitivity (corresponding to a BER=10^{-3}) is approximately –99.5dBm.

D. Discussion

The preceding results suggest that this novel receiver structure may be a viable alternative. Since the prototype implementation has been designed with the proof-of-concept objective in mind, improved performance is expected in an optimized version. With the current digital technology operating at several GHz clock frequencies, the described approach might be extended, at least, to 2.4 GHz band.

The proposed structure requires the flip flop to sample an RF signal centered at f_O (27 MHz in the described example) at a much lower sampling frequency f_S (10 KHz). Note that an error of T_O/8 (T_O =1/ f_O) in the sampling period reduces the sampled value by a factor 1/√2. The situation is similar when using a matched bandpass filter receiver [6]. For the aforementioned values, this translates into a 46 ppm accuracy, which is routinely achievable but requires paying attention to the design. However, it should be pointed out that the current design is bit-synchronous, lending itself to much higher data rates. Increasing the data rate up to f_O /200, which has proved to be feasible [2], would reduce the sampling accuracy requirement to 625 ppm.

On the other hand, while bit synchronization is implied in any communications system, a suitable synchronization method has to be outlined and the associated complexity has

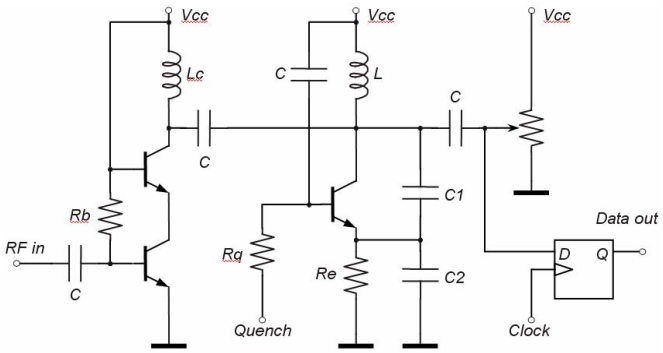

Figure 4. Schematic of the complete prototype receiver.

not to be overseen. Note that in the proposed design the bit and the quench frequency are the same with a delay τ between them. While the preceding experimental results are obtained making use of an external synchronization, a complete receiver design would make use of a delay-locked loop [3] that synchronizes τ near an optimum sampling point. The drift of τ with time would enable bit (or quench) frequency correction in an outer, slower, loop. Quality of the current sampling point could be obtained from an estimate of the BER or by making use of an analog sample and hold stage sampling the absolute value of the SRO output at the same time as the flip flop.

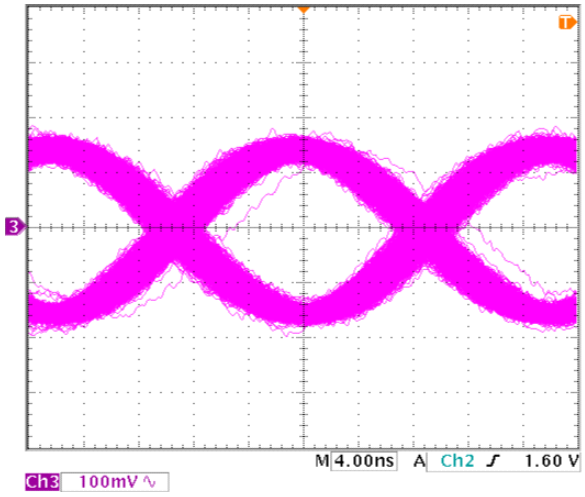

Figure 5. SRO output for a –90 dBm BPSK modulated signal.

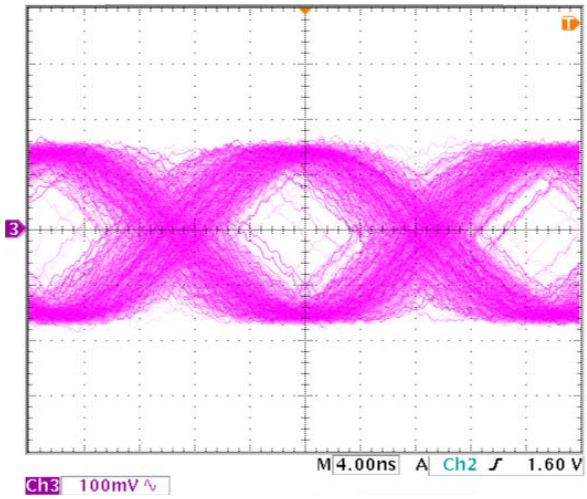

Figure 6. SRO output for a –100 dBm BPSK modulated signal.

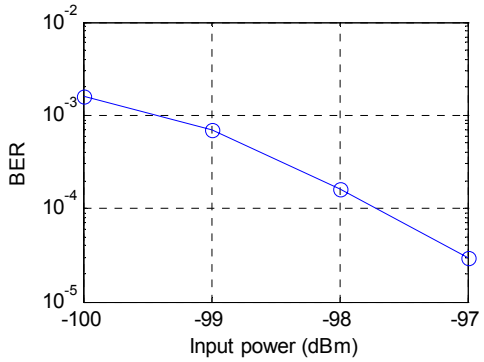

Figure 7. Measured Bit Error Rate vs. input signal power (dBm)

Finally, it is worth to point out that the SRO exhibits a certain sensitivity window around the time point where the oscillator becomes unstable. This means that any input signal that is contained outside this window is wasted. As a consequence, it is possible to transmit BPSK modulated pulses exhibiting a waveform that is matched to the receiver sensitivity window. This may reduce the average transmitted power by at least 7 dB [2] without increasing the BER.

V. Conclusions

This paper has described a superregenerative receiver for BPSK modulated signals. The receiver consists of three building blocks: a low noise and high isolation preamplifier, a SRO and a *D* flip flop. The receiver operation relies on the ability of the SRO to generate RF pulses where the input signal phase information is preserved. The circuit is allowed to operate in the logarithmic mode which is characterized by being much more robust than the linear mode of operation, the latter being the usual mode for ASK superregenerative receivers. In the logarithmic operation mode, the amplitude of the signal generated by the SRO is sufficient to be detected by a conventional *D* flip flop after applying a proper dc shift. The clock signal for the *D* flip flop is a squared and delayed version of the SRO quench signal. In contrast with other alternatives [4], the proposed design has some advantages. First, it does not rely on a specific oscillator topology, second it does not require the active element to sustain oscillation at twice the carrier frequency and, finally, it does not need a final lowpass filter.

Analytical background is provided in the linear operation mode, while logarithmic operation mode is confirmed by PSpice simulation and by a proof-of-concept implementation which operates at 27 MHz, achieving a sensitivity of –99.5 dBm for a bit error rate of 10^{-3}.

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