Low-power current-reused RF front-end based on optimized transformers topology

Ignacio Gil [a], Ignasi Cairó[b], Javier J. Sieiro[c] and José M. López-Villegas[c]

[a] Departament d'Enginyeria Electrònica, Universitat Politècnica de Catalunya, 08222 Colom 1, Terrassa (Barcelona), Spain

[b] EPSON Europe Electronics, Barcelona R&D Laboratory, Avda. Alcalde Barnils, 64-68 08190 Sant Cugat del Vallès (Barcelona), Spain

[c] Departament d'Electrònica, Universitat de Barcelona 08028 Martí i Franquès 1, planta 2 (Barcelona), Spain

Abstract

This paper discusses the design, analysis and performance of a 2.4 GHz fully integrated low-power current-reused receiver front-end implemented in 0.18 μm CMOS technology. The front-end is composed of a single-to-differential low-noise amplifier (LNA), using high-Q differential transformers and inductors and a coupled switching mixer stage. The mixer transconductor and LNA share the same DC current. Measurements of performance show a conversion gain of 28.5 dB, noise figure of 6.6 dB, 1 dB compression point of −32.8 dBm and IIP3 of −23.3 dBm at a 250 kHz intermediate frequency, while dissipating 1.45 mA from a 1.2 V supply.

Keywords: CMOS; Low-noise amplifier; Mixer; Front-end; Low-power consumption; Differential transformer

1. Introduction

Trends in current communication transceivers involve low-power, low-cost and highly integrated circuits. Recently, due to emerging commercial wireless applications, much effort has been devoted to high-frequency low-power consumption RF CMOS solutions, in order to lengthen battery lifetime [1], [2] and [3]. Several applications have been developed near the 2.4 GHz band, such as the IEEE 802.15.4 standard, Bluetooth and IEEE 802.11b. The RF front-end sensitivity is determined by low-noise amplifier (LNA) performance, whereas the mixer stage determines the dynamic range

of most communication systems due to intermodulation distortion [4]. Optimizing the LNA involves some tradeoffs between gain, noise figure (NF), linearity and power consumption [5]. The LNA block is analyzed fully in the literature, and straightforward figures of merit (*FoMs*) have been given as

(1)

$$FoM_{LNA} = \frac{G\,IIP3\,f}{(NF-1)P}$$

where *G* is the LNA's gain, *IIP3* the input-referred third-order intercept point, *P* the DC dissipated power and *f* the operating frequency. The evolution of a defined *FoM* for CMOS LNAs increases almost linearly with $1/L_{\min}$ (inversely with the minimum gate length). This implies that in a rough way the *FoM* is linearly dependent on f_T, since for short channel regimes f_T is also inversely dependent on $L_{\min}$ [6]. Assuming [1] the improvement in performance of LNAs, including low-power behaviour, mainly comes from scaling down the technology. Moreover, from the design point of view, the most suitable way to reduce power is by implementing a current reuse strategy [7] or by means of high-quality factor passives, since device gain is typically linearly dependent on *Q*.

However, particularly for zero-intermediate frequency (IF) or low-IF receivers, the noise of the mixer is also very important, since it can affect the sensitivity of the receiver [8]. Two main approaches can be adopted when considering power device constraints: passive or active mixers. Although the passive mixers have no DC consumption at all and present high linearity, they have no power gain and, therefore, losses involve noise system degradation. This effect can be reduced by means of a preamplifier stage or a two-LNA configuration with an increase in the DC current. The latter approach is typically used by implementing the Gilbert cell (GC) topology, as this is a good compromise in terms of gain, noise, linearity and dissipated power [9]. For a two-LNA configuration, current reuse strategies have also been successfully introduced as a power-saving solution [7] and [10]. Nevertheless, all the structures based on the GC suffer from the need for high-voltage headroom, which is incompatible with low-voltage applications, usually related to low-power applications where a battery is needed. Recently, progress has been made by combining LC-tanks with the GC [11] or using the bulk transconductance, g_{mb}, to achieve some gain. RF or LO signals are injected through the bulk with the result of saving a stacked transistor level [12] and [13]. However, due to g_{mb}, a low gain can be provided. In order to overcome the tradeoff between gain and consumption, we propose a mixed solution based on a combination of a current-reused topology and the implementation of LC tanks based on optimized differential transformers with high-quality factors [14]. Firstly, by stacking a

transconductance mixer block and LNA in a current-reused implementation, the voltage headroom can be reduced. Secondly, the inclusion of high-*Q* passives, such as inductors, implies good chokes and loads and, therefore, the stacking of stages and the gain of the device can be optimized with no extra power consumption requirement.

In this work, an RF front-end at 2.4 GHz based on a fully integrated CMOS single-ended to differential LNA and mixer is presented. The front-end is designed for high gain together with low-power consumption and voltage supply. The aim of the device is to provide good gain and noise performance with a simultaneous low-power consumption level, in order to be integrated into a low-IF architecture to form a low-voltage low-power receiver.

The paper is organized as follows. Section 2 describes the front-end blocks of the LNA and mixer designs and also gives a detailed description of the high-Q LC tanks used. In Section 3, experimental results are presented and discussed. Finally, Section 4 summarizes the main conclusions of this work.

2. Design of the proposed front-end

Fig. 1 and Fig. 2 depict the configuration of the proposed front-end (including LNA and mixer), as well as the LNA small-signal equivalent circuit. The topology is based on a single-ended to differential LNA in a common degenerated inductor source and a double balanced GC with a folded switching stage. The detailed design strategy is explained below, including the high-performance differential transformers used in order to increase the quality factor of the LC-tank resonances. The electrical simulations were developed using Agilent Advanced Design System (ADS) and the electromagnetic simulations (used for integrated inductors and transformers) were performed with Agilent Momentum.

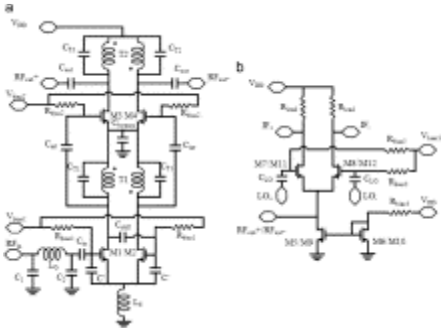

Fig. 1. Small-signal equivalent circuit of the LNA.

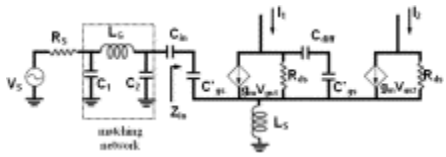

Fig. 2. Schematic of the merged current-reused LNA and I/Q-mixers.

2.1. LNA and mixer transconductance stage

The central part of Fig. 1 shows the schematic of the LNA block. The received RF input signal, RF_{in}, goes through a 50 Ω π-matching network formed by capacitors C_1, C_2 and inductor L_G, followed by a decoupling capacitor C_{in} and a pseudo-differential configuration formed by transistor pair $M1$–$M2$. In order to prevent damage to external pads from electrostatic discharges, C_1 and C_2 actually correspond to the equivalent capacitances of ESD protection diodes. Matching is complemented with additional capacitance, C', and degeneration inductor, L_S. C' enables us to obtain a noise figure equal to the minimum noise figure of a given LNA topology under very low power consumption [15]. L_S is used to increase the impedance at the $M1$–$M2$ source with the aim of avoiding gain and phase-balanced degradation due to parasitic effects, and to obtain a 180° phase difference between the branches . In fact, the parameters L_S and C' must be chosen carefully once the power constraint has been determined. A large C' degrades the effective cut-off frequency of the transistor (in comparison to a transistor with no additional capacitance) and, hence, the gain of the LNA is reduced. However, an overestimated degeneration inductor will increase the minimum noise figure. In order to obtain a fully differential RF amplified signal in $M1$ and $M2$ drain, a bypass capacitor, C_{diff}, copies the signal between the two nodes by preserving the DC component [16]. C_{diff} is built differentially in order to preserve circuit symmetry. In fact, the value of C_{diff} must be calculated carefully, since it has a clear impact in the input impedance, Z_{in}, defined in Fig. 1 and the following equations:

(2)

$$Z_{in} = \frac{1}{j\omega C'_{gs}} + \frac{(L_S \| C'') \left[1 + \frac{\omega_T}{j\omega}\right]}{1 + g_m \left[1 - \frac{C''}{C_{diff}}\right](L_S \| C'')}$$

(3)

$$L_S \| C'' = \frac{j\omega L_S}{1 - \omega^2 L_S C''}$$

(4)

$$C'' = \frac{C_{diff} C'_{gs}}{C_{diff} + C'_{gs}}$$

(5)

$$C'_{gs} = C_{gs} + C'$$

(6)

$$\omega_T = \frac{g_m}{C'_{gs}}$$

If C_{diff} is neglected, the conventional cascode LNA input impedance is obtained as follows:

(7)

$$Z_{in}|_{C_{diff}=0} = \frac{1}{j\omega C'_{gs}} + j\omega L_S + \omega_T L_S$$

A second common-source transistor pair *M*3–*M*4 is stacked and the pair receives an RF signal by means of two decoupling capacitances, C_{int}. An LC tank formed of an optimized differential transformer, *T*1, in combination with two shunt capacitors C_{T1}, as shown in Fig. 3, performs as an improved RF-choke. The tank resonates together with C_{int} and the input capacitances of *M*3 and *M*4. Thanks to the resonance, overall NF is decreased since the gain of the input stage is enhanced and the noise contribution of *M*3–*M*4 is minimized. This structure reduces common-mode noise since the up- and down-conversion even harmonics are also suppressed.

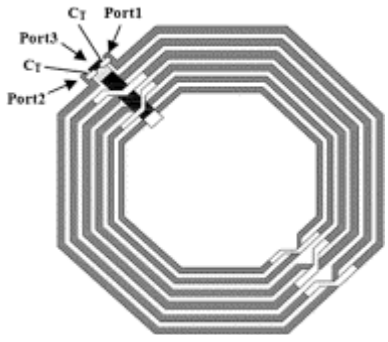

Fig. 3. Layout of the differential 3-port LC-tank. Device presents octagonal topology and it is formed of 2 capacitors, C_T, located compactly way between transformer ports 1–3 and 2–3. Both input and output ports are located in the same corner in order to improve routing.

The insertion of extremely high quality passives is the key to achieve good performance, not only from the power-consumption point of view, but also in order to have excellent chokes for reducing RF leakage between *M*3–*M*4 sources and *M*1–*M*2 drains. The differential voltage gain at the tank's resonance is given by

(8)

$$A_V = -\frac{2g_m/(1-\omega^2 L_S C'_{gs})}{j\omega C'' + (2/R_L)}$$

This equation depends on C_{diff}. In fact, at resonance, the impedance of the transformer is reduced to a real load, R_L. Impedance behaviour equivalent to that of a shunt configuration formed by C'' and half of the transformer appears in the gain, which indicates that the tank's resonance is dependent on C_{diff}. Eq. [8] also indicates that the designer must take into account the product $L_S C'_{gs}$, since it can generate a resonance at $f=1/(L_S C'_{gs})^{1/2}$, which could potentially lead to oscillations and circuit instability. Finally, C_{diff} changes phase with regard to the input node. In order to achieve good performance of the circuit, C_{diff} must be larger than C'_{gs} (e.g., $C_{diff} \approx 10 C'_{gs}$). The following equation gives the correction terms with regard to the typical LNA case [7]:

(9)

$$Z_{in}|_{C_{diff} \gg C'_{gs}} \approx \frac{1}{j\omega C'_{gs}} + j\omega L_S \frac{1-\omega^2 L_S C'_{gs} - g_m \omega_T L_S}{(1-\omega^2 L_S C'_{gs})^2 + (g_m \omega_T L_S)^2} + \omega_T L_S \frac{1}{(1-\omega^2 L_S C'_{gs})^2 + (g_m \omega_T L_S)^2}$$

Regarding NF, conventional noise matching has been developed with the result of similar NF performance in comparison with classical LNA topologies. A large bypass capacitor, C_{bypass}, connected to the *M*3–*M*4 sources provides a reliable AC ground. A second LC tank (formed of a differential transformer, *T*2, and capacitors C_{T2}) is designed as an improved RF-choke and short for common mode in order to resonate at the desired frequency (2.4 GHz at ISM-band) in combination with the output capacitance, C_{out}. In that case the high quality of the passives leads to an optimized load, which enhances the device gain with no extra power dissipation. Finally, the R_{bias1} and R_{bias2} resistor network is included, to bias the transistor pair stages.

The stacked *M*3–*M*4 stage could be reused as the mixer transconductance stage of a double balanced GC in a full receiver front-end. This merged structure reduces DC current with a significant power consumption saving for the overall implementation in a way similar to that in Ref. [8] Therefore, the *M*1 and *M*3 branches share the same bias current (which takes the same value as in the symmetric *M*2 and *M*4 branches).

2.2. Mixer switching stage

In order to avoid a lack of voltage headroom due to the excess of vertical transistor stages, a folded topology for the mixer switching stage has been implemented. These stages are comprised of transistors *M*7–*M*8 and the biasing mirror formed by *M*5–*M*6 (and their symmetrical counterparts *M*11–*M*12; *M*9–*M*10). In terms of dissipated power, the LO switching stage contributes less than a tenth of the overall DC current consumption. Therefore, this topology is suitable from a power point of view. In fact, thanks to an optimized design of passive elements [18], this current-reused topology is the key to reducing overall power consumption.

2.3. Inductors and differential transformer LC-tanks

It is well-known that the quality factor *Q* of passives, mainly inductors and transformers, determines the final achievable performance of RF receivers [19]. As shown in Eq. [2], L_G and L_S directly affect the achievable NF, gain and power consumption. Due to the fact that both inductors are in the single-ended signal path coming from the antenna, they have been laid out as square spirals. To minimize the loss associated with L_G and L_S, the geometries have been computed by following a systematic optimization method [18] with the help of an electromagnetic simulator based on the method of moments (Agilent Momentum). The procedure is based on computing the ohmic loss and the loss associated with the Eddy currents, but maintaining the inductance value and the available area as constraints. The resulting geometry is a tapered spiral with narrower strips in the inner turns (higher loss due to Eddy currents) and wider trips in the external ones (loss dominated by conduction current). For L_G (=10 nH) and L_S (=1 nH), on the left in Fig. 4, the measured Q_{peak} values are 18 and 33, respectively.

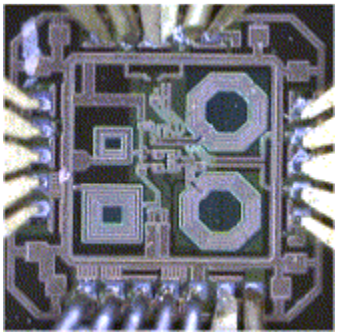

Fig. 4. Layout of the designed LNA and mixer.

The transformer LC-tank has three functions. First, it provides a way for reusing the bias current for the LNA and mixer. Second, it must be able to force a short impedance

condition for the common-mode signal and, therefore, the even harmonics at the output of the LNA are suppressed. Third, it should offer a high-impedance condition (high gain) for the differential mode. Such behaviour can be accomplished when the magnetic coupling factor k between transformer windings is close to −1 (inverter configuration) in combination with a high-quality factor of the passive component. The high-impedance condition can be set through the equivalent parallel resonance. Thus, in such cases, the quality factor will be evaluated using the derivative of the phase θ of the LC-tank at its resonance frequency ω_0, i.e.,

(10)

$$Q = \left| \frac{\omega}{2} \frac{d\theta}{d\omega} \right|_{\omega=\omega_0} = \left| \frac{\omega}{2} \frac{d}{d\omega} \left(\tan^{-1} \left(\frac{imag(Y_{diff})}{real(Y_{diff})} \right) \right) \right|_{\omega=\omega_0}$$

where Y_{diff} represents the differential admittance of the load connected at the drain outputs of transistors $M1$–$M2$ or $M3$–$M4$.

To achieve this required functionality, the inverter transformer LC-tank must be carefully designed. In order to minimize the distance to the transistor drain, the layout is octagonal, as shown in Fig. 3, with the 3 ports located in the same corner forming a 45° angle. Notice that the shunt capacitors C_T that fix the resonance frequency are placed just at the output of the ports. In this way, we avoid the parasitic magnetic couplings due to additional routing traces. The coupling between windings can be maximized using the minimum separation between metal strips and interleaving the metals forming the two coils as much as possible. Additionally, the high-impedance condition for the differential mode can be obtained by increasing Q. Therefore, the former systematic optimization procedure can be applied (notice that both transformers are also tapered structures). Using Eq. [10], the simulated Q value is 22.5 at the frequency of interest, as shown in Fig. 5. The impact of the process variations on the performance has been estimated in a ±6% at resonance frequency, which can potentially degrade the effective Q at resonance frequency. A possible low-cost solution is to introduce a capacitor array, in order to tune these deviations.

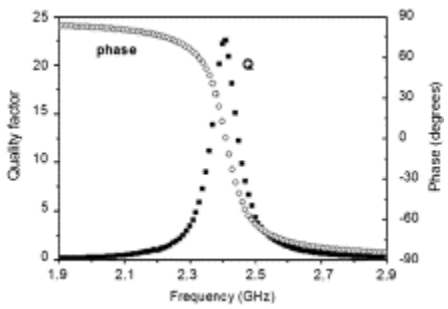

Fig. 5. Simulated phase variation and quality factor for the isolated and coupled configurations when a differential signal drives the input ports.

In order to minimize the overall area of the circuit, the two transformer LC-tanks must be placed as close as possible to each other. However, the magnetic and electric coupling between them can modify the resonance frequency of the structures, detuning the high-impedance condition for the differential signal. The variation in the resonance can be taken as a figure of merit for evaluating the correct minimum distance between tanks that can be compensated with C_{T1} and C_{T2}. Fig. 5 shows the simulated phase variation and the quality factor for the coupled configuration when a differential signal drives the input ports of transformers *T*1 and *T*2 simultaneously.

3. Experimental results

The fully integrated single-ended to differential LNA and mixer has been constructed in 0.18 μm CMOS technology. Fig. 4 shows the microphotograph of the device. The total chip area is 1.9×1.9 mm^2 including pads and ESD protection diodes. On-wafer probing has been performed with a Cascade Microtech Probe Station 12,000, whereas an R&S FSQ26 (including noise figure extraction software, *FS–K*3) power spectrum analyzer has been used to characterize conversion gain, noise figure, compression and linearity. An output DC block together with an external buffer (voltage follower) has been used in order to test the circuit. The aim of this extra testing circuitry is to filter the bias voltage and to present high-input impedance in order to perform measurements by means of the spectrum analyzer. The S11 parameter has been measured using an R&S ZVM vector network analyzer. As can be seen in Fig. 6, good input matching level has been achieved (S11=−12.5 dB at 2.4 GHz). Fig. 7 shows the RF front-end conversion gain and NF obtained vs. local oscillator port power. As can be observed, a gain of 28.5 dB is obtained in the central frequency band for optimum LO power of the order of −3 dBm, whereas NF corresponds to 6.6 dB in the IF band (i.e., 250 kHz), after de-embedding the buffer impact. In order to demonstrate the performance of the circuit at very low power consumption, Fig. 8 depicts the conversion gain in terms of the intermediate frequency, for a lower value of LO power (=−10 dBm). In this case, the conversion gain of the LNA+mixer implementation is higher than 20 dB in the IF frequency range, 250 kHz–1 MHz. Fig. 9 illustrates the measured nonlinearity effects, such as the 1 dB compression point (CP1 dB) and the input third-order intercept point (IIP3) of the RF front-end. The experimental CP1 dB corresponds to −32.8 dBm

whereas −23.3 dBm IIP3 is obtained by performing a two-tone intermodulation test with equal power levels at 2.4 GHz±10 kHz (after de-embedding the buffer impact). Fig. 10 shows the leakage behaviour between ports. Specifically, isolation levels of −47 dB from RF–IF, −52 dB from LO–RF and −31 dB from LO–IF are achieved, including the buffer impact (which corresponds to an attenuation of −20 dB at 2.4 GHz), thus maintaining a good level and avoiding undesired signals. In fact, in the baseband stage, a channel filter will reject those undesired signals. The total current consumption of the proposed LNA is 1.45 mA from a 1.2 V supply, with a resulting DC power dissipation of 1.74 mW. Table 1 summarizes the performance of the proposed current-reused front-end in comparison with previous reported works. Taking into account that the matching network is implemented on chip with ESD diodes, the presented RF front-end performance shows an excellent balance among gain, noise, linearity and consumption. The low value of the noise figure is remarkable inspite of the impact of the phase noise from the VCO and the low IF frequency of 250 kHz where the theoretical main noise source is the flicker contribution; however, in the implemented technology, the flicker corner is below 250 kHz. Higher conversion gain was obtained in comparison with other topologies (Table 1), especially with regard to structures working at similar power consumption levels. The linearity of the device is determined by the intrinsic limitation between the dynamic range and the power dissipation, since for a fixed value of IIP3 it is not possible to decrease power consumption below a specific threshold. Inspite of the fact that the device topology includes the ESD nonlinearity effects, the IIP3 as well as the CP1dB are at a good level (similar to those in previous works). In order to evaluate the real impact of the ESD diodes on the linearity of the receiver an IIP3 simulation of the receiver with and without ESD diodes (using equivalent capacitance) has been performed. A 6 dB degradation of the linearity of the RF front-end is obtained.

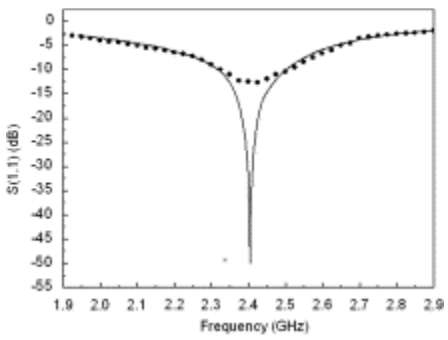

Fig. 6. Simulated (thin line) and measured (dotted line) device return losses.

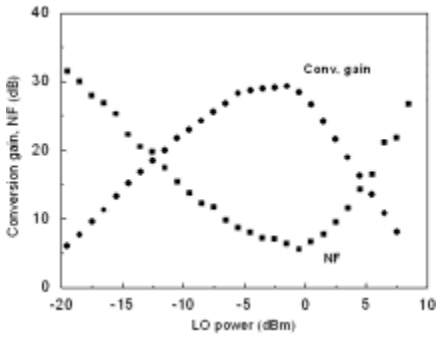

Fig. 7. Measured conversion gain and NF vs. local oscillator power (IF=250 kHz).

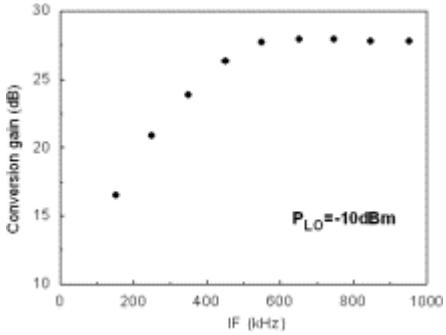

Fig. 8. Measured conversion gain vs. IF band at P_{LO}=−10 dBm.

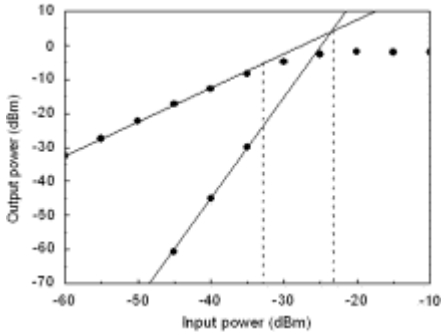

Fig. 9. Measured 1 dB compression point and input third-order intermodulation product (IF=250 kHz).

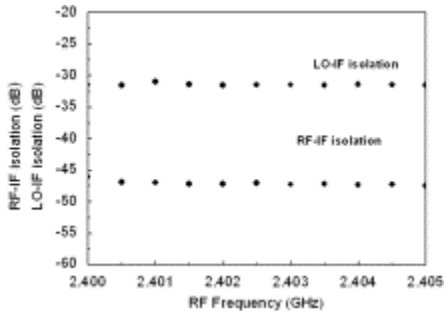

Fig. 10. Measured leakage level between RF–IF and LO–IF ports.

Table 1.

Performance comparison for analog RF front-ends.

	[20][a]	**[21]**	**[22]**	**[23]**	**This work**
Technology	0.18 μm	0.18 μm	0.35 μm	0.18 μm	0.18 μm
	CMOS	CMOS	CMOS	CMOS	CMOS
Frequency (GHz)	2.4	2.4	2.1	2.4	2.4
Conversion gain (dB)	15.3	16	23	12	28.5
Noise figure (dB)	10.1 at 10 MHz IF LO=−4 dBm	<24 at 0.5 MHz IF	3.2 at 5 MHz IF	7.3 at 1 MHz IF LO=0 dBm	6.6 at 250 kHz IF LO=−3 dBm
IIP3 (dBm)	–	−11	>−3	−8	−23.3
CP1 dB(dBm)	−31	−18	–	−18	−32.8
V supply (V)	1.0	1.8	2.7	1.8	1.2
Power (mW)	0.5	1.1	21.6	1.8	1.7

[a] Performance of proposed front-end based on single-balanced mixers.

4. Conclusions

A low-power single-ended to differential LNA and mixer with current-reused topology based on 0.18 μm CMOS technology is designed. Optimized LC tank chokes, loads and inductors have been introduced to minimize power consumption and parasitic influences. The layouts of the passives have been improved in terms of losses (ohmic and magnetically induced) and routing as well. It has been demonstrated that the

power consumption of the RF front-end can be reduced by means of high-Q resonators due to the possibility of implementing efficient stage stacking. The design reduces the transconductance mixer block consumption, since this stage uses the same DC current as the LNA. The device exhibits the following performance at IF band (250 kHz): 28.5 dB gain, 6.6 dB NF, −32.8 dBm CP1 dB and −23.3 dBm IIP3, while dissipating a DC power of 1.74 mW from a 1.2 V supply. To the best of the authors' knowledge, this is an improvement on previously reported performance, especially in terms of NF and gain, achieved by maintaining the IIP3 value.

Acknowledgements

This work has been partially supported by the Spanish Ministerio de Ciencia e Innovación under projects TEC2009-09994 and the AGAUR of the Generalitat de Catalunya (2009SGR-1425).

References

[1] H.-H. Hsieh and L.-H. Lu, A CMOS 5-GHz micro-power LNA, *IEEE Radio Frequency Integrated Circuits Symposium* (2005), pp. 31–34.

[2] T.-K. Nguyen, S.-K. Han and S.-G. Lee, Ultra-low-power 2.4 GHz image-rejection low-noise amplifier, *Electronics Letters* (2005), pp. 842–843.

[3] Y.S. Wang and L.-H. Lu, 5.7 GHz low-power variable-gain LNA in 0.18 μm CMOS, *Electronics Letters* (2005), pp. 66–68.

[4] B. Razavi, RF Microelectronics, Prentice Hall PTR (1998).

[5] T.-K. Nguyen, C.-H. Kim, G.-J. Ihm, M.-S. Yang and S.-G. Lee, CMOS low-noise amplifier design optimization techniques, *IEEE Transactions on Microwave Theory and Techniques* (2004), pp. 1433–1442.

[6] R. Brederlow, W. Weber, J. Saurerer, S. Donnay, P. Wambacq and M. Vertregt, A mixed-signal design roadmap, *IEEE Design and Test of Computers* (2001), pp. 34–46.

[7] A.N. Karanicolas, A 2.7-V 900-MHz CMOS LNA and mixer, *IEEE Journal of Solid-State Circuits* (1996), pp. 1939–1944.

[8] H. Darabi and A.A. Abidi, Noise in RF-CMOS mixers: a simple physical model, *IEEE Transactions on Solid-State Circuits* (2000), pp. 15–25.

[9] T.H. Lee, The Design of CMOS Radio Frequency Integrated Circuits, Cambridge University Press (1998).

[10] M.-F. Huang, S.-Y. Lee, C. J. Kuo, A CMOS even harmonic mixer with current reuse for low power applications, in: Proceedings of the 2004 International Symposium on Low Power Electronics and Design, pp. 290–295.

[11] C.-C. Tang, W.-S. Lu, L.-D. Van and W.-S. Feng, A 2.4-GHz CMOS down-conversion doubly balanced mixer with low supply voltage, *IEEE International Symposium on Circuits and Systems ISCAS* (2001), pp. 794–797.

[12] G. Kathiresan and C. Toumazou, A low voltage bulk driven downconversion mixer core, *IEEE International Symposium on Circuits and Systems ISCAS* (1999), pp. 598–601.

[13] M.J. Deen, R. Murji, A. Fakhr, N. Jafferali and W.L. Ngan, Low-power CMOS integrated circuits for radio frequency applications, *IEEE Proceedings on Circuits, Devices and Systems* (2005), pp. 509–522.

[14] I. Gil, I. Cairo and J.J. Sieiro, Low-power single-to-differential LNA at S-band based on optimised transformer topology and integrated ESD, *Electronics Letters* (2008), pp. 198–199.

[15] P. Andreani and H. Sjoland, Noise optimization of an inductively degenerated CMOS low noise amplifier, *IEEE Transactions on Circuits Systems II, Analog and Digital Signal Process* (2001), pp. 835–841.

[16] M.K. Raja, T.T.C. Boon, K.N. Kumar and W.S. Jau, A fully integrated variable gain 5.75-GHz LNA with no chip active balun for WLAN, *IEEE Radio Frequency Integrated Circuits Symposium* (2003), pp. 439–442.

[17] T. Song, H.-S. Oh, S.-H. Baek, S. Hong and E. Yoon, A 2.4-GHz sub-mW CMOS current-reused receiver front-end for wireless sensor network, *IEEE Microwave and Wireless Components Letters* (2006), pp. 206–208.

[18] J.M. López-Villegas, J. Samitier, C. Cané, P. Losantos and J. Bausells, Improvement of the quality factor of RF integrated inductors by layout optimization, *IEEE Transactions on Microwave Theory and Techniques* (2000), pp. 76–83.

[19] Q. Huang, F. Piazza, P. Orsatti and T. Ohguro, The impact of scaling down to deep submicron on CMOS RF circuits, *IEEE Journal of Solid-State Circuits* (1998), pp. 1023–1036.

[20] T. Song, H.-S. Oh, E. Yoon and S. Hong, A low-power 2.4-GHz current-reused receiver front-end and frequency source for wireless sensor network, *IEEE Journal of Solid-State Circuits* (2007), pp. 1012–1022.

[21] H.J. Bergveld, K.M.M. van Kaam, D.M.W. Leenaerts, K.J.P. Philips, A.W.P. Vaassen and G. Wetzker, A low-power highly digitized receiver for 2.4-GHz-band GFSK applications, *IEEE Radio Frequency Integrated Circuits Symposium* (2004), pp. 347–350.

[22] H. Sjöland, A. Karimi-Sanjaani and A.A. Abidi, A merged CMOS LNA and mixer for a WCDMA receiver, *IEEE Journal of Solid-State Circuits* (2003), pp. 1045–1050.

[23] T.-K. Nguyen, V. Krizhanovskii, J. Lee, S.-K. Han, S.-G. Lee, N.-S. Kim and C.-S. Pyo, A low-power RF direct-conversion receiver/transmitter for 2.4-GHz-band IEEE 802.15.4 standard in 0.18-μm CMOS technology, *IEEE Transactions on Microwave Theory and Techniques* (2006), pp. 4062–4071

Vitae

Ignacio Gil received degrees in Physics and Electronics Engineering in 2000 and 2003, respectively, and his Ph.D. in 2007 from the Universitat Autònoma de Barcelona, Spain.

From 2003 to 2008 he was Assistant Lecturer in Electronics and a researcher with the RF-Microwave Group in the Electronics Engineering Department, Universitat Autonòma de Barcelona. From 2006 to 2008 he worked for Epson Europe Electronics GmbH as RF Engineer, where he developed high-performance integrated RF CMOS transceivers design. In 2008 he joined the Electronics Engineering Department, Universitat Politècnica de Catalunya, Spain as lecturer. His research interests are active and passive RF/microwave devices and metamaterials.

Ignasi Cairó received degrees in Electronics and Telecommunications from the Technical University of Catalonia, Barcelona, Spain, in 1988 and 1992, respectively.

He joined Circutor group in 1995, where he was involved in industrial power electronics and RFID systems. From 1999 to 2003 he worked for Philips Semiconductors. In Nijmegen, the Netherlands, he developed GSM power amplifiers using BiCMOS processes and later in San Jose, California, he was engaged in the development of WLAN transceivers. Since 2003 he has been with Epson Electronics GmbH in Barcelona. His research interests include low-power radio electronics, miniature antenna integration and wireless systems.

Javier Jose Sieiro Cordoba received his degree in Physics, M.Sc. in electronic engineering and Ph.D. in physics from the University of Barcelona, Barcelona, Spain, in 1995, 1999, and 2001, respectively. From 2002 to 2003, he was a member of the Electronic Components Technology and Materials (ECTM) Group, Delft University of Technology, Delft, the Netherlands, where he was involved in modelling passive components and designing RFIC circuits. Since 2003, he has been with the Department of Electronics, University of Barcelona, where he is currently an Associate Lecturer.

José María López-Villegas graduated in Physics in 1985 and received his Ph.D. in Physics in 1990, both from the University of Barcelona. From 1985 to 1987 he was a visiting research fellow at the “Laboratoire d’Electronic Philips, LEP, Paris, France” and worked on the electrical characterization of III–V compound semiconductor devices. In 1990 he joined the Electronics Department at the University of Barcelona, first as Assistant Lecturer and then as a permanent “Professor Titular”, where he is currently the head of the RF group. His research interests are focused on design optimization and tests of RF Systems and Circuits.