Translinear Signal Processing Circuits in Standard CMOS FPAA

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***Abstract*—In this paper, the implementation of signal processing circuits on a novel translinear Field-Programmable Analog Array (FPAA) testchip is reported. The FPAA testchip is based on a 0.35-micron, fully CMOS translinear element, which is the core block of a reconfigurable analog cell. The FPAA embeds a 5 × 5 cell array. As implementation examples, a four-quadrant multiplier with five decade dynamic range and a programmable fourth-order low-pass filter with up to 7 MHz bandwidth have been mapped on the translinear FPAA. 14 cells have been used for the four-quadrant multiplier while 18 cells were needed for the fourth-order low-pass filter.**

***Index Terms*—Mixed-signal, Field Programmable Analog Array, Translinear Cell, Log-domain Filter, Four-Quadrant Multiplier**

I. Introduction

Whenever the design constraints can be fulfilled, Field-Programmable Analog Arrays (FPAA) highly attractive for prototyping and low volume products as a fast and cost-effective alternative to mixed-signal full-custom design.

FPAAs basically consist of an array of configurable analog blocks and they can be classified in several types depending on their operation mode, being either continuous-time or discrete-time and either voltage-mode or current-mode. Continuous-time devices can be implemented by means of translinear elements [1, 2], transconductors [3], current integrators [4] or current conveyors [5], while discrete-time implementations may use switched capacitor topologies [6, 7] or switched current circuits. The FPAAs can be configured for applications such as filtering [8], neural networks [9], industrial control [10], signal processing [11], V-F converters and aerospace communications [12], among others.

Since the 1990's, FPAAs have received the designers attention because this type of devices provides flexibility in analog circuit system design, similar to FPGA (Field-Programmable Gate Arrays) in the digital domain. However, because of scalability issues and the more reduced modularity of analog blocks compared to digital counterparts, the development of reconfigurable analog hardware has been progressing very slowly. Current FPAAs have struggled to establish a solid market base, but they have been plagued by poor performance and a lack of general functionality. Therefore, the FPAAs have not been as well accepted as FPGAs have. Recently, mixed-signal devices that integrate a microcontroller and some analog and digital components that typically surround it constitute an embedded system called PSoC (Programmable System-on-Chip), and have been successfully introduced in the market [13]. This kind of devices already was reported in the late 90's [14].

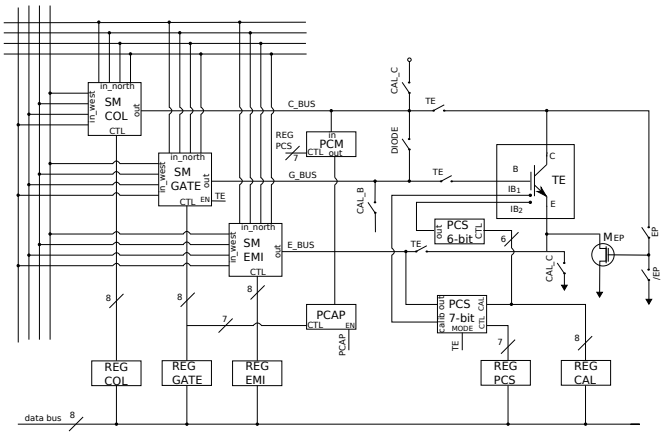

Figure 1. *Block diagram of the Reconfigurable Translinear Cell (RTC) [2]*

In analog VLSI, the translinear approach [15] provides compact and fast implementation of such basic blocks, being very suitable when using bipolar transistor; however, the MOS transistor exhibits an exponential characteristic only in weak inversion, which severely limits speed.

In order to enhance the frequency limitations of translinear circuits in standard CMOS technology, a new translinear cell as a reconfigurable analog block in a FPAA was proposed in [2, 16]. Some of the most common basic operations in FPAA are filtering and non-linear functions, e.g., products and divisions.

This paper aims to the application of an FPAA as a reconfigurable signal processing element. The reconfigurable translinear cell architecture is described in section II. Section III shows the mapping of a four-quadrant multiplier and a fourth order low-pass filter in the FPAA. Finally the simulation results for the multiplier and filter are presented in section IV.

II. Reconfigurable Translinear Cell Architecture

Fig. 1 shows the proposed RTC block diagram. The translinear cell contains the translinear element (TE) [16], a Programmable Current Mirror (PCM) block, 6 and 7-bit Programmable Current Sources (PCS 6-bit) and (PCS 7-bit) blocks, a Programmable CAPacitor (PCAP) block, three

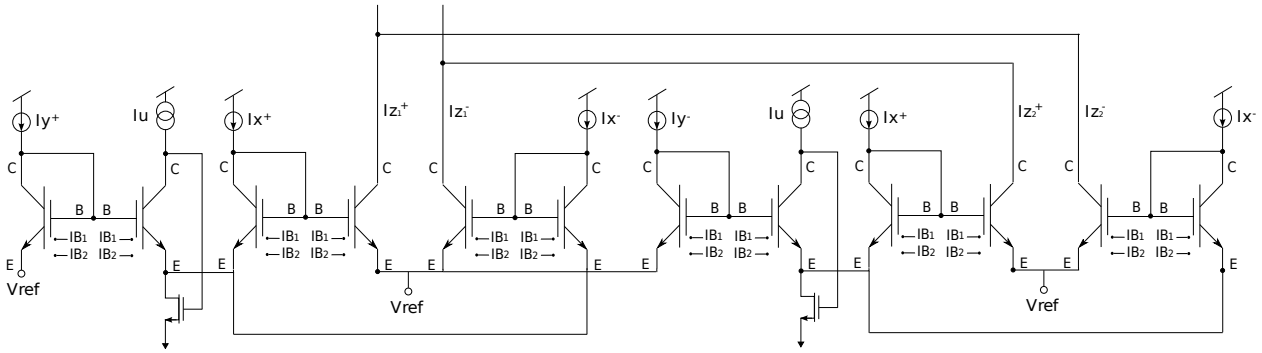

Figure 2. *Four-quadrant multiplier schematic*

Switch Matrices (SM), a configuration memory (REG), configuration switches and an additional MOS transistor.

The main block is the TE, based on a wide dynamic ranges fully CMOS-compatible circuit presented in [16, 17]. The programmable current mirror can be configured to scale input currents by 3, 2, 1, 1/2 and 1/3 times. The range of input and output currents of the mirror must be close to the dynamic range of the translinear element. The 6 and 7-bit programmable current sources provide the two biasing currents to the translinear element, in fact the 7-bit current source can be configured as a general bias source with three different ranges, from 0 to 10 nA, 1 μA and 100 μA. The programmable capacitor is needed for log-domain filters applications. This capacitor can be tunable in a range of $1.25 - 2.5\,pF$. Despite this programmability is limited, cutoff frequency is usually set by means of transconductance in translinear circuits (see eq. 2). The switch matrices provide interconnection among cells and the configuration switches configure the translinear cell, both by means of configuration memories. The MOS transistor in Fig 1 is an alternative to provide an emitter-follower connection forcing the collector current, using the Enz-Punzenberger (EP) configuration [18].

The RTC has 7 different forms to be configured: 1) as pure TE, 2) TE with EP connection, 3) as bias current source cell, 4) as bias current source with a programmable capacitor, 5) as a current mirror cell, 6) as current mirror with a programmable capacitor and finally 7) as pure programmable capacitor cell. The developed FPAA testchip contains a 5×5 RTC array, details on this testchip and layout can be found in [2]. These cells can be connected and configured as desired to form a specific circuit. For the interconnects, four rails in each row and column are provided, and every RTC is connected to the rail of corresponding row and column via switch matrices.

III. Application Examples Mapping

In Fig. 2 a four-quadrant multiplier schematic is depicted. Applying the translinear principle [19], where in a closed loop the product of clockwise currents is equal to the product of counterclockwise current, we obtain:

$$I_o^+ - I_o^- = \frac{(Ix^+ - Ix^-)\,(Iy^+ - Iy^-)}{I_u} \qquad (1)$$

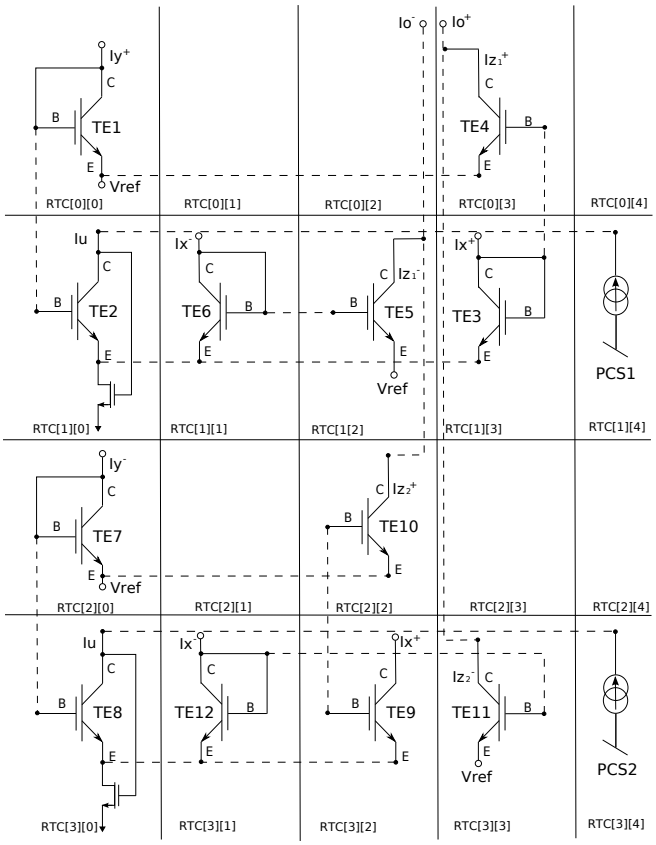

Figure 3. *Four-quadrant multiplier mapping*

Where I_x^+, I_x^-, I_y^+ and I_y^- are the differential inputs, I_u is a bias current source, $I_o^+ = I_{z1}^+ + I_{z2}^-$ and $I_o^- = I_{z2}^+ + I_{z1}^-$ are the differential outputs. The translinear elements from $TE1$ to $TE6$ show the classic topology of a two-quadrant multiplier, and the working principle can be found on [19]. To sketch the four-quadrant multiplier, two topologies of two-quadrant multiplier were cascaded.

Fig. 3 depicts the mapping of the four-quadrant multiplier in a 4×5 slice of the FPAA. To implement this circuit 14 cells were needed, 10 of them configured as translinear elements, 2 cells with EP connection and 2 more cells operating as bias current sources (I_u). The dotted lines show the interconnectiv-

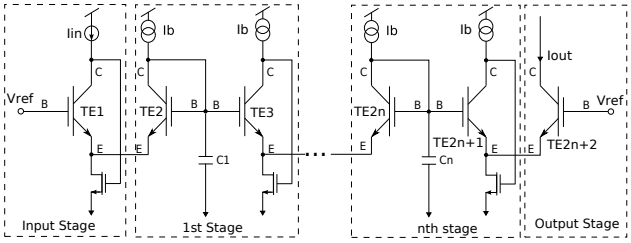

Figure 4. *nth-order low-pass filter schematic*

ity among RTCs by means of switch matrices. The RTCs must be distributed in such a way that inherent circuit symmetry is preserved. Special care should be taken with the switch placement, otherwise an asymmetrical RTC mapping causes different voltage drop on the rails, due to the number of serial connected switches, producing mismatch among RTCs.

Following the same procedure, a fourth-order low-pass filter was mapped, where 18 cells were used to configure the FPAA, 5 of them as translinear elements, 5 cells with EP connection, 4 cells operating as bias current sources (I_b) and 4 more cells operating as bias current sources (I_b) with programmable capacitor (C_i). Fig. 4 shows the general nth-order low-pass filter schematic. The input stage is a translinear element with EP connection, the next stages define the filter order, each i-stage provides a pole by means of capacitor C_i that is placed between TE_{2i} and TE_{2i+1} to ground. The output stage is a simple translinear element. The pole frequency of each filter stage is given by,

$$f_{ci} = \frac{g_{m2i}}{2\pi C_i} \tag{2}$$

Where g_{m2i} is the transconductance of the translinear element $2i$ and C_i is the capacitance that provides the dominant pole at each stage i. With these two parameters the translinear filter can be tuned to a specific cut-off frequency.

IV. Application Examples Results

This section presents simulation results for the four-quadrant multiplier and the fourth-order low-pass filter at transistor level, taking into account the parasitics effects. Simulation results were obtained with Spectre and the programming of the RTC registers was optimized by means of a functional description in Verilog of these digital elements and mixed-signal simulation to achieve short simulation times.

A. Four-Quadrant Multiplier

In Fig. 5 the DC characteristic of the four-quadrant translinear multiplier at different tuning currents is depicted. The parametric analysis shows the different curves with a differential input $I_x = I_x^+ - I_x^-$: $-10\ \mu A$, $-6\ \mu A$, $-2\ \mu A$, $2\ \mu A$, $6\ \mu A$ and $10\ \mu A$. Fig. 6 shows the log-scale linearity in five decades with a differential input $I_x = I_x^+ - I_x^-$: $10\ \mu A$, $1\ \mu A$, $100\ nA$, $10\ nA$ and $1\ nA$.

Fig. 7 shows the multiplier transient response using a constant of $5\ \mu A$ bias added to a $1\ MHz$ sine wave of $2.5\ \mu A_{pp}$ with opposite phase in each input I_x^+ and I_x^-. Input I_y^+ is

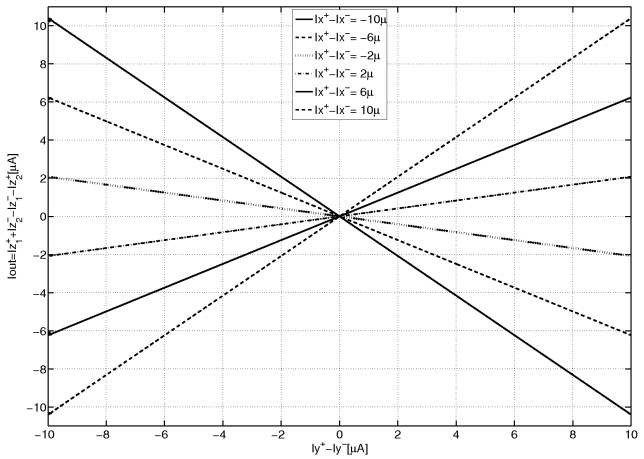

Figure 5. *Four-quadrant translinear multiplier DC response at different tuning currents $I_x = I_x^+ - I_x^-$: $-10\ \mu A$, $-6\ \mu A$, $-2\ \mu A$, $2\ \mu A$, $6\ \mu A$ and $10\ \mu A$*

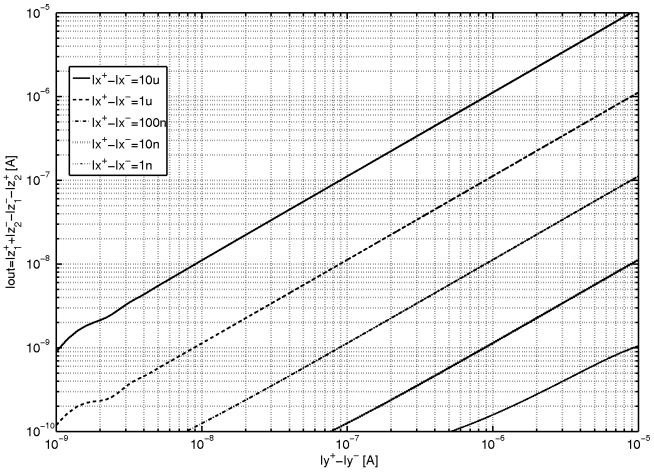

Figure 6. *Four-quadrant translinear multiplier log-scale DC response simulation at different tuning currents $I_x = I_x^+ - I_x^-$: $10\ \mu A$, $1\ \mu A$, $100\ nA$, $10\ nA$, $1\ nA$*

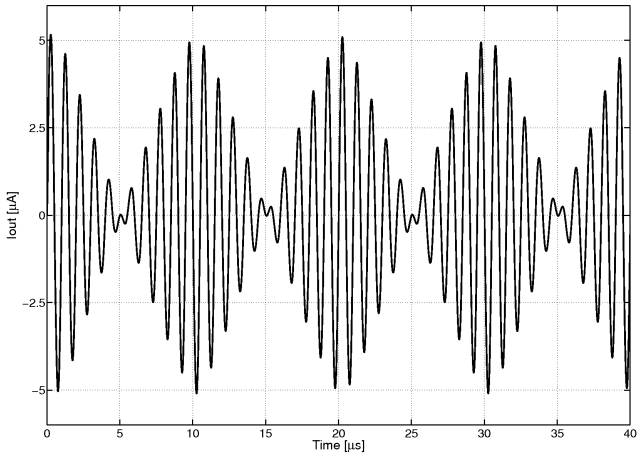

Figure 7. *Transient response of the four-quadrant translinear multiplier*

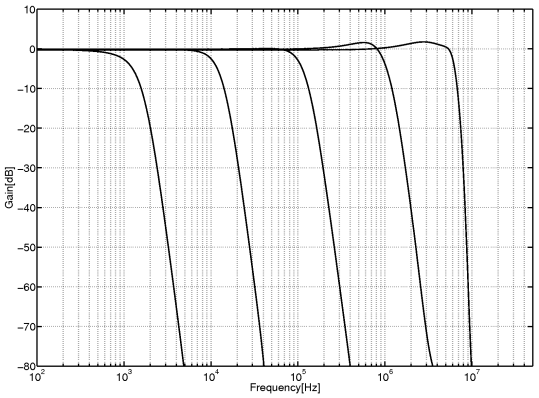

Figure 8. *Fourth-order low-pass filter. Frequency Response at different tuning currents. From left to right tuning current I_b is: 1 nA, 10 nA, 100 nA, 1 μA and 10 μA, with a capacitance of 2.5 pF.*

driven by a 50 kHz triangular wave from 10 μA to 0 μA, while input I_y^- is driven by a 50 kHz triangular wave from 0 μA to 10 μA. The I_u bias currents have been implemented with PCS cells and set to 9.6 μA in all simulation results. The output current is a 5 μA_{pp} sine wave modulated by the triangular wave, as shown. Notice modulated signal phase shift due to triangular wave zero crossings.

B. Fourth-Order Low-Pass Filter

The second signal-processing application is the fourth-order low-pass filter, tuned at different cut-off frequencies, as is shown in Fig. 8. The cut-off frequency was fixed by means of I_b which determines the transconductance. C_i was configured to 2.5 pF for all stages fixing all poles at the same frequency and I_b was set to 1 nA, 10 nA, 100 nA, 1 μA and 10 μA to have cut-off frequencies of 1 kHz, 10 kHz, 100 kHz, 1 MHz and 10 MHz respectively. The last curve has a cut-off frequency at 7 MHz approximately and a steep slope due to the translinaer element bandwidth limitation. The rest of the curves have a slope of 120 dB/dec approximately, corresponding to the expected fourth-order slope. Emitter degeneration by means of an active resistor was needed to reduce variation of the filter DC gain with the cut-off frequency.

V. Conclusion

In this paper we have presented the successful mapping and simulation of two typical signal-processing application circuits, four-quadrant multiplier and fourth-order low-pass filter, based on a 0.35 μm CMOS reconfigurable translinear FPAA. The simulation results validated the reconfigurability and the functionality of the 25-cell field programmable analog array, where each RTC has an area of 232 $\mu m \times$ 159 μm, with an overhead of the configuration memory of 12 %. In particular, for the four-quadrant multiplier the dynamic range reaches five decades and an application as a modulator has been shown, for the low-pass filter a cut-off frequency can be tuned by means of a bias current source I_u. Experimental results on the manufactured testchip will be available in the near future.

Acknowledgment

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