FastIC: A Fast Integrated Circuit for the Readout of High Performance Detectors

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Abstract: This work presents the 8-channel FastIC ASIC developed in CMOS 65 nm technology suitable for the readout of positive and negative polarity sensors in High Energy Physics experiments, Cherenkov detectors and Time-of-Flight systems. The front-end can be configured to perform analog summation of up to 4 single-ended channels before discrimination in view of improving time resolution when segmenting a SiPM. The outputs encode the Time-Of-Arrival information and linear energy measurement which captures the peak amplitude of the input signal in the 5 μA – 25 mA input peak current range. Power consumption of the ASIC is 12 mW/ch with default settings. Measurements of Single Photon Time Resolution with a red-light laser source and a HPK SiPM S13360-3050CS are ≈ 140 ps FWHM.

Keywords: Analogue electronic circuits, Front-end electronics for detector readout, Gamma detectors, Cherenkov detectors.

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Contents

1 Introduction

The detection of low intensity light radiation with precise time and charge resolution is highly demanded in several applications. Cherenkov radiation and scintillation detectors are employed for the identification of elementary particles in High Energy Physics experiments [1–3]. Medical Imaging including technologies such as Time-of-Flight Positron Emission Tomography (ToF-PET) also demand efficient photodetectors coupled to low jitter readout electronics [4–6]. Other applications include Fluorescence-Lifetime Imaging Microscopy (FLIM), Light Detection and Ranging (LIDAR), TOF Mass Spectrometry and Quantum Communications.

This work presents the 8-channel front-end ASIC, referred to as FastIC, designed in a CMOS 65 nm process and a total area of 2×2 mm^2. The FastIC can process the fast signals provided by photodetectors with fast time response and intrinsic amplification, such as photo-multiplier tubes (PMTs), micro-channel plates (MCPs), and Silicon Photomultipliers (SiPMs).

2 FastIC architecture

The architecture of the FastIC is based on the classic multi-branch architecture (i.e., time, energy, and trigger information) with similarities to the HRFlexToT ASIC [4], as illustrated in Figure 1. The front-end stage processes the signals in current mode with an input impedance below 20 Ω and can be programmed to cope with positive and negative input polarity sensors. The 8 readout channels can be configured to work as 4 differential channels. For instance, an SiPM can be readout using both anode and cathode. Alternatively, 4 single-ended sensor signals can be summed, and the discrimination is performed on the resulting pulse. This active summation concept was already introduced in [7], and it is integrated to explore the impact of segmenting a large sensor area into smaller sensors in order to improve the electronic jitter [8, 9].

Each FastIC channel provides the information of Time-of-Arrival (ToA) and a linear energy measurement of the detected photons. Time response is generated through a leading-edge comparator whose output provides a non-Linear Time over Threshold (ToT) response encoding the ToA of
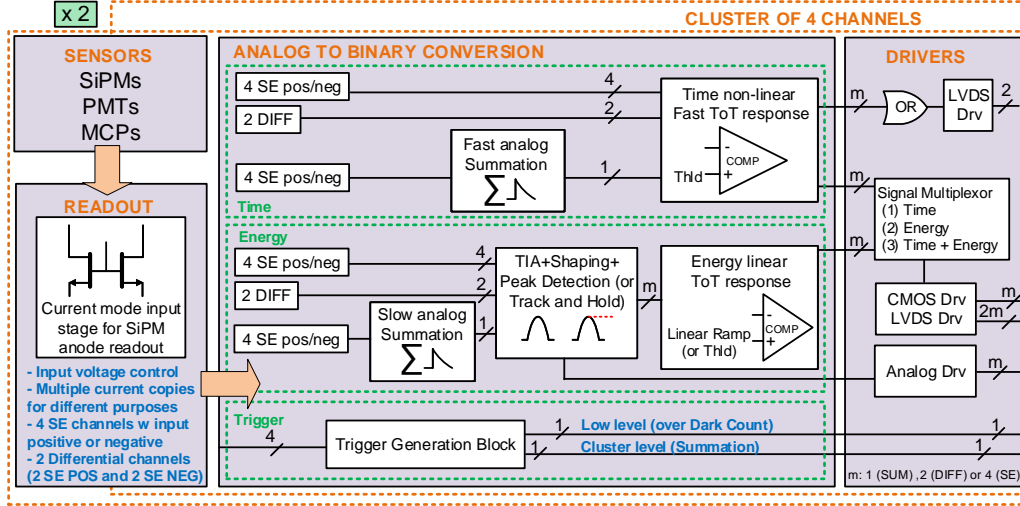
Figure 1: Functional block diagram of the FastIC ASIC.

the events in the rising edge of a pulse. Time response is controlled by a threshold in the comparator that can be configured using an internal register to detect down to a single photon.

The signal processing path for the energy measurement generates a binary pulse whose width is proportional to the collected charge. More specifically, the energy is proportional to the peak amplitude of the event. For instance, the peak amplitude of a SiPM follows a linear relation with respect to the number of photons detected. The energy measurement is achieved with a linearity error below 3% over the entire input dynamic range from 5 uA to 25 mA input peak current.

The signal processing of the linear energy acquisition is achieved by means of the following stages: (1) The front-end input stage generates a current copy (with a configurable gain) from the input sensor once a signal is detected. (2) This current is converted into voltage by means of a Trans-Impedance Amplifier (TIA) with configurable gain. (3) A shaper block is implemented using a passive pole-zero cancellation and a first-order active integrator to reduce the peaking time (rising edge) and decrease the recovery time or tail of the signal (falling edge). (4) A Peak Detector and Hold (PDH) block (it can operate also as a Track and Hold) is used to detect the peak amplitude of the signal. (5) A linear ramp starts, and the rising edge of the energy measurement is generated. (6) A voltage discriminator is employed to compare the detected peak amplitude with the linear ramp and thereby obtain the falling edge of the energy measurement. This linear energy acquisition is governed by a synchronous Finite State Machine. This is the same energy processing scheme used in the HRFlexToT ASIC [4].

Different trigger methods with configurable thresholds are available to indicate when a valid event is captured. A low-level trigger is provided per channel and threshold can be configured to detect events as low as a single photon or above tens of photons to discard low energy events. A cluster trigger is provided as the summation of the input signals for those cases where the signal is spread among several channels. An external trigger can be used for the energy acquisition. Lastly, the time signal can be also employed as a trigger signal.

The output driver can be configured as CMOS single-ended or differential Scalable Low-Voltage Signaling (SLVS). Alternatively, internal analog signals can be read out by means of a

high-speed analog driver per channel capable of driving capacitive loads. A logic OR between the timing signals is output via an SLVS driver in order to capture the fastest timestamp. The different operating modes of the ASIC can be controlled via an I2C communication protocol.

3   Methods

The experimental set-up used to perform time measurements is shown in Figure 2. An external trigger at 500 kHz sends a signal to both the laser driver and the oscilloscope. The laser driver sends a pulse to the laser (PicoQuant PDL 800-D laser at 635 nm and a tuned intensity level of 50% as per the optimal operating conditions, jitter < 20 ps rms and 30 ps pulse width). The laser generates a red photon package that passes through a Single Mode Fiber (Thorlabs 630A-FC SM) to a beam collimator. This is coupled to a liquid crystal optical beam attenuator (Thorlabs LCC1620/M), which can change the attenuation factor depending on the voltage applied. All measurements were taken in an isolated light tight box and temperature was stabilized around 18 °C.

Jitter is analyzed by measuring the time response of the ASIC. The arrival time uncertainty is captured by measuring the delay between the laser trigger signal and the rising edge of the time signal. The number of photons detected is obtained by measuring the width of the time response. For Single-Photon Time Resolution (SPTR) measurements with SiPMs, only those events with a pulse width corresponding to the first photon are selected. For PMTs, all events are recorded, and a time walk correction (TWC) is applied to compensate delay variations. Time walk in a leading-edge discriminator occurs due to the average mean delay varies depending on the number of photons detected, i.e, changes depending on the signal amplitude. Therefore, it introduces a systematic delay variation that can be corrected.
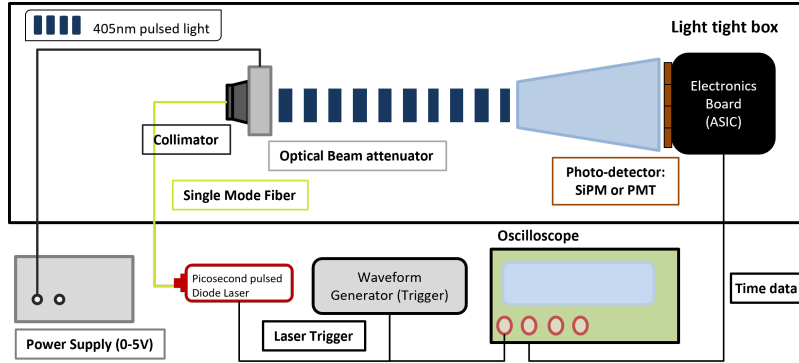

Figure 2: Representation of the experimental setup using a red laser source for time measurements.

4   Evaluation of the FastIC performance

Power consumption of FastIC is 12 mW/ch in single-ended mode (full channel functionality) or 6 mW/ch when only the time branch is used (non-linear ToT operation). The maximum hit rate per channel is 2 MHz using the linear ToT and about 50 MHz when employing the non-linear ToT. Simulation results using a HPK SiPM S13360-3050CS model at 4.5 V over-voltage and parasitic interconnections, resulted in a predicted electronic jitter of 72.6 ps Full Width at Half Maximum (FWHM) at the single photon level in single-ended positive polarity configuration.

This SiPM can be segmented into four smaller sensors and then read with four input channels. The ASIC internally performs an active summation to recover the signal from the different channels and therefore obtain a unique summation output. In this scenario, this predicted electronic jitter decreased to 39.5 ps FWHM when segmenting this 3×3 mm^2 sensor into four 1.5×1.5 mm^2 SiPMs. This improvement in the electronic jitter is due to the reduction in the intrinsic capacitance of the SiPM connected to a single channel. A smaller capacitance translates into a larger slew rate of the input signal and lower noise. However, noise will remain the same after performing the active summation of all the segmented sensors. Thus, the reduction in the electronics jitter comes from the improvement in the slew rate, at the expense of increasing the power consumption since four readout channels are needed. A complete analysis of sensor segmentation can be found in [8, 9].

A HPK PMT R5900 producing pulses with ≈5 ns FWHM, and a datasheet transient time spread of 330 ps FWHM, was tested using the red-light laser. In this case, the negative input polarity was selected for the readout of the PMT resulting in a time jitter of 340 ps FWHM after TWC when using a gaussian fit and 323 ps FWHM when employing a gaussian convoluted with an exponential approximation [10], as shown in Figure 3. This time jitter corresponds to the time uncertainty of detecting tens of photons. TWC is based on calibrating the arrival time of the photons depending on the pulse width of the time response. These results show that the FastIC does not degrade the time response for this detector.
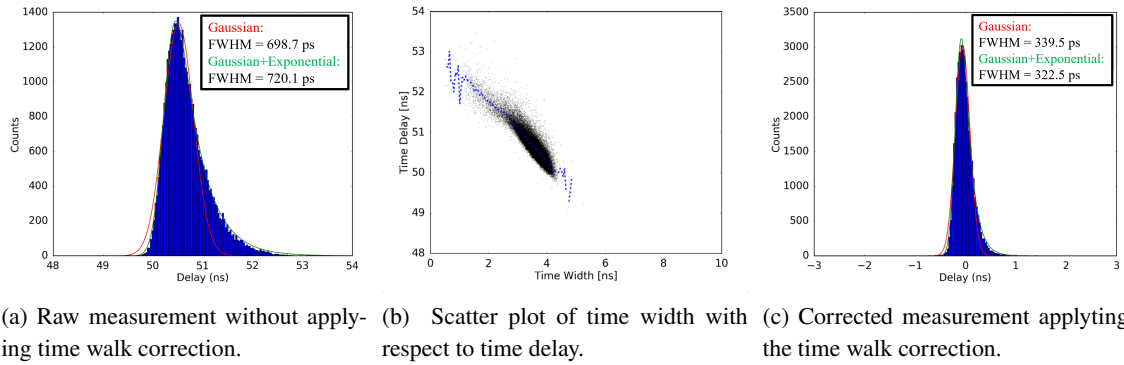

(a) Raw measurement without applying time walk correction.

(b) Scatter plot of time width with respect to time delay.

(c) Corrected measurement applyting the time walk correction.

Figure 3: Time resolution using the negative input polarity for a HPK PMT R5900.

SPTR laboratory measurements using a HPK SiPM S13360-3050CS are ≈140 ps FWHM at 9.9 V over-voltage when employing a gaussian convoluted with an exponential approximation to fit the arrival time data. The HRFlexToT ASIC tested in the same conditions yielded an SPTR of 161.5 ps FWHM at 10 V over-voltage and thus showing that FastIC provides a lower electronic jitter, as illustrated in Figure 4. Note that the measured SPTR is the convolution of the SPTR of the sensor, the laser FWHM and the electronic jitter.

5 Conclusions

FastIC ASIC can be used in several applications such as High Energy Physics, Cherenkov detectors and other Time-of-Flight systems. Currently, FastIC connected to Multi-anode PMTs is being studied for the future upgrade of the Ring-Imaging Cherenkov (RICH) detectors to capture the time
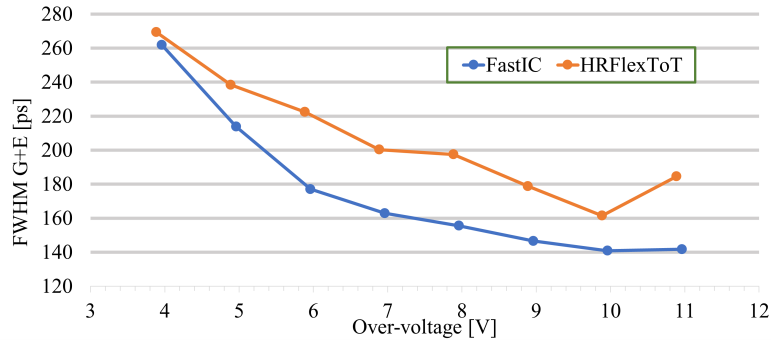
Figure 4: SPTR comparison between FastIC and HRFlexToT ASICs in terms of FWHM. Sensor employed: HPK SiPM S13360-3050CS (3×3 mm^2 pixel, 50 μm cell).

of arrival of Cherenkov photons [2]. Initial measurements show the timing performance of the FastIC ASIC for SiPMs and PMTs. For instance, SPTR using the HPK S13360-3050CS 3×3mm^2 achieves a 12.8% better time response than HRFlexToT. A comparison between the HRFlexToT and other electronics are detailed in [4]. A new version of the ASIC including a TDC [6] with 20 ps time bin and without significantly increasing the power consumption is under development.

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