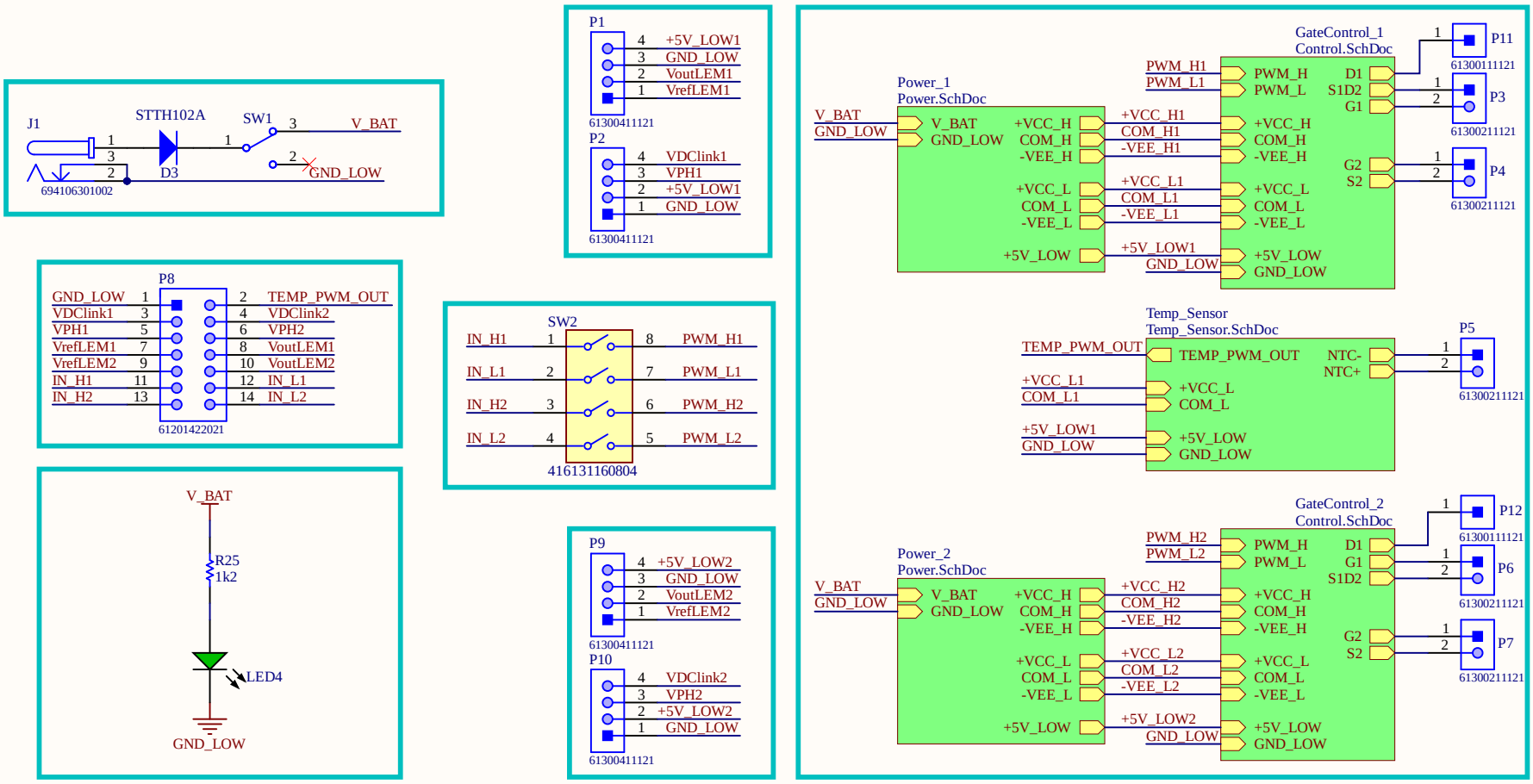
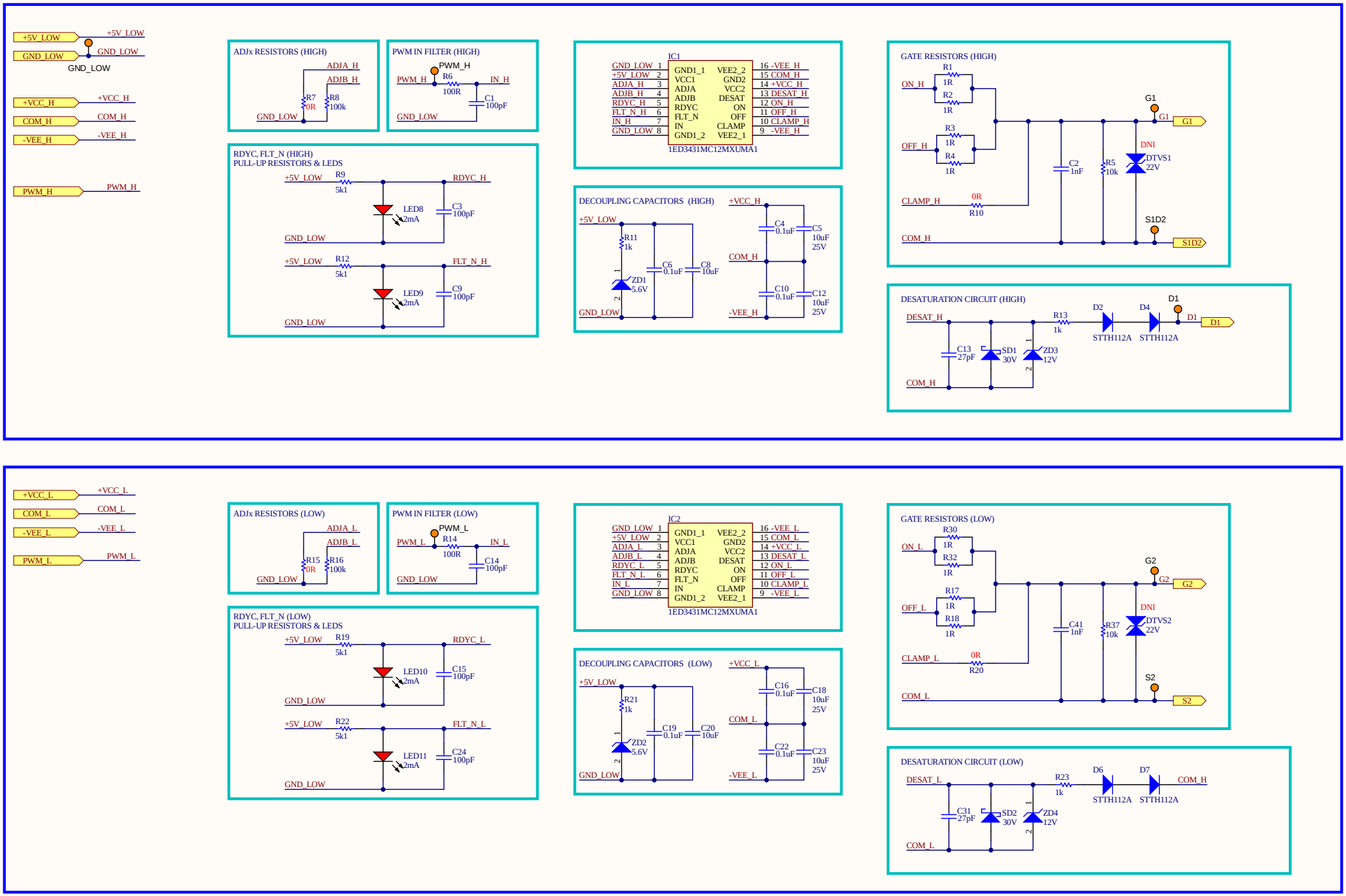
Appendix A:

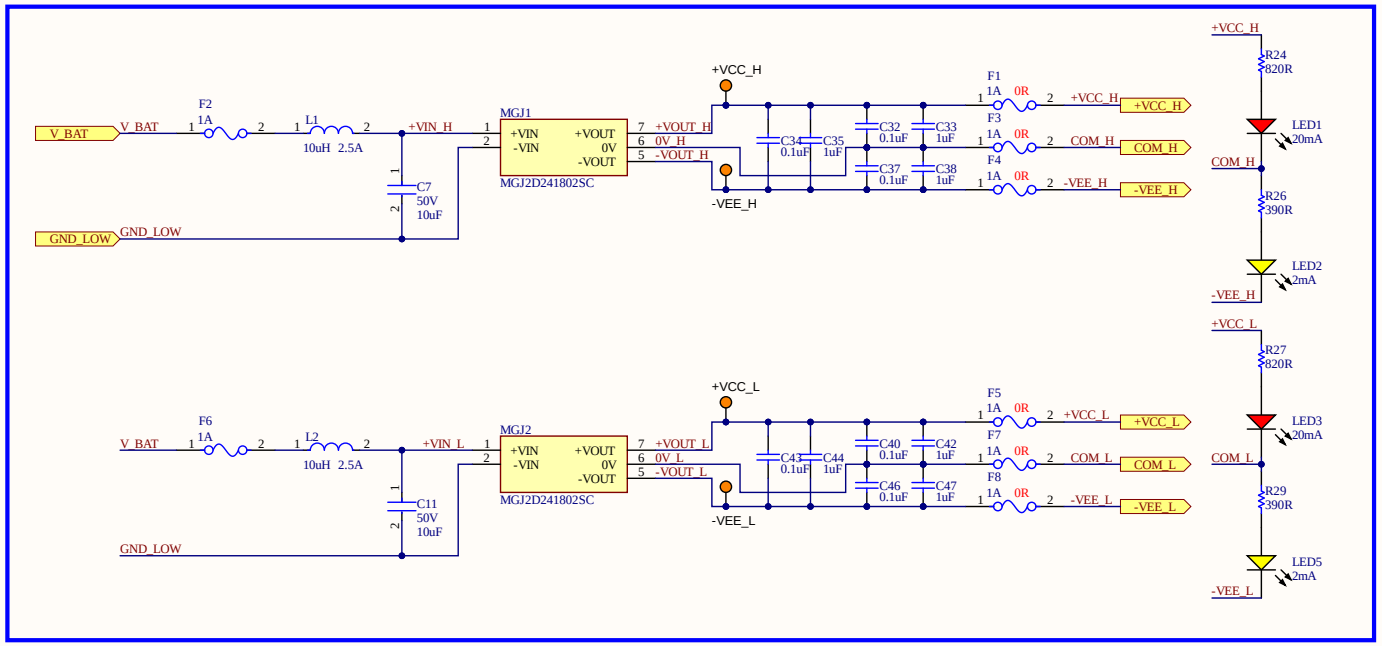
ALTIUM SCHEMATICS NEW GATE DRIVER PCB



Title	Gate Driver Overview Schematic	
Size: A4	Number: 1/4	Revision:
Date: 9/06/2022		
File: GateDriver_Board.Sch		Drawn By: Mikel Aceldegui

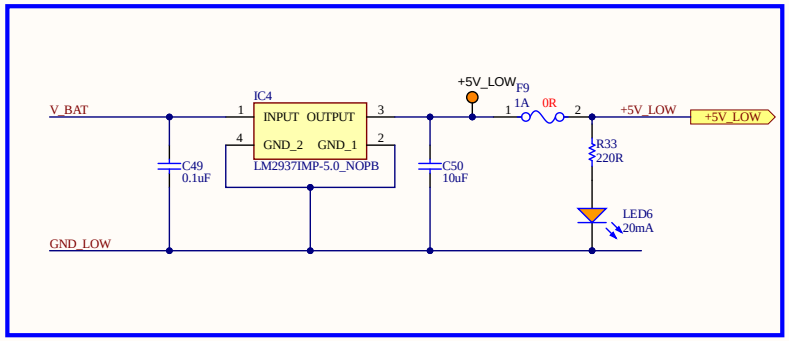


Title	Control Circuit Schematic	
Size: A3	Number: 2/4	Revision:
Date: 9/06/2022		
File: Control.SchDoc		Drawn By: Mikel Aceldegui



MURATA BIPOLAR SUPPLY

Isolated DCDC Converter:
- Manufacturer: MURATA
- Input: 24V
- Bipolar: +18V, -2.5V
- Input filter: Common mode LC (recommended by manufacturer)
- Switching Freq: 100kHz



5V DCDC Converter

A 5V DCDC converter is included to supply the PWM generator and the optocoupler to Isolate the signal of the SiC NTC. (HV Zone)

Title: Power Supply Circuit Schematic		
Size: A3	Number: 3/4	Revision:
Date: 9/06/2022		
File: Power.SchDoc		Drawn By: Mikel Aceldegui

+5V_LOW

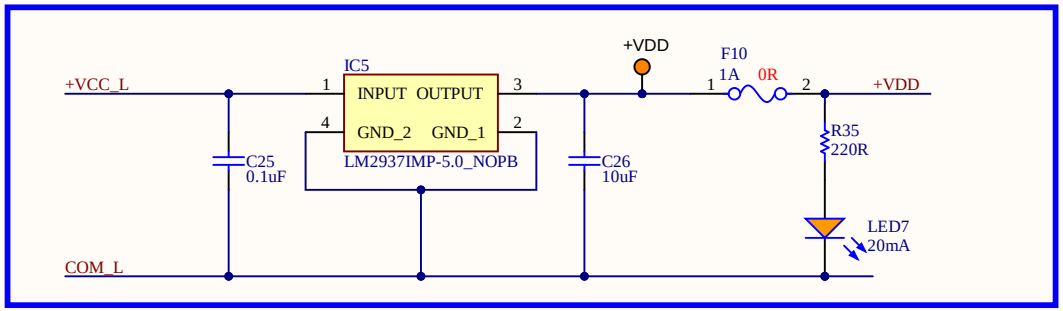
GND_LOW

+VCC_L

COM_L

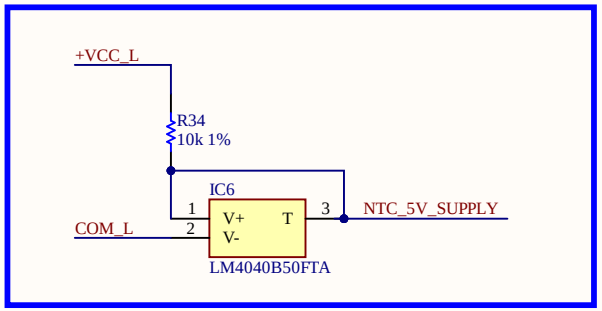
5V DCDC Converter

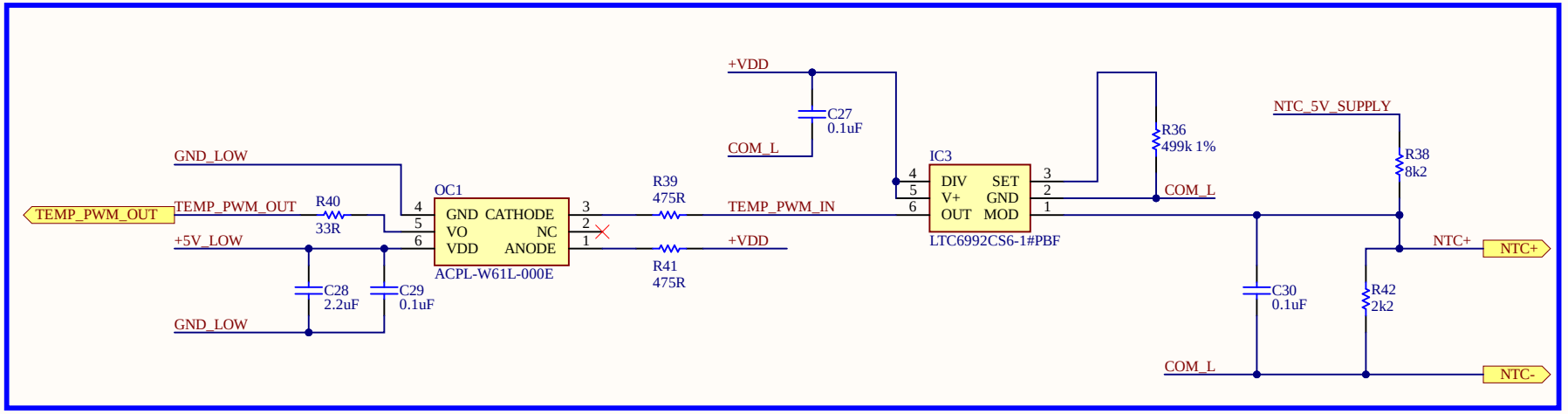
A 5V DCDC converter is included to supply the PWM generator and the optocoupler to Isolate the signal of the SiC NTC. (HV Zone)



5V Shunt Voltage Reference

A 5V Shunt Voltage Reference is included to supply the the SiC NTC. (HV Zone)



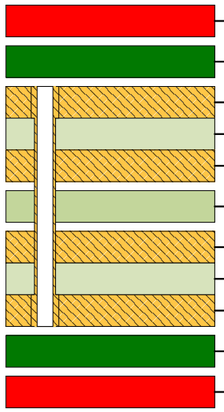


Title	Temperature Sensor Measurament Circuit Schematic	
Size: A4	Number: 4/4	Revision:
Date: 9/06/2022		
File: Temp_Sensor.SchDoc		Drawn By: Mikel Aceldegui

Appendix B:

ALTIUM PCB LAYOUTS NEW GATE DRIVER PCB

Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.01mm	Solder Resist	Solder Mask	GTS
Copper	**Top Layer**	**0.04mm**		**Signal**	**GTL**
Core		*0.25mm*	*FR-4*	*Dielectric*	
Copper	**VCC/GATE**	**0.04mm**		**Signal**	**G1**
Prepreg		*0.13mm*		*Dielectric*	
Copper	**GND/GATE**	**0.04mm**		**Signal**	**G2**
Core		*0.25mm*	*FR-4*	*Dielectric*	
Copper	**Bottom Layer**	**0.04mm**		**Signal**	**GBL**
Surface Material	Bottom Solder	0.01mm	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 0.80mm

	NAME	DATE
DRAWN		06/09/2022

COMMENTS:

DIMENSIONS ARE IN INCHES

TITLE

Layer Stack Manager

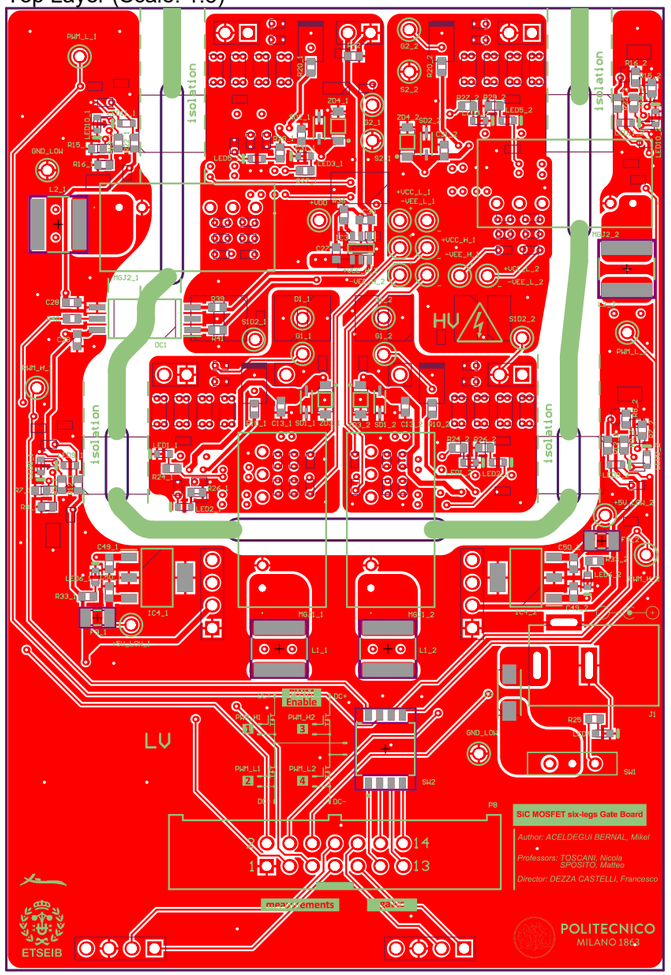
GATE DRIVER PCB

SIZE	DWG. NO.
A3	1/5

SCALE: 1:1

SHEET 1 OF 5

Top Layer (Scale: 1.5)



	NAME	DATE
DRAWN		06/09/2022

COMMENTS:

DIMENSIONS ARE IN INCHES

TITLE

Top Layer PCB Layout

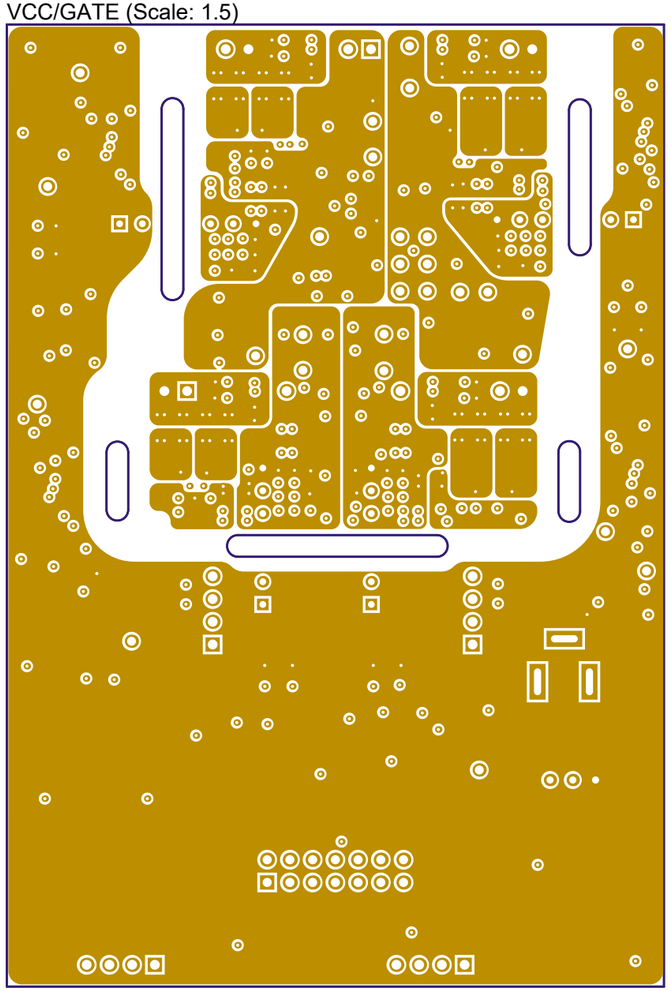
GATE DRIVER PCB

SIZE	DWG. NO.	
A3	2/5	
SCALE: 1:1.5		SHEET 2 OF 5

A | B | C | D

1

VCC/GATE (Scale: 1.5)



2

	NAME	DATE
DRAWN		06/09/2022

COMMENTS:

DIMENSIONS ARE IN INCHES

TITLE

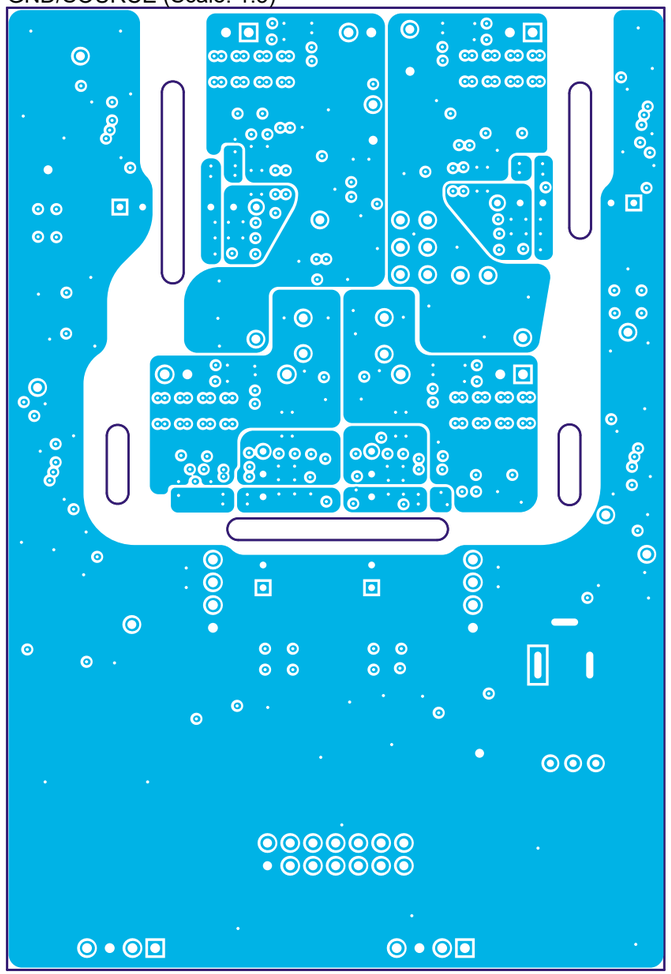
VCC/GATE Layer PCB Layout

GATE DRIVER PCB

SIZE	DWG. NO.
A3	3/5
SCALE: 1:1.5	SHEET 3 OF 5

A | B | C | D

GND/SOURCE (Scale: 1.5)



	NAME	DATE
DRAWN		06/09/2022

COMMENTS:

DIMENSIONS ARE IN INCHES

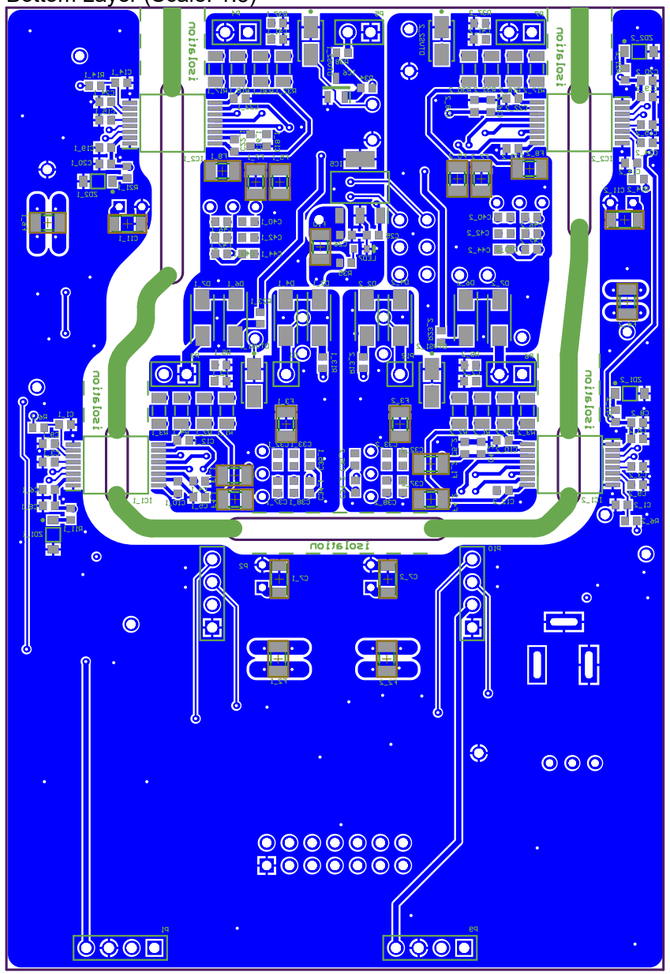
TITLE

GND/SOURCE Layer PCB Layout

GATE DRIVER PCB

SIZE	DWG. NO.
A3	4/5
SCALE: 1:1.5	SHEET 4 OF 5

Bottom Layer (Scale: 1.5)



	NAME	DATE
DRAWN		06/09/2022

COMMENTS:

DIMENSIONS ARE IN INCHES

TITLE

Bottom Layer PCB Layout

GATE DRIVER PCB

SIZE	DWG. NO.
A3	5/5

SCALE: 1:1.5

SHEET 5 OF 5

Appendix C:

DATASHEETS OF MAIN COMPONENTS

EiceDRIVER™ 1ED34x1Mc12M Enhanced

Datasheet

Single-channel 5.7 kV (rms) isolated gate driver IC with adjustable DESAT and soft-off

Features

- 650 V, 1200 V, 1700 V, 2300 V IGBTs, SiC, and Si MOSFETs
- 40 V absolute maximum output supply voltage
- ±3 A, ±6 A, and ±9 A typical sinking and sourcing peak output current
- Separate source and sink outputs for hard switching and with active Miller clamp/clamp driver
- Adjustment pins for parameter configuration from input side
- Precise V_{CEsat} detection (DESAT) with fault output and adjustable filter time and leading edge blanking time with resistor at *ADJB* pin
- Adjustable IGBT soft turn-off after desaturation detection with resistor at *ADJA* pin
- Operation at high ambient temperature up to 125 °C with over-temperature shut down at 160 °C (±10 °C)
- Tight IC-to-IC propagation delay matching ($t_{PDD,max}$ = 30 ns)
- Undervoltage lockout protection with hysteresis for input and output side with active shut-down
- High common-mode transient immunity CMTI = 200 kV/µs
- Small space-saving DSO-16 fine-pitch package with large creepage distance (>8 mm)
- Safety certification
  - UL 1577 recognized (File E311313) with $V_{ISO,test}$ = 6840 V (rms) for 1 s, V_{ISO} = 5700 V (rms) for 60 s
  - VDE 0884-11 approval (Certificate no. 40053980) with V_{IORM} = 1767 V (peak, reinforced)
- Evaluation board available EVAL-1ED3491MX12M

Potential applications

- Industrial motor drives - compact, standard, premium, servo drives
- Solar inverters
- UPS systems
- Welding
- Commercial and agricultural vehicles (CAV)
- Commercial air-conditioning (CAC)
- High-voltage isolated DC-DC converters
- Isolated switch mode power supplies (SMPS)

PG-DSO-16

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Device information

Product type	Output current	CLAMP type[1)]	Isolation class	Marking	OPN
1ED3431MC12M	3 A (typ)	CLAMP	reinforced	3431MC12	1ED3431MC12MXUMA1
1ED3461MC12M	6 A (typ)	CLAMPDRV	reinforced	3461MC12	1ED3461MC12MXUMA1
1ED3491MC12M	9 A (typ)	CLAMPDRV	reinforced	3491MC12	1ED3491MC12MXUMA1
1ED3431MU12M	3 A (typ)	CLAMP	UL 1577	3431MU12	1ED3431MU12MXUMA1
1ED3461MU12M	6 A (typ)	CLAMPDRV	UL 1577	3461MU12	1ED3461MU12MXUMA1
1ED3491MU12M	9 A (typ)	CLAMPDRV	UL 1577	3491MU12	1ED3491MU12MXUMA1

1) Please refer to Chapter 4.5.4.1 for circuit connection to avoid damage to the gate driver IC

Description

The 1ED34x1Mc12M family (X3 Analog) consists of galvanically isolated single channel gate driver ICs in a small PG-DSO-16 package with a large creepage and clearance of 8 mm. The gate driver ICs provide a typical peak output current of 3 A, 6 A, and 9 A.

Adjustable control and protection functions are included to simplify the design of highly reliable systems. All parameter adjustments are done from the input side, including adjustable DESAT filter time, leading edge blanking time, and soft-off current level with only two resistors..

All logic I/O pins are supply voltage dependent 3.3 V or 5 V CMOS compatible and can be directly connected to a microcontroller.

The data transfer across the galvanic isolation is realized by the integrated coreless transformer technology.

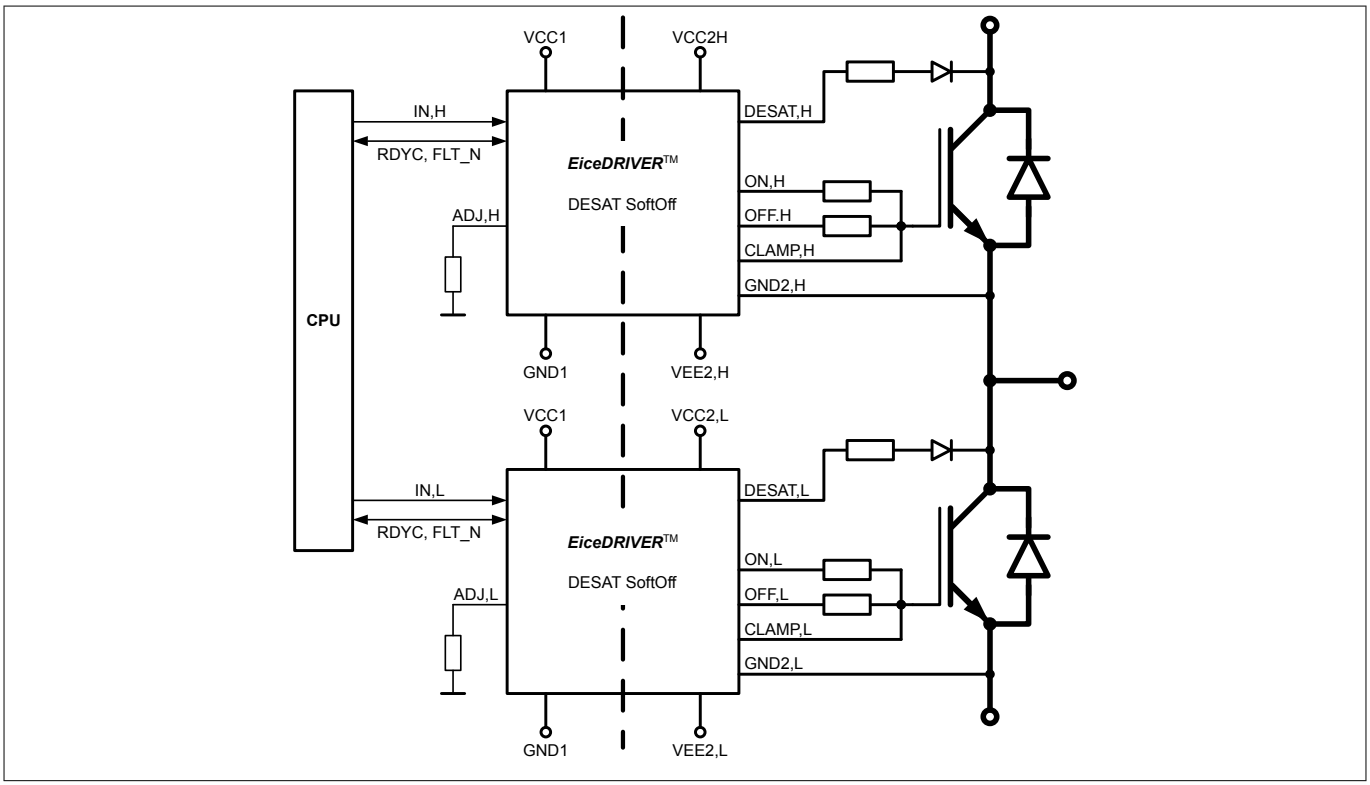


Figure 1 Typical application

Table of contents

Table of contents

1 Block diagram

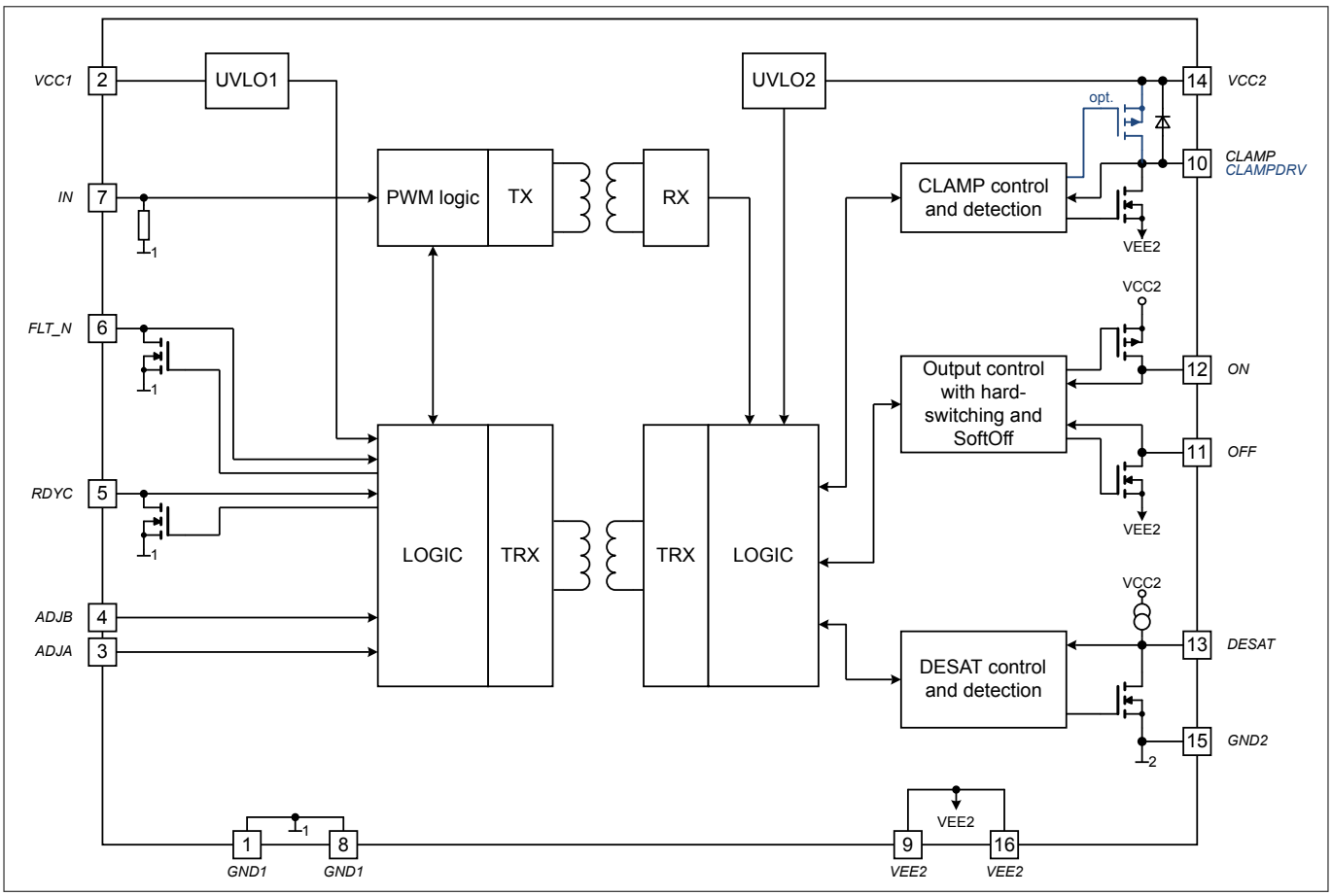


Figure 2 Block diagram

2 Related products

Note: Please consider the gate driver IC power dissipation and insulation requirements for the selected power switch and operating condition.

Product group	Product name	Description
TRENCHSTOP™ IGBT Discrete	IKQ75N120CS6	High Speed 1200 V, 75 A IGBT with anti-parallel diode in TO247-3
	IKW15N120BH6	High Speed 1200 V, 15 A IGBT with anti-parallel diode in TO247
	IHW40N120R5	Reverse conducting 1200 V, 40 A IH IGBT with integrated diode in TO247
CoolSiC™ SiC MOSFET Discrete	IMBF170R650M1	1700 V, 650 mΩ SiC MOSFET in TO263-7 package
	IMBG120R045M1H	1200 V, 45 mΩ SiC MOSFET in TO263-7 package
	IMZ120R350M1H	1200 V, 350 mΩ SiC MOSFET in TO247-4 package
CoolSiC™ SiC MOSFET Module	FS45MR12W1M1_B11	EasyPACK™ 1B 1200 V / 45 mΩ sixpack module
	FF23MR12W1M1_B11	EasyDUAL™ 1B 1200 V, 23 mΩ half-bridge module
	FF6MR12W2M1_B11	EasyDUAL™ 2B 1200 V, 6 mΩ half-bridge module
	F3L11MR12W2M1_B74	EasyPACK™ 2B 1200 V, 11 mΩ 3-Level module in Advanced NPC (ANPC) topology
	F4-23MR12W1M1_B11	EasyPACK™ 1B 1200 V, 23 mΩ fourpack module
TRENCHSTOP™ IGBT Modules	F4-100R17N3E4	EconoPACK™ 3 1700 V, 100 A fourpack IGBT module
	F4-200R17N3E4	EconoPACK™ 3 1700 V, 200 A fourpack IGBT module
	FS150R17N3E4	EconoPACK™ 3 1700 V, 150 A sixpack IGBT module
	FF650R17IE4	PrimePACK™ 3 1700 V, 650 A half-bridge dual IGBT module
	FF1000R17IE4	PrimePACK™ 3 1700 V, 1000 A half-bridge dual IGBT module
	FF1200R17IP5	PrimePACK™ 3+ 1700 V, 1200 A dual IGBT module
	FF1500R17IP5	PrimePACK™ 3+ 1700 V, 1500 A dual IGBT module
	FF1500R17IP5R	PrimePACK™ 3 1700 V, 1500 A dual IGBT module
	FF1800R17IP5	PrimePACK™ 3+ 1700 V, 1800 A dual IGBT module
	FP10R12W1T7_B11	EasyPIM™ 1B 1200 V, 10 A three phase input rectifier PIM IGBT module
	FS100R12W2T7_B11	EasyPACK™ 2B 1200 V, 100 A sixpack IGBT module
	FP150R12KT4_B11	EconoPIM™ 3 1200V three-phase PIM IGBT module
	FS200R12KT4R_B11	EconoPACK™ 3 1200 V, 200 A sixpack IGBT module

3 Pin configuration and functionality

The pin assignment at the gate driver IC generally differentiates between the input side and the output side.

Table 1 General pin assignment

Pins	Designation
1 to 8	input side, input logic signal side, or low voltage side
9 to 16	output side, driver power side, or high voltage side

For simplicity reasons the driver is described as an IGBT driver. For use with MOSFETs and other power switches simply replace any mentioning of collector and emitter with their corresponding pin names.

3.1 Pin configuration

Table 2 Pin configuration table abbreviations

Abbreviation	Description
Pin type	
PWR	Power supply and gate current output pins
I/O	Digital input and output pin
I	Digital input pin
GND	Ground reference pin
AI	Analog input pin
Buffer type	
OD	Open drain output
CMOS	CMOS compatible input threshold levels
PP	Push/pull output buffer
special	Special output/input function, see individual description
Pull device	
PD	Pull-down resistor
CS	Current source

Table 3 Pin configuration

Pin no.	Pin name	Pin type	Buffer type	Pull device	Function
1	*GND1*	GND	–	–	Ground input side
2	*VCC1*	PWR	–	–	Positive power supply input side
3	*ADJA*	AI	special	CS	Parameter adjust set A
4	*ADJB*	AI	special	CS	Parameter adjust set B
5	*RDYC*	I/O	OD, CMOS	–	Combined ready output, high active and fault clear input and soft-off input, low active
6	*FLT_N*	I/O	OD, CMOS	–	Fault output, low active and soft- off input, low active
7	*IN*	I	CMOS	PD, 40 kΩ	Non inverted driver input

(table continues...)

Table 3 (continued) Pin configuration

Pin no.	Pin name	Pin type	Buffer type	Pull device	Function
8	*GND1*	GND	–	–	Ground input side
9	*VEE2*	GND	–	–	Negative power supply output side
10	*CLAMP*	PWR	OD	–	Active Miller clamping, open drain to VEE2 (1ED3431M only)
10	*CLAMPDRV*	PWR	PP	–	Active miller clamping, clamp driver for external MOSFET (1ED3461M, 1ED3491M)
11	*OFF*	PWR, AI	OD	–	Driver sink output
12	*ON*	PWR, AI	OD	–	Driver source output
13	*DESAT*	AI	special	CS, 500 µA	Enhanced desaturation protection
14	*VCC2*	PWR	–	–	Positive power supply output side
15	*GND2*	AI	–	–	Signal ground output side
16	*VEE2*	GND	–	–	Negative power supply output side

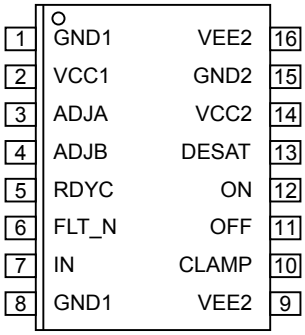


Figure 3 PG-DSO-16 (top view) with CLAMP

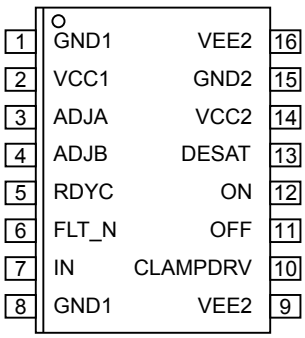


Figure 4 PG-DSO-16 (top view) with CLAMPDRV

3.2 Pin functionality

GND1

Reference ground of the input side. Connect direct to input signal ground.

VCC1

Positive power supply terminal of the input side, connect to 5 V or 3.3 V for proper operation. Place a decoupling capacitor close to this pin and *GND1*.

***ADJA* and *ADJB* parameter adjust input for set A or B**

The pins *ADJA* and *ADJB* are used to adjust two sets of independent parameters of output functions.

Connect a resistor between 1.33 kΩ and 28.0 kΩ to *GND1* to adjust each parameter. All valid resistor values belong to the E96-series with 1% tolerance.

Connecting *ADJA* to *GND1* uses a default value for soft switch-off. Connecting it to *VCC1* is disabling the gate driver IC.

Connecting *ADJB* to *GND1* is disabling the gate driver IC. Connecting it to *VCC1* is setting the function to minimum values.

***RDYC* ready status output, fault-off input and fault-clear input**

Open-drain output reports the correct operation of the device, ready output is high active. Fault-clear input and fault-off input clears a gate driver fault or switch the gate driver output to off with fault-off function, input is low active. Connect to a microcontroller with 5 V or 3.3 V I/O with an external pull-up resistor to *VCC1*. A typical value for this resistor is 2.2 kΩ. The *RDCY* signal is referenced to *GND1*.

***FLT_N* fault output and fault-off input**

Open-drain output reports the failures related to operating of the inverter system to the microcontroller, fault output is active low. Fault-off input switch the gate driver output to off with fault-off function, input is low active. Connect to a microcontroller with 5 V or 3.3 V I/O with an external pull-up resistor to *VCC1*. A typical value for this resistor is 2.2 kΩ. The *FLT_N* signal is referenced to *GND1*.

***IN* non inverting gate driver input**

IN input controls the output of the gate driver IC, the IGBT is turned on if *IN* is set to high. Connect to a PWM output of the microcontroller with 5 V or 3.3 V IO. An internal pull-down resistor ensures IGBT off-state if not connected. A minimum pulse width of typical 103 ns is defined to make the gate driver IC robust against glitches at *IN*.

VEE2

Negative power supply terminal of the output side. Connect to a voltage of 0 V to -25 V referenced to *GND2* for proper operation. Place a decoupling capacitor close to the following pins:

- *VCC2* and *VEE2*
- *GND2* and *VEE2*

If no negative supply voltage is used, all *VEE2* pins have to be connected to *GND2*.

***CLAMP* Miller clamp output, *CLAMPDRV* Miller clamp pre-driver output**

CLAMP: High-current clamp output to hold the gate voltage low during collector-emitter-voltage rise. Connect directly to the gate of the IGBT.

CLAMPDRV: Clamp pre-driver output for the use of an external clamp switch. Connect directly to the gate of a n-channel MOSFET.

OFF driver output

High-current driver sink output to discharge the gate of the external IGBT.The gate driver IC also sinks the Soft-off current at this pin. Connect to the gate of the IGBT via a chosen turn-off gate resistor.

ON driver output

High-current driver source output to charge the gate of the external IGBT and turn it on and sense input for the CLAMP function. Connect to the gate of the IGBT via a chosen turn-on gate resistor.

DESAT enhanced desaturation detection input

Desaturation detection input to monitor the IGBT collector-emitter voltage (V_{CE}) to detect desaturation caused by short circuit events. Connect to the collector of the driven IGBT via a series connection of a protection resistor and a high-voltage diode. The *DESAT* signal is referenced to *GND2*.

VCC2

Positive power supply terminal of the output side. Connect to sufficient supply voltage referenced to *GND2* for proper operation. Place a decoupling capacitor close to the following pins:

- *VCC2* and *VEE2*
- *VCC2* and *GND2*

GND2 reference ground

Reference ground of the output side. Connect to common voltage of a bipolar supply and the emitter of the IGBT. Place a decoupling capacitor close to the following pins:

- *VCC2* and *GND2*
- *GND2* and *VEE2*

4 Functional description

The 1ED34x1Mc12M family (X3 Analog) consists of galvanically isolated single channel gate driver ICs with adjustable feature parametrization by two simple resistors. All adjustments can be done from the low voltage input side.

To start-up the gate driver IC for normal operation both input and output sides of the gate driver IC need to be powered.

The 1ED34x1Mc12M family (X3 Analog) is designed to support various supply configurations on the input and output side. On the output side unipolar and bipolar supply is possible.

The output stage is realized as rail-to-rail. There the gate driver voltage follows the supply voltage without an additional voltage drop. In addition it provides an easy clamping of the gate voltage during short circuit of an external IGBT.

The *RDYC* status output reports correct operation of the gate driver IC like sufficient voltage supply. The *FLT_N* status output reports failures in the application like desaturation detection.

To ensure safe operation the gate driver IC is equipped with an input and output side under-voltage lockout circuit. The UVLO levels are optimized for IGBTs.

The desaturation detection circuit protects the external IGBT from destruction at a short circuit. The gate driver IC reacts on a DESAT fault by turning off the IGBT with the adjustable soft-off method.

The soft turn-off function is used to switch-off the external IGBT in overcurrent conditions in a soft-controlled manner to protect the IGBT against collector emitter over-voltages.

An active Miller clamp function protects the IGBT from parasitic turn-on in fast switching applications.

4.1 Start-up and fault clearing

For normal operation both input and output sides of the gate driver IC need to be powered. A low level at the *FLT_N* pin always indicates a fault condition. In this case the IC starts internal mechanisms for fault clearing.

Input side start-up

1. Voltage at *VCC1* reaches the input UVLO threshold: input side of gate driver IC starts operating
2. *FLT_N* follows input supply voltage
3. Records resistor programmable function from *ADJA* and *ADJB*
4. Waits until output side is powered
5. Initiates internal start-up: Transfers configured values to output side
6. Performs internal self-test

The start-up delay takes approx. 200 µs and is part of the complete start-up time t_{START1}.

Output side start-up

1. Voltage at *VCC2* reaches the output UVLO threshold: output side of gate driver IC starts operating
2. Activates OFF gate driver output: connected gate stays discharged
3. Waits until input side is powered
4. Initiates internal start-up: Receives configured values from input side
5. Performs internal self-test

The start-up delay takes approx. 200 µs and is part of the complete start-up time t_{START2}.

The gate driver IC releases *RDYC* to high to signal a successful start-up and its readiness to operate. The gate driver IC will follow the status of the *IN* signal.

Clearing a fault with *RDYC* to low cycle

1. Set *IN* to low
2. Set *RDYC* to low for a duration longer than the fault clear time t_{CLRMIN}

3. Release *RDYC* to high
   a. If the source of the fault is no longer present, *FLT_N* is released to high
   b. If another fault source is active, *FLT_N* stays low and the cycle needs to be repeated
4. Continue PWM operation

4.2 Supply

The 1ED34x1Mc12M family (X3 Analog) is designed to support various supply configurations. The input side can be used with a 3.3 V or 5 V supply.

The output side requires either an unipolar supply (*VEE2* = *GND2*) or a bipolar supply.

- Individual supply voltages between *VCC2* and *GND2* or *GND2* and *VEE2* shall not exceed 25 V.
- The total supply voltage between *VCC2* and *VEE2* shall not exceed 35 V.

To ensure safe operation of the gate driver IC, it is equipped with an input and output side undervoltage lockout circuit.

Unipolar supply

In unipolar supply configuration the gate driver IC is typically supplied with a positive voltage of 15 V at *VCC2*. *GND2* and *VEE2* are connected together and this common potential is connected to the IGBT emitter.

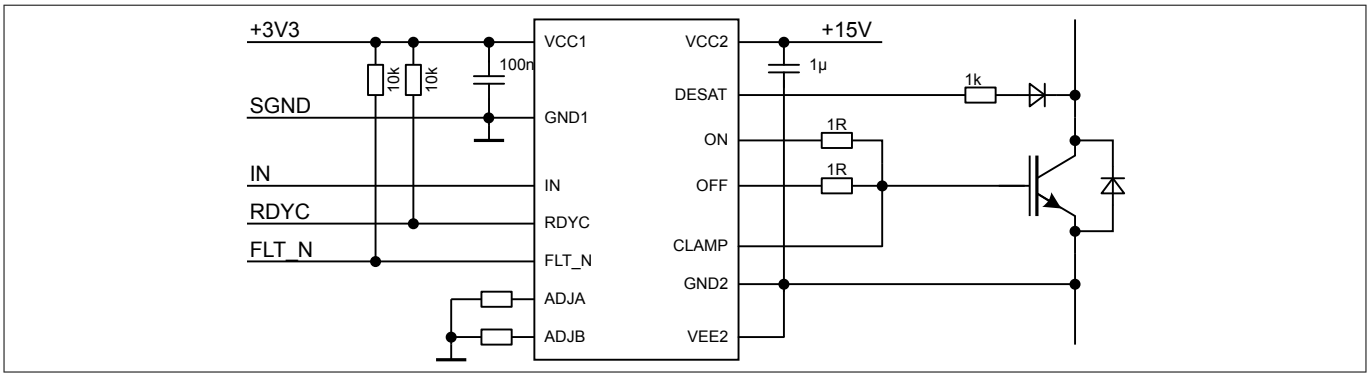


Figure 5 Application example with unipolar supply (1ED3431M)

Bipolar supply

For bipolar supply the gate driver IC is typically supplied with a positive voltage of 15 V at *VCC2* and a negative voltage of -8 V or -15 V at *VEE2* relative to *GND2*.

Between *VCC2* and *VEE2* the maximum potential difference is 35 V.

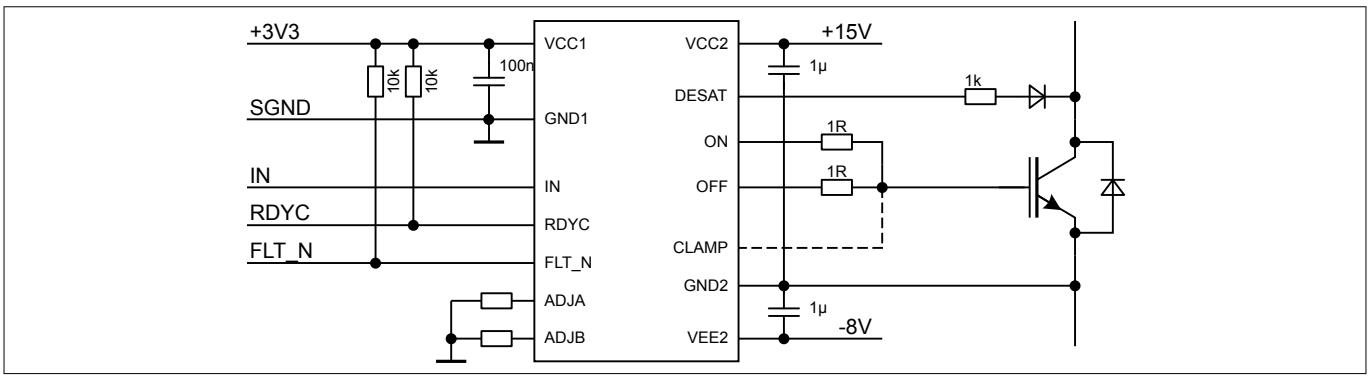


Figure 6 Application example with bipolar supply (1ED3431M)

Negative supply prevents a parasitic turn-on due to the additional voltage margin to the gate turn-on threshold.

VEE2 over GND2 supply connection check

The gate driver IC has a built-in connection check for *VEE2*. A loss of *VEE2* connection will be detected and signaled via *RDYC*.

4.2.1 Input side undervoltage lockout, *VCC1* UVLO

To ensure correct operation of the input side and safe operation of the application the gate driver IC is equipped with an input supply undervoltage lockout for *VCC1*.

UVLO behavior during start-up:

1. The voltage at the supply terminal *VCC1* reaches the V_{UVLO1H} threshold
2. The gate driver IC reads the *ADJA* and *ADJB* resistor values and transfers the configuration to the output side
3. The IC releases the *RDYC* output to **high** and is ready to operate.

The start-up delay takes approx. 200 µs and is part of the complete start-up time t_{START1}.

UVLO behavior during shut-down:

- If the supply voltage V_{VCC1} of the input side drops below V_{UVLO1L} the *RDYC* signal is switched to **low** and the output will be switched off.

The fault signal *FLT_N* follows the input supply voltage.

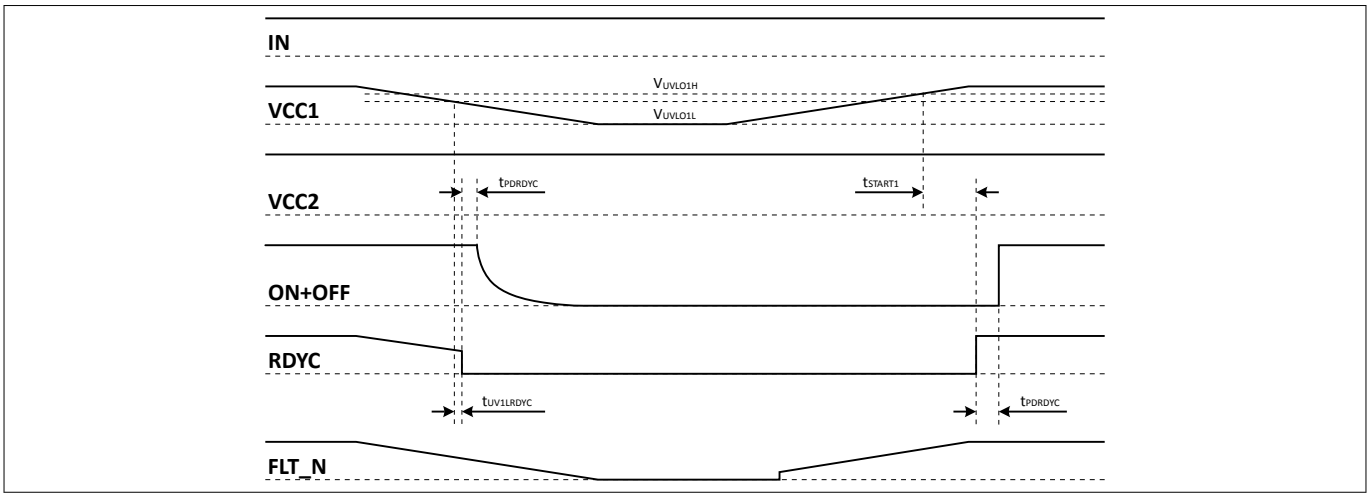


Figure 7 UVLO *VCC1* behavior

4.2.2 Output side under-voltage lockout, *VCC2* UVLO

To ensure correct operation of the output side and safe operation of the IGBT in the application, the gate driver IC is equipped with an output supply undervoltage lockout for *VCC2* versus *GND2*.

UVLO behavior during start-up:

- If the voltage at the supply terminal *VCC2* reaches the V_{UVLO2H} threshold the *RDYC* output is released to **high** and the gate driver IC is ready to operate.

The start-up delay takes approx. 200 µs and is part of the complete start-up time t_{START2}.

UVLO behavior during shut-down:

- If the supply voltage V_{VCC2} of the output side drops below V_{UVLO2L} the *RDYC* signal is switched to **low** and the output will be switched off.

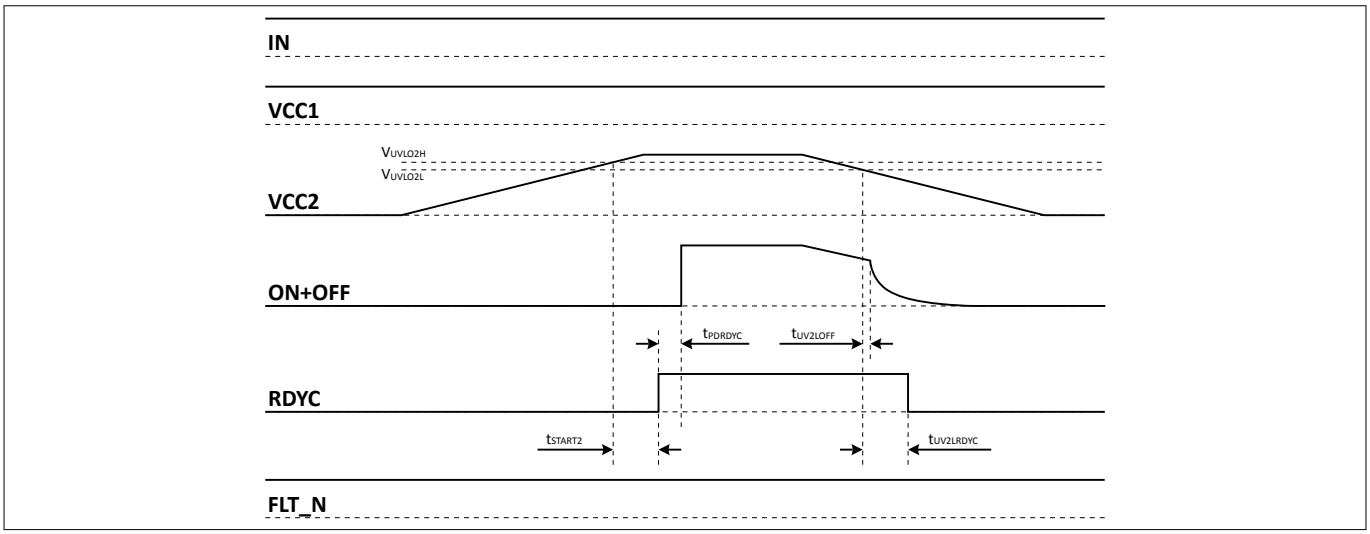


Figure 8 UVLO *VCC2* behavior

Any V_{UVLO2L} event will lead to a fault-off and a *RDYC* low level. Depending of the level of the voltage drop, the gate driver IC either stays in a not ready state and waits for the supply voltage to recover, or it will fully reset the gate driver IC. Both variants differ in the necessary delay of *RDYC* release after the supply voltage has recovered. After a reset, the gate driver IC needs to fully restart until it becomes ready again.

4.3 Input side logic

The input threshold levels are always CMOS compliant. The threshold levels are 30% of *VCC1* for low level and 70% of *VCC1* for high level.

The 1ED34x1Mc12M family (X3 Analog) has three input pins (*IN*, *ADJA*, *ADJB*) and two I/O pins (*RDYC*, *FLT_N*) at the input side.

4.3.1 IN non-inverting driver input

The input pin has a positive logic. To turn on the associated IGBT apply a logic high signal at the *IN* pin. A minimum pulse width of typical 103 ns is defined to make the IC robust against glitches at *IN*.

4.3.2 *RDYC* ready status output, fault-off and fault clear input

The *RDYC* pin is a logic input and open drain output and has three different functions:

- *RDYC* as ready status output of all ready sources
- *RDYC* as fault-off input
- *RDYC* as fault clear input

In a typical application the *RDYC* pins of all gate driver ICs in the inverter are connected together and form a single wire *RDYC* signal.

An external pull-up resistor is required to ensure *RDYC* status output during operation.

Ready sources

- the input side is properly supplied, *VCC1* supply above UVLO1 threshold
- the output side is properly supplied with a positive voltage, *VCC2* supply above UVLO2 threshold
- no *VEE2* over *GND2* failure
- Internal signal transmission is operating nominal
- the *ON* pin monitoring of the gate driver is below *VEE2* + 2 V, IGBT has to be off at start-up

4.3.2.1 *RDYC* fault-off input

Pulling *RDYC* to low disables the operation of the gate driver IC. The gate driver IC ignores *IN* signals as long as the *RDYC* pin stays low and the IC uses its fault-off function to switch-off the IGBT.

The defined minimum pulse width makes the IC robust against glitches at *RDYC*. The gate driver ignores pulses with a shorter duration.

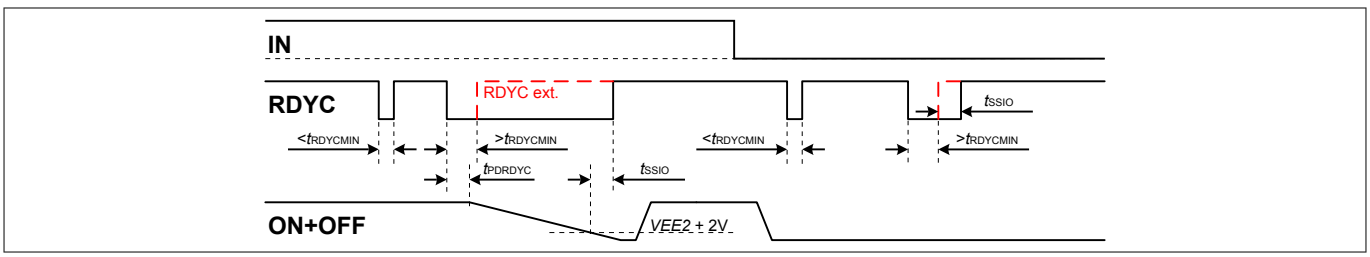


Figure 9 *RDYC* short pulse behavior of external manipulation of the *RDYC* pin

After an external *RDYC* low signal the IC is actively pulling *RDYC* to low until the voltage at *ON* pin falls below the *VEE2*+2 V threshold.

The *RDYC* fault-off input is active low.

4.3.2.2 *RDYC* fault clear input

Setting *RDYC* to low for longer than the fault clear time t_{CLRMIN} will reset the stored fault signal at pin *FLT_N* with the rising edge of *RDYC*. Additionally the following conditions have to be met as well:

- PWM *IN* pin level needs to be low,
- voltage at *ON* pin has dropped below the *VEE2*+2 V threshold, and
- triggering fault condition is no longer present.

The typical fault clear time t_{CLRMIN} is 1.0 µs.

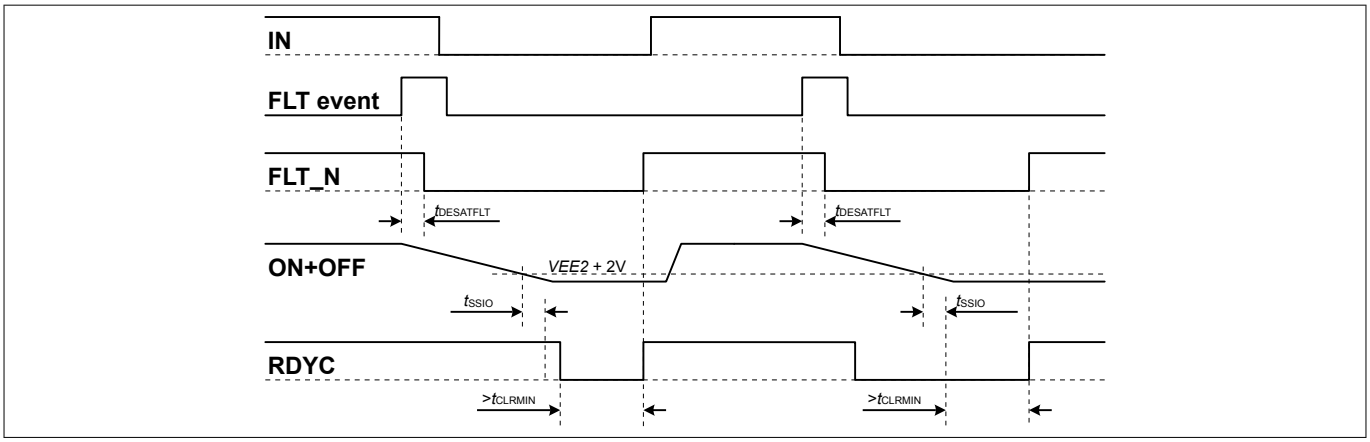


Figure 10 *RDYC* fault clear timing

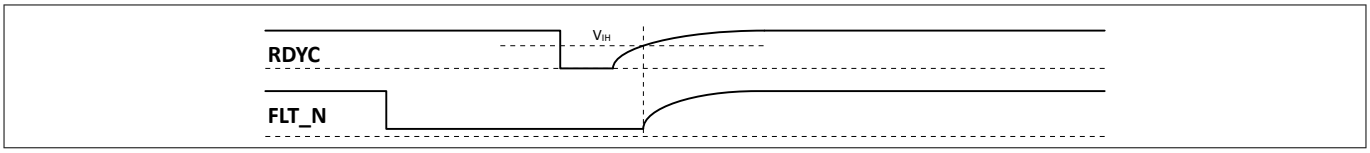


Figure 11 *RDYC* fault clear rising edge to *FLT_N*

4.3.3 *FLT_N* status output and fault-off input

The *FLT_N* pin is a logic input and open drain output and has two different functions:

- *FLT_N* as fault-status output for fault sources
- *FLT_N* as fault-off input

In a typical application the *FLT_N* pins of all gate driver ICs in the inverter are connected together and form a single wire *FLT_N* signal.

An external pull-up-resistor is required to ensure *FLT_N* status output during operation.

Fault sources

The following fault sources can trigger a *FLT_N* pin to low and initiate a fault turn-off:

- desaturation detection of IGBT
- gate driver over temperature protection

4.3.3.1 *FLT_N* fault-off input

Pulling *FLT_N* to low disables the operation of the gate driver IC. The gate driver IC ignores *IN* signals as long as the *FLT_N* pin stays low and the IC uses its fault-off function to switch-off the IGBT.

The defined minimum pulse width makes the gate driver IC robust against glitches at *FLT_N*.

After a low at the *FLT_N* pin either internally or externally applied, the fault event is latched until cleared.

The *FLT_N* fault-off input is active low.

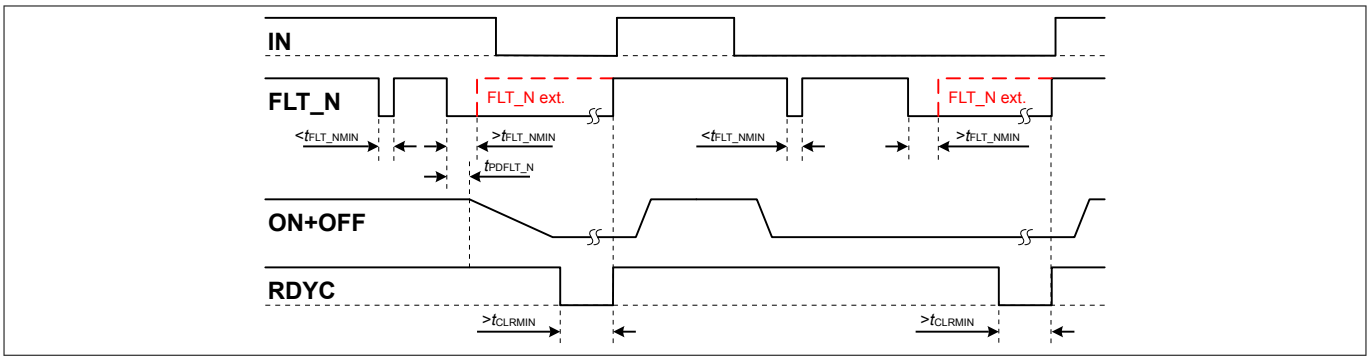


Figure 12 *FLT_N* short pulse behavior of external manipulation of the *FLT_N* pin cleared by *RDYC*

4.4 Desaturation protection

The desaturation detection circuit protects the external IGBT from destruction at a short circuit. The desaturation protection follows the given sequence:

1. Voltage at *DESAT* pin reaches DESAT threshold level, for a period of time exceeding the filter time
2. Gate driver IC output switches the external IGBT off, using the soft-off method
3. Gate driver IC switches *FLT_N* pin to low to indicate the fault to a connected microcontroller
4. Short circuit situation is resolved
   - after the voltage at the *ON* pin has dropped below the *VEE2*+2 V threshold,
   - no other fault condition is present,
   - the input has been turned off and
   - the fault has been cleared using the RDYC low cycle method

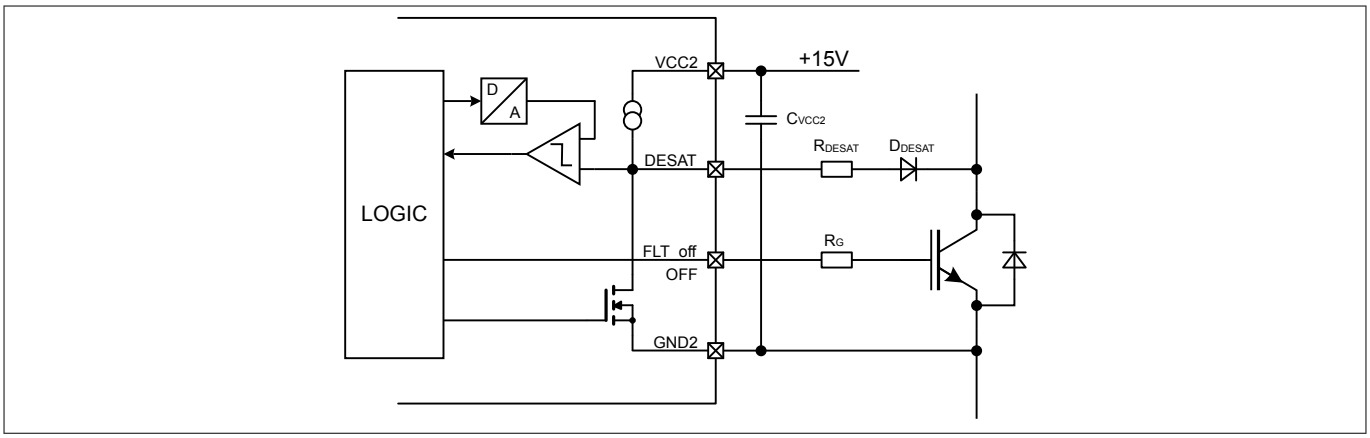


Figure 13 DESAT circuit (only relevant pins shown)

The 1ED34x1Mc12M family (X3 Analog) has a fixed DESAT threshold level of typical 9.18 V. If lower threshold levels are required, the DESAT resistor can be increased. Larger DESAT resistor values lead to lower DESAT threshold voltages. The threshold voltage reduction is equal to the DESAT current multiplied by the DESAT resistance.

The high-precision internal current source results in a minimum impact on the DESAT detection variation.

4.4.1 DESAT behavior

The DESAT function offers a leading edge blanking time and filters to optimize the DESAT detection for application usage.

The leading edge blanking inhibits threshold detection during an IGBT turn on phase. The typical IGBT turn on behavior starts with charging of the gate, commutation of the application load current and finally V_{CE} voltage decrease to V_{CEsat} voltage levels. To prevent the gate driver IC from detecting a false DESAT event, leading edge blanking pauses the DESAT circuit until the time $t_{DESATleb}$ has elapsed.

Following the leading edge blanking time, the gate driver IC forces the DESAT current into the external DESAT circuit. The current typically flows through a protection resistor, a fast high voltage diode and the collector-emitter path of the IGBT. The resulting voltage at the *DESAT* pin is the sum of the voltage drop across this path.

During a short circuit condition, the V_{CE} voltage increases, resulting in a reverse polarity condition of the DESAT diode. The remaining DESAT current also increases the voltage level at the *DESAT* pin and triggers the DESAT threshold. If the pin voltage level stays above the threshold for the duration of the DESAT filter time $t_{DESATfilter}$, the gate driver IC registers the DESAT event and acts accordingly.

The internal processing time after DESAT threshold crossing, filtering and beginning of fault-off is defined as $t_{DESATOUT}$. The duration of the gate discharge during fault-off is defined as $t_{FLTOFFtot}$ and is depending on the soft-off function and the gate load.

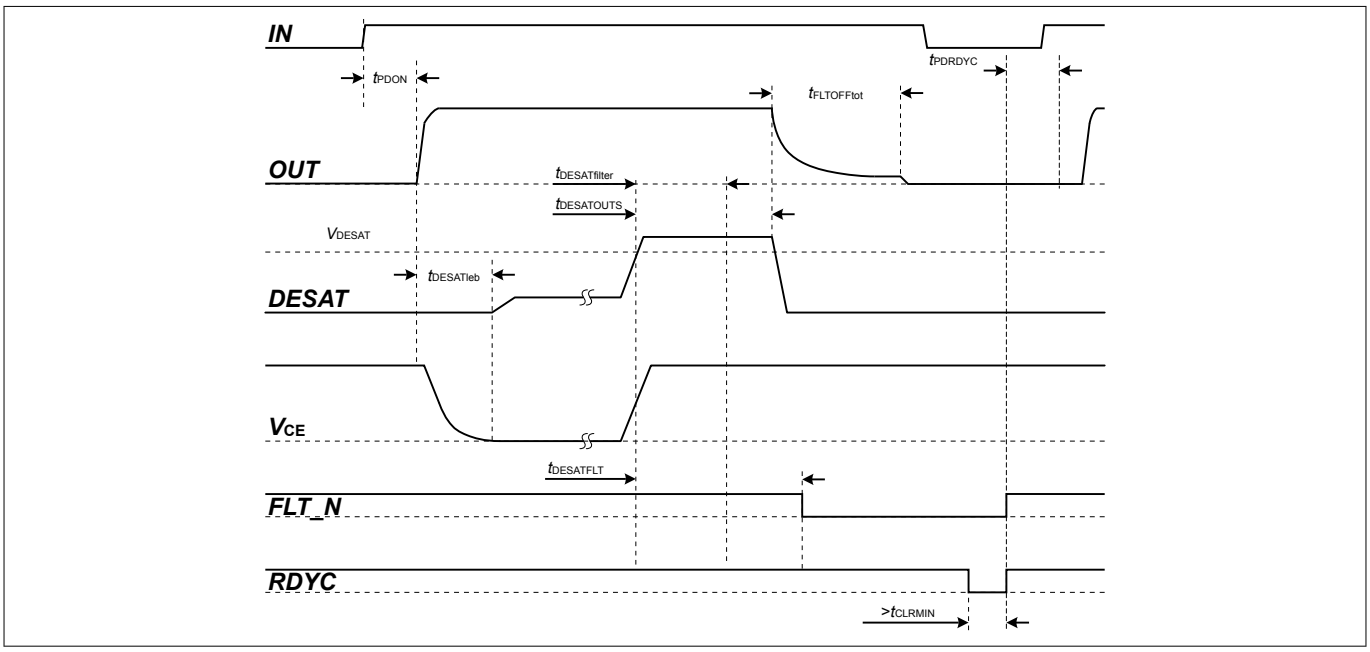


Figure 14 DESAT timing with leading edge blanking, filter and reaction times

4.4.2 DESAT filter and leading edge blanking time adjustment with *ADJB*

The *ADJB* pin configures the DESAT leading edge blanking time and DESAT filter time:

- A resistor from *ADJB* to *GND1* sets the DESAT leading edge blanking time and the DESAT filter time used during DESAT detection
- Use resistors from the E96 resistor-series with 1% tolerance values to achieve accurate parameter configuration
- The gate driver IC reads the resistor value once during start-up
- Connecting *ADJB* to *GND1* inhibits the gate driver operation and stops the start-up sequence
- Connecting *ADJB* to *VCC1* disables the filtering resulting in minimum response times

Table 4 DESAT filter timing ADJB adjustment

DESAT filter time set up	stopped	0	1	2	3	4	5	6	7
Resistance at *ADJB* to *GND1*	< 1.05 kΩ or tied to *GND1*	1.33 kΩ	1.58 kΩ	1.91 kΩ	2.26 kΩ	2.74 kΩ	3.32 kΩ	4.02 kΩ	4.87 kΩ
typ. $t_{DESATleb}$	inhibit gate driver operation	650 ns	650 ns	650 ns	650 ns	650 ns	650 ns	650 ns	650 ns
typ. $t_{DESATfilter}$		1575 ns	1775 ns	1975 ns	2375 ns	2775 ns	3175 ns	3575 ns	3975 ns

Table 4 DESAT filter timing ADJB adjustment

DESAT filter time set up	8	9	10	11	12	13	14	15	default
Resistance at *ADJB* to *GND1*	5.90 kΩ	7.15 kΩ	8.66 kΩ	10.7 kΩ	13.7 kΩ	17.4 kΩ	23.2 kΩ	28.0 kΩ	>45.3 kΩ or tied to *VCC1*
typ. $t_{DESATleb}$	1150 ns	1150 ns	1150 ns	1150 ns	1150 ns	1150 ns	1150 ns	1150 ns	400 ns
typ. $t_{DESATfilter}$	3975 ns	3575 ns	3175 ns	2775 ns	2375 ns	1975 ns	1775 ns	1575 ns	*225* ns

4.5 Gate driver output

The gate driver output side uses MOSFETs to provide a rail-to-rail output. Therefore, the gate drive voltage follows the supply voltage closely.

Due to the low internal voltage drop, the switching behavior of the IGBT is predominantly governed by the external gate resistor. The gate driver IC offers separate sink and source outputs to adapt the gate resistor for turn-on and turn-off separately without additional bypass components.

The cell value x in the following table is placeholder for high or low and indicates that this pin does not influence the resulting gate driver output state. The arrow (→) in cells indicate the transition initiated by the pin of the logic input and gate driver supply pins resulting in a transition to the gate driver output state as listed.

Table 5 Driver output state including transition behavior

Logic input and gate driver supply					**Gate driver output**	
IN	***RDYC***	***FLT_N***	***VCC1***	***VCC2***	***ON***	***OFF***
Static gate driver output state: on and off						
high	high	high	high	high	high	tri-state
low	high	high	high	high	tri-state	low
Transition to not ready and static not ready state						
x	high → low	high	high	high	→ tri-state	→ fault off
x	low	high	high	high	tri-state	low
Transition to fault and static fault state						
x	high	high → low	high	high	→ tri-state	→ fault off
x	high	low	high	high	tri-state	low
Transition with VCC1 power loss and unsupplied input side						
x	x	x	high → low	high	→ tri-state	→ fault off
x	x	x	low	high	tri-state	low
Transition with VCC2 power loss and unsupplied output side						
x	x	x	x	high → low	→ tri-state	→ fault off
x	x	x	x	low	tri-state	active shut down

4.5.1 Turn-on behavior

The 1ED34x1Mc12M family (X3 Analog) is optimized for hard switching turn-on. A turn-on command switches the *ON* pin internally to *VCC2*.

4.5.2 Turn-off and fault turn-off behavior

The gate driver IC supports different turn-off sequences to adapt to different applications and IGBT currents during normal switching operation and in the case of a fault.

Table 6 Turn-off sequences

Turn-off reason	Turn-off sequence		Remark
	Hard switching	Soft turn-off	
normal off	X		
fault turn-off		X	adjustable via *ADJA*

The gate driver fault turn-off behavior can be configured with the *ADJA* pin

Once started, the fault turn-off sequence cannot be interrupted by an *IN* = low turn-off signal.

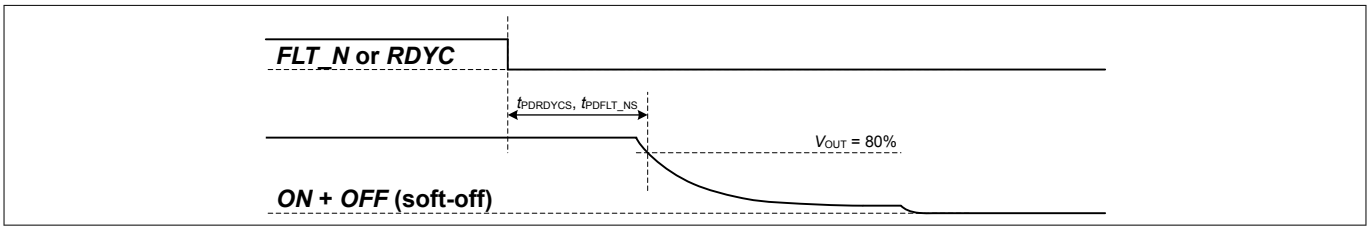


Figure 15 Fault turn-off sequence initiated by *FLT_N* or *RDYC*

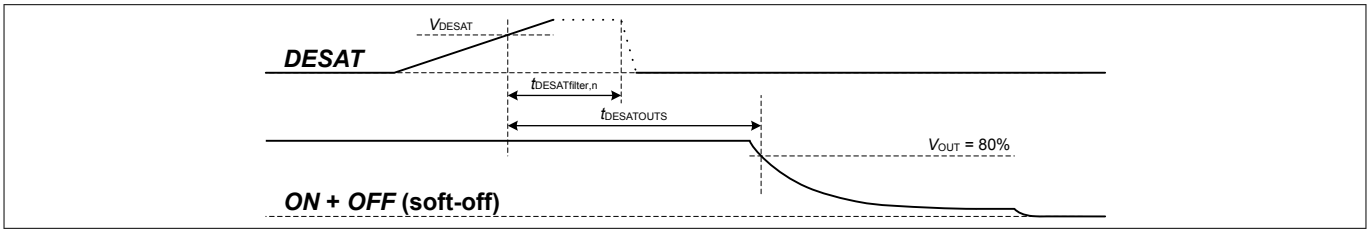


Figure 16 Fault turn-off sequence initiated by DESAT event

4.5.2.1 Hard switching turn-off

The gate driver IC supports hard switching turn-off during normal switching operation. Switching the IGBT gate off by turning on the discharge MOSFET in the output stage, the *OFF* pin is switched to *VEE2* pin.

4.5.2.2 Soft turn-off

The soft turn-off function protects the IGBT against collector-emitter overvoltage during turn off in an overcurrent condition. It turns-off the IGBT with a reduced gate current to reduce the d*i*/d*t* induced overvoltage..

The IGBT gate is connected via *OFF* to an internal current sink circuit. The discharge current is typically lower than the hard switch-off current used for normal operation. Since soft turn-off is a single event after a failure, the gate driver IC can handle the additional power dissipation internally.

Soft turn-off can be configured with the *ADJA* pin. The function is only active during fault turn-off.

The adjustable range depends on the current strength of the gate driver IC:

- 1ED3431M: 15 mA - 233 mA
- 1ED3461M: 29 mA - 466 mA
- 1ED3491M: 44 mA - 699 mA

4.5.2.2.1 Soft-off current source adjustment with *ADJA*

The *ADJA* pin configures the Soft-off function and current level:

- A resistor from *ADJA* pin to *GND1* sets the Soft-off current level for the fault-off function
- Use resistors from the E96 resistor-series with 1% tolerance values to achieve accurate parameter configuration
- The gate driver IC reads the resistor value once during start-up
- Connecting *ADJA* to *GND1* results in a Soft-off function for fault-off with a predefined value
- Connecting *ADJA* to *VCC1* inhibits the gate driver operation and stops the start-up sequence

Table 7 Soft-off adjustment with *ADJA*

Soft-off set up	default	0	1	2	3	4	5	6	7
Resistance from *ADJA* to *GND1*	< 1.05 kΩ or tied to *GND1*	1.33 kΩ	1.58 kΩ	1.91 kΩ	2.26 kΩ	2.74 kΩ	3.32 kΩ	4.02 kΩ	4.87 kΩ
typ. I_{CSOFF} 1ED3431M	146 mA	15 mA	29 mA	44 mA	58 mA	73 mA	87 mA	102 mA	116 mA
typ. I_{CSOFF} 1ED3461M	291 mA	29 mA	58 mA	87 mA	116 mA	146 mA	175 mA	204 mA	233 mA
typ. I_{CSOFF} 1ED3491M	437 mA	44 mA	87 mA	131 mA	175 mA	218 mA	262 mA	306 mA	349 mA

Table 7 Soft-off adjustment with *ADJA*

Soft-off set up	8	9	10	11	12	13	14	15	stopped
Resistance from *ADJA* to *GND1*	5.90 kΩ	7.15 kΩ	8.66 kΩ	10.7 kΩ	13.7 kΩ	17.4 kΩ	23.2 kΩ	28.0 kΩ	>45.3 kΩ or tied to *VCC1*
typ. I_{CSOFF} 1ED3431M	131 mA	146 mA	160 mA	175 mA	189 mA	204 mA	218 mA	233 mA	inhibit gate driver operation
typ. I_{CSOFF} 1ED3461M	262 mA	291 mA	320 mA	349 mA	379 mA	408 mA	437 mA	466 mA	
typ. I_{CSOFF} 1ED3491M	393 mA	437 mA	480 mA	524 mA	568 mA	612 mA	655 mA	699 mA	

4.5.3 Active shut-down

The active shut-down feature ensures a safe IGBT off-state, if the output chip is not supplied. It protects the IGBT against a floating gate. The IGBT gate is always clamped via *OFF* to *VEE2*.

4.5.4 Active Miller clamp

The 1ED34x1Mc12M family (X3 Analog) is equipped with an active Miller clamp function to protect the IGBT from parasitic turn-on in fast switching applications.

After a turn-off command the gate driver IC follows the implemented sequence:

1. Discharge of the IGBT gate while monitoring the voltage level at the *ON* pin
2. Detection of a voltage at the *ON* pin less than a level of *VEE2* + 2.0 V
3. Filtering of the detection to avoid false CLAMP activation and not to influence regular turn-off behavior
4. Activating clamp function to keep IGBT gate at *VEE2* level

4.5.4.1 CLAMP output types

The CLAMP output stage offers two operating modes:

- direct gate clamping with an open drain output for medium clamping current, 1ED3431M variants
- pre-driver output, to clamp IGBT gate with external transistor for high clamping current, 1ED3461M and 1ED3491M variants

Direct gate clamping

Direct gate clamping with an open drain output is tailored for direct clamping of IGBT gate to *VEE2*. The output current capability is typically 2 A. Useful IGBT current rating for direct gate clamping is a collector current of typically smaller than 100 A. Connect the *CLAMP* pin directly to the gate with low inductive tracks.

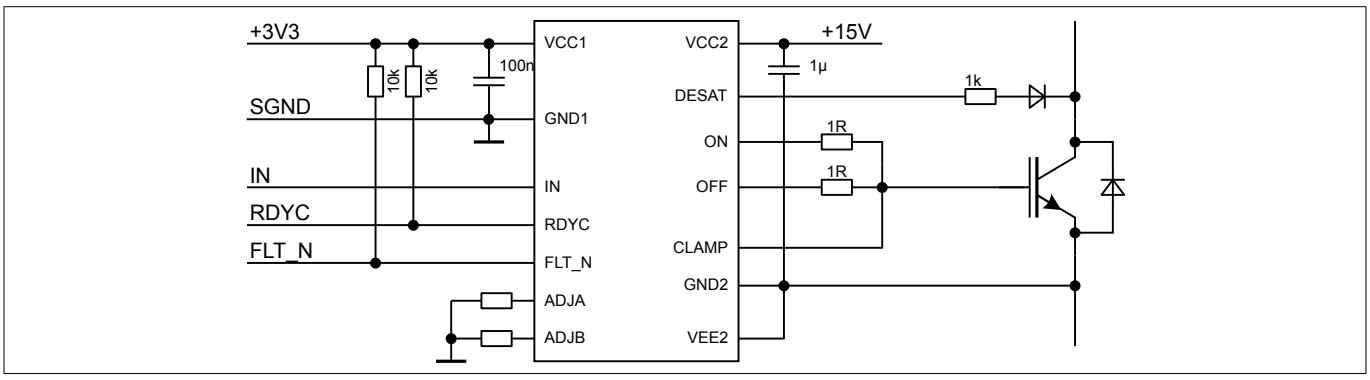


Figure 17 Application example with unipolar supply (1ED3431M)

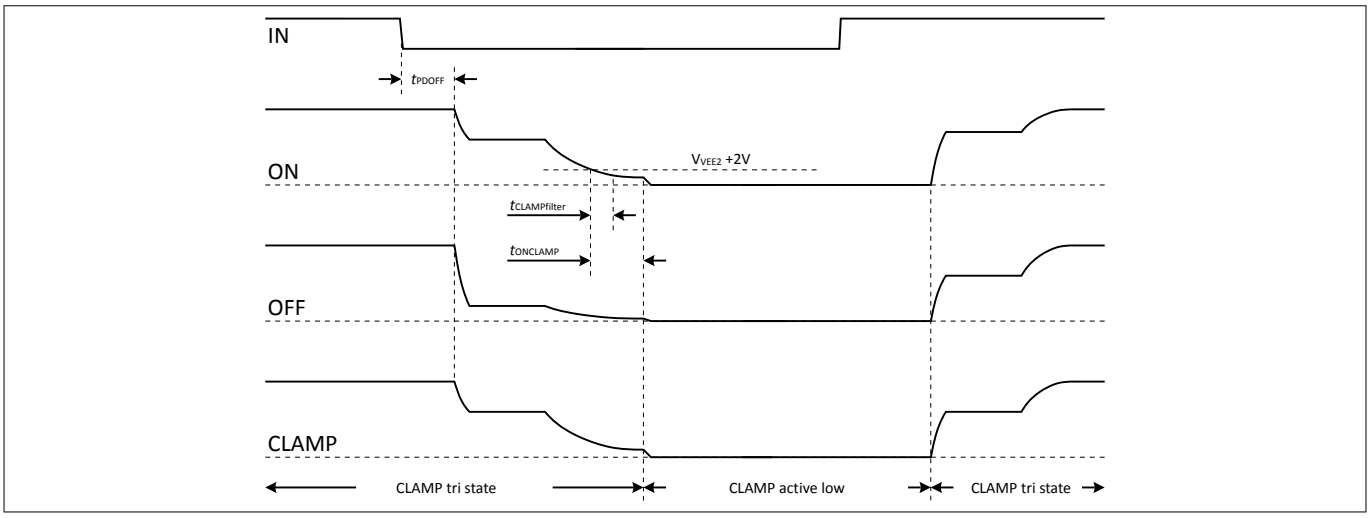


Figure 18 Direct clamp output behavior

Pre-driver output

Track inductance and clamp output resistance reduces the clamping capability for large IGBTs. In this case, select the pre-driver output product variant with an external MOSFET.

The external small signal n-channel MOSFET transistor in combination with the pre-driver output enables clamping of high gate currents. Connect the MOSFET between the *CLAMPDRV* output, *VEE2* pin, and IGBT gate. Due to the pre-driver configuration the clamp current is only limited by the external clamp MOSFET transistor. Depending on the external MOSFET a Miller current clamping up to 20 A can be reached. The clamping MOSFET has to be placed close to the IGBT gate to minimize track resistance and inductance.

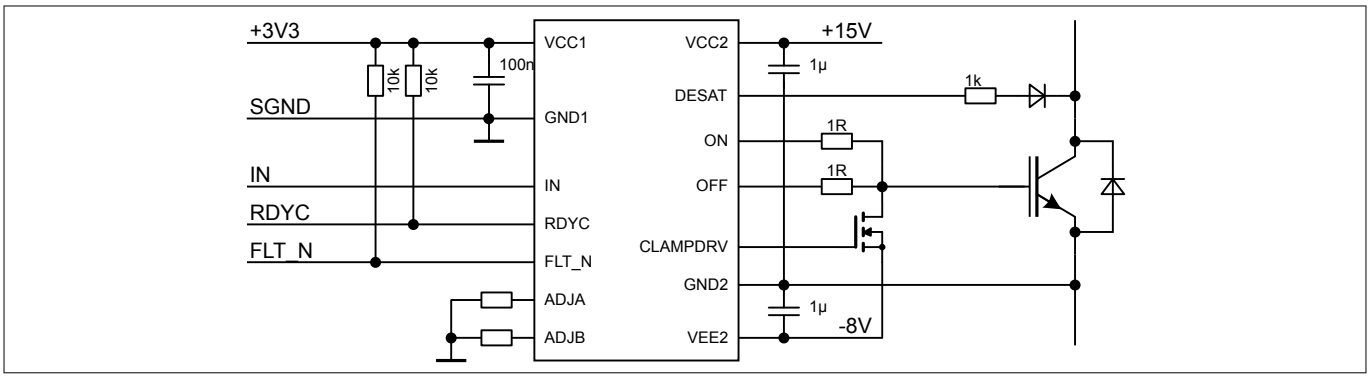


Figure 19 Application example with bipolar supply and CLAMP pre-driver output (1ED3461M, 1ED3491M)

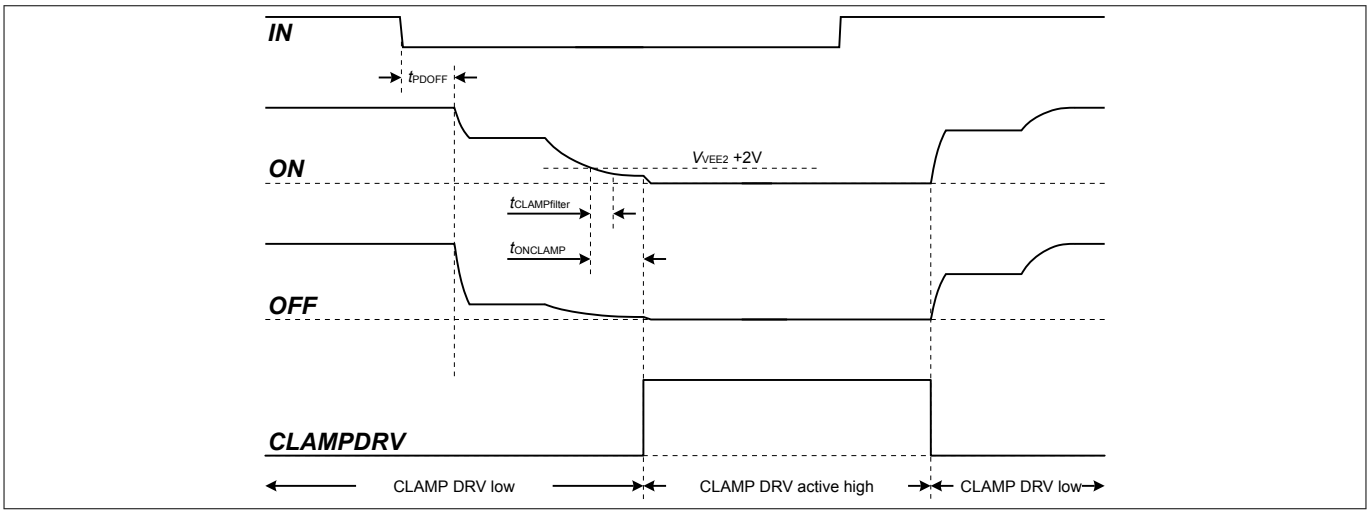


Figure 20 Clamp pre-driver output behavior

4.5.5 Switch-off timeout until forced switch-off

The gate driver IC is equipped with a switch-off timeout monitoring feature. In case the pin monitoring comparator has not registered an off-state within the timeout time this feature activates a forced switch-off.

The monitoring feature secures the IGBT switch-off in case of a connection failure between the *OFF* output and the IGBT gate or a faulty gate resistor. In a forced switch-off all available output switch-off paths (*OFF* and *CLAMP*/*CLAMPDRV*) will be used to hard switch-off the IGBT after such an event.

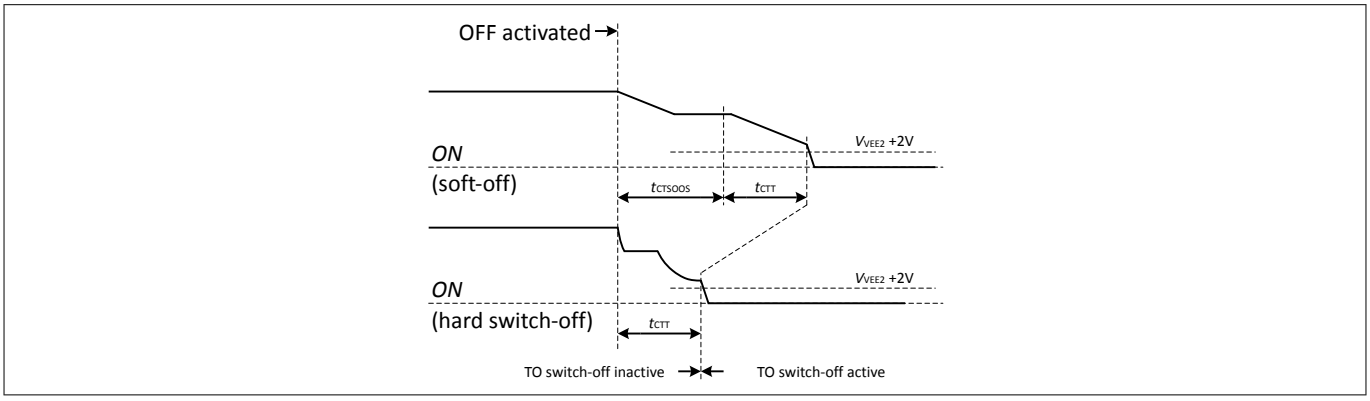


Figure 21 Switch-off timeout behavior

The timing diagram shows the switch-off timeout behavior from the moment of *OFF* output activation until the timeout has elapsed and the *CLAMP* output is activated.

4.6 Short circuit clamping

The integrated short circuit clamping diode limits the IGBT gate over voltage during a short circuit. The over voltage is typically triggered by the capacitive feedback of the Miller capacitance.

The internal diodes from *ON* and *CLAMP* to *VCC2* limit the gate driver voltage to a value slightly higher than the supply voltage. These diode paths are rated for a maximum current of 0.75 A and the duration of 6 µs. Add an external Schottky diode if higher currents are expected or a tighter clamping is desired. Also use an external diode if the active Miller clamping circuit uses the pre-driver output configuration.

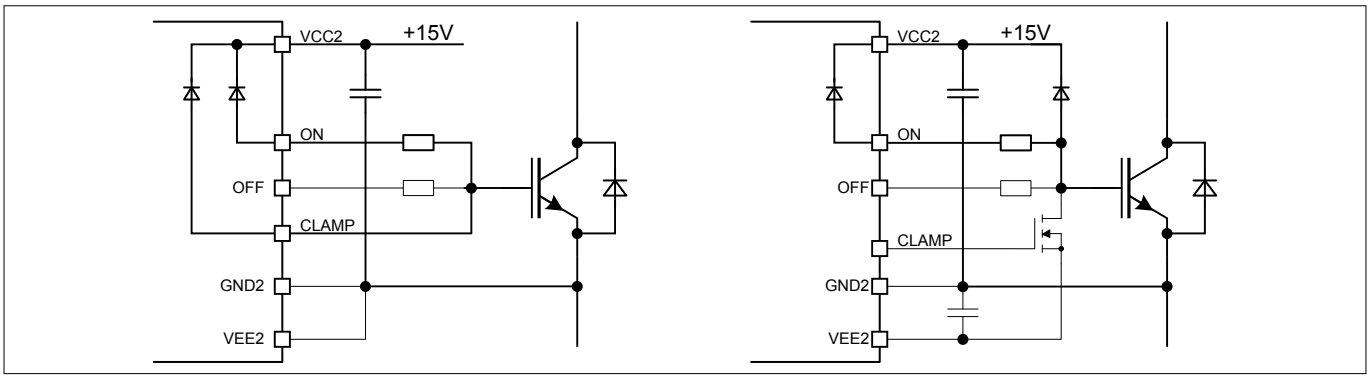


Figure 22 Short circuit clamping circuitry

5 Electrical parameters

5.1 Absolute maximum ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise noted all voltages are given with respect to their respective GND (GND1 for pins 1 to 8, GND2 for pins 9 to 16).

Table 8 Absolute maximum ratings

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input to output offset voltage	V_{OFFSET}	–	2300	V	$V_{VEE2,max}$-$V_{VEE2,min}$ with $V_{VEE2,max} \geq V_{GND1} \geq V_{VEE2,min}$ 1) 2)
Supply voltage input side	V_{VCC1}	-0.3	6.5	V	–
Logic input voltage (*IN*)	$V_{LogicIN}$	-0.3	6.5	V	–
Logic input voltage (*RDYC*, *FLT_N*)	$V_{LogicRF}$	-0.3	6.5	V	–
Logic input voltage (*ADJA*, *ADJB*)	$V_{LogicAD}$	-0.3	6.5	V	–
Open drain logic output current (*RDYC*, *FLT_N*)	$I_{LogicOC}$	–	10	mA	–
Positive supply voltage output side	V_{VCC2}	-0.3	40	V	–
Negative supply voltage output side	V_{VEE2}	-40	0.3	V	–
Maximum supply voltage difference output side (V_{VCC2} - V_{VEE2})	V_{max2}	–	40	V	–
DESAT input voltage	V_{DESAT}	-0.3	V_{VCC2} +0.3	V	–
CLAMP input voltage	V_{CLAMP}	V_{VEE2} -0.3	V_{VCC2} +0.3	V	3)
Maximum *CLAMP* output current	I_{CLAMP}	–	2.4	A	$t < 5$ µs
Gate driver output voltage (*ON*, *OFF*)	V_{OUT}	V_{VEE2} -0.3	V_{max2} +0.3	V	–
Maximum *CLAMP* to *VCC2* diode IGBT short circuit clamping time	t_{CLP}	–	6	µs	$I_{CLAMP/OUT}$ = 0.75 A
Junction temperature	T_J	-40	150	°C	–
Storage temperature	T_{Stg}	-55	150	°C	–
Power dissipation, input side	$P_{D,IN}$	–	100	mW	@T_A = 25 °C
Power dissipation, output side	$P_{D,OUT}$	–	700	mW	@T_A = 25°C 4)
ESD capability: Human body model	V_{ESDHBM}	–	2	kV	5)
ESD capability: Charged device model	V_{ESDCDM}	–	500	V	6)

1) for functional operation only
2) See also Chapter 6 on page 41
3) May be exceeded during short circuit clamping.
4) Derating the power above 65°C with 8 mW/°C

5) According to ANSI/ESDA/JEDEC-JS-001-2017 (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).
6) According to ANSI/ESDA/JEDEC-JS-002-2014 (TC = test condition in volt)

5.2 Thermal parameters

Thermal performance may change significantly with layout and heat dissipation of components in close proximity.

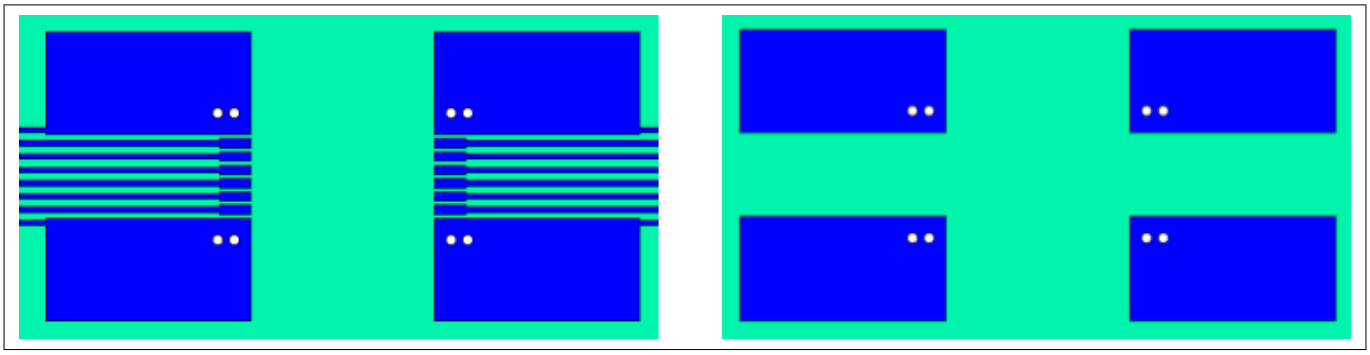


Figure 23 Reference layout for thermal data (Two layer PCB; copper thickness 35 µm; left: top layer; right: bottom layer)

The PCB layout represents the reference layout used for the thermal characterization. Pins 1 and 8 (*GND1*) and pins 9 and 16 (*VEE2*) require ground plane connections for achieving maximum power dissipation. The 1ED34x1Mc12M family (X3 Analog) is conceived to dissipate most of the heat generated through these pins.

Table 9 Thermal parameters

Parameter	Symbol	Value	Unit	Note / Test Condition
Thermal resistance junction to ambient	$R_{THJA,OUT}$	122	K/W	@T_A = 65°C, $P_{D,\,OUT}$ = 400 mW, $P_{D,\,IN}$ = 50 mW, 4 layer test PCB, PG-DSO-16
Characterization parameter junction to package top input side	Ψ_{Jtop}	8	K/W	

5.3 Operating parameters

Note: Within the operating range the IC operates as described in the functional description. Unless otherwise noted all voltages are given with respect to their respective GND (GND1 for pins 1 to 8, GND2 for pins 9 to 16).

Table 10 Operating parameters

Parameter[1)]	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Supply voltage input side	V_{VCC1}	3.0	5.5	V	–
Logic input voltages (*IN*, *RDYC*, *FLT_N*)	$V_{LogicIN}$	-0.3	5.5	V	–
Positive supply voltage output side	V_{VCC2}	13	25	V	–
Negative supply voltage output side	V_{VEE2}	-25	0	V	–

(table continues...)

Table 10 (continued) Operating parameters

Parameter[1]	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Supply voltage difference output side (V_{VCC2} - V_{VEE2})	V_{max2}	13	35	V	–
Ambient temperature	T_A	-40	125	°C	[2]
Switching frequency	f_{SW}	0	250	kHz	max P_D applies
Common mode transient immunity	$\|CMTI\|$	0	200	V/ns	$V_{OFFSET,test}$ = 1500 V

1) Parameter is not subject to production test - verified by design/characterization
2) T_J has to be below over temperature protection temperature T_{OTPOFF}

5.4 Electrical characteristics

Note: The electrical characteristics include the spread of values in supply voltages, load, and junction temperatures within the operating parameters unless specified otherwise. Typical values represent the median values at T_A = 25°C. Unless otherwise noted all voltages are given with respect to their respective GND (GND1 for pins 1 to 8, GND2 for pins 9 to 16).

5.4.1 Voltage supply

Table 11 Voltage supply

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VCC1 UVLO threshold	V_{UVLO1H}	–	2.95	3.05	V	–
	V_{UVLO1L}	2.6	2.8	–	V	–
VCC1 UVLO hysteresis (V_{UVLO1H} - V_{UVLO1L})	V_{HYS1}	0.1	0.14	–	V	–
VCC1 quiescent current	I_{Q1}	–	2.4	4.0	mA	V_{VCC1} = 3.3 V, *IN* = High, *RDYC* = High, *FLT_N* = High
VCC1 operating current	I_{O1}	–	2.4	4.0	mA	V_{VCC1} = 3.3 V, *IN* = 16 kHz, 50%, *RDYC* = High, *FLT_N* = High
VCC2 UVLO threshold	$V_{UVLO2H,0}$	–	12.0	12.6	V	
	$V_{UVLO2L,0}$	10.4	11.0	–	V	
VCC2 UVLO hysteresis ($V_{UVLO2H,0}$ - $V_{UVLO2L,0}$)	$V_{HYS2,0}$	0.75	1.0	–	V	
VEE2 not connected detection threshold	$V_{VEE2,NC}$	–	0.5	–	V	V_{VEE2} - V_{GND2}
VCC2 quiescent current	I_{Q2}	–	3.9	5	mA	V_{VCC2} = 15 V, V_{VEE2} = -8 V, *OUT* = High, *DESAT* = Low
VCC2 operating current	I_{O2}	–	3.9	5	mA	V_{VCC2} = 15 V, V_{VEE2} = -8 V, *OUT* = 16 kHz, 50%, *DESAT* = Low, C_{LOAD} = 100 pF

5.4.2 Logic input and output

Table 12 Logic input and output

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Logic low input voltage (*IN*, *RDYC*, *FLT_N*)	$V_{LogicINL}$	–	–	30	%	of V_{VCC1}
Logic high input voltage (*IN*, *RDYC*, *FLT_N*)	$V_{LogicINH}$	70	–	–	%	of V_{VCC1}
Logic low output voltage (*RDYC*, *FLT_N*)	V_{RDYC5}, V_{FLT_N5}	–	–	300	mV	I_{SINK} = 5 mA
Logic input pull down resistor (*IN*)	R_{INPD}	33	40	47	kΩ	–
Logic input pull down resistor (*RDYC*, *FLT_N*)	R_{RDYCPD}, R_{FLT_NPD}	0.8	1.0	1.2	MΩ	–

5.4.3 Analog input

Resistor values outside of the 1% tolerance range results in the gate driver IC selecting either the lower or higher step for the corresponding function.

Table 13 Analog input

Parameter[1)]	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Analog input resistor (*ADJA*, *ADJB*)	R_{ADJx0}	–	1.33	–	kΩ	all resistor values are from the E96-series with 1% tolerance
	R_{ADJx1}	–	1.58	–		
	R_{ADJx2}	–	1.91	–		
	R_{ADJx3}	–	2.26	–		
	R_{ADJx4}	–	2.74	–		
	R_{ADJx5}	–	3.32	–		
	R_{ADJx6}	–	4.02	–		
	R_{ADJx7}	–	4.87	–		
	R_{ADJx8}	–	5.90	–		
	R_{ADJx9}	–	7.15	–		
	R_{ADJx10}	–	8.66	–		
	R_{ADJx11}	–	10.7	–		
	R_{ADJx12}	–	13.7	–		
	R_{ADJx13}	–	17.4	–		
	R_{ADJx14}	–	23.2	–		
	R_{ADJx15}	–	28.0	–		

1) Parameter is not subject to production test - verified by design/characterization

5.4.4 Gate driver

Note: High and low level output currents are absolute values without an information of current direction.

Table 14 Gate driver

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High level output voltage	V_{ON0}	–	V_{VCC2} + 0.87	V_{VCC2} + 1.01	V	I_{ON} = 500 mA[1]
High level output peak current 1ED3431M	I_{ON}	2.6	3.8	–	A	[2] [3] C_{LOAD} = 33 nF
High level output on resistance 1ED3431M	$R_{DSON,H}$	0.51	1.12	2.24	Ω	I_{ON} = 67 mA[3]
Low level output peak current 1ED3431M	I_{OFF}	2.0	2.5	–	A	[2] [4] C_{LOAD} = 33 nF
Low level ouput on resistance 1ED3431M	$R_{DSON,L}$	0.31	0.82	1.64	Ω	I_{OFF} = 67 mA[4]
High level output peak current 1ED3461M	I_{ON}	5.2	7.5	–	A	[2] [3] C_{LOAD} = 68 nF
High level output on resistance 1ED3461M	$R_{DSON,H}$	0.26	0.56	1.13	Ω	I_{ON} = 133 mA[3]
Low level output peak current 1ED3461M	I_{OFF}	4.0	5.0	–	A	[2] [4] C_{LOAD} = 68 nF
Low level ouput on resistance 1ED3461M	$R_{DSON,L}$	0.16	0.41	0.83	Ω	I_{OFF} = 133 mA[4]
High Level output peak current 1ED3491M	I_{ON}	7.9	11	–	A	[2] [3] C_{LOAD} = 100 nF
High level output on resistance 1ED3491M	$R_{DSON,H}$	0.17	0.38	0.75	Ω	I_{ON} = 200 mA[3]
Low Level output peak current 1ED3491M	I_{OFF}	6.0	7.5	–	A	[2] [4] C_{LOAD} = 100 nF
Low level ouput on resistance 1ED3491M	$R_{DSON,L}$	0.11	0.28	0.55	Ω	I_{OFF} = 200 mA[4]
Active Shut Down Voltage *OFF* 1ED3431M	V_{ACTSD}[5]	–	–	V_{VEE2} +2.4	V	I_{OUT} = 67 mA,V_{VCC2} open
Active Shut Down Voltage *OFF* 1ED3461M	V_{ACTSD}[5]	–	–	V_{VEE2} +2.4	V	I_{OUT} = 133 mA,V_{VCC2} open
Active Shut Down Voltage *OFF* 1ED3491M	V_{ACTSD}[5]	–	–	V_{VEE2} +2.4	V	I_{OUT} = 200 mA,V_{VCC2} open

1) Integrated diode *ON* vs. *VCC2* clamping test
2) Parameter is not subject to production test - verified by design/characterization
3) *IN* = High, *ON* = High; *VCC2-ON* = 15 V; R_G = 0.1 Ω; *VCC2* = 15 V; *VEE2* = -8 V
4) *IN* = Low, *OFF* = Low; *OFF-VEE2* = 15 V; R_G = 0.1 Ω; *VCC2* = 15 V; *VEE2* = -8 V

5) With reference to *VEE2*

5.4.5 Active Miller clamp

Table 15 Active Miller clamp

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High level clamp voltage	$V_{CLAMPH0}$	–	V_{VCC2} +1.5	V_{VCC2} +1.63	V	I_{CLAMP} = 500 mA[1) 2)]
	$V_{CLAMPH1}$	–	V_{VCC2} +0.9	V_{VCC2} +1.1	V	I_{CLAMP} = 50 mA[1) 2)]
Clamp-driver high level output voltage (1ED3461M, 1ED3491M)	$V_{CLAMPDH1}$	V_{VEE2}+7.5	V_{VEE2}+9.5	V_{VEE2}+11.5	V	I_{CLAMPH} = 5 mA[3)]
	$V_{CLAMPDH2}$	V_{VEE2}+4.5	V_{VEE2}+6.7	–	V	I_{CLAMPH} = 50 mA[3)]
Clamp-driver high level output peak current (1ED3461M, 1ED3491M)	I_{CLAMPH}	0.20	0.27	–	A	[4)] *VCC2* = 15 V; *VEE2* = 0 V; C_{CLAMP} = 100 nF; R_{CLAMP} = 1 Ω
Clamp/Clamp-driver output low level current	$I_{CLAMPL,2}$	1.1	1.8	–	A	[4)] *VCC2* = 15 V; *VEE2* = 0 V; V_{CLAMP} = 2 V; C_{CLAMP} = 100 nF; R_{CLAMP} = 0.1 Ω
Clamp/Clamp-driver output low level current	$I_{CLAMPL,5}$	2.2	3.5	–	A	[4)] *VCC2* = 15 V; *VEE2* = 0 V; V_{CLAMP} = 5 V; C_{CLAMP} = 100 nF; R_{CLAMP} = 0.1 Ω
Clamp/Clamp-driver output low level ON resistance	$R_{DSON,CLP}$	0.50	0.85	1.35	Ω	I_{CLAMPL} = 200 mA
Clamp threshold voltage	V_{ON_CLAMP}	1.5	2.0	2.5	V	Related to *VEE2*
Clamp filter time	$t_{CLAMPfilter}$	195	235	275	ns	
CLAMP reaction time in CLAMP mode	t_{CLAMP_ON}	16 + $t_{CLAMPfilter}$	23 + $t_{CLAMPfilter}$	35 + $t_{CLAMPfilter}$	ns	[4) 5)] C_{LOAD} = 100 pF
CLAMP reaction time in CLAMP driver mode	t_{CLAMPD_ON}	24 + $t_{CLAMPfilter}$	35 + $t_{CLAMPfilter}$	53 + $t_{CLAMPfilter}$	ns	[4) 6)] C_{LOAD} = 100 pF
Switch-off time-out time	t_{CTT}	–	2.4	–	µs	[4)]
Switch-off time-out soft-off offset time	t_{CTSOOS}	–	2.4	–	µs	[4)] additional time-out delay during soft-off

1) Integrated diode *CLAMP* vs. *VCC2* clamping test
2) only valid for direct clamping: *IN* = High, *OUT* = High
3) only valid for clamp pre-driver output: *IN* = Low, *OUT* = Low
4) Parameter is not subject to production test - verified by design/characterization
5) CLAMP mode reaction time specified with 3.3 kΩ pull-up from *CLAMP* to 3.3 V, from CLAMP threshold until reaching 0.8 V (falling) at *CLAMP* pin

6) CLAMP driver mode reaction time specified from CLAMP threshold until reaching 0.8 V (rising) at *CLAMP(DRV)* pin

5.4.6 Dynamic characteristics

Dynamic characteristics are measured with V_{VCC1} = 5 V, V_{VCC2} = 15 V and V_{VEE2} = -8 V unless specified otherwise.

Table 16 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input pulse suppression time *IN*	t_{INMIN}	98	103	108	ns	–
Input pulse suppression time *RDYC*/*FLT_N* for enable / fault off	$t_{RDYCMIN}$, t_{FLT_NMIN}	85	100	115	ns	–
Input pulse width *RDYC* for *FLT_N* reset (Fault clear time)	t_{CLRMIN}	–	1.0	1.2	µs	
Input *IN* to output propagation delay *ON*	t_{PDON}	226	244	270	ns	C_{LOAD} = 100 pF, V_{IN} = 70%, V_{OUT}=20%
Input *IN* to output propagation delay *OFF*	t_{PDOFF}	218	236	262	ns	C_{LOAD} = 100 pF, V_{IN} = 30%, V_{OUT}=80%
Input to output propagation delay distortion (t_{PDOFF} - t_{PDON})	t_{PDISTO}	-23	-8	7	ns	C_{LOAD} = 100 pF
Input *IN* to output propagation delay distortion between any devices (t_{PDON}-t_{PDON}) or (t_{PDOFF}-t_{PDOFF})	t_{PDD}	–	–	30	ns	*1)* same conditions (V_{IN}, V_{VCC1}, V_{VCC2} and V_{VEE2}, C_{LOAD}, T_A)
State synchronization time between input and output	t_{SSIO}	–	–	13	µs	*1)*
Input *RDYC* to output on propagation delay	t_{PDRDYC}	447	523	600	ns	C_{LOAD} = 100 pF; *IN* high; V_{RDYC} = 70%, V_{OUT}=20%
Input *RDYC* or *FLT_N* to Soft-off output propagation delay	$t_{PDRDYCS}$, t_{PDFLT_NS}	323	361	407	ns	C_{LOAD} = 100 pF, V_{Signal} = 30%, V_{OUT}=80%, Soft-off function $I_{CSOFF,15}$
Input RDYC or FLT_N to hard switch-off output propagation delay	$t_{PDRDYCH}$, t_{PDFLT_NH}	303	342	384	ns	C_{LOAD} = 100 pF, V_{Signal} = 30%, V_{OUT}=80%, OFF function
Rise time 1ED3431M	t_{RISE}	–	15	30	ns	C_{LOAD} = 1 nF, V_{OUT}: 20% to 80%

(table continues...)

Table 16 (continued) Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Fall time 1ED3431M	t_{FALL}	–	15	30	ns	C_{LOAD} = 1 nF, V_{OUT}: 80% to 20%
Rise time 1ED3461M	t_{RISE}	–	15	30	ns	C_{LOAD} = 2.2 nF, V_{OUT}: 20% to 80%
Fall Time 1ED3461M	t_{FALL}	–	15	30	ns	C_{LOAD} = 2.2 nF, V_{OUT}: 80% to 20%
Rise Time 1ED3491M	t_{RISE}	–	15	30	ns	C_{LOAD} = 3.3 nF, V_{OUT}: 20% to 80%
Fall Time 1ED3491M	t_{FALL}	–	15	30	ns	C_{LOAD} = 3.3 nF, V_{OUT}: 80% to 20%

1) Parameter is not subject to production test - verified by design/characterization

5.4.7 Desaturation protection

All parameters valid for *VCC1* = 5 V, *VCC2* = 15 V, and *VEE2* = 0 V unless specified otherwise.

Table 17 Desaturation protection

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
DESAT charge current	I_{DESATC}	470	500	525	µA	V_{DESAT} = 0 V
DESAT voltage divider resistance	R_{DVD}	259	312.5	366	kΩ	between *DESAT* and *GND2* pins
DESAT clamp and discharge ON resistance	$R_{DSON,D}$	–	7.7	25.0	Ω	I_{DESATD} = 200 mA
DESAT threshold level	V_{DESAT}	8.88	9.18	9.48	V	–
DESAT leading edge blanking time	$t_{DESATleb,d}$	356	400	444	ns	*ADJB* depending, V_{ON} 20% rising to V_{DESAT} = 1 V, C_{LOAD} = 100 pF, C_{DESAT} = 2 pF,
	$t_{DESATleb,s}$	597	650	703	ns	
	$t_{DESATleb,l}$	1077	1150	1223	ns	
DESAT filter time (default)	$t_{DESATfilter,def}$	190	*225*	263	ns	*ADJB* = *VCC1*
DESAT filter time (*ADJB* adjustable)	$t_{DESATfilter,A}$	1476	1575	1684	ns	*ADJB* depending
	$t_{DESATfilter,B}$	1667	1775	1895	ns	
	$t_{DESATfilter,C}$	1857	1975	2105	ns	
	$t_{DESATfilter,D}$	2238	2375	2526	ns	
	$t_{DESATfilter,E}$	2619	2775	2947	ns	
	$t_{DESATfilter,F}$	3000	3175	3368	ns	

(table continues...)

Table 17 (continued) Desaturation protection

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
	$t_{DESATfilter,G}$	3381	3575	3789	ns	
	$t_{DESATfilter,H}$	3762	3975	4211	ns	
DESAT sense to *FLT_N* low delay	$t_{DESATFLT}$	623	743	883	ns	V_{FLT_N} = 30%, I_{FLT_N} = 5 mA, $t_{DESATfilter,def}$, C_{FLT_N} = 100 pF
DESAT sense to *OFF* low delay, Soft-off	$t_{DESATOUTS}$	287 + $t_{DESATfilter}$	333 + $t_{DESATfilter}$	382 + $t_{DESATfilter}$	ns	V_{OUT} = 80%, C_{LOAD} = 100 pF, $I_{CSOFF,15}$

5.4.8 Soft-off current source

Soft-off current source values specified at *OFF* pin at V_{OFF} = 3 V with unipolar supply of V_{VCC2} = 15 V.

Table 18 Current source turn-off

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Soft-off current source current 1ED3431M	$I_{CSOFF,0}$	10	15	19	mA	depends on resistor value at *ADJA*
	$I_{CSOFF,1}$	24	29	36	mA	
	$I_{CSOFF,2}$	35	44	52	mA	
	$I_{CSOFF,3}$	47	58	70	mA	
	$I_{CSOFF,4}$	58	73	87	mA	
	I_{CSOFF5}	70	87	105	mA	
	$I_{CSOFF,6}$	82	102	122	mA	
	$I_{CSOFF,7}$	93	116	140	mA	
	$I_{CSOFF,8}$	105	131	157	mA	
	$I_{CSOFF,9}$	116	146	175	mA	
	$I_{CSOFF,10}$	128	160	192	mA	
	$I_{CSOFF,11}$	140	175	210	mA	
	$I_{CSOFF,12}$	151	189	227	mA	
	$I_{CSOFF,13}$	163	204	245	mA	
	$I_{CSOFF,14}$	175	218	262	mA	
	$I_{CSOFF,15}$	186	233	280	mA	
Soft-off current source current 1ED3461M	$I_{CSOFF,0}$	22	29	36	mA	depends on resistor value at *ADJA*
	$I_{CSOFF,1}$	45	58	72	mA	
	$I_{CSOFF,2}$	70	87	105	mA	
	$I_{CSOFF,3}$	93	116	140	mA	
	$I_{CSOFF,4}$	116	146	175	mA	
	$I_{CSOFF,5}$	140	175	210	mA	
	$I_{CSOFF,6}$	163	204	245	mA	
	$I_{CSOFF,7}$	186	233	280	mA	
	$I_{CSOFF,8}$	210	262	314	mA	
	$I_{CSOFF,9}$	233	291	349	mA	
	$I_{CSOFF,10}$	256	320	384	mA	
	$I_{CSOFF,11}$	280	349	419	mA	
	$I_{CSOFF,12}$	303	379	454	mA	
	$I_{CSOFF,13}$	326	408	489	mA	
	$I_{CSOFF,14}$	349	437	524	mA	

(table continues...)

Table 18 (continued) Current source turn-off

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
	$I_{CSOFF,15}$	373	466	559	mA	
Soft-off current source current 1ED3491M	$I_{CSOFF,0}$	34	44	54	mA	depends on resistor value at *ADJA*
	$I_{CSOFF,1}$	70	87	105	mA	
	$I_{CSOFF,2}$	105	131	157	mA	
	$I_{CSOFF,3}$	140	175	210	mA	
	$I_{CSOFF,4}$	175	218	262	mA	
	$I_{CSOFF,5}$	210	262	314	mA	
	$I_{CSOFF,6}$	245	306	367	mA	
	$I_{CSOFF,7}$	280	349	419	mA	
	$I_{CSOFF,8}$	314	393	472	mA	
	$I_{CSOFF,9}$	349	437	524	mA	
	$I_{CSOFF,10}$	384	480	577	mA	
	$I_{CSOFF,11}$	419	524	629	mA	
	$I_{CSOFF,12}$	454	568	681	mA	
	$I_{CSOFF,13}$	489	612	734	mA	
	$I_{CSOFF,14}$	524	655	786	mA	
	$I_{CSOFF,15}$	559	699	839	mA	

5.4.9 Over-temperature protection

Table 19 Over-temperature protection

Parameter[1)]	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Over-temperature protection level	T_{OTPOFF}	150	160	170	°C	

1) Parameter is not subject to production test - verified by design/characterization

6 Insulation characteristics

The following isolation classes are available for the 1ED34x1Mc12M family (X3 Analog).

Table 20 Product isolation classes

Product name	Marking	Insulation characteristics	Values specified in	UL values
1ED34x1MU12M	34x1MU12	UL 1577 certified insulation	-	Table 23
1ED34x1MC12M	34x1MC12	Reinforced insulation	Table 22	Table 23

Table 21 Safety limiting values

This coupler is suitable for rated insulation only within the given safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Description	Symbol	Characteristic	Unit
Maximum ambient safety temperature	T_S	150	°C
Maximum input-side power dissipation at T_A = 25°C	P_{SI}	100	mW
Maximum output-side power dissipation at T_A = 25°C[1)]	P_{SO}	1000	mW
Maximum driver output current (*ON*, *OFF*)[2)]	I_{OUT}		A
1ED3431MC		2.4	
1ED3461MC		4.8	
1ED3491MC		7.2	

1) IC output-side power dissipation is derated linearly at 8 mW/°C above 65 °C
2) Maximum pulse length of t = 5 µs

6.1 Certified according to VDE 0884-11 reinforced insulation (Certificate no. 40053980)

Valid for parts with part name 1ED34x1MC12M, x indicate different variants.

This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 22 Reinforced insulation according to VDE 0884-11

Description	Symbol	Characteristic	Unit
Installation classification per EN 60664-1, Table 1			–
for rated mains voltage ≤ 150 V (rms)		I-IV	
for rated mains voltage ≤ 300 V (rms)		I-IV	
for rated mains voltage ≤ 600 V (rms)		I-III	
for rated mains voltage ≤1000 V (rms)		I-II	
Climatic classification		40/125/21	–
Pollution degree (EN 60664-1)		2	–
Minimum external clearance	*CLR*	>8	mm
Minimum external creepage	*CPG*	>8	mm
Minimum comparative tracking index	*CTI*	400	–

(table continues...)

Table 22 (continued) Reinforced insulation according to VDE 0884-11

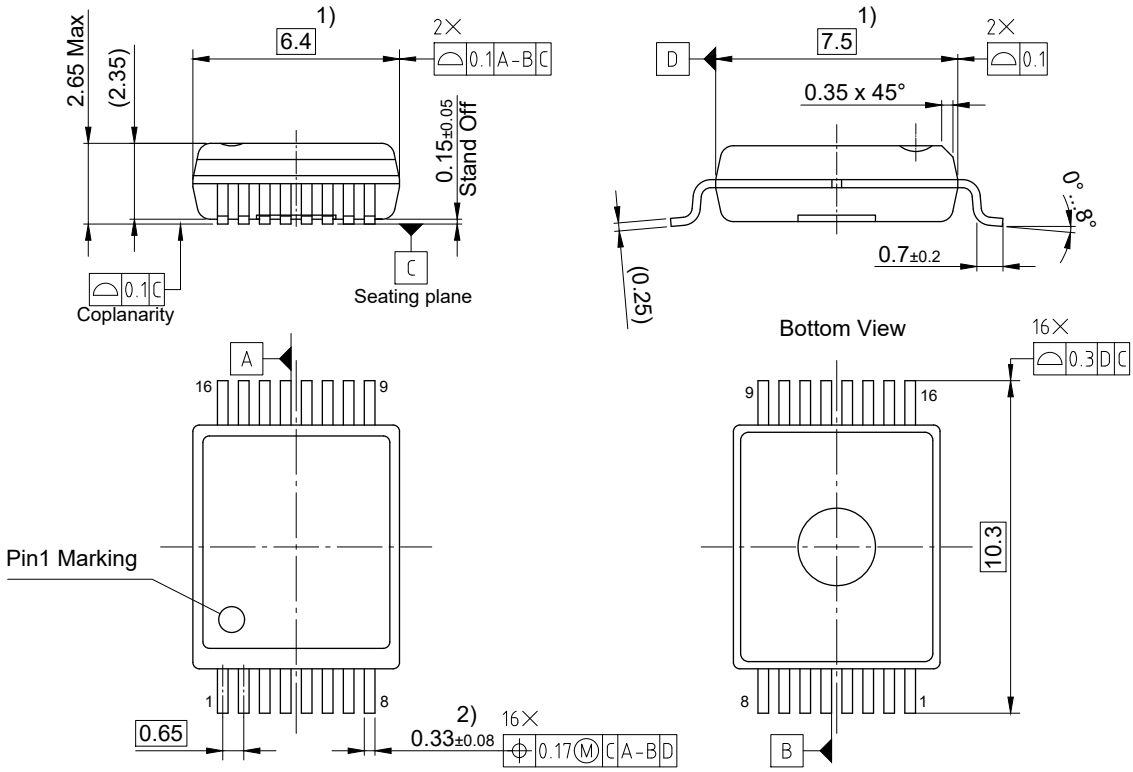
Description	Symbol	Characteristic	Unit
Apparent charge, method a $V_{pd(ini),a} = V_{IOTM}$, $V_{pd(m)} = 1.6 \times V_{IORM}$, $t_{ini} = 1$ min	q_C	<5	pC
Apparent charge, method b $V_{pd(ini),b} = V_{IOTM} \times 1.2$, $V_{pd(m)} = 1.875 \times V_{IORM}$, $t_{ini} = 1$ s	q_C	<5	pC
Isolation resistance at $T_{A,max}$	R_{IO}	$> 10^{11}$	Ω
Isolation resistance at T_S	R_{IO_S}	$> 10^9$	Ω
Maximum rated transient isolation voltage	V_{IOTM}	8000	V (peak)
Maximum repetitive insulation voltage	V_{IORM}	1767	V (peak)
Maximum surge isolation voltage for reinforced isolation $V_{TEST} = V_{IOSM} \times 1.6$	V_{IOSM}	6875	V (peak)
Insulation capacitance	C_{IO}	1.7	pF

6.2 Recognized under UL 1577 (File E311313)

Table 23 Recognized under UL 1577

Description	Symbol	Characteristic	Unit
Insulation withstand voltage/1 min	V_{ISO}	5700	V (rms)
Insulation test voltage/1 s	$V_{ISO, TEST}$	6840	V (rms)

7 Package information



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Dambar protrusion shall be maximum 0.1 mm total in excess of lead width
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 24 PG-DSO-16-28/33 - 300 mil 16-pin fine pitch plastic green dual small outline package

8 Application notes

8.1 Reference layout for thermal data

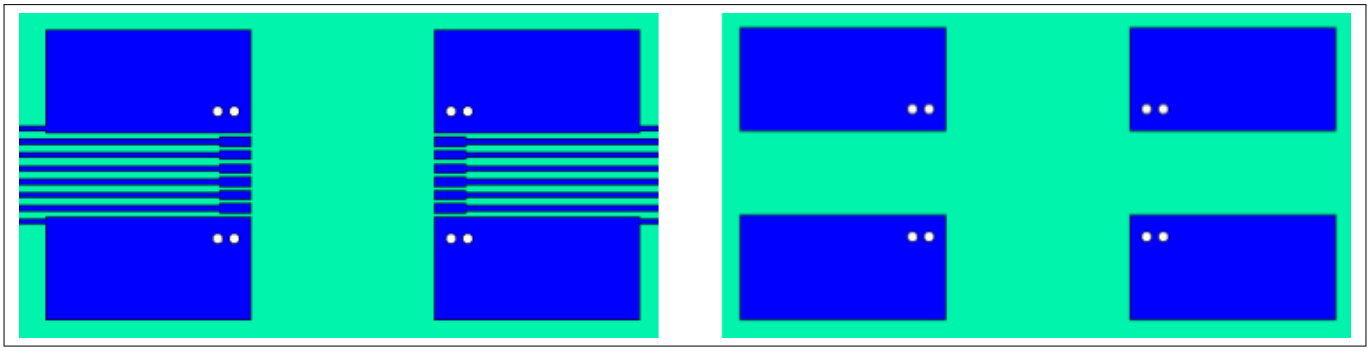


Figure 25 Reference layout for thermal data (Two layer PCB; copper thickness 35 µm; left: top layer; right: bottom layer)

The PCB layout represents the reference layout used for the thermal characterization. Pins 1 and 8 (*GND1*) and pins 9 and 16 (*VEE2*) require ground plane connections for achieving maximum power dissipation. The 1ED34x1Mc12M family (X3 Analog) is conceived to dissipate most of the heat generated through these pins.

8.2 Printed circuit board guidelines

Following factors should be taken into account for an optimum PCB layout.

- Sufficient spacing should be kept between high voltage isolated side and low voltage side circuits.
- The same minimum distance between two adjacent high-side isolated parts of the PCB should be maintained to increase the effective isolation and reduce parasitic coupling.
- In order to ensure low supply ripple and clean switching signals, bypass capacitor trace lengths should be kept as short as possible.

Revision history

Revision history

Reference	Description
v2.1 (2021-02-15)	• Change footnotes to table notes • added param V_{OFFSET} • update package drawing to latest revision • update certification status
(2021-09-01)	New version number schema: Target/Preliminary datasheet: 0.XY; Final datasheet: 1.XY
1.10 (2021-10-08)	• Certification information update (VDE certification) • Fix unit and conditions in certification table according to standards • Related product table update

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Murata Power Solutions

MGJ2 Series

5.2kVDC Isolated 2W Gate Drive DC-DC Converters

FEATURES

- Optimised bipolar output voltages for IGBT/ Mosfet gate drives
- Reinforced insulation to UL60950 recognised
- ANSI/AAMI ES60601-1, 1 MOPP/2 MOOP's recognised[3]
- 5.2kVDC isolation test voltage 'Hi Pot Test'
- Ultra low coupling capacitance
- SIP package style
- 5V, 12V, 15V & 24V inputs
- +15V/-3V, +15V/-5V, +15V/-8.7V, +15V/-15V, +17V/-9V, +18V/-2.5V, +20V/-3.5V & +20V/-5V outputs
- Operation to 100°C
- Characterised CMTI >200kV/µS
- Continuous barrier withstand voltage 2.4kVDC
- Characterised partial discharge performance

PRODUCT OVERVIEW

The MGJ2 series of DC-DC converters is ideal for powering 'high side' and 'low side' gate drive circuits for IGBTs and Mosfets in bridge circuits. A choice of asymmetric output voltages allows optimum drive levels for best system efficiency and EMI. The MGJ2 series is characterised for high isolation and dv/dt requirements commonly seen in bridge circuits used in motor drives and inverters, while the MGJ2 industrial grade temperature rating and construction gives long service life and reliability.

SELECTION GUIDE

Order Code	Nominal Input Voltage	Output Voltage 1	Output Voltage 2	Output Current 1	Output Current 2	Input Current at Rated Load	Load Regulation (Typ)	Load Regulation (Max)	Ripple & Noise (Typ)[2]	Ripple & Noise (Max)[2]	Efficiency (Min)	Efficiency (Typ)	Isolation Capacitance	MTTF[1]	
														MIL.	Tel.
	V	V	V	mA			%		mVp-p		%		pF	kHrs	
MGJ2D051505SC	5	15	-5	80	40	360	5.7	7	30	50	71	76	3	2095	
MGJ2D051509SC	5	15	-8.7	80	40	390	6	7	30	50	73	77.5	3	1902	
MGJ2D051515SC	5	15	-15	67	67	492	7	8.5	20	35	74	78	3	2629	
MGJ2D051802SC	5	18	-2.5	80	80	410	9	12	20	50	70	75	3	1376	31920
MGJ2D052003SC	5	20	-3.5	80	80	470	8	11	20	50	72	77	3	1253	32603
MGJ2D052005SC	5	20	-5	80	40	440	6.2	8	30	50	74	78.5	3	1655	
MGJ2D121503SC	12	15	-3	95	95	170	8	10	25	50	76	80	3	2014	80644
MGJ2D121505SC	12	15	-5	80	40	150	4.7	6	30	50	76	80	3	2339	
MGJ2D121509SC	12	15	-8.7	80	40	155	5.3	7.5	30	50	76	80	3	2296	
MGJ2D121515SC	12	15	-15	67	67	203	6.0	7	24	40	78	82	3	2707	
MGJ2D121802SC	12	18	-2.5	80	80	170	8	11	20	50	74	80	3	1553	36519
MGJ2D122003SC	12	20	-3.5	80	80	190	7	10	20	50	77	82	3	1371	36431
MGJ2D122005SC	12	20	-5	80	40	195	5.5	8	30	45	78	82	3	1799	
MGJ2D151505SC	15	15	-5	80	40	120	5	7	30	50	75	80	3	2374	
MGJ2D151509SC	15	15	-8.7	80	40	130	5	7	30	50	76	80	3	2736	
MGJ2D151515SC	15	15	-15	67	67	167	5.5	7	23	35	75	79	3	2100	
MGJ2D151802SC	15	18	-2.5	80	80	130	8	11	20	50	73	79	3	1392	32908
MGJ2D152003SC	15	20	-3.5	80	80	150	7	10	20	50	76	81	3	2000	80000
MGJ2D152005SC	15	20	-5	80	40	145	6	8	30	50	78	81	3	1864	
MGJ2D241503SC	24	15	-3	95	95	90	8	10	25	50	76	80	4	2535	70910
MGJ2D241505SC	24	15	-5	80	40	75	4.6	7	30	50	75	80.5	4	2194	
MGJ2D241509SC	24	15	-8.7	80	40	80	4.8	7	30	50	77	82	4	2275	
MGJ2D241709SC	24	17	-9	80	80	105	6	8	30	50	78	83	4	1050	47000
MGJ2D241802SC	24	18	-2.5	80	80	90	8	11	20	50	74	80	4	1461	32315
MGJ2D242003SC	24	20	-3.5	80	80	90	7	10	20	50	76	82	4	1333	32482
MGJ2D242005SC	24	20	-5	80	40	90	6	8	30	50	78	82	4	1725	

INPUT CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Voltage range	Continuous operation, 5V input types	4.5	5	5.5	V
	Continuous operation, 12V input types	10.8	12	13.2	
	Continuous operation, 15V input types	13.5	15	16.5	
	Continuous operation, 24V input types	21.6	24	26.4	
Input reflected ripple	051505, 051509, 051515, 052003 & 052005 types		40		mA
	121503, 121505, 121509, 121515, 122003, 122005, 151505, 151509, 151515 & 152005 types		20		
	051802, 241505, 241509, 241709, 241802 & 242005 types		15		
	122003, 121802, 151802, 152003, 241503, 241802 & 242003 types		10		

For full details go to www.murata-ps.com/rohs

1. Calculated using MIL-HDBK-217 FN2 and Telecordia SR-332 calculation model with nominal input voltage at full load.
2. See ripple & noise test method.
3. ANSI/AAMI ES60601-1 recognition is currently pending for the MGJ2D241709SC, MGJ2Dxx1515SC, MGJ2Dxx1802SC, MGJ2Dxx1503SC and MGJ2Dxx2003SC variants.

All specifications typical at T_A=25°C, nominal input voltage and rated output current unless otherwise specified.

OUTPUT CHARACTERISTICS					
Parameter	Conditions	Min.	Typ.	Max.	Units
Rated Power	T_A=-40ºC to 100ºC			2	W
Voltage Set Point Accuracy	See tolerance envelopes				
Line regulation	High V_{IN} to low V_{IN}		1.0	1.2	%/%

ISOLATION CHARACTERISTICS						
Parameter		Conditions		Min.	Typ.	Max.	Units
Isolation test voltage		Production tested for 1 second		5200			VDC
		Qualification tested for 1 minute		5200			
Resistance		Viso= 500VDC			1		GΩ
Continuous barrier withstand voltage		Non-safety barrier application				2400	VDC
Safety standard	UL60950-1	MGJ2Dxx1515SC types	Basic/supplementary			200	Vrms
		All others	Reinforced			150	
			Basic/supplementary			300	
	ANSI/AAMI ES60601-1	MGJ2Dxx1515SC types	1 MOOP			200	
		All others[1]	1 MOOP			300	
			2 MOOP/1 MOPP			200	

GENERAL CHARACTERISTICS					
Parameter	Conditions	Min.	Typ.	Max.	Units
Switching frequency	All other types		45		kHz
	MGJ2Dxx1802SC & MGJ2D241503SC types		50		

TEMPERATURE CHARACTERISTICS					
Parameter	Conditions	Min.	Typ.	Max.	Units
Specification	All output types (see safety approval section for limitations)	-40		100	°C
Storage		-55		125	
Case Temperature above ambient	5V input types		24		
	All other input types		20		
Cooling	Free air convection				

ABSOLUTE MAXIMUM RATINGS	
Short-circuit protection	Continuous
Lead temperature 1mm from case for 10 seconds	260°C
Input voltage V_{IN}, MGJ2D05xxxxSC	5.5V
Input voltage V_{IN}, MGJ2D12xxxxSC	13.2V
Input voltage V_{IN}, MGJ2D15xxxxSC	16.5V
Input voltage V_{IN}, MGJ2D24xxxxSC	26.4V
Wave Solder	Wave Solder profile not to exceed the profile recommended in IEC 61760-1 Section 6.1.3. Please refer to application notes for further information.

1. ANSI/AAMI ES60601-1 recognition is currently pending for the MGJ2D241709SC, MGJ2Dxx1515SC, MGJ2Dxx1802SC, MGJ2Dxx1503SC and MGJ2Dxx2003SC variants.

TECHNICAL NOTES

ISOLATION VOLTAGE

'Hi Pot Test', 'Flash Tested', 'Withstand Voltage', 'Proof Voltage', 'Dielectric Withstand Voltage' & 'Isolation Test Voltage' are all terms that relate to the same thing, a test voltage, applied for a specified time, across a component designed to provide electrical isolation, to verify the integrity of that isolation.

Murata Power Solutions MGJ2 series of DC-DC converters are all 100% production tested at 5.2kVDC for 1 second and have been qualification tested at 5.2kVDC for 1 minute.

The MGJ2 series is recognised by Underwriters Laboratory, please see safety approval section for more information. When the insulation in the MGJ2 series is not used as a safety barrier, i.e. provides functional isolation only, continuous or switched voltages across the barrier up to 2.4kV are sustainable. This is established by measuring the partial discharge Inception voltage in accordance with IEC 60270. Please contact Murata for further information.

REPEATED HIGH-VOLTAGE ISOLATION TESTING

It is well known that repeated high-voltage isolation testing of a barrier component can actually degrade isolation capability, to a lesser or greater degree depending on materials, construction and environment. We therefore strongly advise against repeated high voltage isolation testing, but if it is absolutely required, that the voltage be reduced by 20% from specified test voltage.

SAFETY APPROVAL

MGJ2Dxx1515SC

ANSI/AAMI ES60601-1

The MGJ2Dxx1515SC variants are pending recognition by Underwriters Laboratory (UL) to ANSI/AAMI ES60601-1 and provides 1 MOOP (Means Of Operator Protection) based upon a working voltage of 200 Vrms max and 280 Vpk max., between Primary and Secondary and between Primary and its Enclosure, in a maximum ambient temperature of 85°C and/or case temperature limit of 130°C (case temperature measured on the face opposite the pins).

File Number E202895 applies.

UL60950

The MGJ2Dxx1515SC variants have been recognised by Underwriters Laboratory (UL) to UL60950 for basic/supplementary insulation to a working voltage of 200Vrms in a maximum ambient temperature of 85°C and/or case temperature limit of 130°C (case temperature measured on the face opposite the pins).

File number E151252 applies.
Creepage and clearance 2mm
Working altitude 4000m

Fusing

The MGJ2 Series of converters are not internally fused so to meet the requirements of UL an anti-surge input line fuse should always be used with ratings as defined below.
MGJ2D051515SC: 2A
MGJ2D121515SC: 750mA
MGJ2D151515SC: 750mA
All fuses should be UL recognised and rated to 125V.

All other variants

ANSI/AAMI ES60601-1

The MGJ2 series has been recognised by Underwriters Laboratory (UL) to ANSI/AAMI ES60601-1 and provides 1 MOOP (Means Of Operator Protection) based on a working voltage of 300Vrms or 2 MOOP based upon a working voltage of 200 Vrms, and 1 MOPP (Mean Of Patient Protection) based on a working voltage of 200Vrms., between Primary and Secondary. The MGJ2D241709SC, MGJ2Dxx1802SC, MGJ2Dxx1503SC and MGJ2Dxx2003SC variants are currently pending recognition.

File number E202895 applies.

UL60950

The MGJ2 series is recognised by Underwriters Laboratory (UL) to UL60950 for reinforced insulation to a working voltage of 150Vrms and for basic/supplementary insulation to a working voltage of 300Vrms.

File number E151252 applies.

Over voltage category	OVC I	OVC II
Working voltage	150Vrms	300Vrms
Working altitude	2000m	2000m
Creepage & clearance	2mm	2mm

Fusing

The MGJ2 Series of converters are not internally fused so to meet the requirements of UL an anti-surge input line fuse should always be used with ratings as defined below.
MGJ2D05xxxxSC: 1.25A
MGJ2D12xxxxSC: 750mA
MGJ2D15xxxxSC: 750mA
MGJ2D24xxxxSC: 750mA
All fuses should be UL recognised and rated to 125V.

RoHS COMPLIANCE INFORMATION

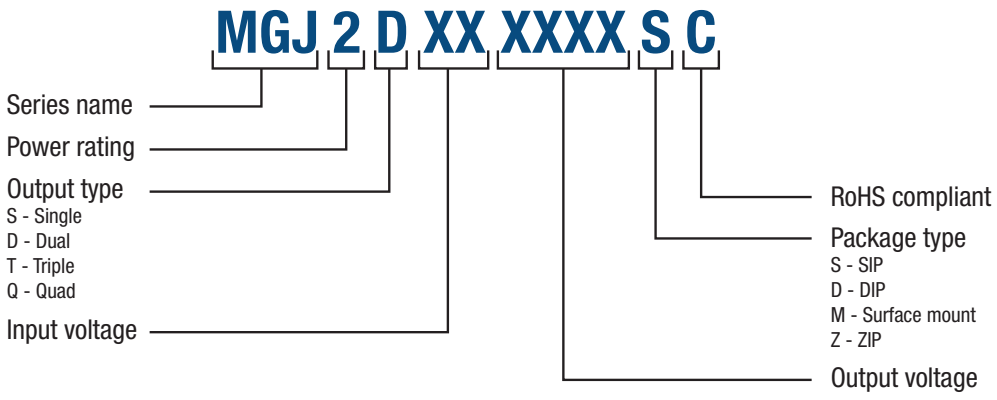
This series is compatible with RoHS soldering systems with a peak wave solder temperature of 260ºC for 10 seconds. Please refer to application notes for further information. The pin termination finish on this product series is Tin Plate, Hot Dipped over Matte Tin with Nickel Preplate. The series is backward compatible with Sn/Pb soldering systems. For further information, please visit www.murata-ps.com/rohs

ENVIRONMENTAL VALIDATION TESTING

The following tests have been conducted on this product series, as part of our design verification process. The datasheet characteristics specify user operating conditions for this series, please contact Murata if further information about the tests is required.

Test	Standard	Condition
Temperature cycling	MIL-STD-883 Method 1010, Condition B	10 cycles between two chambers set to achieve -55°C and +125°C.The dwell time shall not be less than 10min.
Humidity bias	JEDEC JESD22-A101	85°C ± 2°C, 85% ± 5% R.H. for >1000 hours.
High temperature storage life	JEDEC JESD22-A103, Condition A	125°C +10/-0°C for ≥1000 hours.
Vibration	MIL-STD-883 Method 2007, Condition A	1.5mm pk-pk / 20g pk min, 20-2000Hz, 4 sweeps in each of 3 mutually perpendicular axes at 3 oct/min.
Shock	MIL-STD-883 Method 2002, Condition A	500g 1.0ms half sine, 5 shocks in each direction of 3 mutually perpendicular axis.
ESD	JEDEC JESD22-A114	HBM Testing Standard at 3 stress levels; 2.0kV, 4.0kV and 8.0kV.
Bump	IEC Class 4M5 of ETS 300 019-2-4	Shock Spectrum Type II, 6mS duration, 250m/s² 500 bumps in 6 directions.
Solderability	IPC/ECA J-STD-002, Test A and A1	SnPb (Test A) For leaded solderability the parts are conditioned in a steam ager for 8 hours ±15 min. at a temperature of 93±3°C. Dipped in solder at 245°C ±5°C for 5 +0/-0.5 seconds. Pb-free (Test A1) For lead free solderability the parts are conditioned in a steam ager for 8 hours ± 15 min. at a temperature of 93±3°C. Dipped in solder at 255°C ±5°C for 5 +0/-0.5 seconds.
Solder heat	JEDEC JESD22-B106	The test sample is subjected to a molten solder bath at 260 ±5°C for 10 seconds (96SC tin/ silver/copper).
Solder heat (hand)	MIL-STD-202 Method 210, Condition A	The soldering iron is heated to 350°C ± 10°C and applied to the terminations for a duration of 4 to 5 seconds.
Solvent cleaning	Resistance to cleaning agents.	Solvent – Novec 71IPA & Topklean EL-20A. Pulsed ultrasonic immersion 45°C- 65°C
Solvent Resistance	MIL-STD-883 Method 2015	Separate samples subjected to solvent A, solvent B and solvent D
Lead Integrity (Adhesion)	MIL-STD-883 Method 2025	Leads are bent through 90º until a fracture occurs.
Lead Integrity (Fatigue)	MIL-STD-883 Method 2004, condition B_2	The leads are bent to an angle of 15º. Each lead is subjected to 3 cycles.
Lead Integrity (Tension/Pull)	MIL-STD-883 Method 2004, Condition A_1	Pull of 0.227kg applied for 30 seconds. The force is then increased until the pins snap.

PART NUMBER STRUCTURE



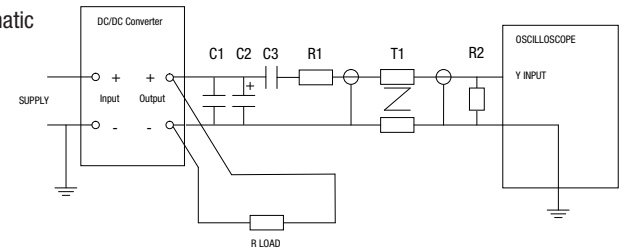
CHARACTERISATION TEST METHODS

Ripple & Noise Characterisation Method

Ripple and noise measurements are performed with the following test configuration.

C1	1µF X7R multilayer ceramic capacitor, voltage rating to be a minimum of 3 times the output voltage of the DC-DC converter
C2	10µF tantalum capacitor, voltage rating to be a minimum of 1.5 times the output voltage of the DC-DC converter with an ESR of less than 100mΩ at 100 kHz
C3	100nF multilayer ceramic capacitor, general purpose
R1	450Ω resistor, carbon film, ±1% tolerance
R2	50Ω BNC termination
T1	3T of the coax cable through a ferrite toroid
RLOAD	Resistive load to the maximum power rating of the DC-DC converter. Connections should be made via twisted wires
Measured values are multiplied by 10 to obtain the specified values.	

Differential Mode Noise Test Schematic



APPLICATION NOTES

Minimum load

The minimum load to meet datasheet specification is 10% of the full rated load across the specified input voltage range. Lower than 10% minimum loading will result in an increase in output voltage, which may rise to typically 1.25 times the specified output voltage if the output load falls to less than 5%.

Gate Drive Applications Advisory Note

For general guidance for product usage in gate drive applications please refer to "gate drive application notes".

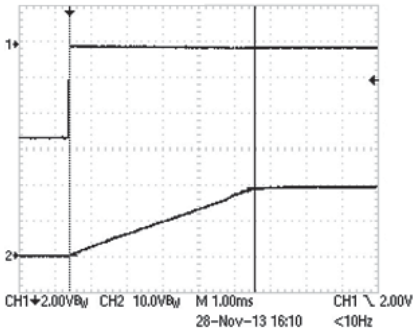
Capacitive loading and start up

Typical start up times for this series, with a typical input voltage rise time of 2.2µs and output capacitance of 10µF, are shown in the table below. The product series will start into capacitance ranging from 47µF up to 220µF with increased start times.

	Start-up time ms
MGJ2D051505SC	3
MGJ2D051509SC	4.5
MGJ2D051515SC	21
MGJ2D051802SC	4
MGJ2D052003SC	5
MGJ2D052005SC	5
MGJ2D121503SC	3
MGJ2D121505SC	3
MGJ2D121509SC	4
MGJ2D121515SC	14.5
MGJ2D121802SC	5
MGJ2D122003SC	5
MGJ2D122005SC	5.5

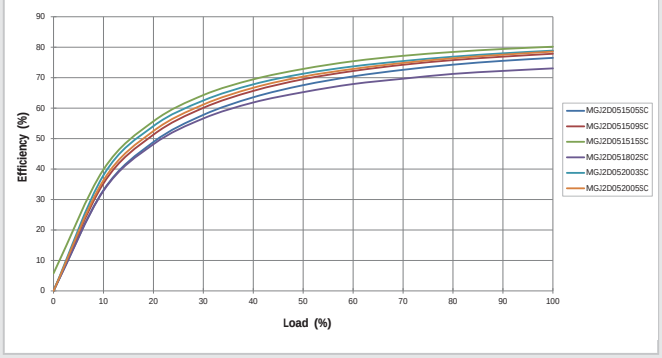
	Start-up time ms
MGJ2D151505SC	2.5
MGJ2D151509SC	3
MGJ2D151515SC	10.5
MGJ2D151802SC	3
MGJ2D152003SC	5
MGJ2D152005SC	4.5
MGJ2D241503SC	3
MGJ2D241505SC	3
MGJ2D241509SC	3
MGJ2D241709SC	4
MGJ2D241802SC	3
MGJ2D242003SC	4
MGJ2D242005SC	4

Typical Start-Up Wave Form

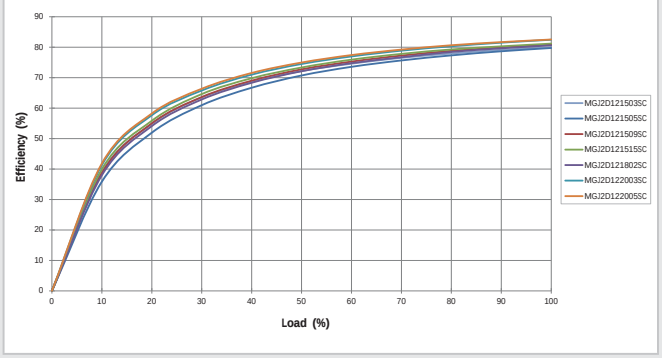


EFFICIENCY VS LOAD

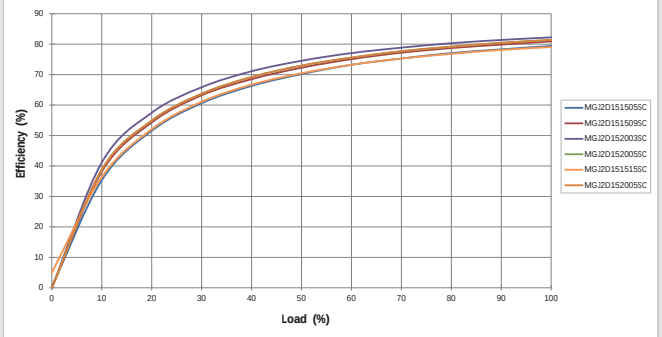
5V INPUT



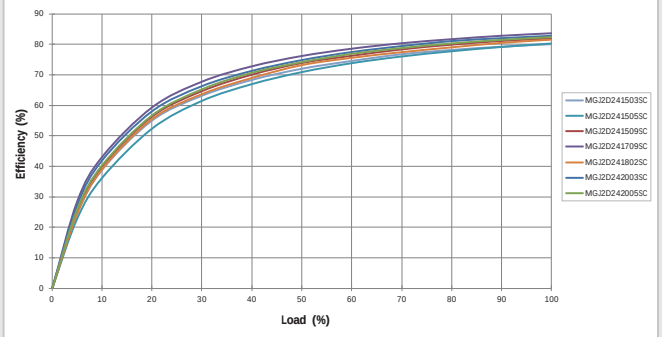
12V INPUT



15V INPUT

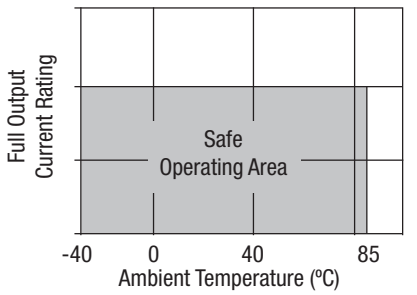


24V INPUT

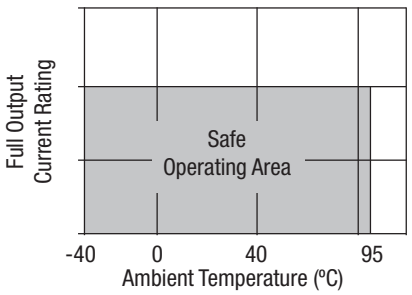


TEMPERATURE DERATING GRAPHS

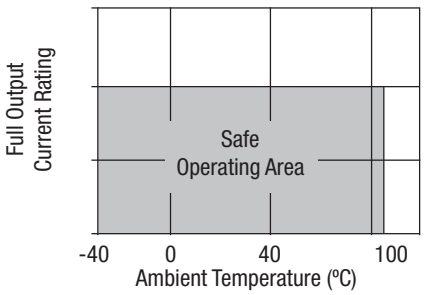
051515, 051802, 052003, 121503, 121515 & 151515



051505, 052005, 121802, 122003, 151802, 152003, 241802 & 242003



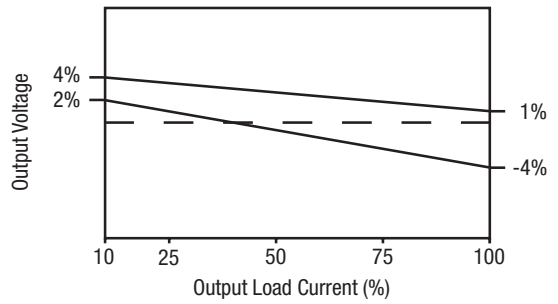
All other variants



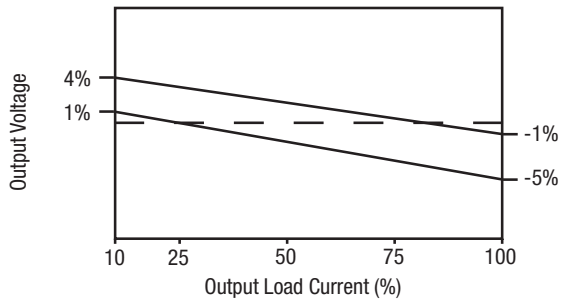
POSITIVE OUTPUT VOLTAGE TOLERANCE ENVELOPES

The voltage tolerance envelopes show typical load regulation characteristics for this product series. The tolerance envelope is the maximum output voltage variation due to changes in output loading and set point accuracy.

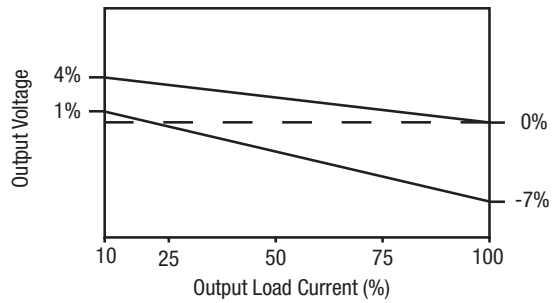
051505, 051509, 151505 & 151509



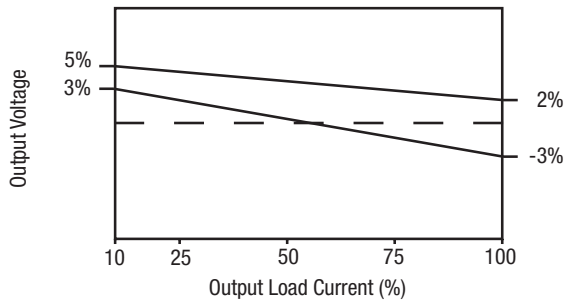
122005, 152005 & 242005



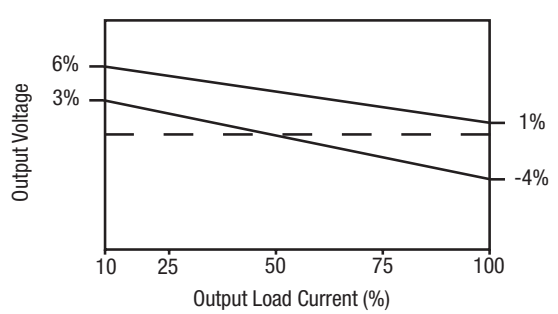
121509, 241509 & 052005



121505 & 241505



121515 & 151515



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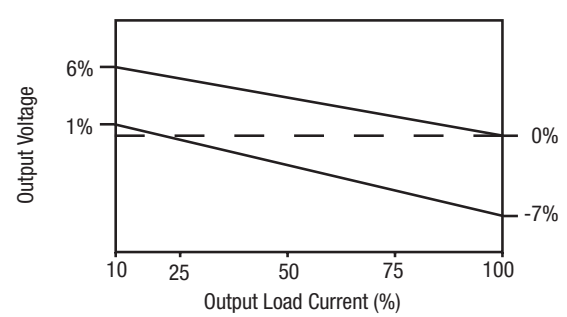
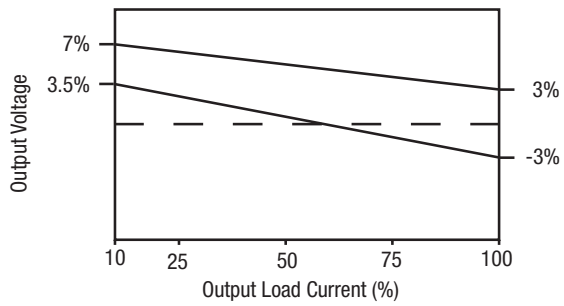
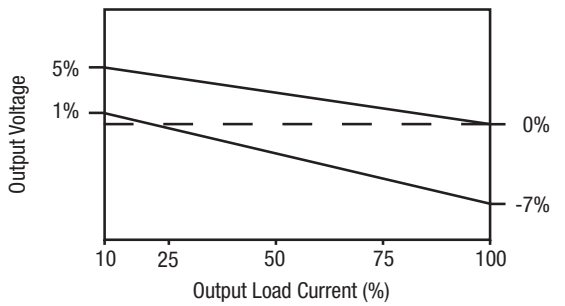


POSITIVE OUTPUT VOLTAGE TOLERANCE ENVELOPES (Continued)

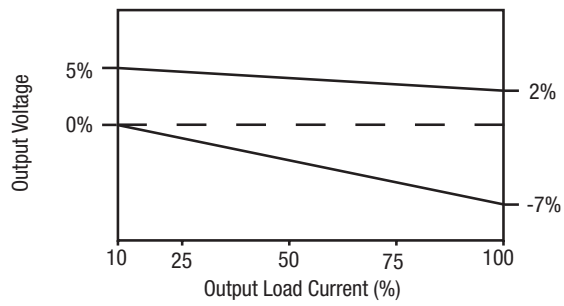
241709



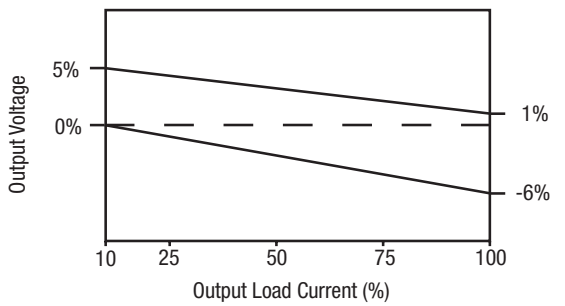
052003



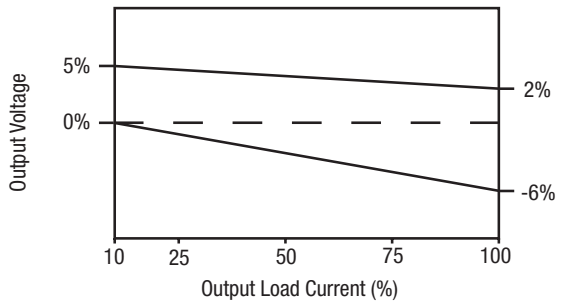
122003, 152003 & 242003



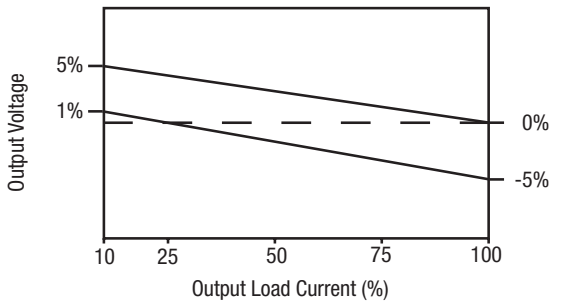
051802



121802, 151802 & 241802



121503



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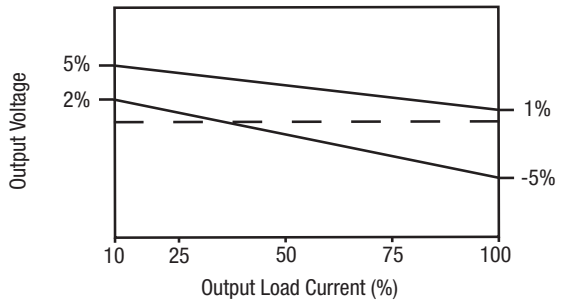
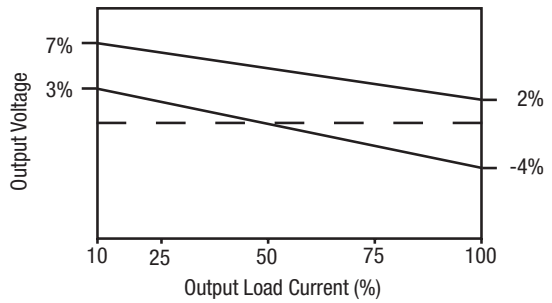
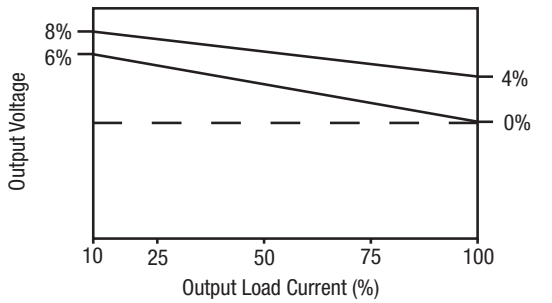


NEGATIVE OUTPUT VOLTAGE TOLERANCE ENVELOPES

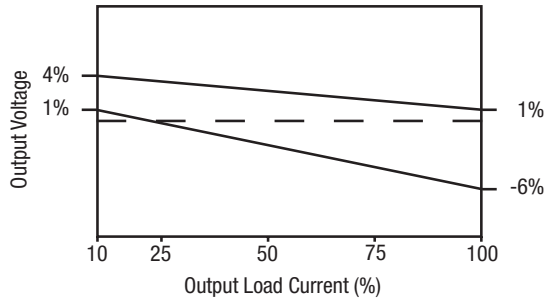
051509, 052005, 121505, 122005, 152005 & 242005



151505



121509 & 241509



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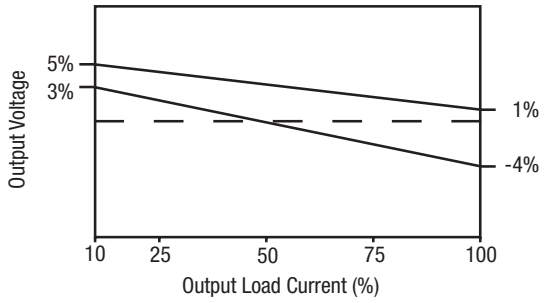
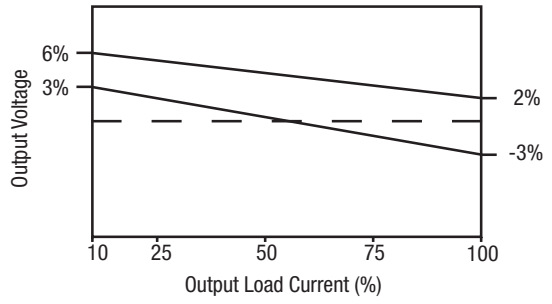
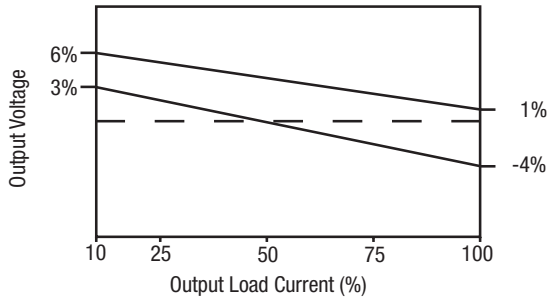


151509 & 241505

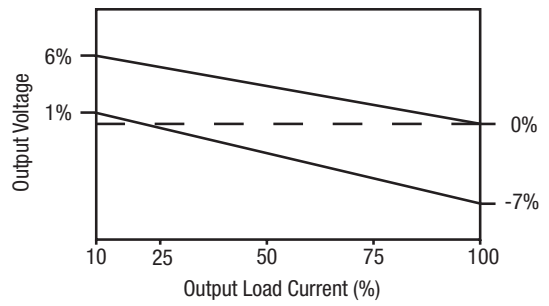


121515 & 151515

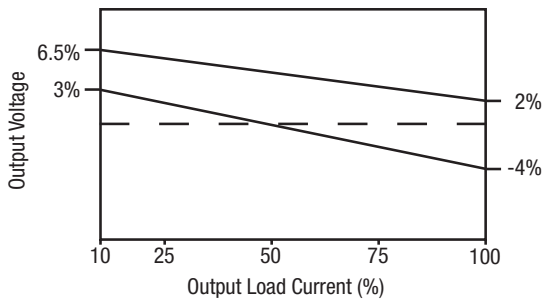


NEGATIVE OUTPUT VOLTAGE TOLERANCE ENVELOPES (Continued)

051515



241709



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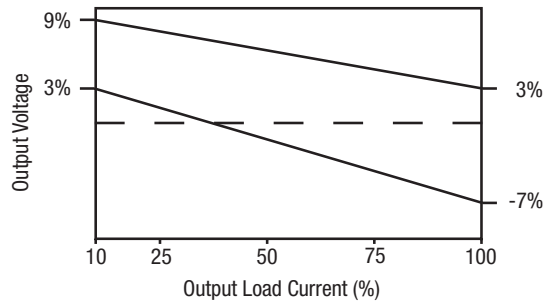
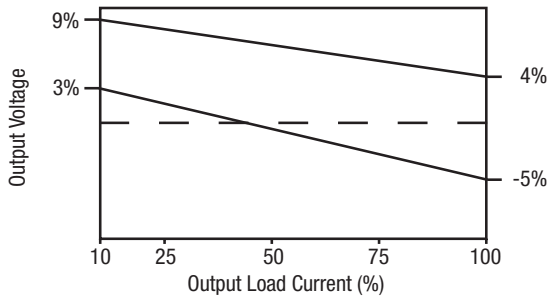
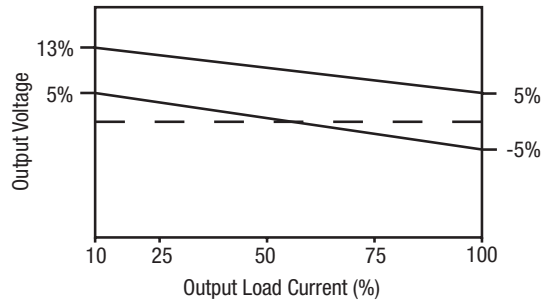


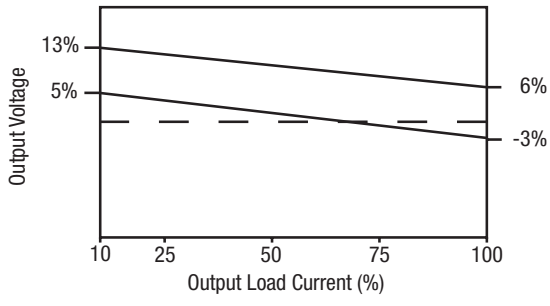
122003, 152003 & 242003



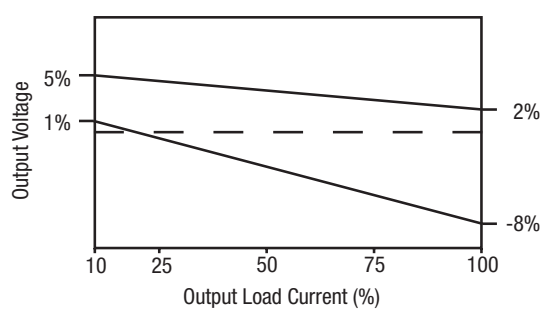
051802



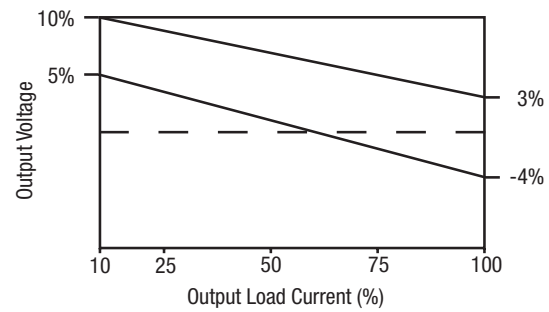
121802, 151802 & 241802



121503

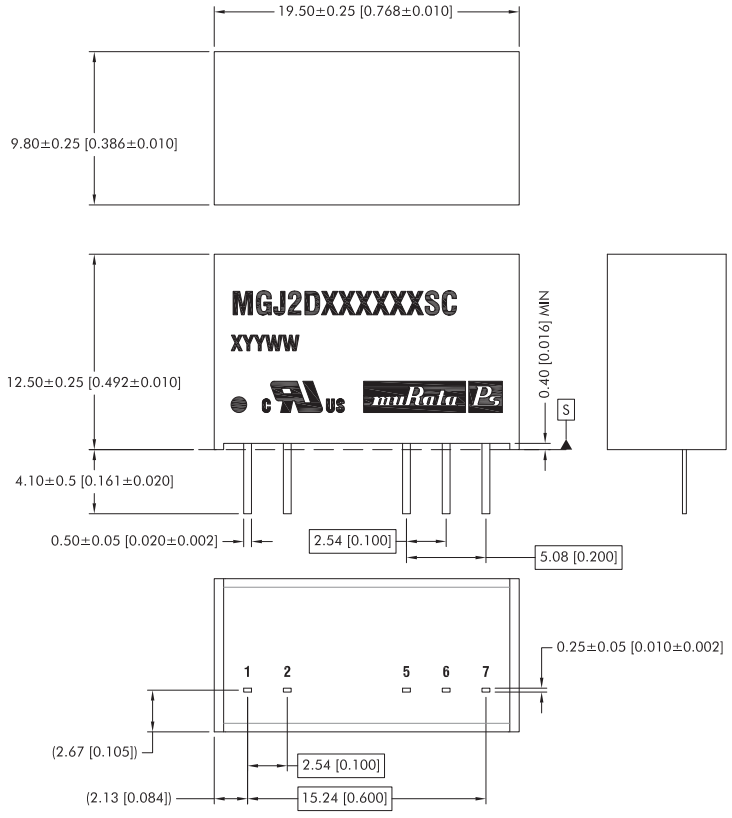


241503



PACKAGE SPECIFICATIONS

MECHANICAL DIMENSIONS



All dimensions in mm ±0.25mm (inches ±0.01). All pins on a 2.54 (0.1) pitch and within ±0.25 (0.01) of true position.

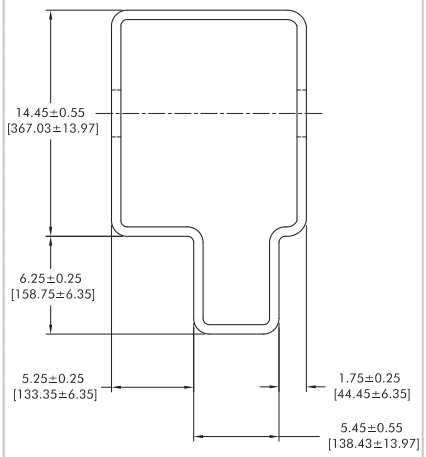
Weight: 4.3g

PIN CONNECTIONS

Pin Output

Pin	Function
1	$+V_{IN}$
2	$-V_{IN}$
5	$-V_{OUT}$
6	0V
7	$+V_{OUT}$

Tube outline dimensions

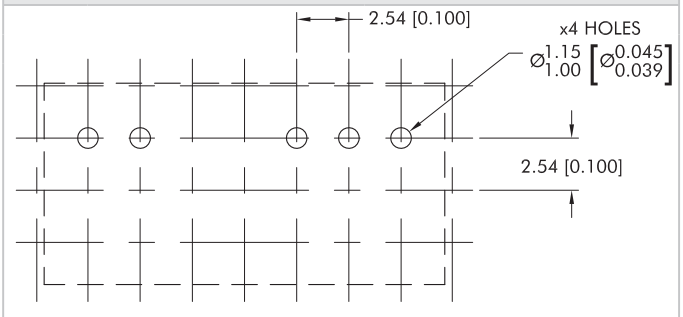


Unless otherwise stated all dimensions in mm (inches).

Tube length : 525mm [20.669] ±2.0 [0.079]

Tube Quantity : 25

RECOMMENDED FOOTPRINT DETAILS



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- Aircraft equipment
- Aerospace equipment
- Undersea equipment
- Power plant control equipment
- Medical equipment
- Transportation equipment (automobiles, trains, ships, etc.)
- Traffic signal equipment
- Disaster prevention / crime prevention equipment
- Data Processing equipment

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Refer to: https://www.murata.com/en-eu/products/power/requirements

TimerBlox: Voltage-Controlled Pulse Width Modulator (PWM)

FEATURES

- **Pulse Width Modulation (PWM) Controlled by Simple 0V to 1V Analog Input**
- **Four Available Options Define Duty Cycle Limits**
  - **Minimum Duty Cycle at 0% or 5%**
  - **Maximum Duty Cycle at 95% or 100%**
- **Frequency Range: 3.81Hz to 1MHz**
- Configured with 1 to 3 Resistors
- <1.7% Maximum Frequency Error
- PWM Duty Cycle Error < 3.7% Maximum
- Frequency Modulation (VCO) Capability
- 2.25V to 5.5V Single Supply Operation
- 115µA Supply Current at 100kHz
- 500µs Start-Up Time
- CMOS Output Driver Sources/Sinks 20mA
- –55°C to 125°C Operating Temperature Range
- Available in Low Profile (1mm) SOT-23 (ThinSOT™) and 2mm × 3mm DFN
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- PWM Servo Loops
- Heater Control
- LED Dimming Control
- High Vibration, High Acceleration Environments
- Portable and Battery-Powered Equipment

DESCRIPTION

The LTC®6992 is a silicon oscillator with an easy-to-use analog voltage-controlled pulse width modulation (PWM) capability. The LTC6992 is part of the TimerBlox® family of versatile silicon timing devices.

A single resistor, R_{SET}, programs the LTC6992's internal master oscillator frequency. The output frequency is determined by this master oscillator and an internal frequency divider, N_{DIV}, programmable to eight settings from 1 to 16384.

$$f_{OUT} = \frac{1MHz}{N_{DIV}} \bullet \frac{50k\Omega}{R_{SET}}, N_{DIV} = 1,4,16 \ldots 16384$$

Applying a voltage between 0V and 1V on the MOD pin sets the duty cycle.

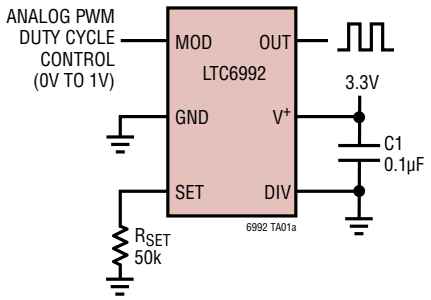
The four versions differ in their minimum/maximum duty cycle. Note that a minimum duty cycle limit of 0% or maximum duty cycle limit of 100% allows oscillations to stop at the extreme duty cycle settings.

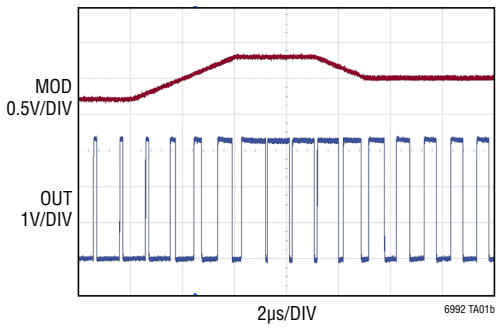
DEVICE NAME	PWM DUTY CYCLE RANGE
LTC6992-1	0% to 100%
LTC6992-2	5% to 95%
LTC6992-3	0% to 95%
LTC6992-4	5% to 100%

For easy configuration of the LTC6992, use the TimerBlox LTC6992: PWM Web-Based Design Tool.

TYPICAL APPLICATION

1MHz Pulse Width Modulator



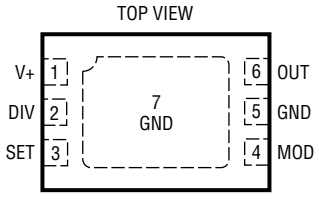


Rev. D

ABSOLUTE MAXIMUM RATINGS (Note 1)

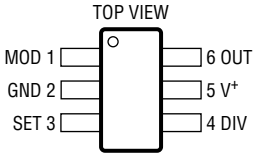
Supply Voltage (V^+) to GND 6V
Maximum Voltage On Any Pin
.....$(GND – 0.3V) \leq V_{PIN} \leq (V^+ + 0.3V)$
Operating Temperature Range (Note 2)
LTC6992C.....–40°C to 85°C
LTC6992I.....–40°C to 85°C
LTC6992H.....–40°C to 125°C
LTC6992MP.....–55°C to 125°C
Specified Temperature Range (Note 3)
LTC6992C.....0°C to 70°C
LTC6992I.....–40°C to 85°C
LTC6992H.....–40°C to 125°C
LTC6992MP.....–55°C to 125°C
Junction Temperature .....150°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature (Soldering, 10 sec)
S6 Package.....300°C

PIN CONFIGURATION



DCB PACKAGE
6-LEAD (2mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 64°C/W, θ_{JC} = 10.6°C/W
EXPOSED PAD (PIN 7) IS GND, PCB CONNECTION IS OPTIONAL



S6 PACKAGE
6-LEAD PLASTIC TSOT-23

T_{JMAX} = 150°C, θ_{JA} = 192°C/W, θ_{JC} = 51°C/W

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6992CDCB-1#TRMPBF	LTC6992CDCB-1#TRPBF	LDXC	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC6992IDCB-1#TRMPBF	LTC6992IDCB-1#TRPBF	LDXC	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6992HDCB-1#TRMPBF	LTC6992HDCB-1#TRPBF	LDXC	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6992CS6-1#TRMPBF	LTC6992CS6-1#TRPBF	LTDXB	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6992IS6-1#TRMPBF	LTC6992IS6-1#TRPBF	LTDXB	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6992HS6-1#TRMPBF	LTC6992HS6-1#TRPBF	LTDXB	6-Lead Plastic TSOT-23	–40°C to 125°C
LTC6992CDCB-2#TRMPBF	LTC6992CDCB-2#TRPBF	LDXF	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC6992IDCB-2#TRMPBF	LTC6992IDCB-2#TRPBF	LDXF	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6992HDCB-2#TRMPBF	LTC6992HDCB-2#TRPBF	LDXF	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6992CS6-2#TRMPBF	LTC6992CS6-2#TRPBF	LTDXD	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6992IS6-2#TRMPBF	LTC6992IS6-2#TRPBF	LTDXD	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6992HS6-2#TRMPBF	LTC6992HS6-2#TRPBF	LTDXD	6-Lead Plastic TSOT-23	–40°C to 125°C
LTC6992CDCB-3#TRMPBF	LTC6992CDCB-3#TRPBF	LFCP	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC6992IDCB-3#TRMPBF	LTC6992IDCB-3#TRPBF	LFCP	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6992HDCB-3#TRMPBF	LTC6992HDCB-3#TRPBF	LFCP	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6992CS6-3#TRMPBF	LTC6992CS6-3#TRPBF	LTFCQ	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6992IS6-3#TRMPBF	LTC6992IS6-3#TRPBF	LTFCQ	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6992HS6-3#TRMPBF	LTC6992HS6-3#TRPBF	LTFCQ	6-Lead Plastic TSOT-23	–40°C to 125°C
LTC6992CDCB-4#TRMPBF	LTC6992CDCB-4#TRPBF	LFCR	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC6992IDCB-4#TRMPBF	LTC6992IDCB-4#TRPBF	LFCR	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6992HDCB-4#TRMPBF	LTC6992HDCB-4#TRPBF	LFCR	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6992CS6-4#TRMPBF	LTC6992CS6-4#TRPBF	LTFCS	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6992IS6-4#TRMPBF	LTC6992IS6-4#TRPBF	LTFCS	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6992HS6-4#TRMPBF	LTC6992HS6-4#TRPBF	LTFCS	6-Lead Plastic TSOT-23	–40°C to 125°C
LTC6992MPS6-1#TRMPBF	LTC6992MPS6-1#TRPBF	LTDXB	6-Lead Plastic TSOT-23	–55°C to 125°C
LTC6992MPS6-2#TRMPBF	LTC6992MPS6-2#TRPBF	LTDXD	6-Lead Plastic TSOT-23	–55°C to 125°C
LTC6992MPS6-3#TRMPBF	LTC6992MPS6-3#TRPBF	LTFCQ	6-Lead Plastic TSOT-23	–55°C to 125°C
LTC6992MPS6-4#TRMPBF	LTC6992MPS6-4#TRPBF	LTFCS	6-Lead Plastic TSOT-23	–55°C to 125°C
AUTOMOTIVE PRODUCTS**				
LTC6992IS6-1#WTRMPBF	LTC6992IS6-1#WTRPBF	LTDXB	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6992HS6-1#WTRMPBF	LTC6992HS6-1#WTRPBF	LTDXB	6-Lead Plastic TSOT-23	–40°C to 125°C
LTC6992IS6-2#WTRMPBF	LTC6992IS6-2#WTRPBF	LTDXD	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6992HS6-2#WTRMPBF	LTC6992HS6-2#WTRPBF	LTDXD	6-Lead Plastic TSOT-23	–40°C to 125°C
LTC6992IS6-3#WTRMPBF	LTC6992IS6-3#WTRPBF	LTFCQ	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6992HS6-3#WTRMPBF	LTC6992HS6-3#WTRPBF	LTFCQ	6-Lead Plastic TSOT-23	–40°C to 125°C
LTC6992IS6-4#WTRMPBF	LTC6992IS6-4#WTRPBF	LTFCS	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6992HS6-4#WTRMPBF	LTC6992HS6-4#WTRPBF	LTFCS	6-Lead Plastic TSOT-23	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 2.25V to 5.5V, V_{MOD} = 0V to V_{SET}, DIVCODE = 0 to 15 (N_{DIV} = 1 to 16,384), R_{SET} = 50k to 800k, R_{LOAD} = 5k, C_{LOAD} = 5pF unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Oscillation Frequency								
f_{OUT}	Output Frequency				3.81		1000000	Hz
Δf_{OUT}	Frequency Accuracy (Note 4)	3.81Hz ≤ f_{OUT} ≤ 1MHz		 ●		±0.8	±1.7 ±2.4	% %
$\Delta f_{OUT}/\Delta T$	Frequency Drift Over Temperature			●		±0.005		%/°C
$\Delta f_{OUT}/\Delta V^+$	Frequency Drift Over Supply	V^+ = 4.5V to 5.5V V^+ = 2.25V to 4.5V		● ●		0.25 0.08	0.65 0.18	%/V %/V
	Long-Term Frequency Stability	(Note 10)				90		ppm/√kHr
	Period Jitter (Note 9)	N_{DIV} = 1				1.2		$\%_{P-P}$
		N_{DIV} = 4				0.4 0.07		$\%_{P-P}$ $\%_{RMS}$
		N_{DIV} = 16				0.15 0.022		$\%_{P-P}$ $\%_{RMS}$
Pulse Width Modulation								
ΔD	PWM Duty Cycle Accuracy	V_{MOD} = 0.2•V_{SET} to 0.8•V_{SET} V_{MOD} = 0.2•V_{SET} to 0.8•V_{SET} V_{MOD} < 0.2•V_{SET} or V_{MOD} > 0.8•V_{SET}		 ● ●		±3.0	±3.7 ±4.5 ±4.9	% % %
D_{MAX}	Maximum Duty Cycle Limit	LTC6992-1/LTC6992-4, POL = 0, V_{MOD} = 1V		●	100			%
		LTC6992-2/LTC6992-3, POL = 0, V_{MOD} = 1V		●	90.5	95	99	%
D_{MIN}	Minimum Duty Cycle Limit	LTC6992-1/LTC6992-3, POL = 0, V_{MOD} = 0V		●			0	%
		LTC6992-2/LTC6992-4, POL = 0, V_{MOD} = 0V		●	1	5	9.5	%
$t_{S,PWM}$	Duty Cycle Settling Time (Note 6)	t_{MASTER} = t_{OUT}/N_{DIV}				8•t_{MASTER}		µs
Power Supply								
V^+	Operating Supply Voltage Range			●	2.25		5.5	V
	Power-On Reset Voltage			●			1.95	V
I_S	Supply Current	R_L = ∞, R_{SET} = 50k, N_{DIV} = 1	V^+ = 5.5V	●		365	450	µA
			V^+ = 2.25V	●		225	285	µA
		R_L = ∞, R_{SET} = 50k, N_{DIV} = 4	V^+ = 5.5V	●		350	420	µA
			V^+ = 2.25V	●		225	280	µA
		R_L = ∞, R_{SET} = 50k, N_{DIV} ≥ 16	V^+ = 5.5V	●		325	390	µA
			V^+ = 2.25V	●		215	265	µA
		R_L = ∞, R_{SET} = 800k, N_{DIV} = 1 to 16,384	V^+ = 5.5V	●		120	170	µA
			V^+ = 2.25V	●		105	150	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 2.25V to 5.5V, V_{MOD} = 0V to V_{SET}, DIVCODE = 0 to 15 (N_{DIV} = 1 to 16,384), R_{SET} = 50k to 800k, R_{LOAD} = 5k, C_{LOAD} = 5pF unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Inputs							
V_{SET}	Voltage at SET Pin		●	0.97	1.00	1.03	V
$\Delta V_{SET}/\Delta T$	V_{SET} Drift Over Temperature		●		±75		µV/°C
R_{SET}	Frequency-Setting Resistor		●	50		800	kΩ
	MOD Pin Input Capacitance				2.5		pF
	MOD Pin Input Current		●			±10	nA
$V_{MOD,HI}$	V_{MOD} Voltage for Maximum Duty Cycle	LTC6992-1/LTC6992-4, POL = 0, D = 100% LTC6992-2/LTC6992-3, POL = 0, D = 95%	●		0.90•V_{SET} 0.86•V_{SET}	0.936•V_{SET}	V V
$V_{MOD,LO}$	V_{MOD} Voltage for Minimum Duty Cycle	LTC6992-1/LTC6992-3, POL = 0, D = 0% LTC6992-2/LTC6992-4, POL = 0, D = 5%	●	0.064•V_{SET}	0.10•V_{SET} 0.14•V_{SET}		V V
V_{DIV}	DIV Pin Voltage		●	0		V^+	V
$\Delta V_{DIV}/\Delta V^+$	DIV Pin Valid Code Range (Note 5)	Deviation from Ideal V_{DIV}/V^+ = (DIVCODE + 0.5)/16	●			±1.5	%
	DIV Pin Input Current		●			±10nA	
Digital Output							
$I_{OUT(MAX)}$	Output Current	V^+ = 2.7V to 5.5V			±20		mA
V_{OH}	High Level Output Voltage (Note 7)	V^+ = 5.5V, I_{OUT} = –1mA V^+ = 5.5V, I_{OUT} = –16mA	● ●	5.45 4.84	5.48 5.15		V V
		V^+ = 3.3V, I_{OUT} = –1mA V^+ = 3.3V, I_{OUT} = –10mA	● ●	3.24 2.75	3.27 2.99		V V
		V^+ = 2.25V, I_{OUT} = –1mA V^+ = 2.25V, I_{OUT} = -8mA	● ●	2.17 1.58	2.21 1.88		V V
V_{OL}	Low Level Output Voltage (Note 7)	V^+ = 5.5V, I_{OUT} = 1mA V^+ = 5.5V, I_{OUT} = 16mA	● ●		0.02 0.26	0.04 0.54	V V
		V^+ = 3.3V, I_{OUT} = 1mA V^+ = 3.3V, I_{OUT} = 10mA	● ●		0.03 0.22	0.05 0.46	V V
		V^+ = 2.25V, I_{OUT} = 1mA V^+ = 2.25V, I_{OUT} = 8mA	● ●		0.03 0.26	0.07 0.54	V V
t_r	Output Rise Time (Note 8)	V^+ = 5.5V, R_{LOAD} = ∞ V^+ = 3.3V, R_{LOAD} = ∞ V^+ = 2.25V, R_{LOAD} = ∞			1.1 1.7 2.7		ns ns ns
t_f	Output Fall Time (Note 8)	V^+ = 5.5V, R_{LOAD} = ∞ V^+ = 3.3V, R_{LOAD} = ∞ V^+ = 2.25V, R_{LOAD} = ∞			1.0 1.6 2.4		ns ns ns

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC6992C is guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 3: The LTC6992C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6992C is designed, characterized and expected to meet specified performance from –40°C to 85°C but it is not tested or QA sampled at these temperatures. The LTC6992I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6992H is guaranteed to meet specified performance from –40°C to 125°C. The LTC6992MP is guaranteed to meet specified performance from –55°C to 125°C.

Note 4: Frequency accuracy is defined as the deviation from the f_{OUT} equation, assuming R_{SET} is used to program the frequency.

Note 5: See Operation section, Table 1 and Figure 2 for a full explanation of how the DIV pin voltage selects the value of DIVCODE.

Note 6: Duty cycle settling time is the amount of time required for the output to settle within ±1% of the final duty cycle after a ±10% change in the setting (±80mV step in V_{MOD}).

Note 7: To conform to the Logic IC Standard, current out of a pin is arbitrarily given a negative value.

Note 8: Output rise and fall times are measured between the 10% and the 90% power supply levels with 5pF output load. These specifications are based on characterization.

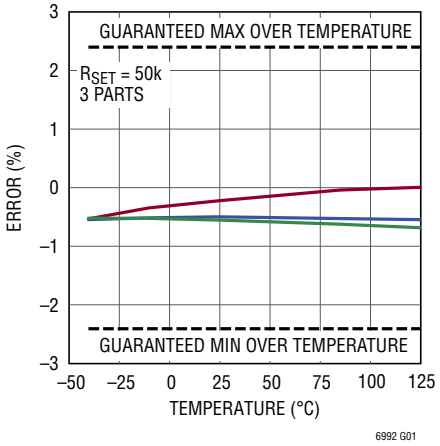
Note 9: Jitter is the ratio of the peak-to-peak deviation of the period to the mean of the period. This specification is based on characterization and is not 100% tested.

Note 10: Long-term drift of silicon oscillators is primarily due to the movement of ions and impurities within the silicon and is tested at 30°C under otherwise nominal operating conditions. Long-term drift is specified as ppm/$\sqrt{kHr}$ due to the typically nonlinear nature of the drift. To calculate drift for a set time period, translate that time into thousands of hours, take the square root and multiply by the typical drift number. For instance, a year is 8.77kHr and would yield a drift of 266ppm at 90ppm/$\sqrt{kHr}$. Drift without power applied to the device may be approximated as 1/10th of the drift with power, or 9ppm/$\sqrt{kHr}$ for a 90ppm/$\sqrt{kHr}$ device.

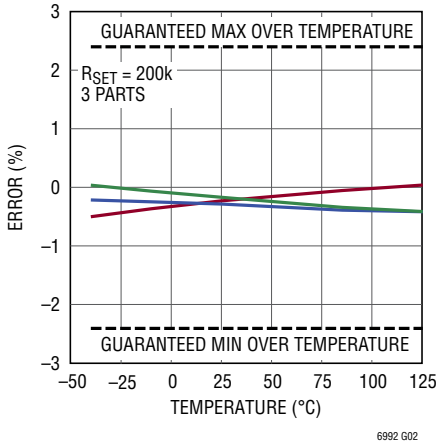
TYPICAL PERFORMANCE CHARACTERISTICS

V^+ = 3.3V, R_{SET} = 200k, and T_A = 25°C, unless otherwise noted.

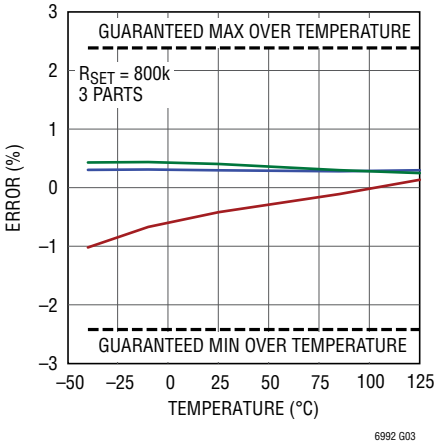
Frequency Error vs Temperature



Frequency Error vs Temperature



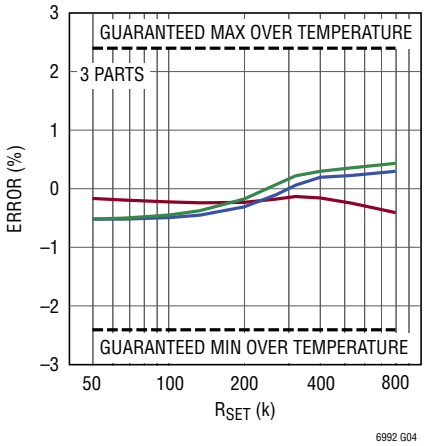
Frequency Error vs Temperature



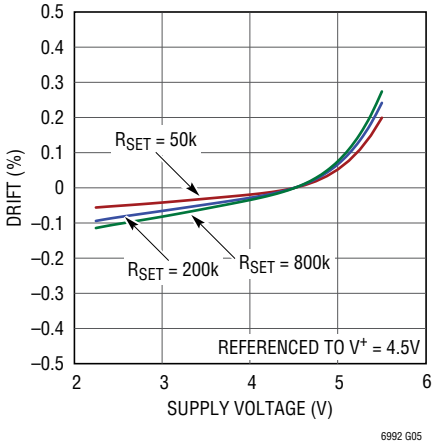
TYPICAL PERFORMANCE CHARACTERISTICS

V^+ = 3.3V, R_{SET} = 200k, and T_A = 25°C, unless otherwise noted.

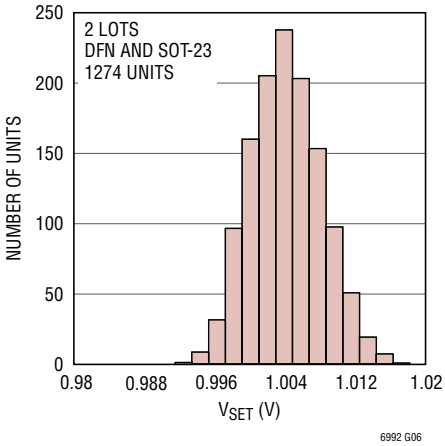
Frequency Error vs R_{SET}



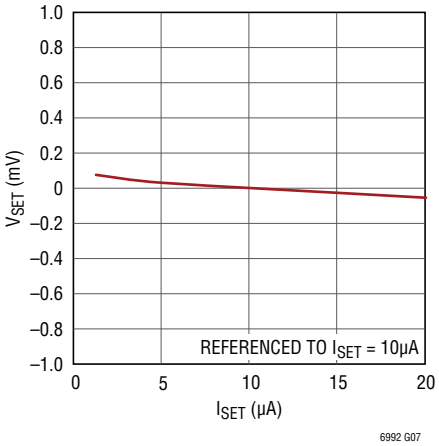
Frequency Drift vs Supply Voltage



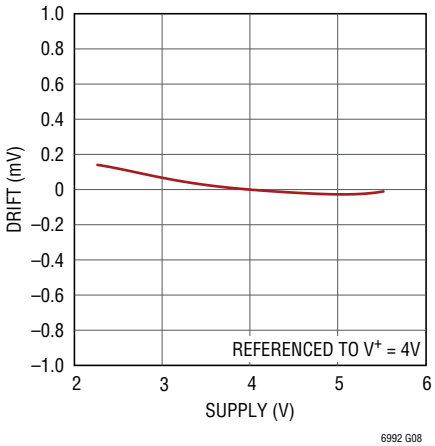
Typical V_{SET} Distribution



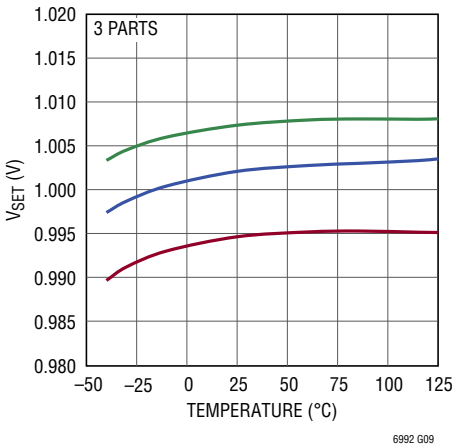
V_{SET} Drift vs I_{SET}



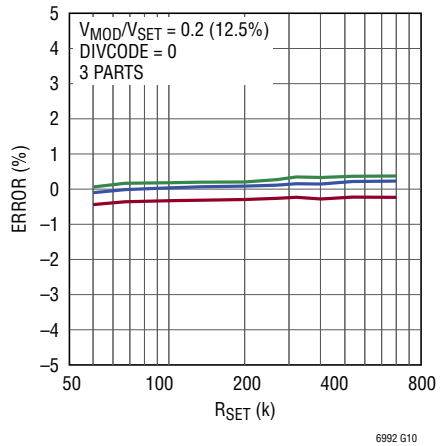
V_{SET} Drift vs Supply



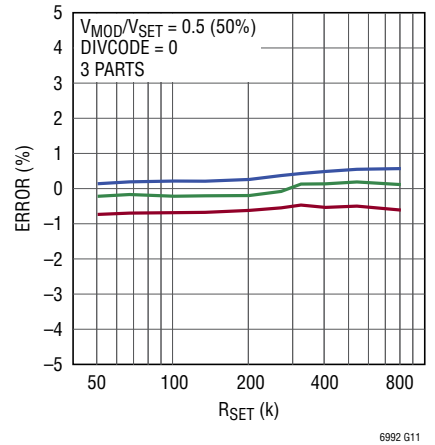
V_{SET} vs Temperature



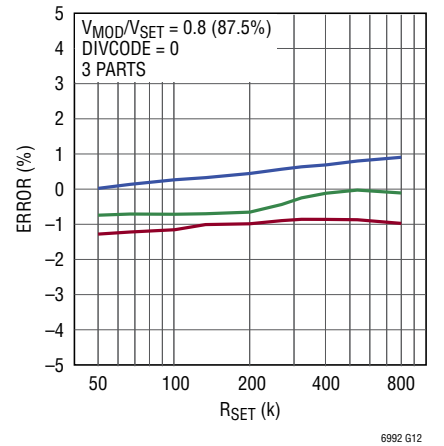
N_{DIV} = 1 Duty Cycle Error vs R_{SET}



N_{DIV} = 1 Duty Cycle Error vs R_{SET}



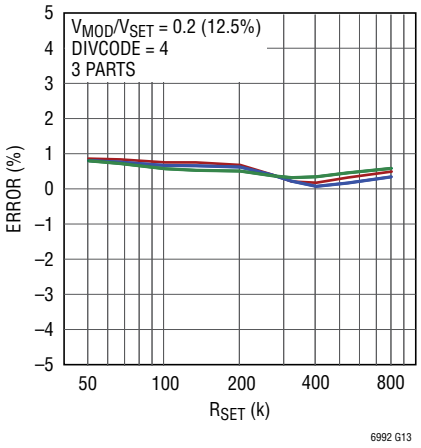
N_{DIV} = 1 Duty Cycle Error vs R_{SET}



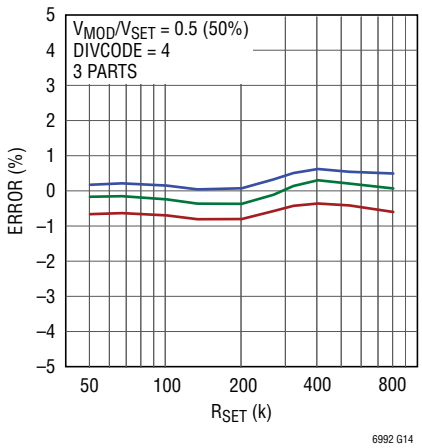
TYPICAL PERFORMANCE CHARACTERISTICS

V^+ = 3.3V, R_{SET} = 200k, and T_A = 25°C, unless otherwise noted.

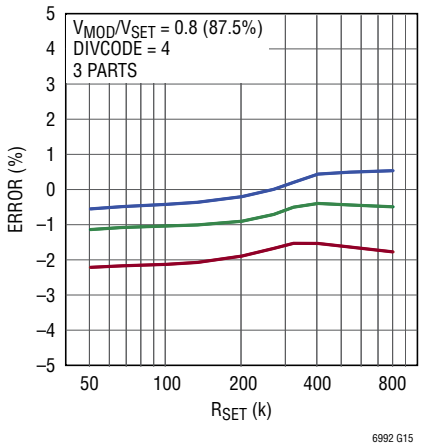
N_{DIV} > 1 Duty Cycle Error vs R_{SET}



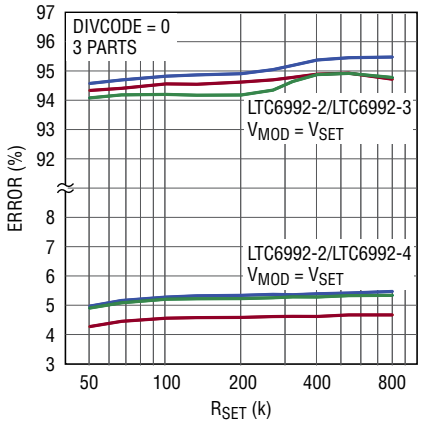
N_{DIV} > 1 Duty Cycle Error vs R_{SET}



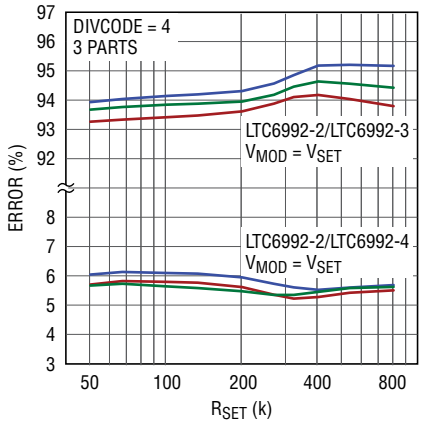
N_{DIV} > 1 Duty Cycle Error vs R_{SET}



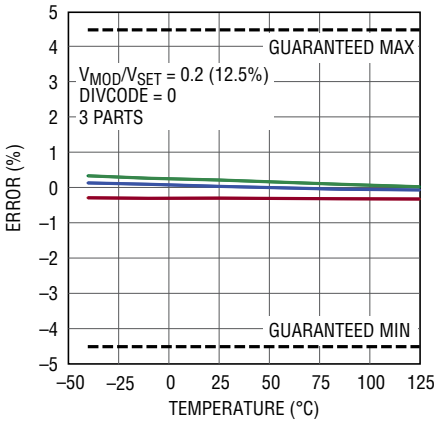
N_{DIV} = 1 Duty Cycle Clamps vs R_{SET}



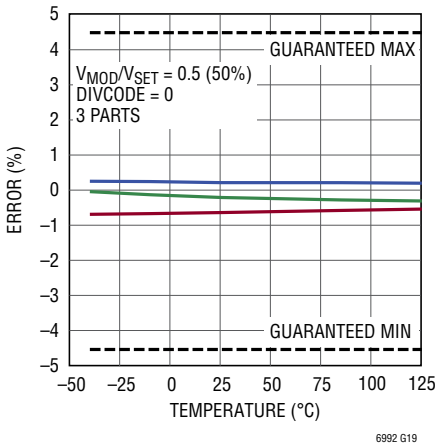
N_{DIV} > 1 Duty Cycle Error vs R_{SET}



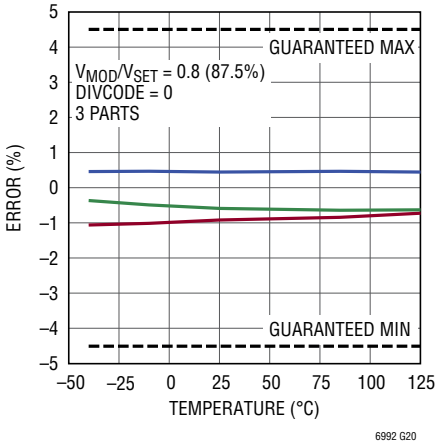
N_{DIV} = 1 Duty Cycle Error vs Temperature



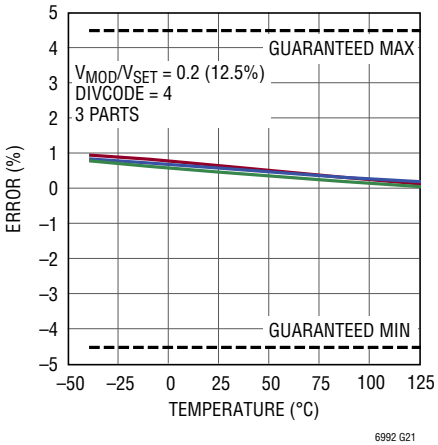
N_{DIV} = 1 Duty Cycle Error vs Temperature



N_{DIV} = 1 Duty Cycle Error vs Temperature



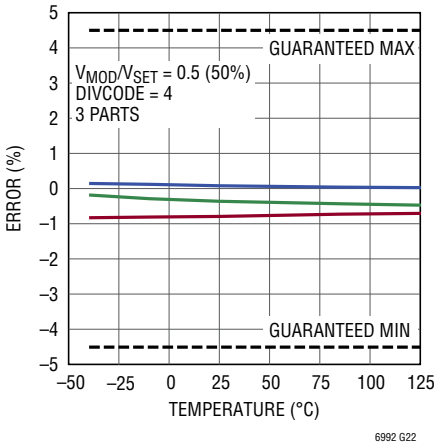
N_{DIV} > 1 Duty Cycle Error vs Temperature



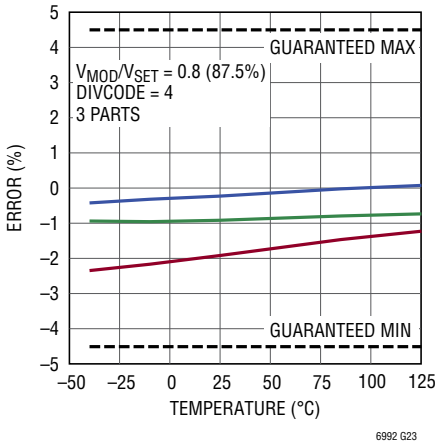
TYPICAL PERFORMANCE CHARACTERISTICS

V^+ = 3.3V, R_{SET} = 200k, and T_A = 25°C, unless otherwise noted.

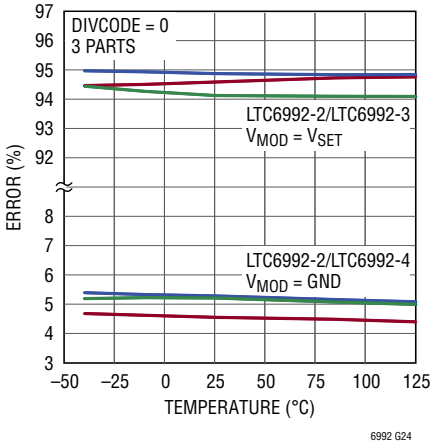
N_{DIV} > 1 Duty Cycle Error vs Temperature



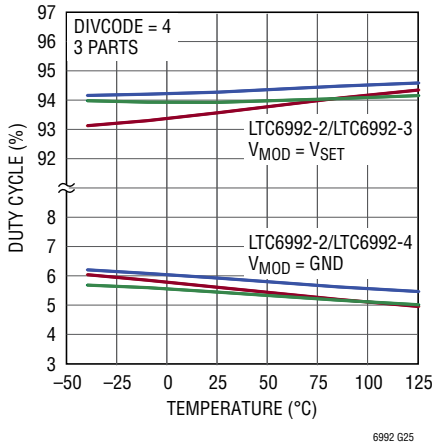
N_{DIV} > 1 Duty Cycle Error vs Temperature



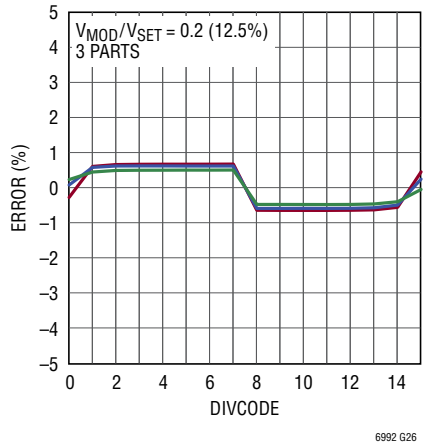
N_{DIV} = 1 Duty Cycle Clamps vs Temperature



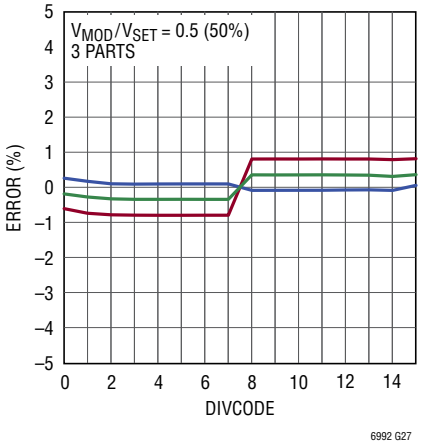
N_{DIV} > 1 Duty Cycle Clamps vs Temperature



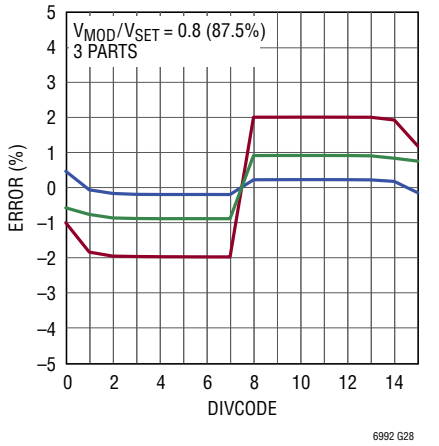
Duty Cycle Error vs DIVCODE



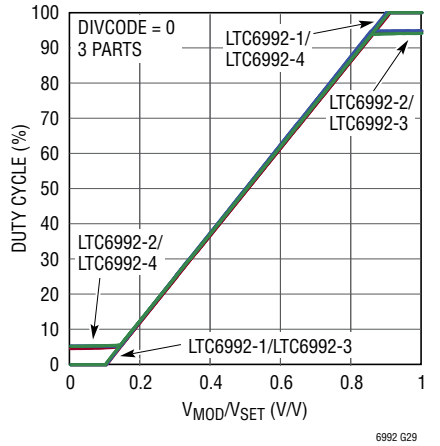
Duty Cycle Error vs DIVCODE



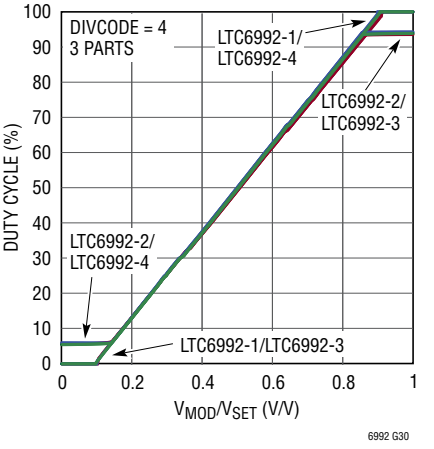
Duty Cycle Error vs DIVCODE



N_{DIV} = 1 Duty Cycle vs V_{MOD}/ V_{SET}



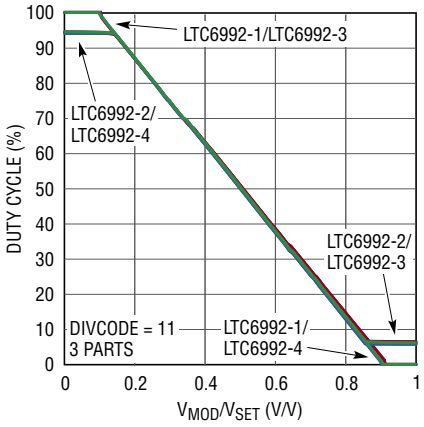
N_{DIV} > 1 Duty Cycle vs V_{MOD}/ V_{SET}



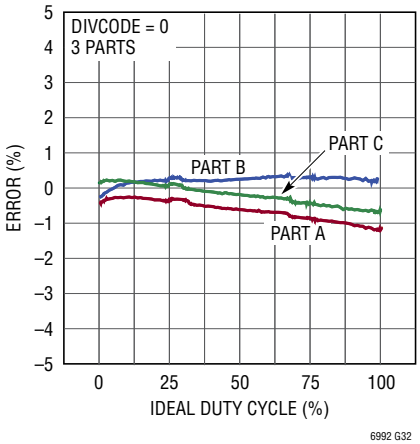
TYPICAL PERFORMANCE CHARACTERISTICS

V^+ = 3.3V, R_{SET} = 200k, and T_A = 25°C, unless otherwise noted.

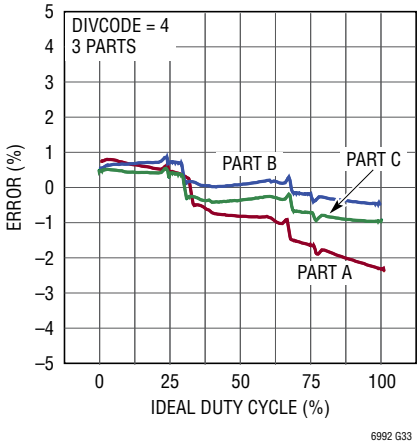
N_{DIV} > 1 Duty Cycle vs V_{MOD}/V_{SET}



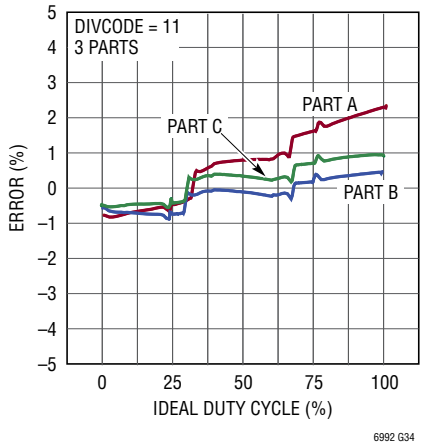
N_{DIV} = 1 Duty Cycle Error vs Ideal



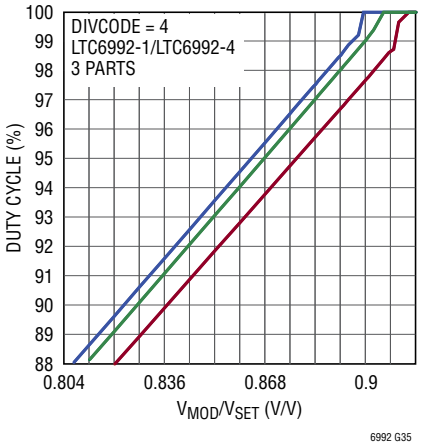
N_{DIV} > 1 Duty Cycle Error vs Ideal



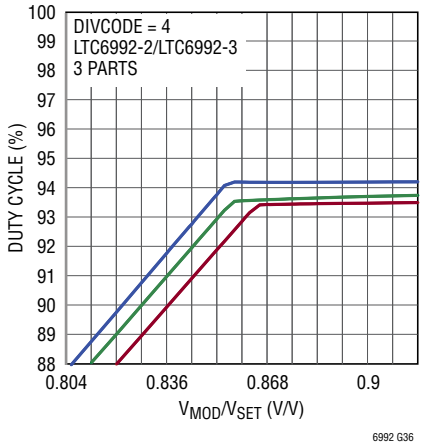
N_{DIV} > 1 Duty Cycle Error vs Ideal



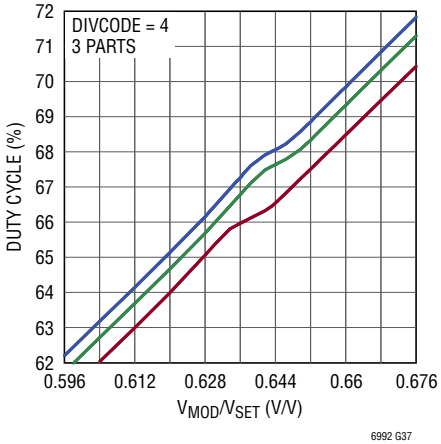
Linearity Near 100% Duty Cycle



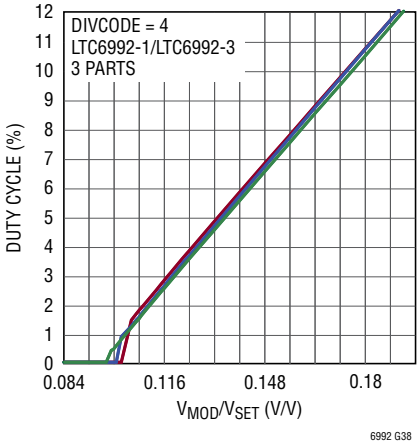
Linearity Near 95% Duty Cycle



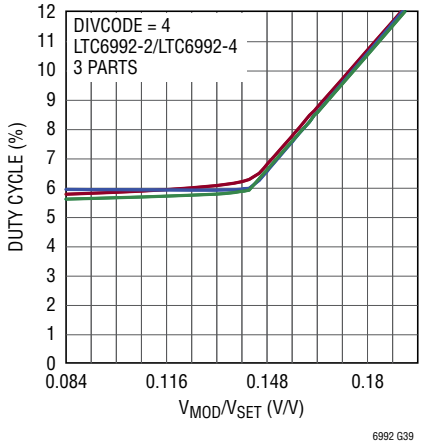
Linearity Near 67% Duty Cycle



Linearity Near 0% Duty Cycle



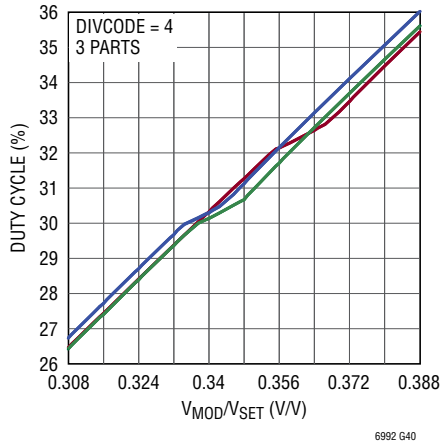
Linearity Near 5% Duty Cycle



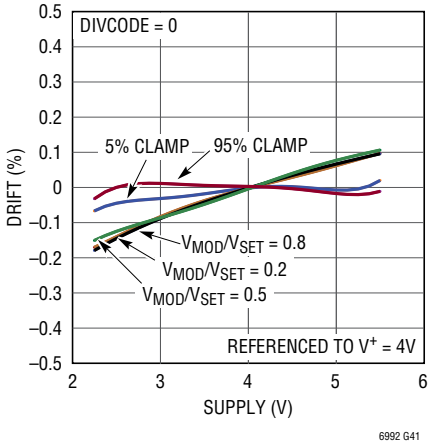
TYPICAL PERFORMANCE CHARACTERISTICS

V^+ = 3.3V, R_{SET} = 200k, and T_A = 25°C, unless otherwise noted.

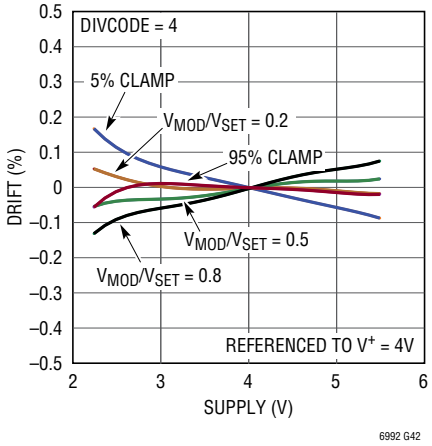
Linearity Near 31% Duty Cycle



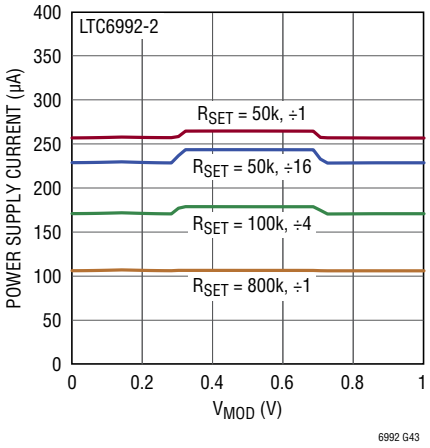
N_{DIV} = 1 Duty Cycle Drift vs Supply



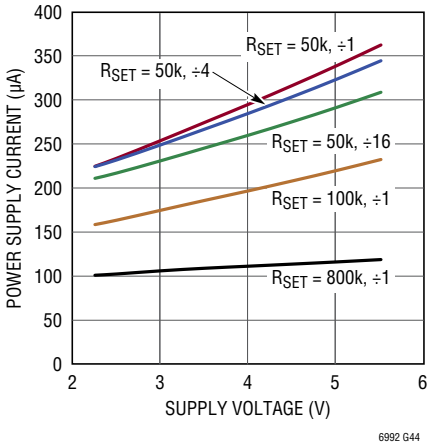
N_{DIV} > 1 Duty Cycle Drift vs Supply



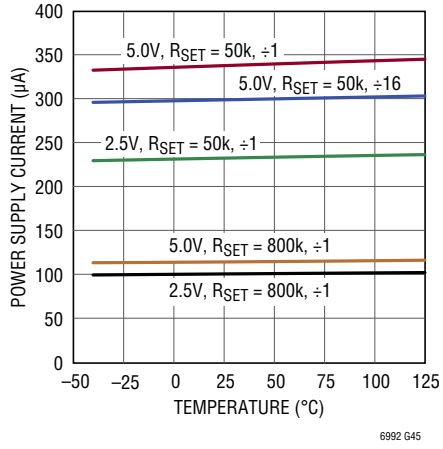
Supply Current vs V_{MOD}



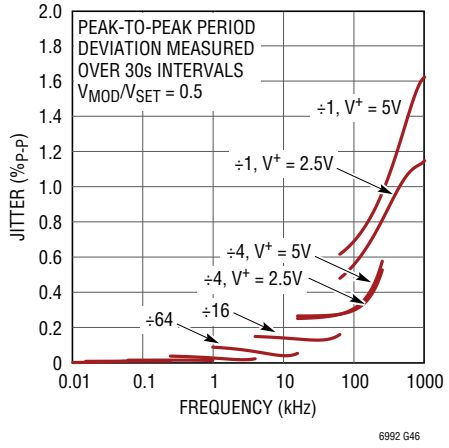
Supply Current vs Supply Voltage



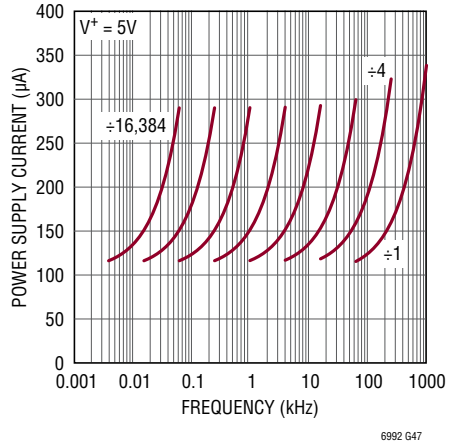
Supply Current vs Temperature



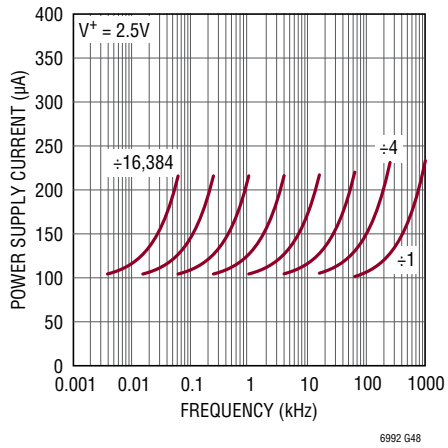
Jitter vs Frequency



Supply Current vs Frequency, 5V



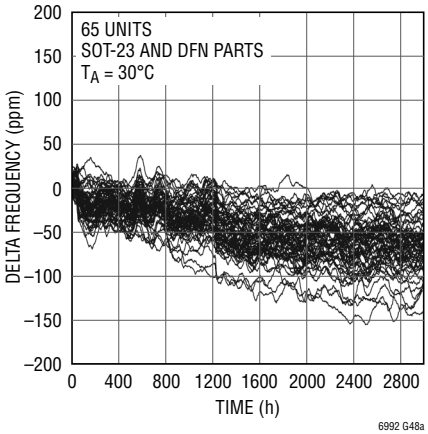
Supply Current vs Frequency, 2.5V



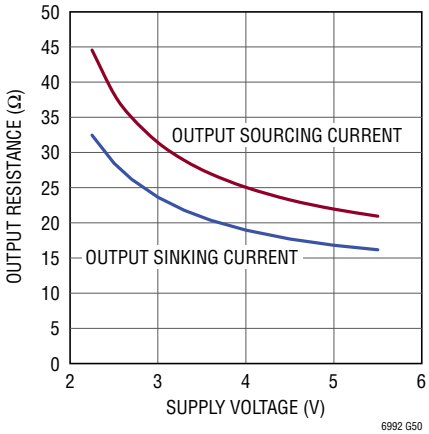
TYPICAL PERFORMANCE CHARACTERISTICS

V^+ = 3.3V, R_{SET} = 200k, and T_A = 25°C, unless otherwise noted.

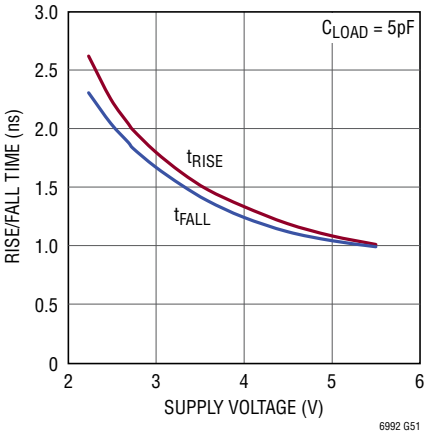
Typical Frequency Error vs Time (Long-Term Drift)



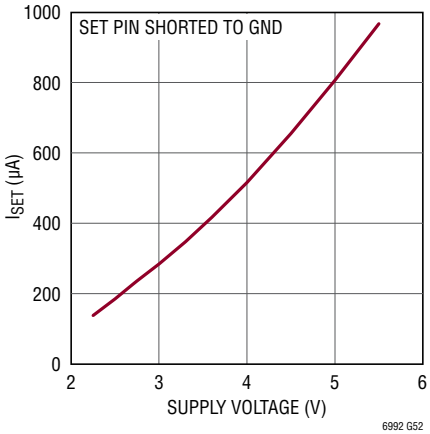
Output Resistance vs Supply Voltage



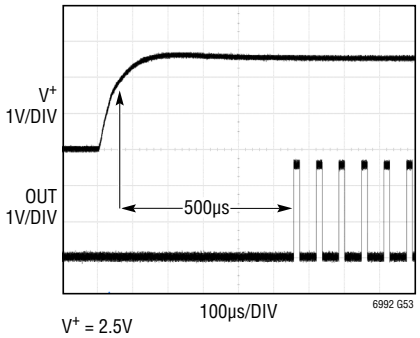
Rise and Fall Time vs Supply Voltage



Typical I_{SET} Current Limit vs V^+

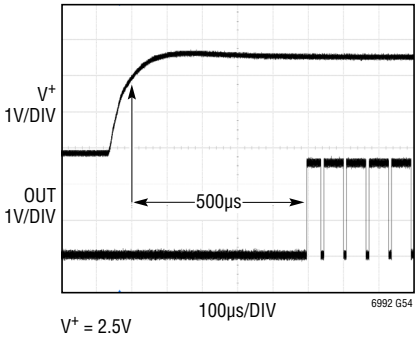


Typical Start-Up, POL = 0



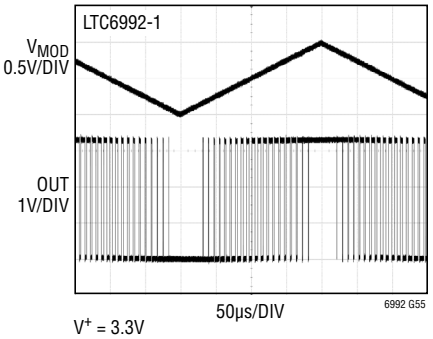
V^+ = 2.5V
DIVCODE = 3 (÷64)
R_{SET} = 50k
V_{MOD} = 0.3V (~25% DUTY CYCLE)

Typical Start-Up, POL = 1



V^+ = 2.5V
DIVCODE = 12 (÷64, POL = 1)
R_{SET} = 50k
V_{MOD} = 0.2V (~87.5% DUTY CYCLE)

125kHz Full Modulation



V^+ = 3.3V
DIVCODE = 1
R_{SET} = 100k

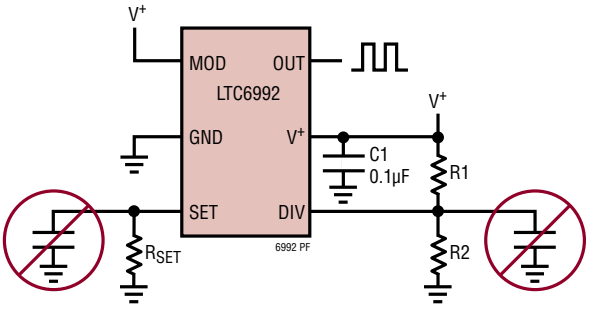
PIN FUNCTIONS (DCB/S6)

V+ (Pin 1/Pin 5): Supply Voltage (2.25V to 5.5V). This sup-ply should be kept free from noise and ripple. It should be bypassed directly to the GND pin with a 0.1µF capacitor.

DIV (Pin 2/Pin 4): Programmable Divider and Polarity Input. The DIV pin voltage (V_{DIV}) is internally converted into a 4-bit result (DIVCODE). V_{DIV} may be generated by a resistor divider between V+ and GND. Use 1% resistors to ensure an accurate result. The DIV pin and resistors should be shielded from the OUT pin or any other traces that have fast edges. Limit the capacitance on the DIV pin to less than 100pF so that V_{DIV} settles quickly. The MSB of DIVCODE (POL) determines if the PWM signal is inverted before driving the output. When POL = 1 the transfer function is inverted (duty cycle decreasing as V_{MOD} increases).

SET (Pin 3/Pin 3): Frequency-Setting Input. The voltage on the SET pin (V_{SET}) is regulated to 1V above GND. The amount of current sourced from the SET pin (I_{SET}) programs the master oscillator frequency. The I_{SET} current range is 1.25µA to 20µA. The output oscillation will stop if I_{SET} drops below approximately 500nA. A resistor connected between SET and GND is the most accurate way to set the frequency. For best performance, use a precision metal or thin film resistor of 0.5% or better tolerance and 50ppm/°C or better temperature coefficient. For lower accuracy applications an inexpensive 1% thick film resistor may be used.

Limit the capacitance on the SET pin to less than 10pF to minimize jitter and ensure stability. Capacitance less than 100pF maintains the stability of the feedback circuit regulating the V_{SET} voltage.

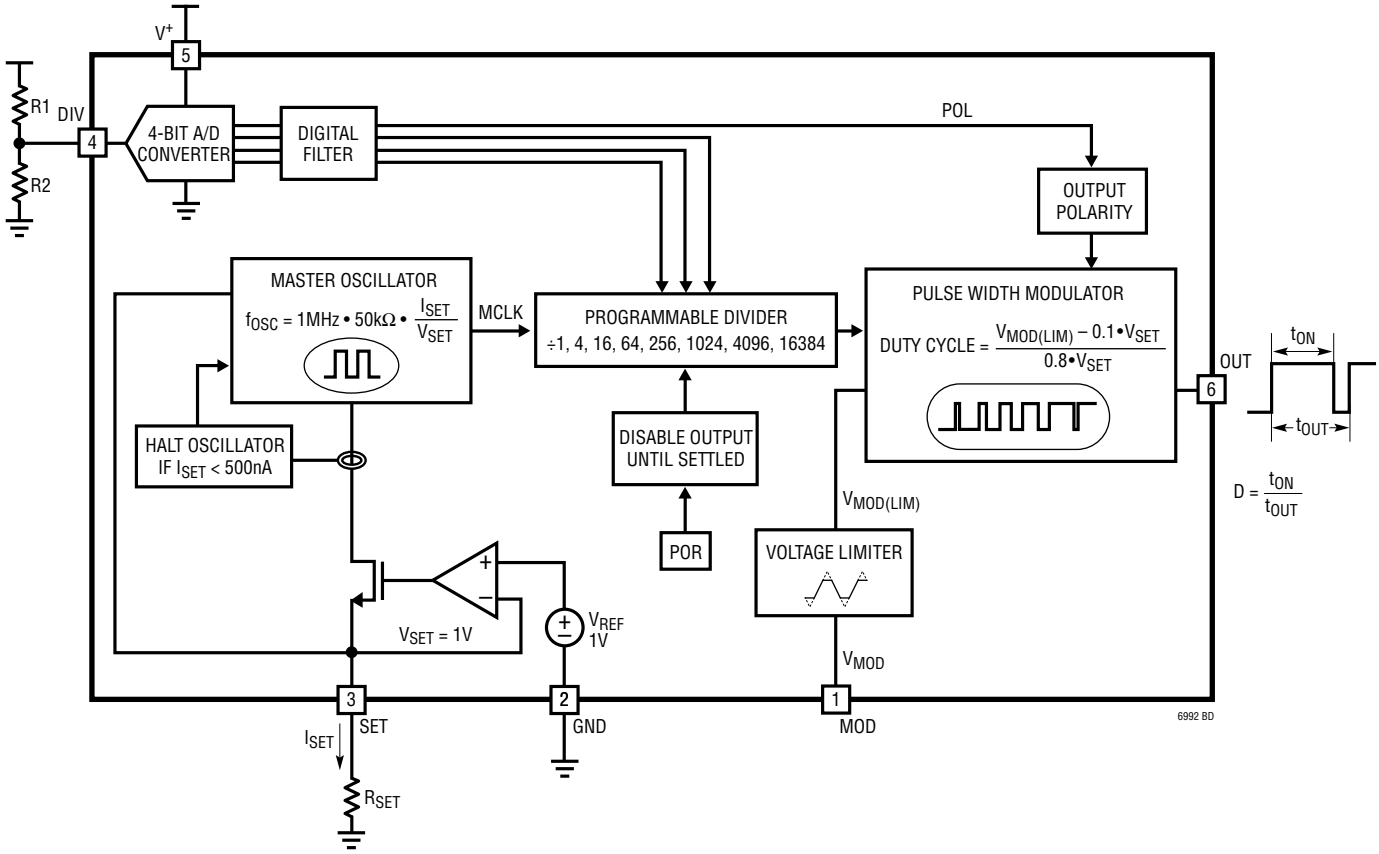


MOD (Pin 4/Pin 1): Pulse-Width Modulation Input. The voltage on the MOD pin controls the output duty cycle. The linear control range is between 0.1•V_{SET} and 0.9•V_{SET} (approximately 100mV to 900mV). Beyond those limits, the output will either clamp at 5% or 95%, or stop oscillating (0% or 100% duty cycle), depending on the version.

GND (Pin 5/Pin 2): Ground. Tie to a low inductance ground plane for best performance.

OUT (Pin 6/Pin 6): Oscillator Output. The OUT pin swings from GND to V+ with an output resistance of approximately 30Ω. The duty cycle is determined by the voltage on the MOD pin. When driving an LED or other low-impedance load a series output resistor should be used to limit the source/sink current to 20mA.

BLOCK DIAGRAM (S6 Package Pin Numbers Shown)



OPERATION

The LTC6992 is built around a master oscillator with a 1MHz maximum frequency. The oscillator is controlled by the SET pin current (I_{SET}) and voltage (V_{SET}), with a 1MHz • 50k conversion factor that is accurate to ±0.8% under typical conditions.

$$f_{MASTER} = \frac{1}{t_{MASTER}} = 1MHz \bullet 50k \bullet \frac{I_{SET}}{V_{SET}}$$

A feedback loop maintains V_{SET} at 1V ±30mV, leaving I_{SET} as the primary means of controlling the output frequency. The simplest way to generate I_{SET} is to connect a resistor (R_{SET}) between SET and GND, such that $I_{SET} = V_{SET}/R_{SET}$. The master oscillator equation reduces to:

$$f_{MASTER} = \frac{1}{t_{MASTER}} = \frac{1MHz \bullet 50k}{R_{SET}}$$

From this equation, it is clear that V_{SET} drift will not affect the output frequency when using a single program resistor (R_{SET}). Error sources are limited to R_{SET} tolerance and the inherent frequency accuracy Δf_{OUT} of the LTC6992.

R_{SET} may range from 50k to 800k (equivalent to I_{SET} between 1.25µA and 20µA).

The LTC6992 includes a programmable frequency divider which can further divide the frequency by 1, 4, 16, 64, 256, 1024, 4096 or 16384 before driving the OUT pin. The divider ratio N_{DIV} is set by a resistor divider attached to the DIV pin.

$$f_{OUT} = \frac{1}{t_{OUT}} = \frac{1MHz \bullet 50k}{N_{DIV}} \bullet \frac{I_{SET}}{V_{SET}}$$

With R_{SET} in place of V_{SET}/I_{SET} the equation reduces to:

$$f_{OUT} = \frac{1}{t_{OUT}} = \frac{1MHz \bullet 50k}{N_{DIV} \bullet R_{SET}}$$

DIVCODE

The DIV pin connects to an internal, V^+ referenced 4-bit A/D converter that determines the DIVCODE value. DIVCODE programs two settings on the LTC6992:

1. DIVCODE determines the output frequency divider setting, N_{DIV}.
2. DIVCODE determines the output polarity, via the POL bit.

V_{DIV} may be generated by a resistor divider between V^+ and GND as shown in Figure 2.

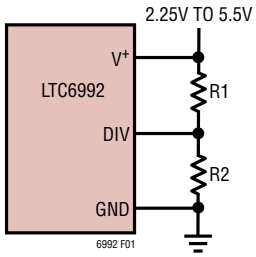


Figure 1. Simple Technique for Setting DIVCODE

OPERATION

Table 1. DIVCODE Programming

DIVCODE	POL	N_{DIV}	RECOMMENDED f_{OUT}	R1 (kΩ)	R2 (kΩ)	V_{DIV}/V^+
0	0	1	62.5kHz to 1MHz	Open	Short	≤0.03125 ±0.015
1	0	4	15.63kHz to 250kHz	976	102	0.09375 ±0.015
2	0	16	3.906kHz to 62.5kHz	976	182	0.15625 ±0.015
3	0	64	976.6Hz to 15.63kHz	1000	280	0.21875 ±0.015
4	0	256	244.1Hz to 3.906kHz	1000	392	0.28125 ±0.015
5	0	1024	61.04Hz to 976.6Hz	1000	523	0.34375 ±0.015
6	0	4096	15.26Hz to 244.1Hz	1000	681	0.40625 ±0.015
7	0	16384	3.815Hz to 61.04Hz	1000	887	0.46875 ±0.015
8	1	16384	3.815Hz to 61.04Hz	887	1000	0.53125 ±0.015
9	1	4096	15.26Hz to 244.1Hz	681	1000	0.59375 ±0.015
10	1	1024	61.04Hz to 976.6Hz	523	1000	0.65625 ±0.015
11	1	256	244.1Hz to 3.906kHz	392	1000	0.71875 ±0.015
12	1	64	976.6Hz to 15.63kHz	280	1000	0.78125 ±0.015
13	1	16	3.906kHz to 62.5kHz	182	976	0.84375 ±0.015
14	1	4	15.63kHz to 250kHz	102	976	0.90625 ±0.015
15	1	1	62.5kHz to 1MHz	Short	Open	≥0.96875 ±0.015

Table 1 offers recommended 1% resistor values that accurately produce the correct voltage division as well as the corresponding N_{DIV} and POL values for the recommended resistor pairs. Other values may be used as long as:

1. The V_{DIV}/V^+ ratio is accurate to ±1.5% (including resistor tolerances and temperature effects).
2. The driving impedance (R1||R2) does not exceed 500kΩ.

If the voltage is generated by other means (i.e. the output of a DAC) it must track the V^+ supply voltage. The last column in Table 1 shows the ideal ratio of V_{DIV} to the supply voltage, which can also be calculated as:

$$\frac{V_{DIV}}{V^+} = \frac{DIVCODE + 0.5}{16} \pm 1.5\%$$

For example, if the supply is 3.3V and the desired DIVCODE is 4, V_{DIV} = 0.281 • 3.3V = 928mV ± 50mV.

Figure 2 illustrates the information in Table 1, showing that N_{DIV} is symmetric around the DIVCODE midpoint.

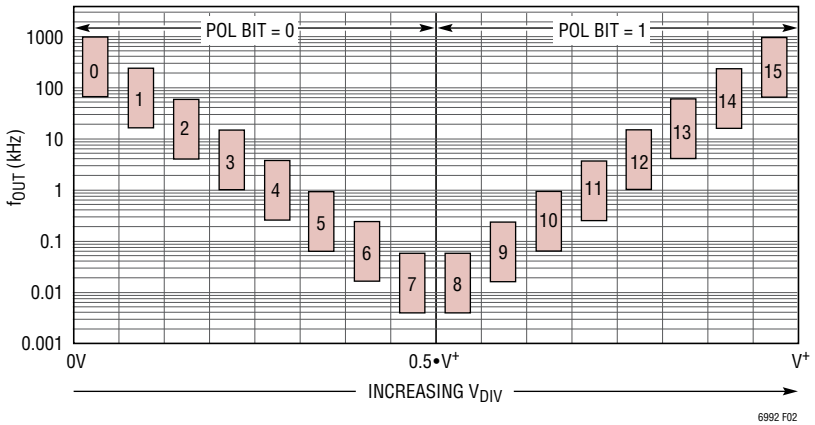


Figure 2. Frequency Range and POL Bit vs DIVCODE

OPERATION

Pulse Width (Duty Cycle) Modulation

The MOD pin is a high impedance analog input providing direct control of the output duty cycle. The duty cycle is proportional to the voltage applied to the MOD pin, V_{MOD}.

$$\text{Duty Cycle} = D = \frac{V_{MOD}}{0.8 \bullet V_{SET}} - \frac{1}{8}$$

The PWM duty cycle accuracy ΔD specifies that the above equation is valid to within ±4.5% for V_{MOD} between 0.2 • V_{SET} and 0.8 • V_{SET} (12.5% to 87.5% duty cycle).

Since V_{SET} = 1V ±30mV, the duty cycle equation may be approximated by the following equation.

$$\text{Duty Cycle} = D \cong \frac{V_{MOD} - 100mV}{800mV}$$

The V_{MOD} control range is approximately 0.1V to 0.9V. Driving V_{MOD} beyond that range (towards GND or V^+) will have no further affect on the duty cycle.

Duty Cycle Limits

The only difference between the four versions of the LTC6992 is the limits, or clamps, placed on the output duty cycle. The LTC6992-1 generates output duty cycles ranging from 0% to 100%. At 0% or 100% the output will stop oscillating and rest at GND or V^+, respectively.

The LTC6992-2 will never stop oscillating, regardless of the V_{MOD} level. Internal clamping circuits limit its duty cycle to a 5% to 95% range (1% to 99% guaranteed). Therefore, its V_{MOD} control range is 0.14 • V_{SET} to 0.86 • V_{SET} (approximately 0.14V to 0.86V).

The LTC6992-3 and LTC6992-4 complete the family by providing one-sided clamping. The LTC6992-3 allows 0% to 95% duty cycle, and the LTC6992-4 allows 5% to 100% duty cycle.

Output Polarity (POL Bit)

The duty cycle equation describes a proportional transfer function, where duty cycle increases as V_{MOD} increases. The LTC6992 includes a POL bit (determined by the DIVCODE as described earlier) that inverts the output signal. This makes the duty cycle gain negative, reducing duty cycle as V_{MOD} increases.

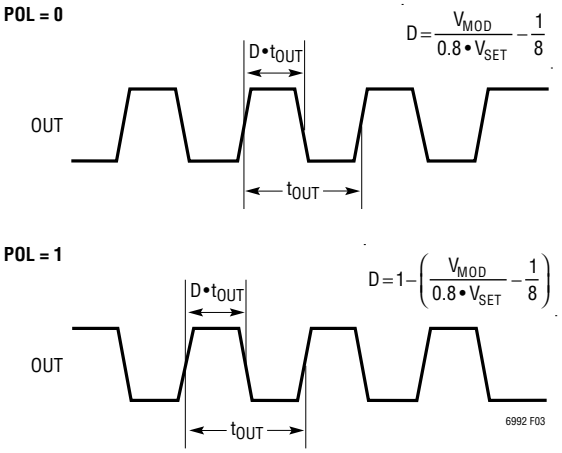


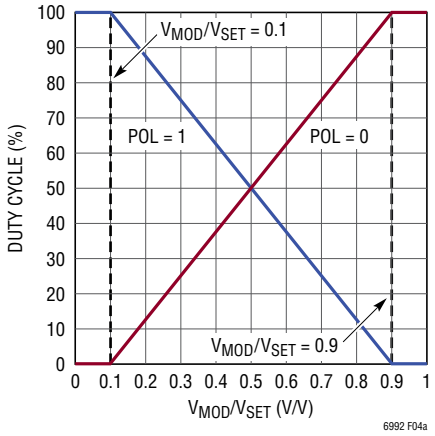
Figure 3. POL Bit Functionality

OPERATION

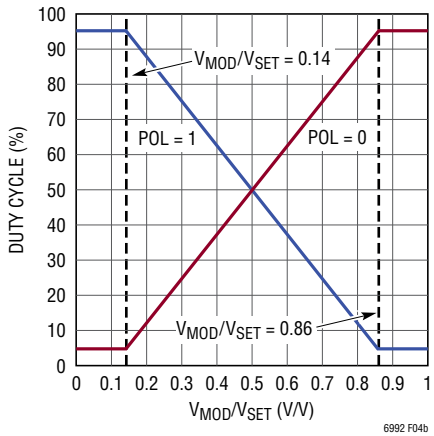
POL = 1 forces a simple logic inversion, so it changes the duty cycle range of the LTC6992-3 (making it 100% to 5%) and LTC6992-4 (making it 95% to 0%). These transfer functions are detailed in Figure 4.

Table 2. Duty Cycle Ranges

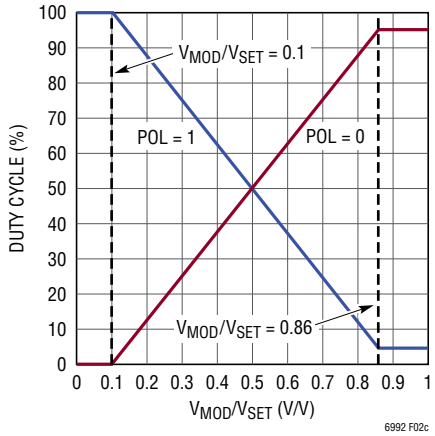
PART NUMBER	DUTY CYCLE RANGE vs V_{MOD} = 0V → 1V	
	POL = 0	POL = 1
LTC6992-1	0% to 100%	100% to 0%
LTC6992-2	5% to 95%	95% to 5%
LTC6992-3	0% to 95%	100% to 5%
LTC6992-4	5% to 100%	95% to 0%



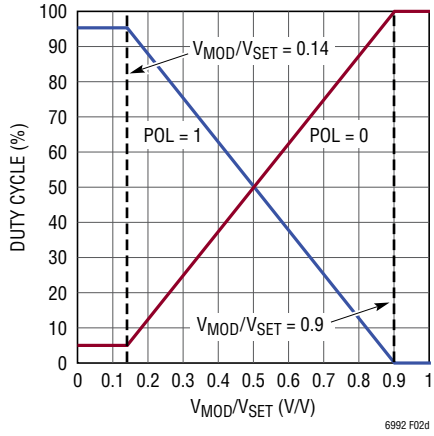
LTC6992-1



LTC6992-2



LTC6992-3



LTC6992-4

Figure 4. PWM Transfer Functions for All LTC6992 Family Parts

OPERATION

Changing DIVCODE After Start-Up

Following start-up, the A/D converter will continue monitoring V_{DIV} for changes. Changes to DIVCODE will be recognized slowly, as the LTC6992 places a priority on eliminating any "wandering" in the DIVCODE. The typical delay depends on the difference between the old and new DIVCODE settings and is proportional to the master oscillator period.

$$t_{DIVCODE} = 16 \bullet (\Delta DIVCODE + 6) \bullet t_{MASTER}$$

A change in DIVCODE will not be recognized until it is stable, and will not pass through intermediate codes. A digital filter is used to guarantee the DIVCODE has settled to a new value before making changes to the output. Then the output will make a clean (glitchless) transition to the new divider setting.

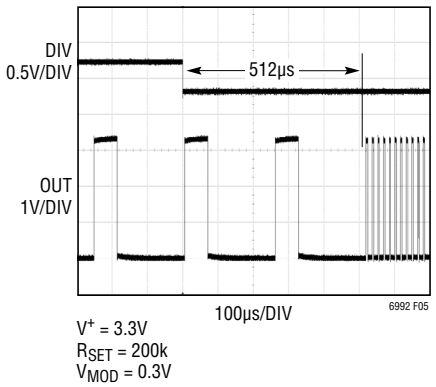


Figure 5. DIVCODE Change from 3 to 1

Start-Up Time

When power is first applied, the power-on reset (POR) circuit will initiate the start-up time, t_{START}. The OUT pin is held low during this time. The typical value for t_{START} ranges from 0.5ms to 8ms depending on the master oscillator frequency (independent of N_{DIV}):

$$t_{START(TYP)} = 500 \bullet t_{MASTER}$$

The output will begin oscillating after t_{START}. If POL = 0 the first pulse has the correct width. If POL = 1 (DIVCODE ≥ 8), the first pulse width can be shorter or longer than expected, depending on the duty cycle setting, and will never be less than 25% of t_{OUT}.

During start-up, the DIV pin A/D converter must determine the correct DIVCODE before the output is enabled. The start-up time may increase if the supply or DIV pin voltages are not stable. For this reason, it is recommended to minimize the capacitance on the DIV pin so it will properly track V^+. Less than 100pF will not affect performance.

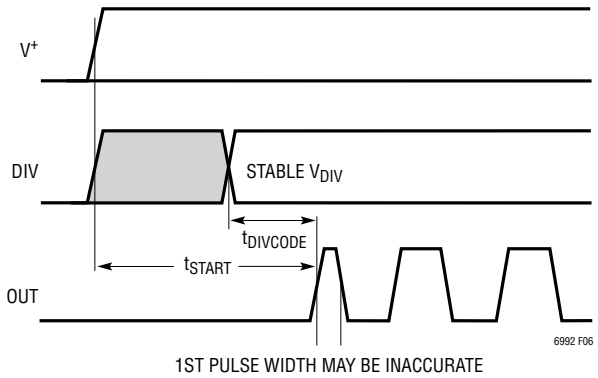


Figure 6. Start-Up Timing Diagram

APPLICATIONS INFORMATION

Basic Operation

The simplest and most accurate method to program the LTC6992 is to use a single resistor, R_{SET}, between the SET and GND pins. The design procedure is a four step process. After choosing the proper LTC6992 version and POL bit setting, select the N_{DIV} value and then calculate the value for the R_{SET} resistor.

Alternatively, Analog Devices offers the easy to use TimerBlox Designer tool to quickly design any LTC6992 based circuit. Use the free TimerBlox LTC6992: PWM Web-Based Design Tool.

Step 1: Selecting the POL Bit Setting

Most applications will use POL = 0, resulting in a positive transfer function. However, some applications may require a negative transfer function, where increasing V_{MOD} reduces the output duty cycle. For example, if the LTC6992 is used in a feedback loop, POL = 1 may be required to achieve negative feedback.

Step 2: Selecting the LTC6992 Version

The difference between the LTC6992 versions is observed at the endpoints of the duty cycle control range. Applications that require the output to never stop oscillating should use the LTC6992-2. On the other hand, if the output should be allowed to rest at GND or V^+ (0% or 100% duty cycle), select the LTC6992-1.

The LTC6992-3 and LTC6992-4 clamp the duty cycle at only one end of the control range, allowing the output to stop oscillating at the other extreme. If POL = 1 the clamp will swap from low duty cycle to high, or vice-versa. Refer to Table 2 and Figure 4 for assistance in selecting the proper version.

Step 3: Selecting the N_{DIV} Frequency Divider Value

As explained earlier, the voltage on the DIV pin sets the DIVCODE which determines both the POL bit and the N_{DIV} value. For a given output frequency, N_{DIV} should be selected to be within the following range.

$$\frac{62.5kHz}{f_{OUT}} \le N_{DIV} \le \frac{1MHz}{f_{OUT}} \quad (1a)$$

To minimize supply current, choose the lowest N_{DIV} value (generally recommended). For faster start-up or decreased jitter, choose a higher N_{DIV} setting. Alternatively, use Table 1 as a guide to select the best N_{DIV} value for the given application.

With POL already chosen, this completes the selection of DIVCODE. Use Table 1 to select the proper resistor divider or V_{DIV}/V^+ ratio to apply to the DIV pin.

Step 4: Calculate and Select R_{SET}

The final step is to calculate the correct value for R_{SET} using the following equation.

$$R_{SET} = \frac{1MHz \bullet 50k}{N_{DIV} \bullet f_{OUT}} \quad (1b)$$

Select the standard resistor value closest to the calculated value.

Example: Design a PWM circuit that satisfies the following requirements:

- f_{OUT} = 20kHz
- Positive V_{MOD} to duty cycle response
- Output can reach 100% duty cycle, but not 0%
- Minimum power consumption

Step 1: Selecting the POL Bit Setting

For positive transfer function (duty cycle increases with V_{MOD}), choose POL = 0.

Step 2: Selecting the LTC6992 Version

To limit the minimum duty cycle, but allow the maximum duty cycle to reach 100%, choose LTC6992-4. (Note that if POL = 1 the LTC6992-3 would be the correct choice.)

Step 3: Selecting the N_{DIV} Frequency Divider Value

Choose an N_{DIV} value that meets the requirements of Equation (1a).

$$3.125 \le N_{DIV} \le 50$$

Potential settings for N_{DIV} include 4 and 16. N_{DIV} = 4 is the best choice, as it minimizes supply current by using

APPLICATIONS INFORMATION

a large R_{SET} resistor. POL = 0 and N_{DIV} = 4 requires DIVCODE = 1. Using Table 1, choose the R1 and R2 values to program DIVCODE = 1.

Step 4: Select R_{SET}

Calculate the correct value for R_{SET} using Equation (1b).

$$R_{SET} = \frac{1MHz \bullet 50k}{4 \bullet 20kHz} = 625k$$

Since 625k is not available as a standard 1% resistor, substitute 619k if a 0.97% frequency shift is acceptable. Otherwise, select a parallel or series pair of resistors such as 309k and 316k to attain a more precise resistance.

The completed design is shown in Figure 7.

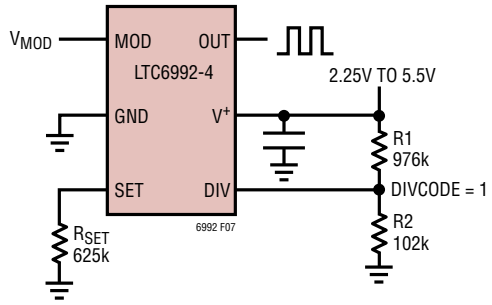


Figure 7. 20kHz PWM Oscillator

Duty Cycle Sensitivity to ΔV_{SET}

The output duty cycle is proportional to the ratio of V_{MOD}/V_{SET}. Since V_{SET} can vary up to ±30mV from 1V it can effectively gain or attenuate V_{MOD}, as shown below when ΔV_{SET} is added to the equation.

$$D = \frac{V_{MOD}}{0.8 \bullet (V_{SET} + \Delta V_{SET})} - \frac{1}{8}$$

For many designs, the absolute V_{MOD} to duty cycle accuracy is not critical. For others, making the simplifying assumption of ΔV_{SET} = 0V creates the potential for additional duty cycle error, which increases with V_{MOD}, reaching a maximum of 3.4% if ΔV_{SET} = –30mV.

$$\Delta D \cong -\frac{V_{MOD}}{800mV} \bullet \frac{\Delta V_{SET}}{V_{SET}} \cong -\left(D_{IDEAL} + \frac{1}{8}\right) \bullet \frac{\Delta V_{SET}}{V_{SET}}$$

Figure 8 demonstrates the worst-case impact of this variation (if V_{SET} is at its 0.97V or 1.03V limits).

This error is in addition to the inherent PWM duty cycle accuracy spec ΔD (±4.5%), so care should be taken if accuracy at high duty cycles (V_{MOD} near 0.9V) is critical.

Sensitivity to ΔV_{SET} can be eliminated by making V_{MOD} proportional to V_{SET}. For example, Figure 9 shows a simple circuit for generating an arbitrary duty cycle. The equation for duty cycle does not depend on V_{SET} at all.

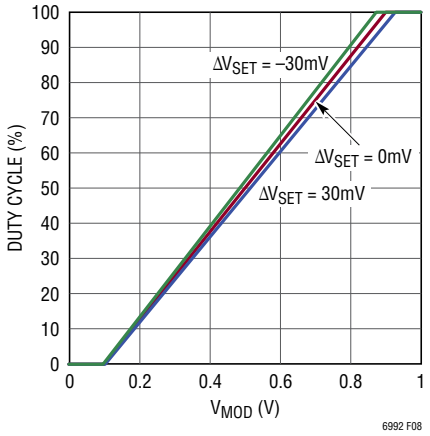


Figure 8. Duty Cycle Variation Due to ΔV_{SET}

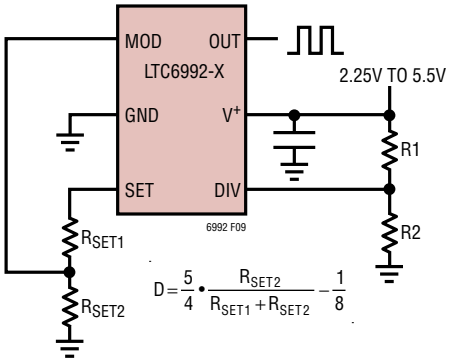


Figure 9. Fixed-Frequency, Arbitrary Duty Cycle Oscillator

APPLICATIONS INFORMATION

I_{SET} Extremes (Master Oscillator Frequency Extremes)

When operating with I_{SET} outside of the recommended 1.25µA to 20µA range, the master oscillator operates outside of the 62.5kHz to 1MHz range in which it is most accurate.

The oscillator will still function with reduced accuracy for I_{SET} < 1.25µA. At approximately 500nA, the oscillator output will be frozen in its current state. The output could halt in a high or low state. This avoids introducing short pulses while frequency modulating a very low frequency output.

At the other extreme, it is not recommended to operate the master oscillator beyond 2MHz because the accuracy of the DIV pin ADC will suffer.

Pulse Width Modulation Bandwidth and Settling Time

The LTC6992 has a wide PWM bandwidth, making it suitable for a variety of feedback applications. Figure 10 shows that the frequency response is flat for modulation frequencies up to nearly 1/10 of the output frequency. Beyond that point, some peaking may occur (depending on N_{DIV} and average duty cycle setting).

Duty cycle settling time depends on the master oscillator frequency. Following a ±80mV step change in V_{MOD}, the duty cycle takes approximately eight master clock cycles (8 • t_{MASTER}) to settle to within 1% of the final value. Examples are shown in Figure 11a and Figure 11b.

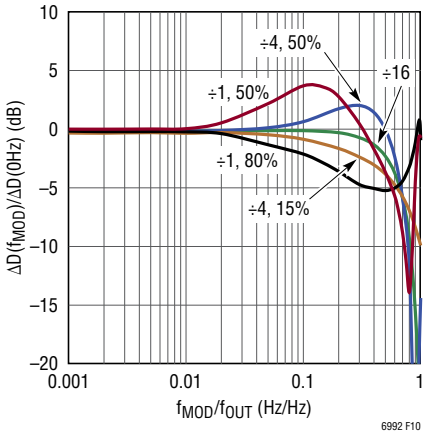
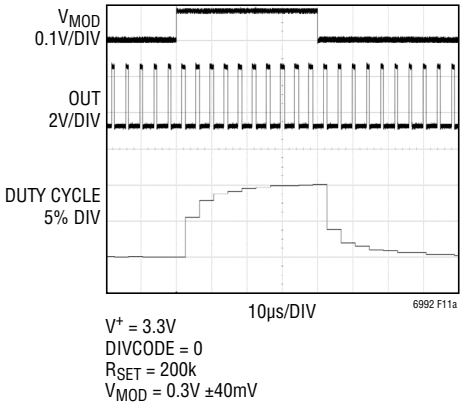
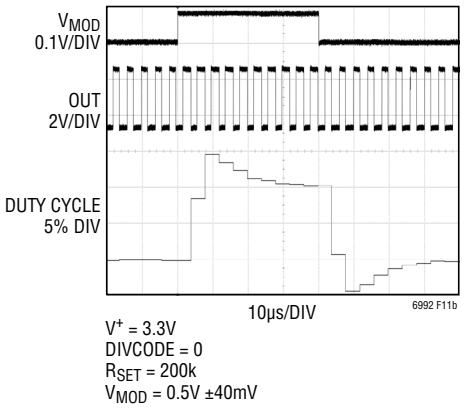


Figure 10. PWM Frequency Response



(a) 25% Duty Cycle



(b) 50% Duty Cycle

Figure 11. PWM Settling Time

APPLICATIONS INFORMATION

Power Supply Current

The power supply current varies with frequency, supply voltage and output loading. It can be estimated under any condition using the following equation:

If N_{DIV} = 1 (DIVCODE = 0 or 15):

$$I_{S(TYP)} \approx V^+ \bullet f_{OUT} \bullet (39pF + C_{LOAD})$$

$$\cdots + \frac{V^+}{320k\Omega} + \frac{V^+ \bullet \text{Duty Cycle}}{R_{LOAD}} + 2.2 \bullet I_{SET} + 85\mu A$$

If N_{DIV} > 1 (DIVCODE = 1 or 14):

$$I_{S(TYP)} \approx V^+ \bullet N_{DIV} \bullet f_{OUT} \bullet 27pF$$

$$\cdots + V^+ \bullet f_{OUT} \bullet (28pF + C_{LOAD})$$

SUPPLY BYPASSING AND PCB LAYOUT GUIDELINES

The LTC6992 is a 2.4% accurate silicon oscillator when used in the appropriate manner. The part is simple to use and by following a few rules, the expected performance is easily achieved. Adequate supply bypassing and proper PCB layout are important to ensure this.

Figure 12 shows example PCB layouts for both the TSOT-23 and DFN packages using 0603 sized passive components. The layouts assume a two layer board with a ground plane layer beneath and around the LTC6992. These layouts are a guide and need not be followed exactly.

1. Connect the bypass capacitor, C1, directly to the V+ and GND pins using a low inductance path. The connection from C1 to the V+ pin is easily done directly on the top layer. For the DFN package, C1's connection to GND is also simply done on the top layer. For the TSOT-23, OUT can be routed through the C1 pads to allow a good C1 GND connection. If the PCB design rules do not allow that, C1's GND connection can be accomplished through multiple vias to the ground plane. Multiple vias for both the GND pin connection to the ground plane and the C1 connection to the ground plane are recommended to minimize the inductance. Capacitor C1 should be a 0.1µF ceramic capacitor.
2. Place all passive components on the top side of the board. This minimizes trace inductance.
3. Place R_{SET} as close as possible to the SET pin and make a direct, short connection. The SET pin is a current summing node and currents injected into this pin directly modulate the operating frequency. Having a short connection minimizes the exposure to signal pickup.
4. Connect R_{SET} directly to the GND pin. Using a long path or vias to the ground plane will not have a significant affect on accuracy, but a direct, short connection is recommended and easy to apply.
5. Use a ground trace to shield the SET pin. This provides another layer of protection from radiated signals.
6. Place R1 and R2 close to the DIV pin. A direct, short connection to the DIV pin minimizes the external signal coupling.

APPLICATIONS INFORMATION

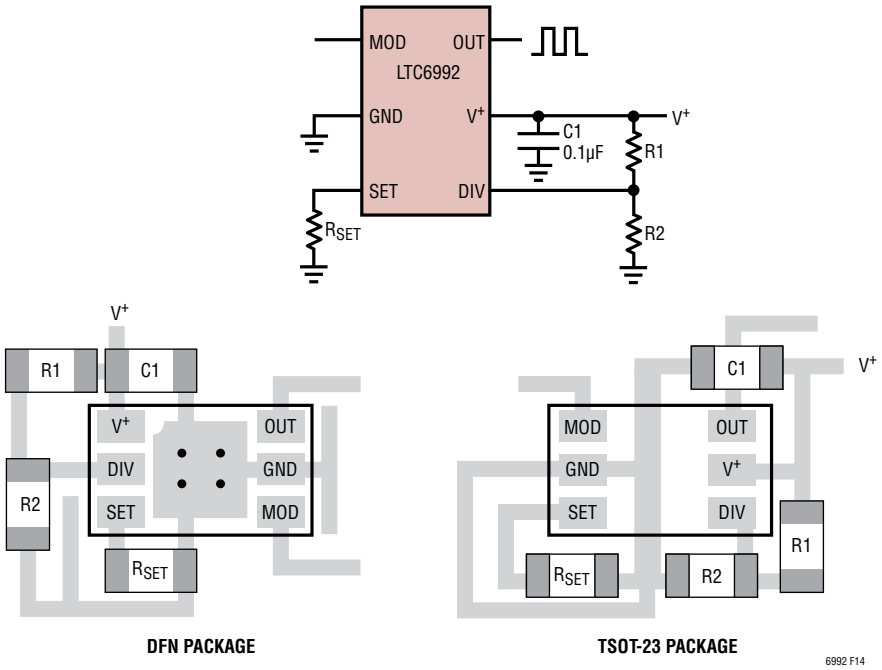
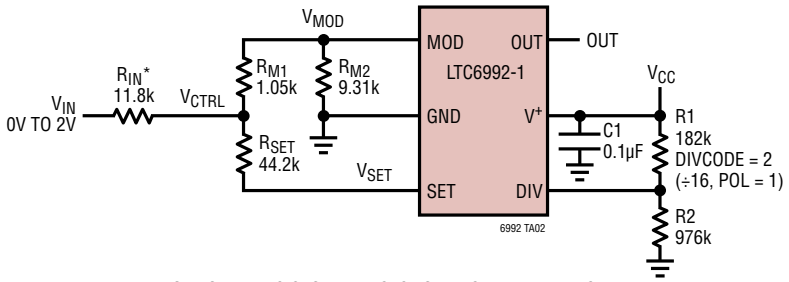


Figure 12. Supply Bypassing and PCB Layout

TYPICAL APPLICATIONS

Constant On-Time Modulator



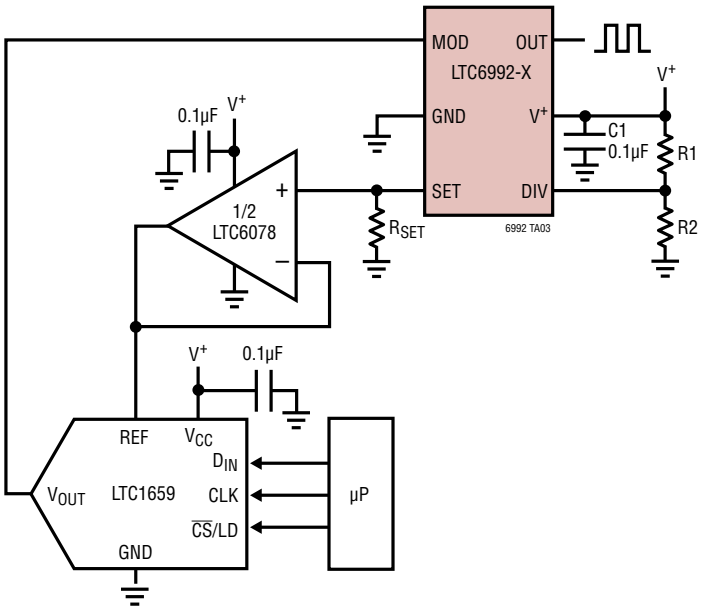
*OPTIONAL RESISTOR ADJUSTS FOR DESIRED V_{IN} RANGE.

IF $\frac{R_{M2}}{R_{M1}+R_{M2}} = 0.9$ THEN $t_{ON} = N_{DIV} \bullet 1.125\mu s \bullet \frac{R_{SET}}{50k}$

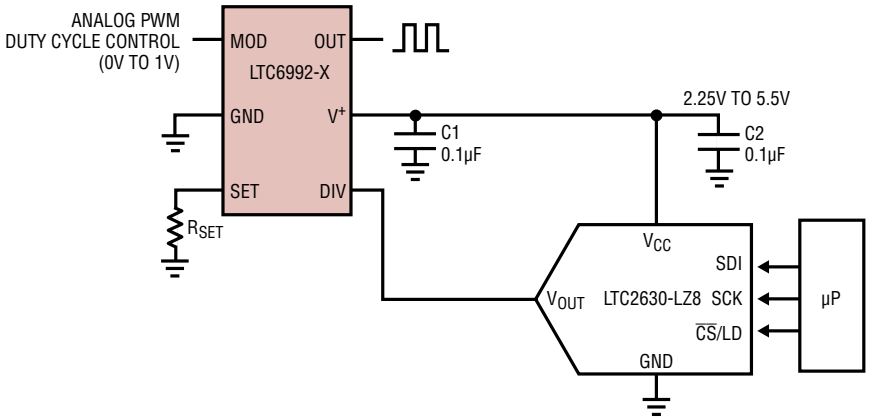
AS V_{IN} INCREASES, t_{OUT} INCREASES AND DUTY CYCLE DECREASES (BECAUSE POL = 1) TO MAINTAIN A CONSTANT t_{ON}. FOR CONSTANT OFF-TIME, JUST CHANGE DIVCODE SO POL = 0.

TYPICAL APPLICATIONS

Digitally Controlled Duty Cycle with Internal V_{REF} Reference Variation Eliminated



Programming N_{DIV} Using an 8-Bit DAC

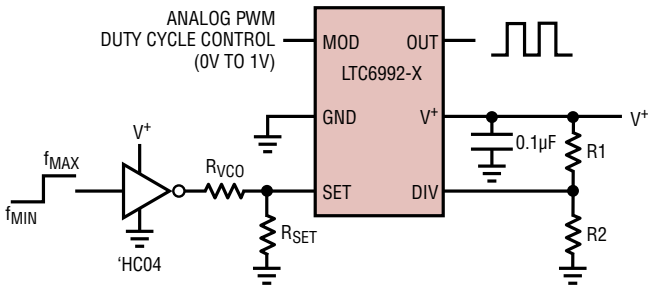


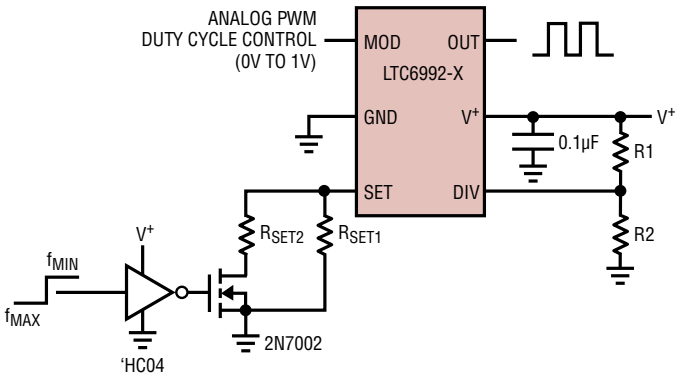
DIVCODE	DAC CODE
0	0
1	24
2	40
3	56
4	72
5	88
6	104
7	120
8	136
9	152
10	168
11	184
12	200
13	216
14	232
15	255

6992 TA04

TYPICAL APPLICATIONS

Changing Between Two Frequencies

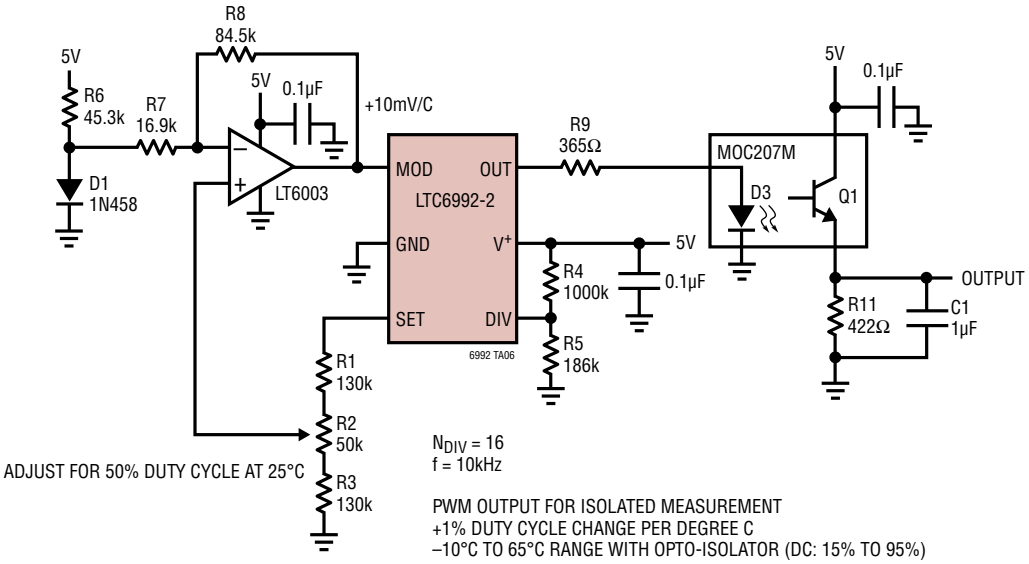




NOTES
WHILE THIS CIRCUIT IS SIMPLER THAN THE CIRCUIT TO THE RIGHT, ITS FREQUENCY ACCURACY IS WORSE DUE TO THE EFFECT OF V^+ SUPPLY VARIATION FROM SYSTEM TO SYSTEM AND OVER TEMPERATURE.

NOTES
1. WHEN THE NMOSFET IS OFF, THE FREQUENCY IS SET BY $R_{SET} = R_{SET1}$.
2. WHEN THE NMOSFET IS ON, THE FREQUENCY IS SET BY $R_{SET} = R_{SET1} \parallel R_{SET2}$.
3. V^+ SUPPLY VARIATION IS NOT A FACTOR AS THE SWITCHING RESISTOR IS EITHER FLOATING OR CONNECTED TO GROUND.

Simple Diode Temperature Sensor

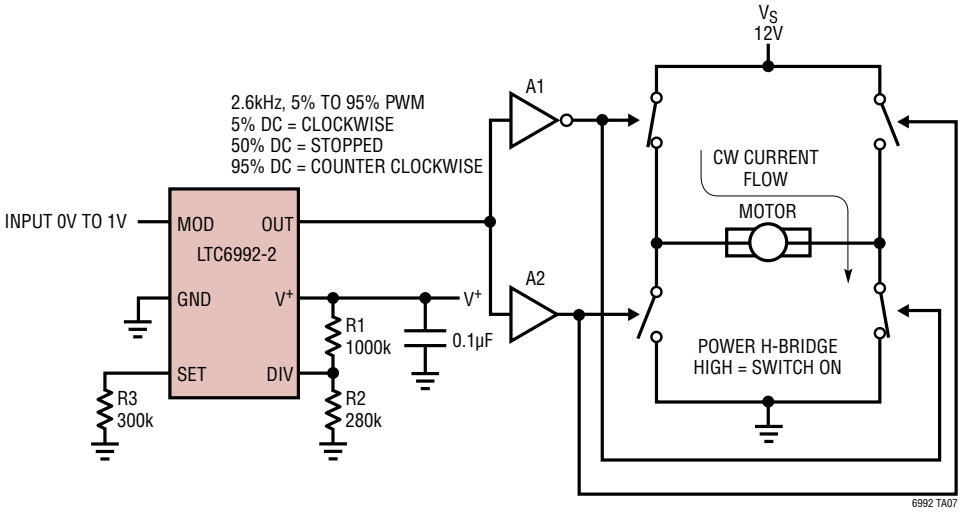


$N_{DIV} = 16$
f = 10kHz

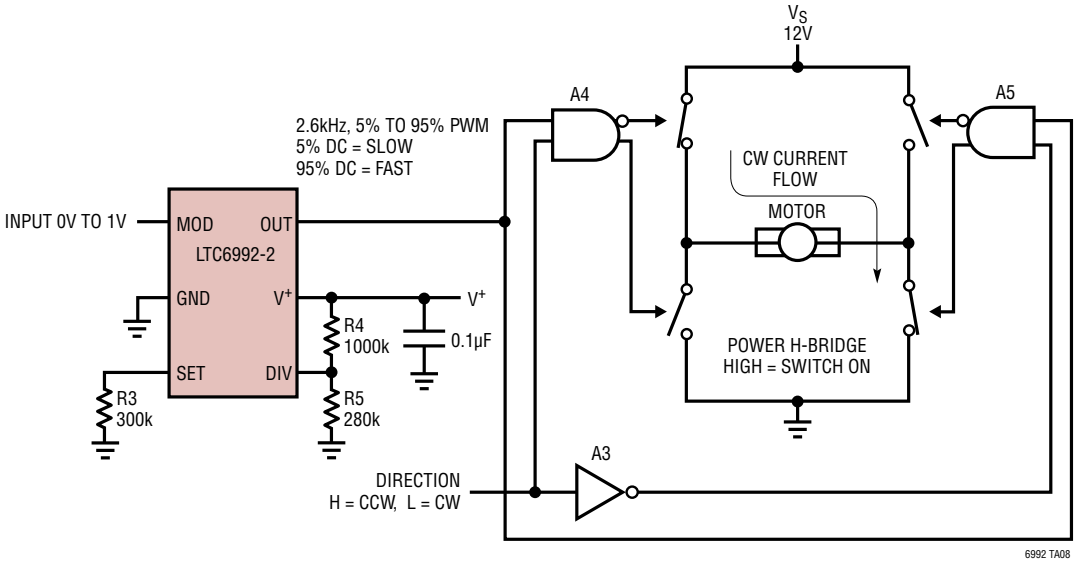
PWM OUTPUT FOR ISOLATED MEASUREMENT
+1% DUTY CYCLE CHANGE PER DEGREE C
–10°C TO 65°C RANGE WITH OPTO-ISOLATOR (DC: 15% TO 95%)

TYPICAL APPLICATIONS

Motor Speed/Direction Control for Full H-Bridge (Locked Anti-Phase Drive)

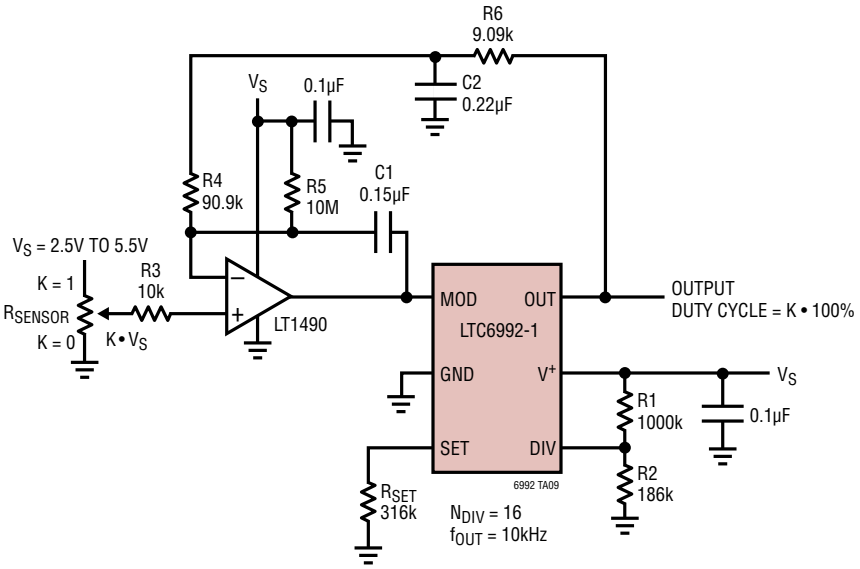


Motor Speed/Direction Control for Full H-Bridge (Sign/Magnitude Drive)

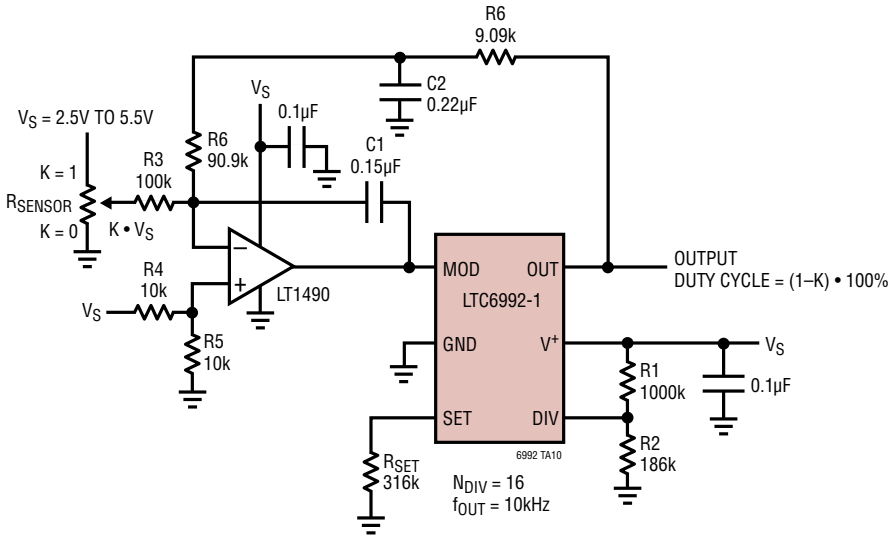


TYPICAL APPLICATIONS

Ratiometric Sensor to Pulse Width, Non-Inverting Response

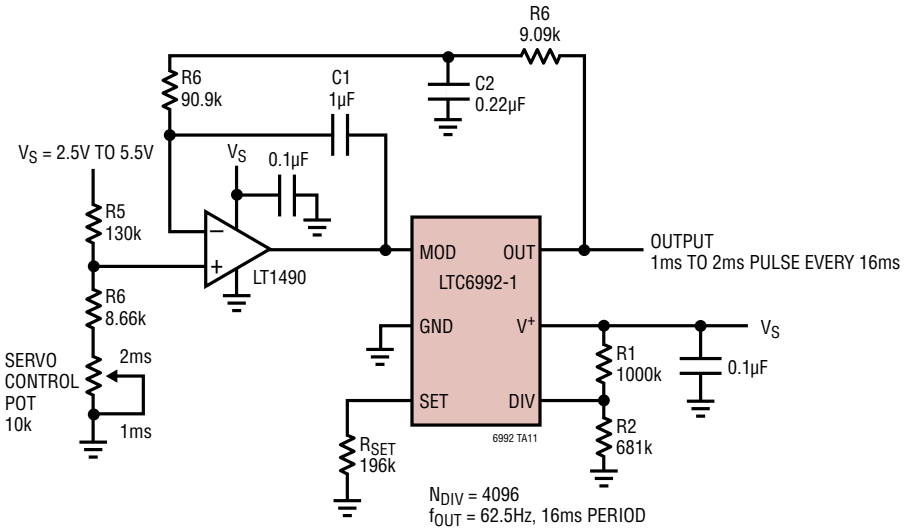


Ratiometric Sensor to Pulse Width, Inverting Response

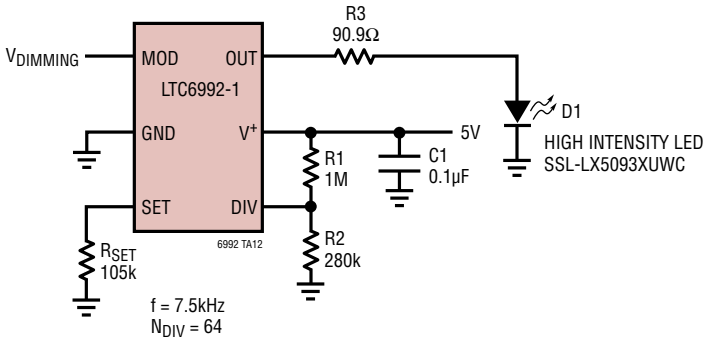


TYPICAL APPLICATIONS

Radio Control Servo Pulse Generator

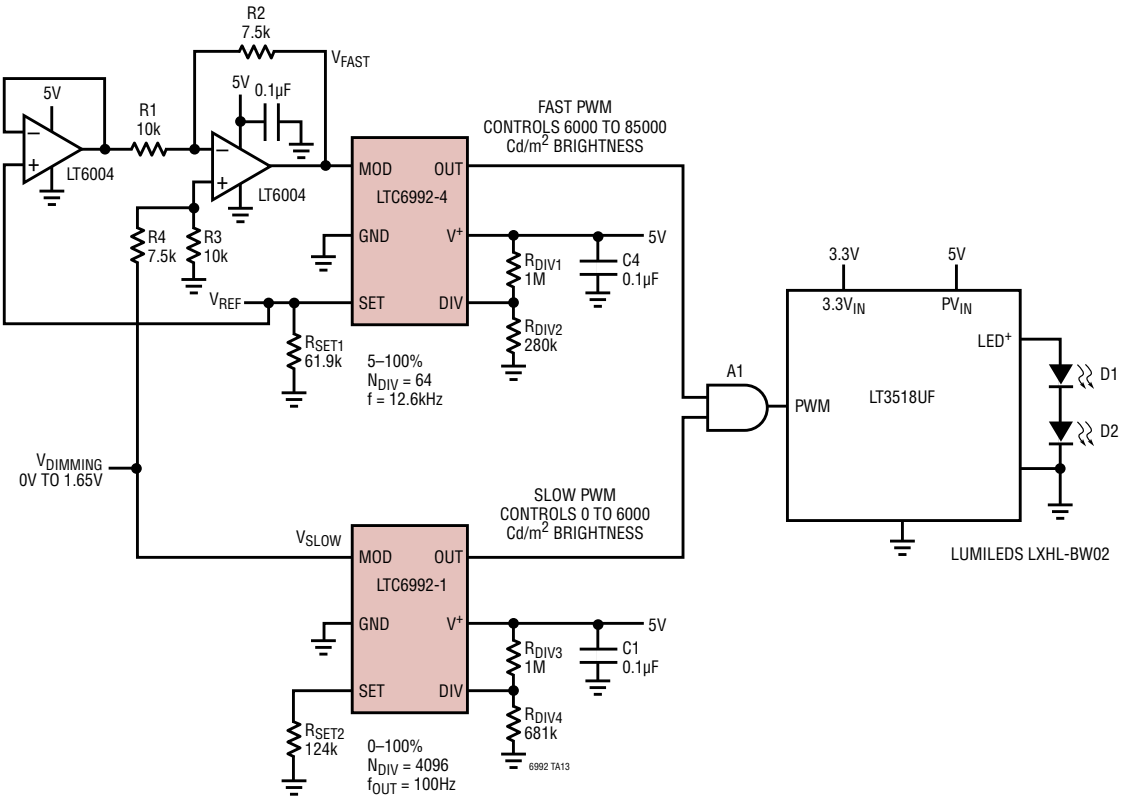


Direct Voltage Controlled PWM Dimming (0 to 15000 Cd/m^2 Intensity)

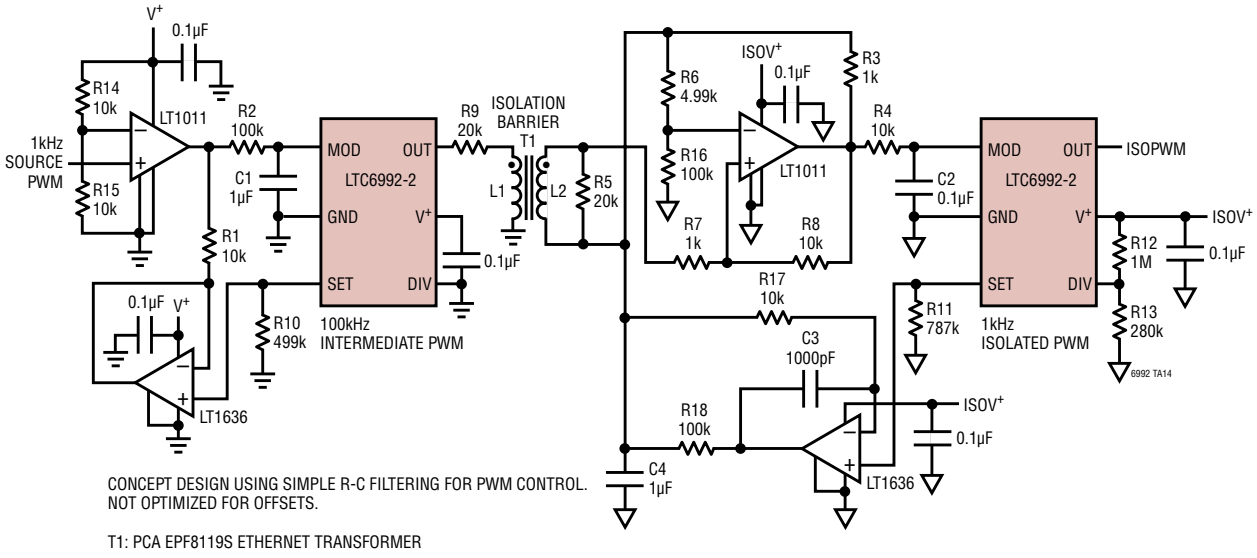


TYPICAL APPLICATIONS

Wide Range LED Dimming (0 to 85000 Cd/m^2 Brightness)



Isolated PWM (5% to 95%) Controller

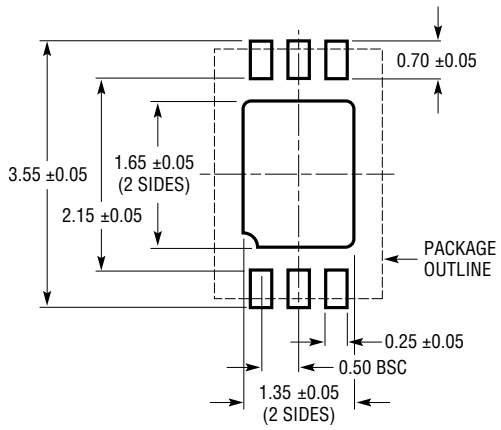


CONCEPT DESIGN USING SIMPLE R-C FILTERING FOR PWM CONTROL.
NOT OPTIMIZED FOR OFFSETS.

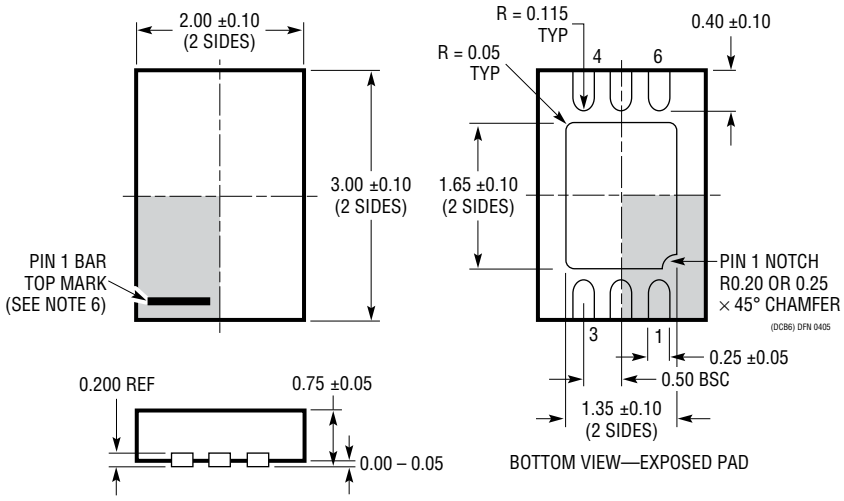
T1: PCA EPF8119S ETHERNET TRANSFORMER

PACKAGE DESCRIPTION

DCB Package
6-Lead Plastic DFN (2mm × 3mm)
(Reference LTC DWG # 05-08-1715 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

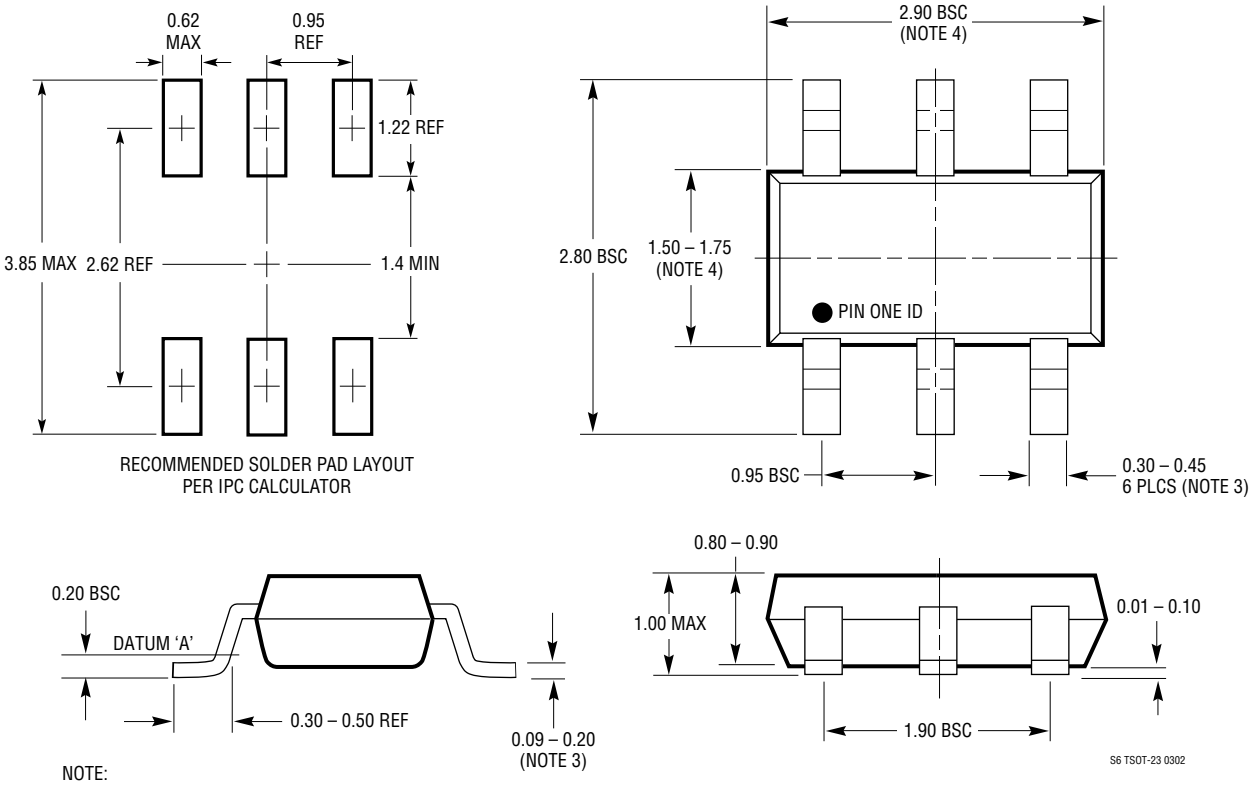


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (TBD)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



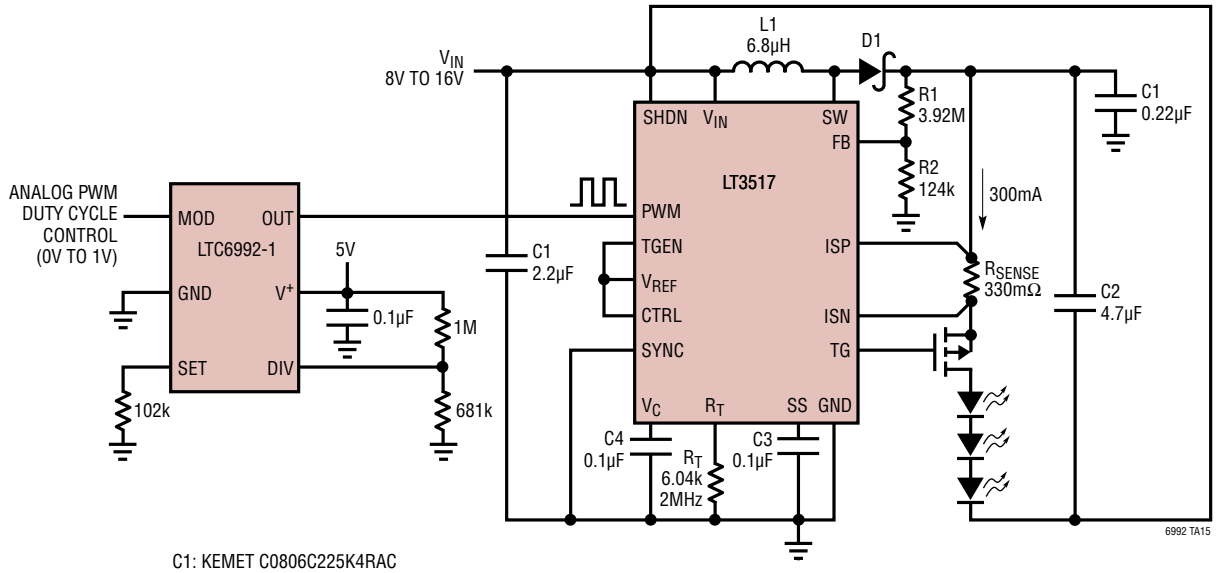
NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/11	Revised θ_{JA} value for TSOT package in the Pin Configuration.	2
		Added Note 7 for V_{OH} and V_{OL} in the Electrical Characteristics table.	4
		Minor edit to the Block Diagram.	12
		Minor edit to the equation in the “Duty Cycle Sensitivity to ΔV_{SET}” section.	19
		Revised Typical Application drawings.	25
B	07/11	Revised Description and Order Information sections	1 to 3
		Added additional information to $\Delta f_{OUT}/\Delta V^+$ and included Note 11 in Electrical Characteristics section	3, 4
		Added Typical Frequency Error vs Time curve to Typical Performance Characteristics section	11
		Added text to Basic Operation paragraph in Applications Information section	19
		Corrected f_{OUT} value in Typical Application drawing 6692 TA13	29
C	01/12	Added MP-Grade	1, 2, 3, 5
D	11/19	Added AEC-Q100 Qualified Note to Front Page	1
		Added W-Grade Order Information	3

TYPICAL APPLICATION

PWM Controller for LED Driver



C1: KEMET C0806C225K4RAC
C2: KEMET C1206C475K3RAC
C3, C4: MURATA GRM21BR71H104KA01B
C5: MURATA GRM21BR71H224KA01B
D1: DIODE DFLS160
L1: TOKO B992AS-6R8N
LEDS: LUXEON I (WHITE)
M1: ZETEX ZXMP6A13FTA

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1799	1MHz to 33MHz ThinSOT Silicon Oscillator	Wide Frequency Range
LTC6900	1MHz to 20MHz ThinSOT Silicon Oscillator	Low Power, Wide Frequency Range
LTC6906/LTC6907	10kHz to 1MHz or 40kHz ThinSOT Silicon Oscillator	Micropower, I_{SUPPLY} = 35µA at 400kHz
LTC6930	Fixed Frequency Oscillator, 32.768kHz to 8.192MHz	0.09% Accuracy, 110µs Start-Up Time, 105µA at 32kHz
LTC6990	TimerBlox, Voltage Controlled Oscillator	Frequency from 488Hz to 1MHz, No Caps, 2.2% Accurate
LTC6991	TimerBlox, Very Low Frequency Clock with Reset	Cycle Time from 2ms to 9.5 Hours, No Caps, 2.2% Accurate
LTC6993	TimerBlox, Monostable Pulse Generator	Resistor Set Pulse Width from 1µs to 34sec, No Caps, 3% Accurate
LTC6994	TimerBlox, Delay Block/Debouncer	Resistor Set Delay from 1µs to 34sec, No Caps Required, 3% Accurate

Vincotech

10-PC124PA040MR-L638F18Y

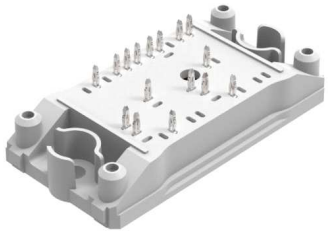
target datasheet

***fast* PACK 0 H** **1200 V / 40 mΩ**

Features

- H-bridge or 2x half-bridge
- SiC MOS
- fsw up to 250kHz
- Thermistor

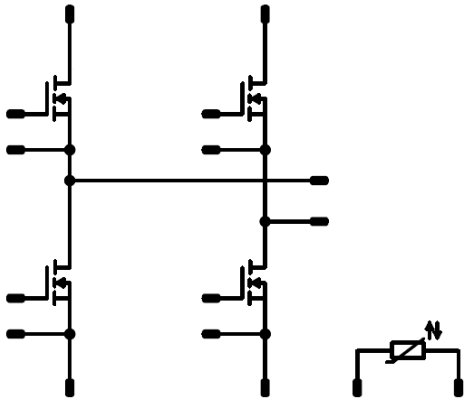
flow 0 12mm housing



Target applications

- Power Supply

Schematic



Types

- 10-PC124PA040MR-L638F18Y

Maximum Ratings

T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Condition	Value	Unit
Half-Bridge Switch				
Drain-source voltage	V_{DSS}		1200	V
Drain current	I_D	T_j = T_{jmax} T_s = 80 °C	32	A
Peak drain current	I_{DM}	t_p limited by T_{jmax}	137	A
Total power dissipation	P_{tot}	T_j = T_{jmax} T_s = 80 °C	73	W
Gate-source voltage	V_{GSS}		-4/22	V
Maximum Junction Temperature	T_{jmax}		175	°C

Maximum Ratings

T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Condition	Value	Unit
Module Properties				
Thermal Properties				
Storage temperature	T_{stg}		-40…+125	°C
Operation temperature under switching condition	T_{jop}		-40…(T_{jmax} - 25)	°C
Isolation Properties				
Isolation voltage	V_{isol}	DC Test Voltage t_p = 2 s	4000	V
Creepage distance			min. 12,7	mm
Clearance			9,61	mm
Comparative Tracking Index	CTI		> 200	

Characteristic Values

Parameter	Symbol	Conditions					Value			Unit
			V_{GE} [V] V_{GS} [V]	V_{CE} [V] V_{DS} [V]	I_C [A] I_D [A]	T_j [°C]	Min	Typ	Max	
Half-Bridge Switch										
Static										
Drain-source on-state resistance	$r_{DS(on)}$		18		20	25 125 150		39 52 60	50	mΩ
Gate-source threshold voltage	$V_{GS(th)}$	V_{GS} = V_{DS}			0,01	25	2,7		5,6	V
Gate to Source Leakage Current	I_{GSS}		22 -4	0		25			100 -100	nA
Zero Gate Voltage Drain Current	I_{DSS}		0	1200		25			10	µA
Internal gate resistance	r_g							7		Ω
Gate charge	Q_g							107		
Gate to source charge	Q_{GS}		18	600	20	25		22		nC
Gate to drain charge	Q_{GD}							41		
Short-circuit input capacitance	C_{iss}							1337		
Short-circuit output capacitance	C_{oss}	f= 1 MHz	0	800		25		76		pF
Reverse transfer capacitance	C_{rss}							27		
Reverse Diode Static										
Forward voltage	Vsd		0		20	25		3,20		V
Thermal										
Thermal resistance junction to sink	$R_{th(j-s)}$	phase-change material λ = 3,4 W/mK						1,31		K/W
Thermistor										
Rated resistance	R					25		22		kΩ
Deviation of R_{100}	$\Delta_{R/R}$	R_{100} = 1484 Ω				100	-5		5	%
Power dissipation	P					25		5		mW
Power dissipation constant						25		1,5		mW/K
B-value	$B_{(25/50)}$	Tol. ±1 %				25		3962		K
B-value	$B_{(25/100)}$	Tol. ±1 %				25		4000		K
Vincotech NTC Reference									I	

Vincotech

Ordering Code & Marking

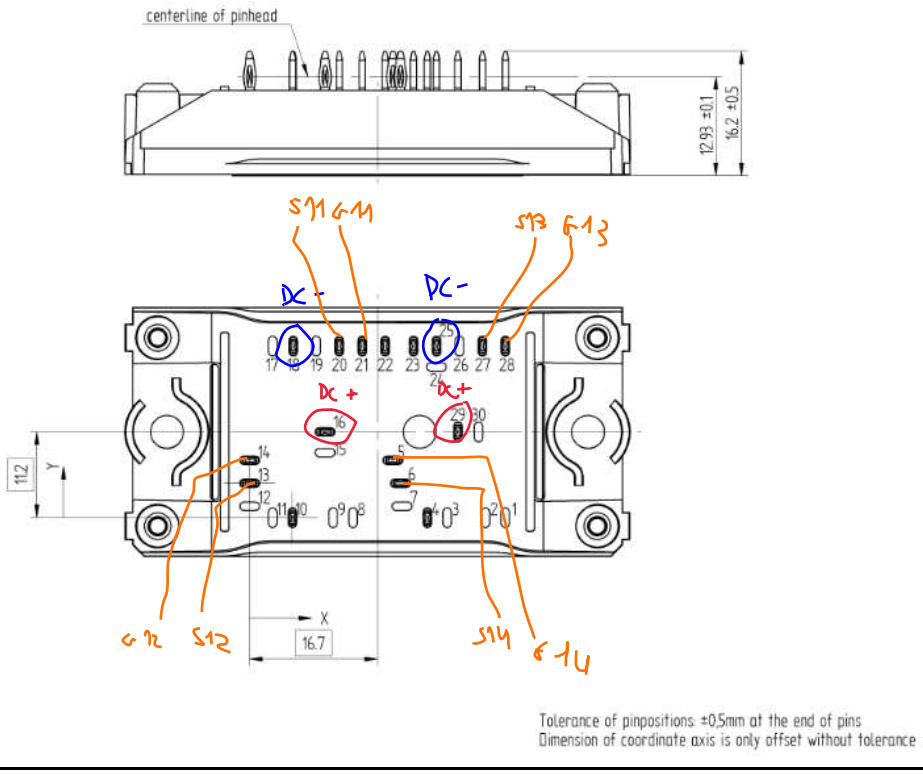
Version	Ordering Code
without thermal paste 12mm housing with Press-fit pins	10-PC124PA040MR-L638F18Y

NN-NNNNNNNNNNNNN
TTTTTTVV WWYY UL
VIN LLLLL SSSS

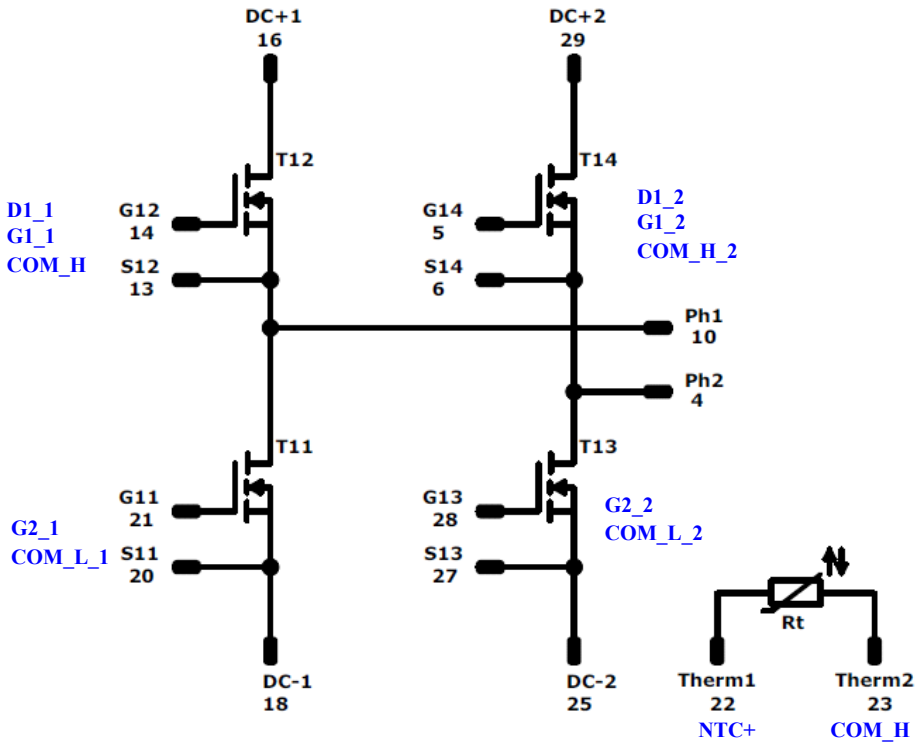
		Name		Date code	UL & VIN	Lot	Serial
Text		NN-NNNNNNNNNNNNN-TTTTTTVV		WWYY	UL VIN	LLLLL	SSSS
Datamatrix	Type&Ver		Lot number	Serial	Date code		
	TTTTTTTVV		LLLLL	SSSS	WWYY		

Outline

Pin table [mm]			
Pin	X	Y	Function
1	not assembled		
2	not assembled		
3	not assembled		
4	23,2	0	Ph2
5	18,7	7,5	G14
6	19,7	4,5	S14
7	not assembled		
8	not assembled		
9	not assembled		
10	5,6	0	Ph1
11	not assembled		
12	not assembled		
13	0	4,5	S12
14	0	7,5	G12
15	not assembled		
16	9,85	11,2	DC+1
17	not assembled		
18	5,7	22,4	DC-1
19	not assembled		
20	11,7	22,4	S11
21	14,7	22,4	G11
22	17,7	22,4	Therm1
23	21,4	22,4	Therm2
24	not assembled		
25	24,4	22,4	DC-2
26	not assembled		
27	30,4	22,4	S13
28	33,4	22,4	G13
29	27,2	11,2	DC+2
30	not assembled		



Pinout



Identification

ID	Component	Voltage	Current	Function	Comment
T11,T12,T13,T14	MOSFET	1200 V	40 mΩ	Half-Bridge Switch	
Rt	Thermistor			Thermistor	

Packaging instruction				
Standard packaging quantity (SPQ) **135**	>SPQ	Standard	<SPQ	Sample

Handling instruction
Handling instructions for *flow* 0 packages see vincotech.com website.

Package data
Package data for *flow* 0 packages see vincotech.com website.

UL recognition and file number
This device is certified according to UL 1557 standard, UL file number E192116. For more information see vincotech.com website.

Document No.:	Date:	Modification:	Pages
10-PC124PA040MR-L638F18Y-T1-14	10 Jun. 2016		

Product status definition		
Datasheet Status	**Product Status**	**Definition**
Target	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. The data contained is exclusively intended for technically trained staff.

MSC030SDA120B

Datasheet

Zero Recovery Silicon Carbide Schottky Diode

Final

January 2018

Microsemi

Power Matters.™

Contents

1 Revision History

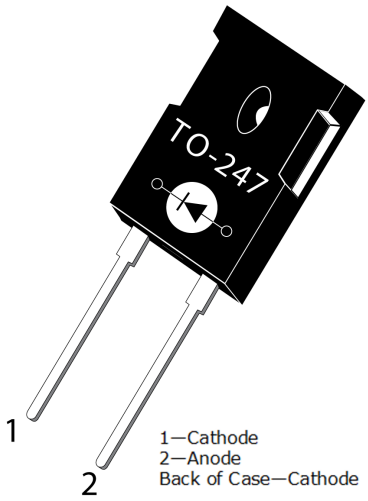
The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision A

Revision A was published in January 2018. It is the first publication of this document.

2 Product Overview

The silicon carbide (SiC) power Schottky barrier diodes (SBD) product line from Microsemi increases your performance over silicon diode solutions while lowering your total cost of ownership for high-voltage applications. The MSC030SDA120B is a 1200 V, 30 A SiC SBD in a two-lead TO-247 package shown below.



2.1 Features

The following are key features of the MSC030SDA120B device:

- Low forward voltage
- Low leakage current
- No reverse recovery current/no forward recovery
- Avalanche energy rated
- RoHS compliant

2.2 Benefits

The following are benefits of the MSC030SDA120B device:

- Higher-reliability systems
- Minimizes heat sink requirements
- Higher efficiency

2.3 Applications

The MSC030SDA120B device is designed for the following applications:

- H/EV powertrain and EV charger
- Power supply and distribution
- PV inverter, converter, and industrial motor drives
- Smart grid transmission and distribution
- Aviation

3 Electrical Specifications

This section details the electrical specifications for the MSC030SDA120B device.

3.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings for the MSC030SDA120B device.

All Ratings: T_C = 25 °C unless otherwise specified.

Table 1 • Absolute Maximum Ratings

Symbol	Parameter		Ratings	Unit
V_R	Maximum DC reverse voltage		1200	V
V_{RRM}	Maximum peak repetitive reverse voltage			
V_{RWM}	Maximum working peak reverse voltage			
I_F	Maximum DC forward current	T_C = 25 °C	65	A
		T_C = 135 °C	29	
		T_C = 145 °C	24	
I_{FRM}	Repetitive peak forward surge current (T_C = 25 °C, t_p = 8.3 ms, half sine wave)		92	
I_{FSM}	Non-repetitive forward surge current (T_C = 25°C, t_p = 8.3 ms, half sine wave)		165	
P_{TOT}	Power dissipation	T_C = 25 °C	259	W
		T_C = 110 °C	112	
T_J , T_{STG}	Operating junction and storage temperature range		–55 to 175	°C
T_L	Lead temperature for 10 seconds		300	
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, L = 0.22 mH, peak I_L = 30 A)		100	mJ

The following table shows the thermal and mechanical characteristics of the MSC030SDA120B device.

Table 2 • Thermal and Mechanical Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
$R_{\theta JC}$	Junction-to-case thermal resistance		0.4	0.58	°C/W
W_T	Package weight		0.22		oz
			5.9		g
Torque	Maximum mounting torque			10	lb-in
				1.1	N-m

3.2 Electrical Performance

The following table shows the static characteristics of the MSC030SDA120B device.

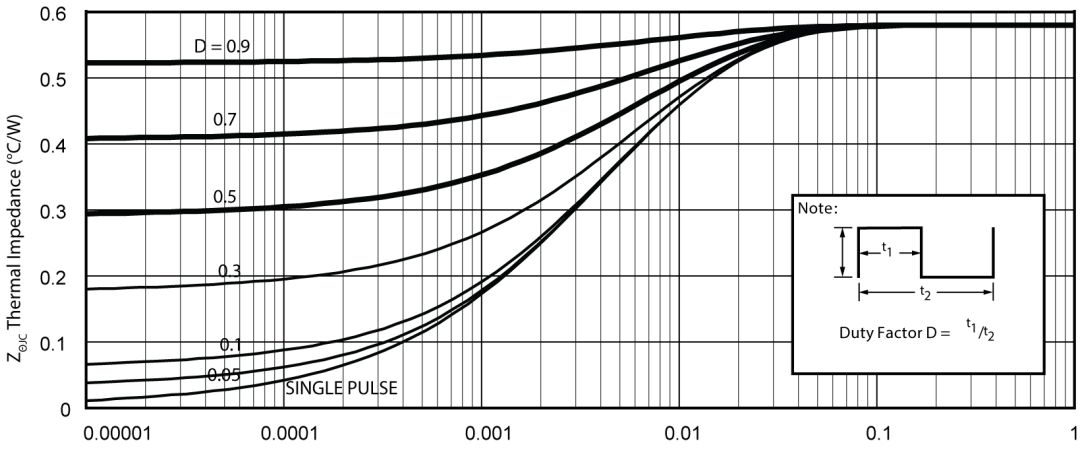
Table 3 • Static Characteristics

Symbol	Characteristic/Test Conditions		Min	Typ	Max	Unit
V_F	Forward Voltage	I_F = 30 A, T_J = 25 °C		1.5	1.8	V
		I_F = 30 A, T_J = 175 °C		2.1		
I_{RM}	Reverse leakage current	V_R = 1200 V, T_J = 25 °C		9	200	µA
		V_R = 1200 V, T_J = 175 °C		150		
Q_C	Total capacitive charge V_R = 600 V, T_J = 25 °C			130		nC
C_J	Junction capacitance V_R = 400 V, T_J = 25 °C, ƒ = 1 MHz			141		pF
	Junction capacitance V_R = 800 V, T_J = 25 °C, ƒ = 1 MHz			105		

3.3 Performance Curves

This section shows the typical performance curves for the MSC030SDA120B device.

Figure 1 • Maximum Transient Thermal Impedance



Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

Figure 2 • Forward Current vs. Forward Voltage

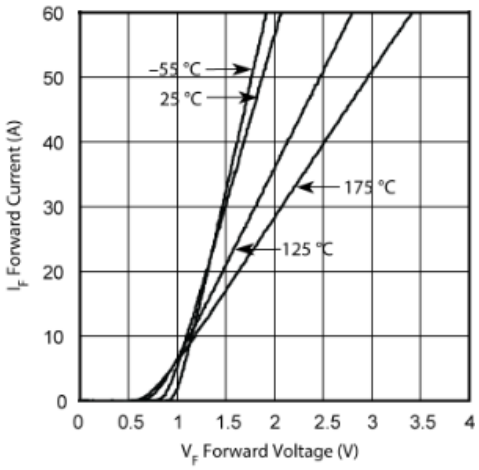


Figure 3 • Max Forward Current vs. Case Temp

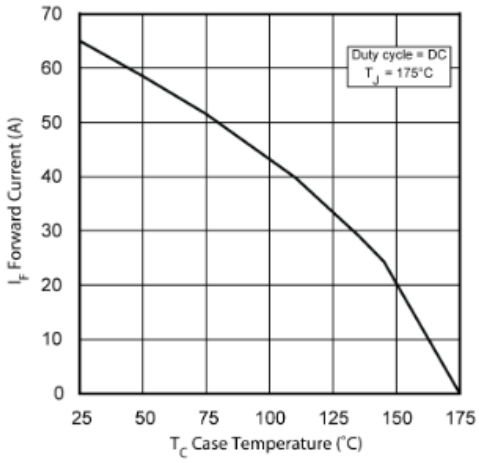


Figure 4 • Max Power Dissipation vs. Case Temp

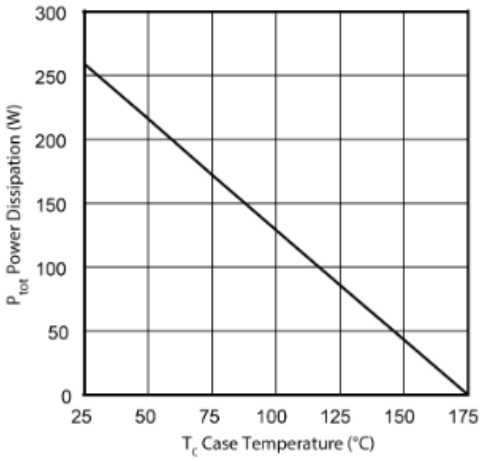


Figure 5 • Reverse Current vs. Reverse Voltage

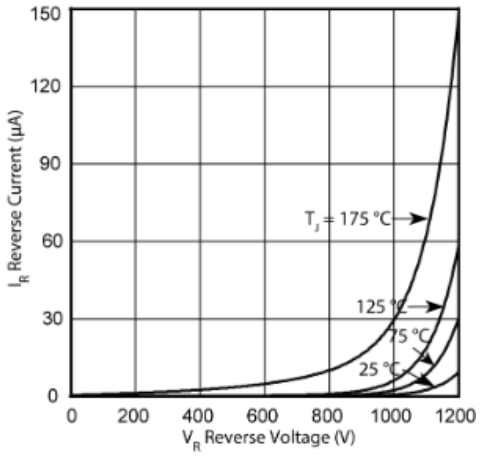


Figure 6 • Total Capacitive Charge vs. Reverse Voltage

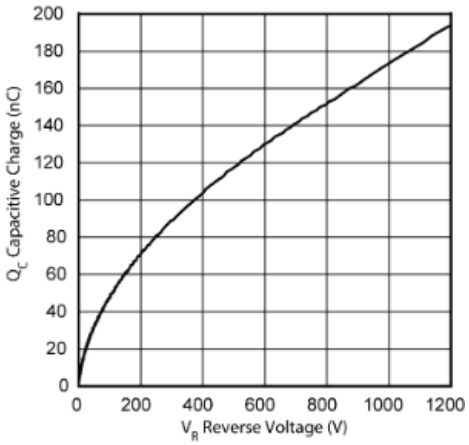
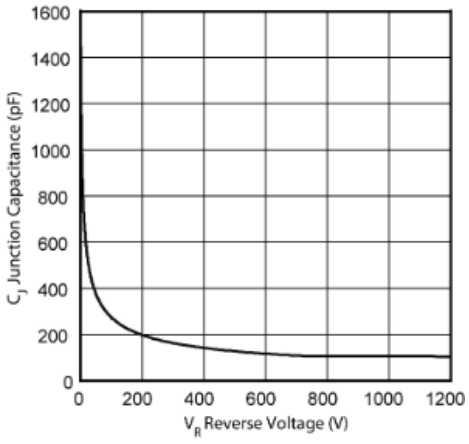


Figure 7 • Junction Capacitance vs. Reverse Voltage



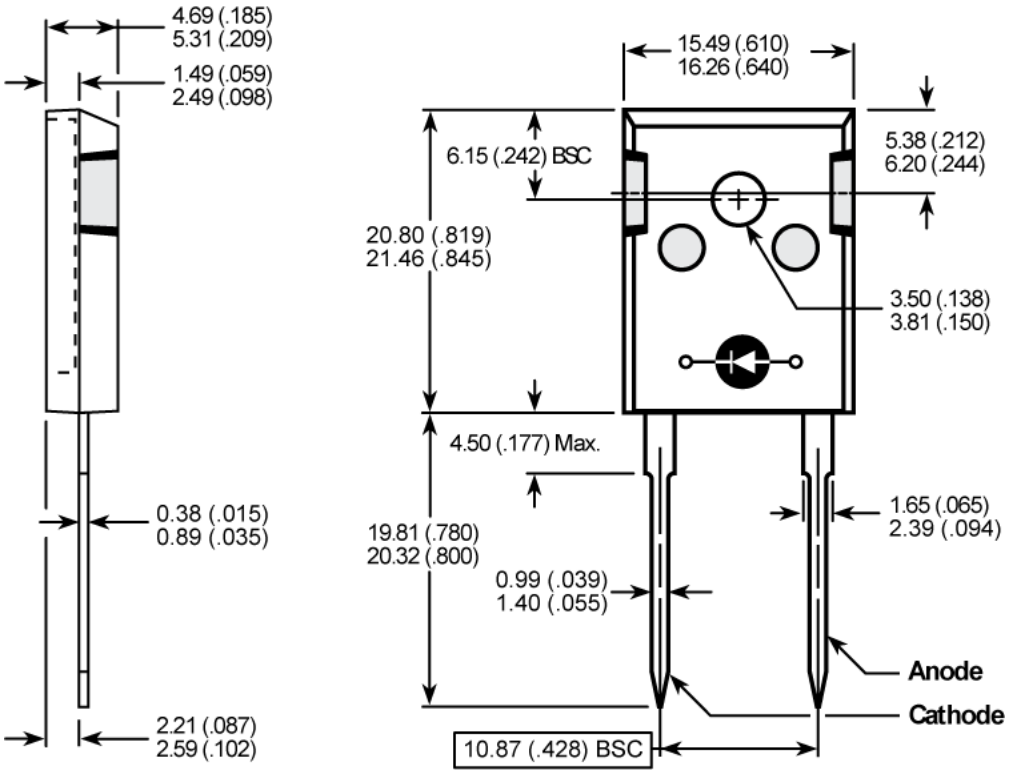
4 Package Specification

This section outlines the package specification for the MSC030SDA120B device.

4.1 Package Outline Drawing

This section details the TO-247 package drawing of the MSC030SDA120B device. Dimensions are in millimeters and (inches).

Figure 8 • Package Outline Drawing



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