Vendor Session 1: ATE and Test Quality

Track Chair: Stephan Eggersgluess, Siemens EDA, Germany
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SIEMENS

Improving Test Quality and Reliability via In-system/In-field Testing

Lee HARRISON (Siemens EDA – United Kingdom)

The quality and reliability of integrated circuits are under constant scrutiny as they are being widely deployed for safety-critical applications such as automotive or industrial applications such as datacenters. Manufacturing test (a.k.a. time t=0 testing) relies on various fault models to improve the quality of devices being shipped. To address stringent quality requirements, the industry is rapidly adopting advanced fault models targeting cell-internal defects, interconnect bridges and opens, and cell neighborhood defects, to either replace or augment the traditional fault models for improving overall test quality. In-system or in-field testing (often termed as t>0 testing) has been used for quite some time, but the need for better test quality has prompted development of newer test solutions that would allow re-using the existing infrastructure for manufacturing test and enable structural monitoring of the ICs in a periodic manner. In this talk, we will highlight some of the test solutions that are being widely adopted for in-system testing, discuss the challenges related to stringent memory and time requirements, and present potential DFT architectures that are being considered for preemptively detecting reliability related issues such as silent data corruption.

ADVANTEST

How ACS enables an Open Innovation Ecosystem for AI/ML applications in the Semiconductor Value Chain

Matthias SAUER, Sonny BANWARI (ADVANTEST – Germany)

Semiconductor test, like many industries, is experiencing a data revolution. With unprecedented demand for electronics of ever higher complexity and quality, achieving these goals requires ever increasing efforts. In today's semiconductor market, data-driven methodologies increasingly demand high-performance compute and machine learning solutions as well as data availability. However, due to compute resource or environmental limitations, these solutions are often hard to establish on an actual testing environment. As a solution, we will demonstrate the use of ACS Edge for real-time, secure workloads while benefiting from the execution environment flexibility offered by modern containerization technology in conjunction with an unmatched innovation ecosystem of AI/ML applications from the semiconductor industry's top analytics companies.

TERADYNE

The Need for New DFT Approaches to Scan

Thomas KOEHLER (TERADYNE, Germany)

In the semiconductor fabrication process, engineers continue to innovate, enabling smaller transistors and higher density circuits. As individual transistors become complex 3D structures, the intricacies of device failures and the exponential growth in transistor count continue to evolve for leading edge processes, creating quality challenges as new devices are manufactured. With more transistors to test and new failure modes due to the advanced technologies, the amount of total Test Data Volume continues to grow at an exponential pace. The existing standard approaches to DFT structural testing, such as scan, have encountered practical limitations, in part due to data bandwidth from limited GPIO rates and the limited or reducing number of pins available for scan. The industry is evaluating multiple options to overcome these limitations, which also offer new opportunities to semiconductor companies. This presentation will explore leveraging the ability to perform DFT test across the silicon lifecycles, from ATE, to System Level Test (SLT), and even through to the final in-field environment