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Effect of Current Distortion and Unbalanced Loads on Semiconductors Reliability

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ABSTRACT This article presents a reliability analysis of a 4-wire grid-tied inverter under different loading conditions, considering unbalanced loads and harmonic distortion in the current consumed. The proposed power converter is used as a case study to assess the impact of current disturbances on the semiconductors' reliability. The 4-wire inverter analyzed is implemented with a 3-leg SiC MOSFET power module and a neutral wire connected to the midpoint of the DC-link. The analysis is founded on the literature's reliability curves for power switches. As key take-home findings, the addition of harmonic content in the load current plays a dominant role in the semiconductors' expected lifetime, especially for the low-frequency harmonics, e.g., third harmonic. Furthermore, the phase delay of the harmonic current content is revealed as a critical factor in the semiconductor's reliability. Additionally, the existence of unbalanced loads substantially modifies the reliability of the semiconductors of the inverter. The results confirm that converters' reliability is highly dependent on the loading conditions and harmonic content, so identifying the most critical conditions is inevitable.

INDEX TERMS Reliability, silicon carbide, MOSFETs, harmonic distortion, current imbalances.

I. INTRODUCTION

The reliability of grid-tied converters has been extensively studied in the past years. Multiple analyses can be found in the literature. However, such analyses have often been performed only for ideal operating conditions without regard to possible disturbances to these systems.

For example, the presence of low-frequency harmonic distortion in the grid voltage may lead the converters connected to it to operate with a distorted current. The presence of harmonics can change the shape of the current and, thus, the inverter's thermal load, which, if not taken into account, can affect the expected lifetime of the equipment [1].

This paper analyzes the effect on the semiconductors' reliability of unbalanced and harmonic distorted currents for a 4-wire inverter. The obtained results can be extrapolated to any kind of equipment that operates under these conditions such as, 4-wire inverters for isolated microgrids [2], three-phase power factor correction (PFC) rectifiers [3], uninterruptable power supplies (UPS) [4], active filters [5], or inverters for drives and EV traction systems [6].

The increasing use of microgrids and isolated grids leads to systems that inherently operate under these conditions [7]–[9]. In a microgrid, the presence of nonlinear loads, i.e., with high current THD, and single-phase type, can be high. Consequently, converters operating as power sources for these microgrids, [10]–[12], need to work reliably with these types of loads, and their estimated operating lifetime must consider them. The same considerations apply to UPS systems as portrayed in [4].

Typically, PFC rectifiers consume unbalanced currents when connected to unbalanced grids [13]. As pointed out in [14], this is also a common situation for AC/DC grid-tied inverters with a *dq0*-based control.

Finally, active filters are typically used to balance the current consumed from the grid and, at the same time, eliminate the current harmonic content [15]–[18]. Consequently, its current usually is unbalanced between phases and presents a high harmonic distortion.

As it has been exposed, these operating conditions are not uncommon and shall be considered. However, the effect of these disturbances has generally been overlooked in the literature, and few examples are reported. In [19], the authors analyze the impact of reactive power injection on PV inverters' reliability. In [20], the effect of grid voltage unbalances on the reliability of adjustable speed drives is studied. However, only the capacitors' reliability is analyzed.

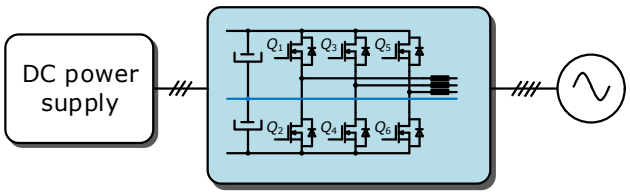

FIGURE 1. Platform simplified diagram.

In [21] and [22], the authors analyze the reliability of single-phase transformerless PV inverters. In [23], the authors propose an optimized design method for transformerless PV inverters considering its reliability. In all the cases, the analyses are performed considering a null THD. Therefore, the possibility of operating with a current with harmonic content is not considered.

Reducing the harmonic content and current unbalances in motor control algorithms is a hot topic in the literature [24]–[28]. However, most of the solutions proposed are complex. Usually, the inverters used for motor control applications do not include these features. Therefore, it is interesting to analyze the effect of the disturbances on reliability. In [29], the semiconductor reliability for a three-phase inverter used in a wind turbine is analyzed. By the nature of the study, the presence of unbalanced loads is unlikely. However, the presence of low-frequency harmonics in the current cannot be ruled out. Due to AC machines' manufacturing limitations, the back electromotive force (EMF) is not purely sinusoidal and has harmonic content [30]. Consequently, it is likely to have a harmonic distortion in the currents [31]. Its effect may be relevant for the semiconductors' reliability, and it has not been considered. Finally, [32] presents a three-phase inverter reliability analysis for more electric aircraft. An airplane can be regarded as a microgrid. Therefore, as mentioned previously, it can have single-phase and nonlinear loads, which increase the current imbalances in the inverter and the harmonic current content. Again, the effect that such disturbances may have on semiconductors' reliability has not been considered.

In [33], the authors analyze an active filter's IGBTs' reliability. However, it does not consider the phase delay of the harmonics compensated. As proved in our paper, this is a critical point in the semiconductors' reliability.

It is critical to analyze the effect of imbalances and harmonic current distortion on semiconductors' reliability for all the reasons mentioned above. This paper proposes a comparative methodology to establish the impact on the semiconductors' reliability of current imbalances and harmonic content. In [34], the authors present a similar analysis to assess the effect of different modulation strategies on semiconductors' reliability. The authors use a power converter as a case study and, with the help of established lifetime models, assess the variation in reliability with different modulation strategies.

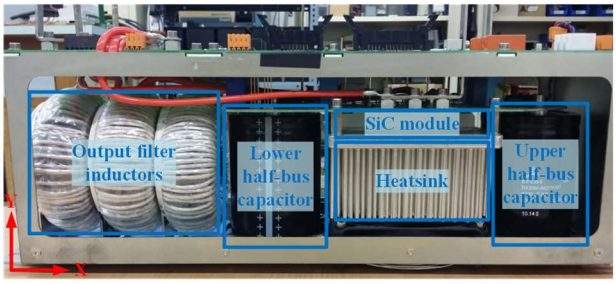

FIGURE 2. The proposed platform. The lateral of the platform is opened to show the internal elements.

Both disturbances are analyzed separately, considering different cases. The reliability values for each case are compared against a base case. The results show that unbalanced loads reduce the semiconductors' reliability if some phases are overloaded. Furthermore, the harmonic content is proved to be a stress factor that can substantially reduce the semiconductors' reliability. Additionally, the phase delay of the harmonic is confirmed to play an extremely relevant role in the semiconductors' reliability.

The paper is organized as follows. First, a brief description of the 4-wire inverter is done. Next, the different operation cases analyzed in the paper are presented. The reliability models used for the comparative analysis are presented, and the results are discussed. Next, the cases with harmonic content are analyzed in-depth to understand their differences. Finally, conclusions are drawn.

II. HARDWARE DESCRIPTION

Fig. 1 shows a simplified diagram of the 4-wire inverter analyzed. The inverter is supplied by an adjustable DC voltage source providing between 680 V and 800 V. The inverter itself consists of a three-branch module of SiC MOSFETs (Wolfspeed CCS050M12CM2 [35]). The DC-link is split into two half-buses. Like this, the midpoint can be accessed to connect the neutral line and easily implement a 4-wire system. The DC-link consists of two capacitors (EPCOS B43564A6278M000 [36]). The capacitors' reliability is not under this paper's scope and is analyzed separately in another paper [37].

The outputs of the semiconductors are connected to an output filter implemented with three inductors. Each phase's current is independently controlled using Fractional Proportional Resonant (FPR) controllers [38].

Fig. 2 shows the inverter with open sides to see the internal elements. On the left, the three inductors of the output filter can be seen. Next to them is the lower half-bus capacitor. The SiC power module is mounted on a heatsink with forced convection. The fan is mounted under the heatsink and includes an air inlet. Finally, on the right-hand side is mounted the upper half-bus capacitor. For the current application, the converter is mounted rotated 90 degrees on the X-axis shown in Fig. 2. The converter is completely closed on the sides for the platform analyzed, and only an air outlet is left on the left-hand side to let out the hot air. Table I summarizes the main parameters of the power converter.

TABLE I
INVERTER PARAMETERS.

Parameter	Value
Phase nominal apparent power: S_{ph} (kVA)	6.0
Phase nominal current: I_{ph} (A_{RMS})	26.0
Output current maximum THD (%)	30
DC-link capacitance (μF)	2700
DC-link nominal voltage (V)	800
Grid frequency (Hz)	50
Grid line voltage (V_{RMS})	400

The converter is mounted on a large cabinet with other elements, such as the DC power supply, a low-frequency isolation transformer for the DC power supply, and the necessary switchgear to connect the inverter to the AC grid and the control boards. Because of its size and multiple elements, the cabinet can be modeled as an environment with a constant temperature since its thermal inertia is substantial. For this paper, the cabinet temperature is assumed to be a constant value of 25 °C.

III. WORKING CASES

The effect of current imbalances and harmonic distortion is analyzed separately. The obtained results are compared with a base case to get a good picture of the reliability variation.

The base case selected is the operation of the power converter with a three-phase balanced load and each phase with the nominal active power. Therefore, the active power (P_{base}) is 18 kW.

Three different cases are analyzed to assess the reliability variation with unbalanced loads. One of the phases is operated with 0 current in all of them. The other two phases are operated with the following current and total output power

a) I_{ph} and $0.66P_{base}$
b) $1.05I_{ph}$ and $0.7P_{base}$
c) $1.20I_{ph}$ and $0.8P_{base}$

For cases b and c, the converter is operated with a slight current overload in two phases.

Last, four different cases are analyzed to assess the reliability variation with loads with harmonic distortion. The three phases are operated with the nominal balanced current at the fundamental frequency (f). A 30% content of the third harmonic is added in each phase.

a) I_{ph} at f and $0.3I_{ph}$ at $3f$ with phase delay 0 rad.
b) I_{ph} at f and $0.3I_{ph}$ at $3f$ with phase delay π/2 rad.
c) I_{ph} at f and $0.3I_{ph}$ at $3f$ with phase delay π rad.
d) I_{ph} at f and $0.3I_{ph}$ at $3f$ with phase delay 3π/2 rad.

The harmonic distortion added is limited to the third harmonic. As analyzed in [1], the low-frequency harmonics have a higher impact on the semiconductors' thermal load and, consequently, a higher impact on the reliability [39].

The currents and power for all the cases are summarized in Table II.

All the cases analyzed are not realistic operation profiles for a power converter. Nevertheless, they are helpful in the analysis of the reliability variation.

IV. RELIABILITY MODELS

A. SIMULATION MODEL

Simulations are performed with a power electronics simulation software to determine T_{jm} and ΔT_j for each scenario. The power electronics simulation software integrates into one simulation, the electrical simulation, including the control implemented in discrete-time and the thermal simulation.

The models provided by the manufacturer on their website [40] are used to implement the thermal simulation. The models include look-up tables to determine both switching and conduction losses. The turn-on and turn-off energies are provided at different currents, voltages, and temperatures. The gate resistance is taken into account for calculating the switching losses as well. The voltage drop on the MOSFET is

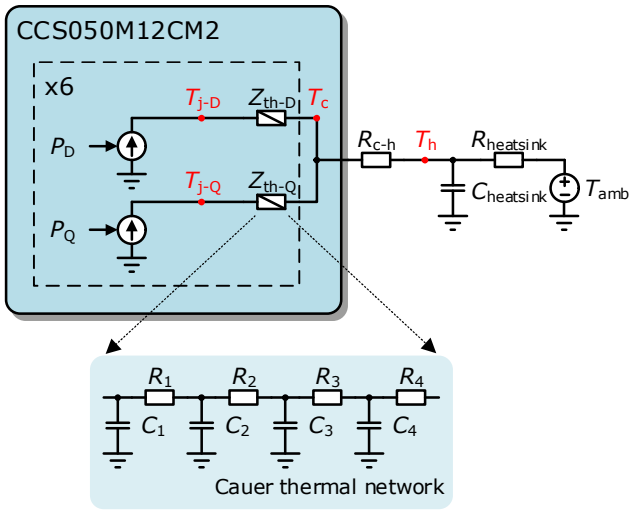

FIGURE 3. Semiconductors thermal network.

TABLE II
ELECTRICAL PARAMETERS OF THE DIFFERENT CASES.

Case	$I_{a\text{-}50Hz}$ (A_{RMS})	I_a (A_{RMS})	P_a (kW)	$I_{b\text{-}50Hz}$ (A_{RMS})	I_b (A_{RMS})	P_b (kW)	$I_{c\text{-}50Hz}$ (A_{RMS})	I_c (A_{RMS})	P_c (kW)	3rd harmonic content (%)	3rd harmonic phase delay (rad)
1	26.0	26.0	6.0	26.0	26.0	6.0	26.0	26.0	6.0	0	--
2a	26.0	26.0	6.0	26.0	26.0	6.0	0	0	0	0	--
2b	27.3	27.3	6.3	27.3	27.3	6.3	0	0	0	0	--
2c	31.2	31.2	7.2	31.2	31.2	7.2	0	0	0	0	--
3a	26.0	27.1	6.0	26.0	27.1	6.0	26.0	27.1	6.0	30	0
3b	26.0	27.1	6.0	26.0	27.1	6.0	26.0	27.1	6.0	30	π/2
3c	26.0	27.1	6.0	26.0	27.1	6.0	26.0	27.1	6.0	30	π
3d	26.0	27.1	6.0	26.0	27.1	6.0	26.0	27.1	6.0	30	3π/2

TABLE III
SIMULATION RESULTS

		Q1 & Q2				Q3 & Q4				Q5 & Q6			
Case	T_h (°C)	T_{jm} (°C)	ΔT_j (°C)	I_B (A)	N_f (cycles)	T_{jm} (°C)	ΔT_j (°C)	I_B (A)	N_f (cycles)	T_{jm} (°C)	ΔT_j (°C)	I_B (A)	N_f (cycles)
1	45.56	61.93	7.47	17.34	$2.42{\cdot}10^{10}$	61.93	7.47	17.34	$2.42{\cdot}10^{10}$	61.93	7.47	17.34	$2.42{\cdot}10^{10}$
2a	40.49	55.81	7.44	17.34	$2.66{\cdot}10^{10}$	55.81	7.44	17.34	$2.66{\cdot}10^{10}$	46.98	0.49	1.92	$2.44{\cdot}10^{16}$
2b	41.12	57.09	7.82	18.20	$2.03{\cdot}10^{10}$	57.09	7.82	18.20	$2.03{\cdot}10^{10}$	47.73	0.49	1.92	$2.42{\cdot}10^{16}$
2c	46.88	61.48	9.14	20.67	$0.84{\cdot}10^{10}$	61.48	9.14	20.67	$0.84{\cdot}10^{10}$	50.27	0.49	1.92	$2.33{\cdot}10^{16}$
3a	45.41	61.69	8.43	18.25	$1.38{\cdot}10^{10}$	61.69	8.43	18.25	$1.38{\cdot}10^{10}$	61.69	8.43	18.25	$1.38{\cdot}10^{10}$
3b	46.58	63.75	7.58	18.08	$2.17{\cdot}10^{10}$	63.75	7.58	18.08	$2.17{\cdot}10^{10}$	63.75	7.58	18.08	$2.17{\cdot}10^{10}$
3c	46.92	64.25	7.42	17.74	$2.39{\cdot}10^{10}$	64.25	7.42	17.74	$2.39{\cdot}10^{10}$	64.25	7.42	17.74	$2.39{\cdot}10^{10}$
3d	46.59	63.75	8.48	18.00	$1.32{\cdot}10^{10}$	63.75	8.48	18.00	$1.32{\cdot}10^{10}$	63.75	8.48	18.00	$1.32{\cdot}10^{10}$

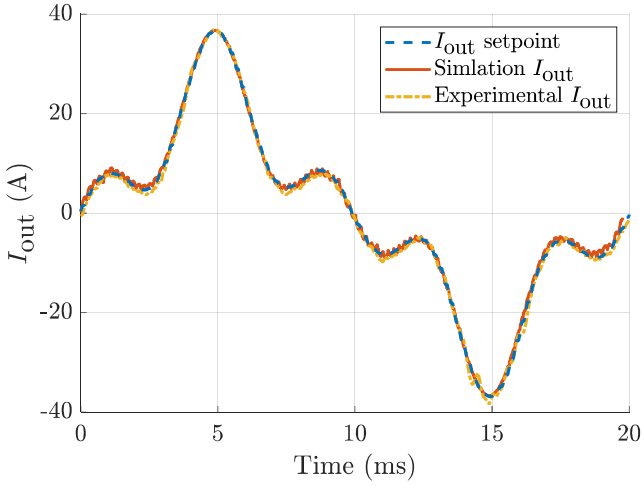

FIGURE 4. Current waveforms comparison between the experimental and the simulation results.

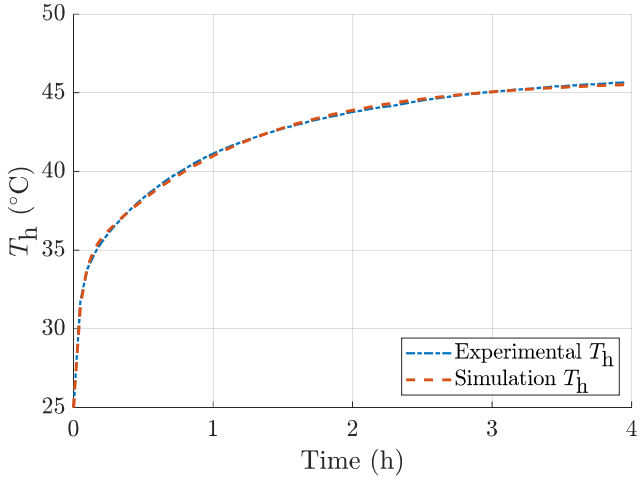

FIGURE 5. Experimental setup results. Heatsink temperature measurement operating in case 1 conditions. Refer to Table II for cases reference.

also provided for different currents and temperatures to calculate the conduction losses.

Additionally, the model includes a thermal network of the module. The radiator with forced convection [41] used has been simplified as a thermal resistance, $R_{heatsink}$, 0.103 K·W^{-1}, and a thermal capacitance, $C_{heatsink}$, 1.67 kJ·K^{-1}. Fig. 3 shows the resulting thermal network. As stated previously, for all the cases analyzed, the ambient temperature (T_{amb}) was set at 25 °C.

The software calculates the losses by interpolating from the temperature, current, and operating voltage.

Fig. 4 shows the response of the power converter for an output current (I_{out}) setpoint of 15.6 A_{RMS} at 50 Hz, 5.2 A_{RMS} at 150 Hz, and 5.2 A_{RMS} at 250 Hz, marked in blue. In orange is shown the output current calculated with the simulations, and in yellow is shown the output current measured in the experimental setup. The output current is sampled at the converter's switching frequency, f_{sw}, 30 kHz. For the sake of clarity, only one phase is measured.

The inverter analyzed is a piece of commercial equipment designed bearing in mind its compactness. Consequently, the gate drivers are placed on top of the power module, making it impossible to access the semiconductors to measure their temperature directly. Therefore, it is not possible to validate the simulation results with experimental measurements. Nevertheless, as pointed out before, the goal is to compare different cases without obtaining exact reliability values. Consequently, the simulation results are sufficient for the current analysis.

The simulation results are summarized in Table III. For each case is provided the heatsink temperature (T_h), the average junction temperature (T_{jm}), the junction temperature swing (ΔT_j), and the bond wire current (I_B) of each MOSFET and their estimated number of cycles to failure (N_f). The MOSFET's labeling is depicted in Fig. 1.

For the unbalanced load cases (2a-2c), the load current on phase c is null. Despite this, the MOSFETs switch, and their currents are not null due to the current ripple at the high-frequency switching.

Fig. 5 shows, in blue, the experimental setup heatsink temperature (T_h) measured with a K-type thermocouple sampled every 5 minutes with a thermocouple data logger. With the power converter operating in case 1 conditions. And, in orange, the heatsink temperature calculated with the simulations. The simulation results match the dynamic response of the experimental setup closely. Moreover, the steady-state experimental heatsink temperature, 45,78 °C, matches the temperature simulation results closely, Table III.

B. LIFETIME MODEL

For the inverter analyzed, a power module based on SiC MOSFETs is used. From the analyses performed by different authors, [42]–[47], it is clear that the number of cycles to

failure, N_f, is closely related to the average junction temperature, T_{jm}, and the junction temperature swing, ΔT_j.

Considering this, we propose calculating the N_f value with the CIPS2008 model [48]. The CIPS2008 model is based on the model obtained from the LESIT project [49]. The CIPS2008 model calculates N_f based on the average semiconductor temperature (T_{jm}) and the temperature swing in a period (ΔT_j). Additionally, it considers other parameters such as the power-on-time (t_{on}), the current for each bond wire (I_B), the voltage class of the chip (V_C), and the diameter of the bond wires (D_B). The different parameters' effect is adjusted with experimental constants (A and β_1–β_6). The calculation of the number of cycles to failure is expressed as

$$N_f = A \cdot \Delta T_j^{\beta_1} \cdot e^{\frac{\beta_2}{T_{jm}+273.15}} \cdot t_{on}^{\beta_3} \cdot I_B^{\beta_4} \cdot V_C^{\beta_5} \cdot D_B^{\beta_6}. \quad (1)$$

The authors of the CIPS2008 model developed it as a lifetime model for power modules. Therefore, N_f is calculated considering the typical failure mechanisms for power modules, such as bond wire liftoff and thermal fatigue of solder joints, [49], which are still present in a SiC MOSFET power module. Consequently, it is suitable for our analysis.

The constants of a lifetime model (A and β_1–β_6) shall be adjusted for every power module. When it comes to a comparative analysis, identifying the model parameters is not crucial. The constants contain the semiconductors' technologic factor, which is irrelevant to performing comparisons among different cases. This paper's scope is to get a series of comparable results to assess the importance of current disturbances in semiconductors' reliability. The interest is not in the exact N_f value for each case, but N_f's variations depending on the case analyzed. The same approach is followed in other comparative reliability analyses [33], [34].

The parameters used in (1) are summarized in Table IV and were extracted from [50], or they can be obtained from the manufacturer's datasheet [35].

TABLE IV
PARAMETERS OF THE CIPS2008 LIFETIME MODEL.

Parameter	Value
A (cycles)	$2.03 \cdot 10^{14}$
β_1	-4.416
β_2	1285
β_3	-0.463
β_4	-0.716
β_5	-0.761
β_6	-0.5
t_{on} (s)	10^{-2}
V_C	12
D_B (µm)	380

The diameter of the bond wires was obtained by performing direct microscopic measurements on a module. The number of bond wires in parallel is three. For the case under study, t_{on} is 10 ms. It corresponds to half period of the grid. The t_{on}, V_C, and D_B parameters are constant for the four cases analyzed. I_B is dependant on the case and phase analyzed. The MOSFET RMS current for each case is determined with the help of simulations.

The semiconductors module includes a freewheeling SiC Schottky diode [51] in parallel with the MOSFETs' body diode. This diode is usually no longer included because the body diode provides a good enough switching performance.

Additionally, the MOSFETs can drive current in both directions. In the studied module, when the current flows from source to drain, it is shared between the MOSFET, the body diode, and the external freewheeling diode. Therefore, the current flowing through the freewheeling diode is low, and consequently, its thermal load is low [1]. Notably, the temperature swing, ΔT_j, is low. From (1), it can be deduced that a low ΔT_j leads to an unrealistic N_f estimation,

$$\lim_{\Delta T_j \to 0} N_f = \infty, \quad (2)$$

for this reason, these diodes are excluded from the study.

It is worth noting that, according to (1), we expect a decrease in the number of cycles to failure with T_{jm}, which increases with T_{amb}. However, in this paper, the ambient temperature was held constant.

V. DISCUSSION

A reliability block diagram (RBD) has been chosen to model the system-level reliability. This approach is the most appropriate since the system does not have redundancies [52]. Failure of a single semiconductor would cause a system failure. Fig. 6 shows the RBD used for the reliability analysis.

The system reliability function (R_{sys}) can be determined from the MOSFETs reliability function (R_{Qi}) as

$$R_{sys} = \prod R_{Qi}, \quad (3)$$

with i = 1…6.

A computational software was used to implement Monte Carlo simulations to obtain the reliability functions of each MOSFET considering variability in the parameters of (1). One hundred thousand simulations have been performed for each case to obtain the probabilistic distribution of the estimated lifetime (N_f) of each MOSFET.

Typically, semiconductors fail because of wearout mechanisms. Mostly, bond wire liftoff or substrate delamination, which are accelerated over time [39].

Consequently, it has been considered that the probabilistic distributions follow a two-parameter Weibull distribution. Therefore, their probability density function (pdf) can be expressed as

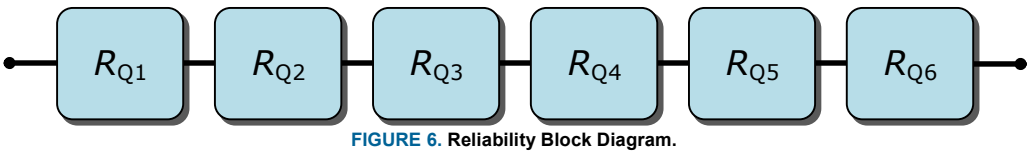

FIGURE 6. Reliability Block Diagram.

$$f(t) = \frac{\beta}{\eta^{\beta}} \cdot t^{\beta-1} \cdot e^{-\left(\frac{t}{\eta}\right)^{\beta}}, \quad (4)$$

being η the scale parameter and β the shape parameter of the Weibull distribution.

It has been considered for (1) that the parameters A, ΔT_j, β_1, β_2, β_4, and T_{jm} follow a normal distribution with the mean value (μ) described in Table III and Table IV and a standard deviation (σ) such that 3σ is equivalent to 5 % of the average value.

From the pdf, the reliability function ($R(t)$) can be obtained from the cumulative distribution function (cdf) ($F(t)$), leaving the expression as

$$R(t) = 1 - F(t) = 1 - \int_0^t f(t)dt = e^{-\left(\frac{t}{\eta}\right)^{\beta}}. \quad (5)$$

Table V summarizes the values of the MOSFET's reliability functions for the different cases analyzed.

TABLE V
SEMICONDUCTORS' RELIABILITY FUNCTION PARAMETERS.

	Q1 to Q4		Q5 & Q6	
Case	**η [years]**	**β**	**η [years]**	**β**
1	16.83	5.56	16.83	5.56
2a	18.44	5.57	>1000	8.61
2b	14.13	5.48	>1000	8.60
2c	6.17	5.22	>1000	8.67
3a	9.60	5.36	9.60	5.36
3b	15.01	5.55	15.01	5.55
3c	16.61	5.57	16.61	5.57
3d	9.22	5.36	9.22	5.36

The results shown in Table V already offer some interesting results. The scale parameter (η) for the different MOSFETs is similar except for the MOSFETs with a 0 load current, cases 2a to 2c. Nevertheless, the addition of harmonic content can reduce it by more than 40%, case 3d. Moreover, the unbalanced operation can reduce it even further, more than 60%, case 2c.

With these values, the reliability curves have been obtained. Fig. 7 shows a comparison of the power converter reliability with unbalanced loads. Fig. 8 compares the power converter reliability with distorted harmonic loads.

Table VI summarizes the B_{10} value, i.e., the point in which 10% of the samples have failed, for each case.

TABLE VI
B_{10} VALUE FOR EACH CASE.

Case	**B_{10} [years]**
1	8.1
2a	10.8
2b	8.2
2c	3.5
3a	4.5
3b	7.2
3c	8.0
3d	4.3

From Fig. 7 and Table VI, we can conclude that unbalanced loads affect the system's reliability. If the legs' current does not exceed the nominal value, 2a, the reliability is increased. However, if the phase current is increased to partially compensate for the power reduction, 2b, and 2c, the reliability can rapidly decrease. For case 2b, we can see that despite the total output power being only 70% of the nominal power, the B_{10} value is almost the same as the base case. For case 2c, with a total output power of 80% of the nominal power, the B_{10} value has substantially decreased by almost 60%.

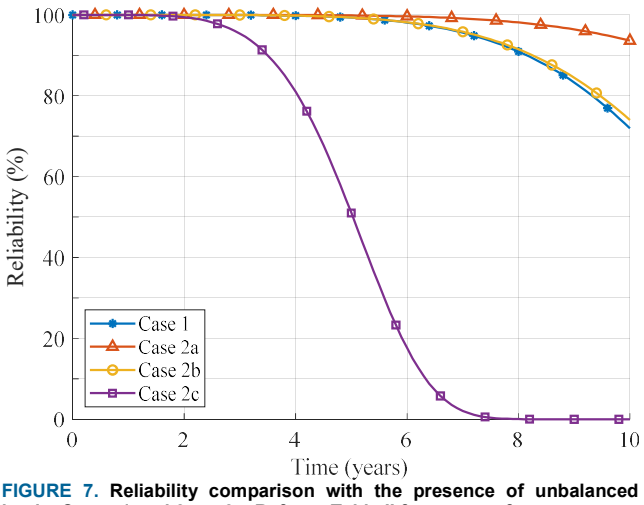

FIGURE 7. Reliability comparison with the presence of unbalanced loads. Cases 1 and 2a to 2c. Refer to Table II for cases reference.

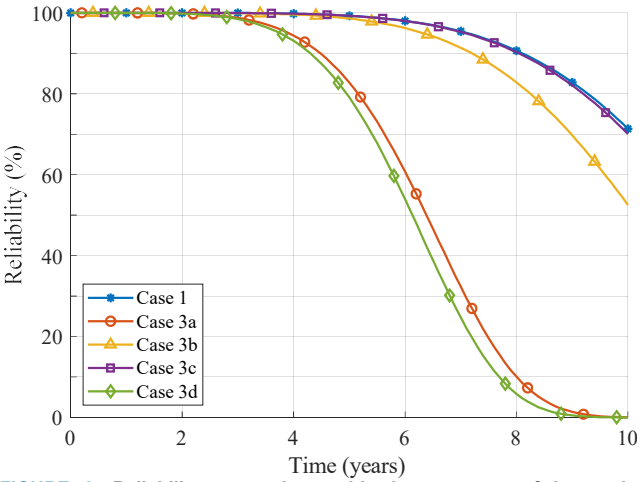

FIGURE 8. Reliability comparison with the presence of harmonic distortion. Cases 1 and 3a to 3d. Refer to Table II for cases reference.

From Fig. 8 and Table VI, we can conclude that harmonic distortion can also reduce the system's reliability. Case 3d has a B_{10} value almost 50% smaller than the base case. On the contrary, case 3c shows similar reliability. It can be seen that the phase delay of the harmonic current plays a highly relevant role. Therefore, harmonic distortion must be analyzed carefully and cannot be limited to the RMS value. The shape of the current is relevant.

Consequently, for power converters used in applications prone to the appearance of these disturbances, microgrids [7], [8], [10]–[12], PFCs [13], [14] or active filters [15]–[18], the reliability analysis has to take into account the appearance of these disturbances. Omitting them from the analysis can lead to wrong estimations of the system's reliability.

VI. HARMONIC DISTORTION ANALYSIS

The results obtained for the cases with harmonic distortion, 3a to 3d, are counter-intuitive. One could expect a more

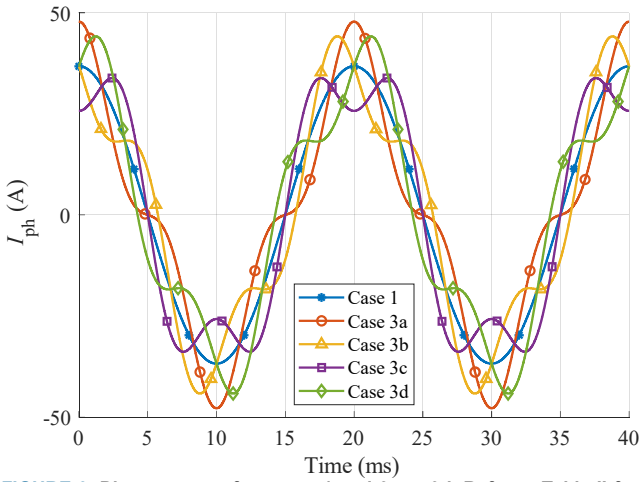

FIGURE 9. Phase current for cases 1 and 3a to 3d. Refer to Table II for cases reference.

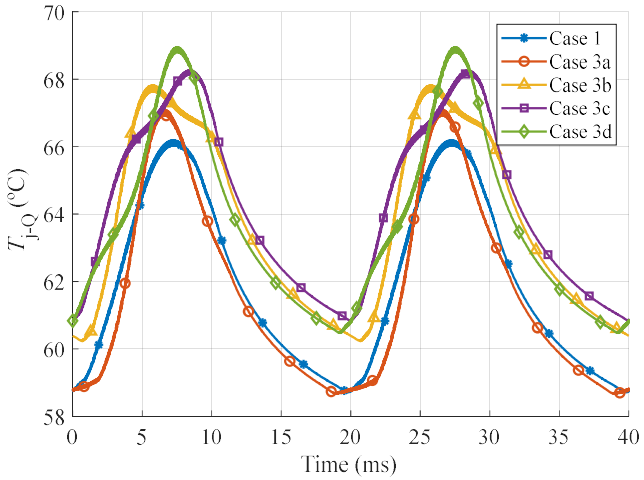

FIGURE 10. MOSFET junction temperature for cases 1 and 3a to 3d. Refer to Table II for cases reference.

significant reliability reduction with the cases with a higher peak current. However, it is not like this.

Fig. 9 shows the output currents for cases 1 and 3a to 3d. As it can be seen, the larger peak current corresponds to case 3a; however, the reliability reduction is higher for case 3d, which has a lower peak current. Additionally, cases 3b and 3d have the same peak current but highly different B_{10} values.

The results in Table III help to explain the significant differences. Among cases 1 and 3a to 3d, the only parameters of (1) that change are T_{jm}, ΔT_j, and I_B.

The parameter that is causing the most significant N_f variations is ΔT_j. The variation of T_{jm} is always lower than 4%, and the effect on the exponential term of (1) is low, less than 3%. The maximum ΔT_j variation is a 13.5% increase between case 1 and case 3d, and the parameter β_1 is substantially bigger than the other exponential coefficients (β_3 to β_6). Consequently, the main drive for the N_f variation is ΔT_j.

Consequently, the ΔT_j variation caused by the harmonic content addition is the root of the reliability variation. Fig. 10 shows the junction temperature of the MOSFETs for cases 1 and 3a to 3d. As expected from the values shown in Table III, the mean junction temperature is similar in all the cases, but the temperature swing varies.

Fig. 11 summarizes the procedure followed to analyze the difference in the temperature swing among the different cases. First, with the help of a power electronics simulation software, PLECS, the MOSFET power losses are calculated. Next, with the help of a computational software, MATLAB, the power losses are low-pass filtered to eliminate the components at frequencies equal or greater than the switching frequency. Using the Fourier transform, the power losses are decomposed into fundamental (50 Hz) and its harmonics. Finally, with each harmonic's magnitude (α_k) and argument (ϕ_k), the effect in ΔT_j amplitude and shape of the MOSFET thermal network is analyzed.

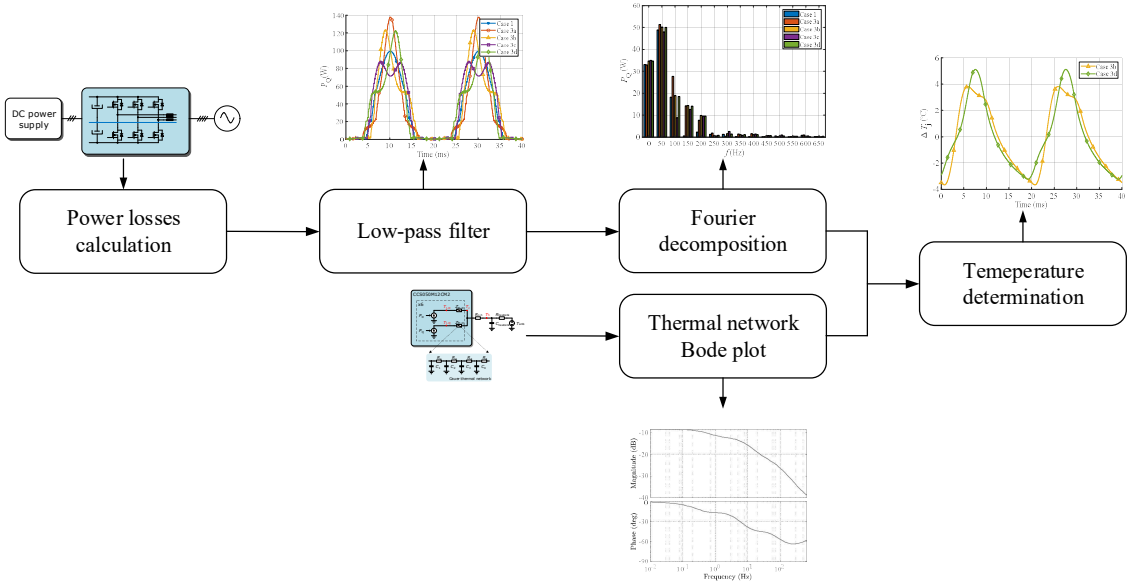

FIGURE 11. Methodology followed for the temperature swing analysis.

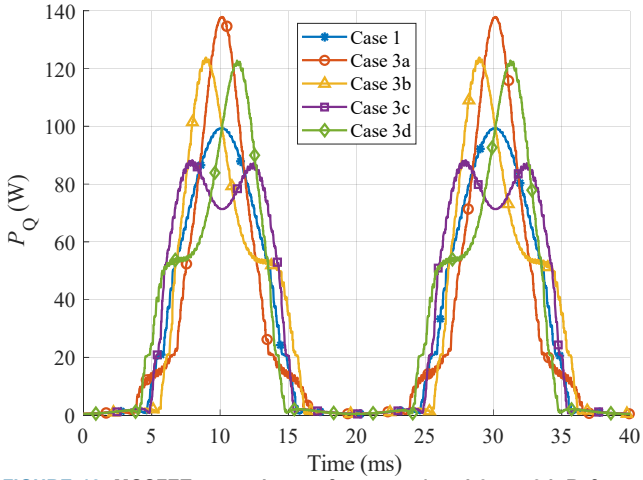

FIGURE 12. MOSFET power losses for cases 1 and 3a to 3d. Refer to Table II for cases reference.

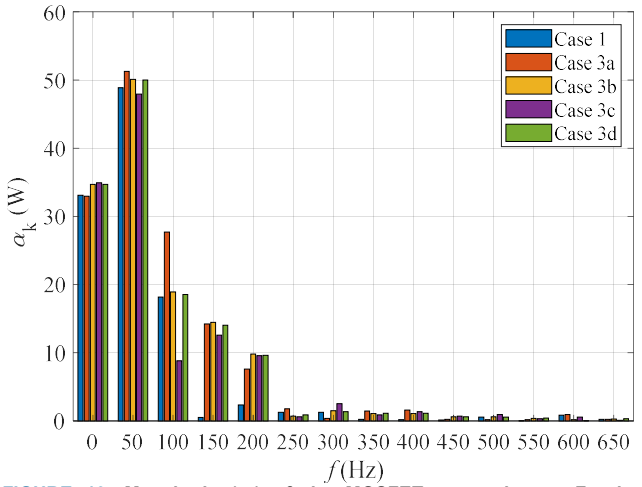

FIGURE 13. Magnitude (α_k) of the MOSFET power losses Fourier decomposition for cases 1 and 3a to 3d. Refer to Table II for cases reference.

Fig. 12 shows the filtered power losses for cases 1 and 3a to 3d. Fig. 13 shows each harmonic's magnitude. The power losses at frequencies greater than 0 Hz contribute to the temperature swing.

These two figures provide relevant information. First, it can be seen that, as expected, case 3a shows a higher peak in the power losses than the other cases. The power losses at frequencies greater than 0 Hz are the highest among all the cases. Despite this, the temperature swing is not the biggest.

Additionally, the power losses between cases 3b and 3d are similar in shape. Furthermore, their Fourier decompositions have similar magnitude (α_k) values, as shown in Fig. 13. Nevertheless, their temperature swing and reliability differ substantially.

The key point is the thermal network's frequency response and its interaction with the power losses argument (ϕ_k) for each harmonic. Fig. 14 shows the MOSFET's thermal network bode diagram. The transfer function of the thermal network is a complex equation that can be calculated following the detailed approach proposed in [53],

$$Z_i(s) = \frac{1}{\frac{1}{Z_{i+1}+R_i}+C_i s}, \tag{6}$$

being C_i and R_i the thermal capacitance and resistance of the different layers, see Fig. 3.

With the thermal network gain (G_k) and phase (φ_k) for each harmonic obtained from Fig. 14 together with the power losses Fourier decomposition coefficients (α_k, ϕ_k), it is possible to calculate the temperature swing as the superposition of multiple sinusoidal waveforms,

$$\Delta T_j(t) = \sum_{k=1}^{13} G_k \cdot \alpha_k \cdot \cos(2\pi k f t + \varphi_k + \phi_k). \tag{7}$$

Fig. 15 shows the ΔT_j calculated with this methodology for cases 3b and 3d. As it can be seen, it matches the simulation results as expected. It confirms that 2 cases with similar power dissipation in absolute values can have different temperature

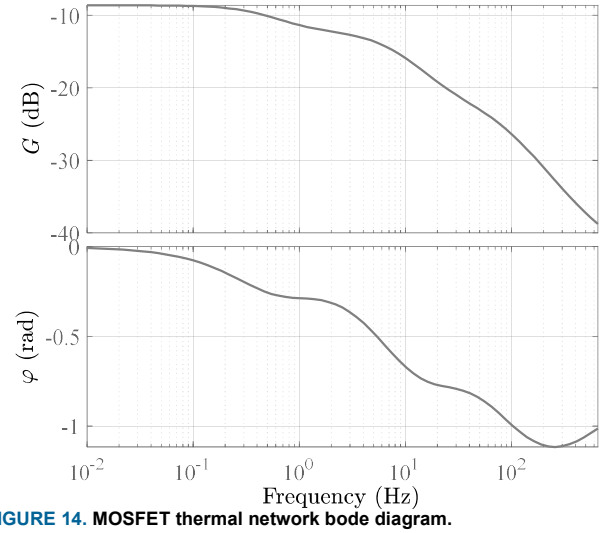

FIGURE 14. MOSFET thermal network bode diagram.

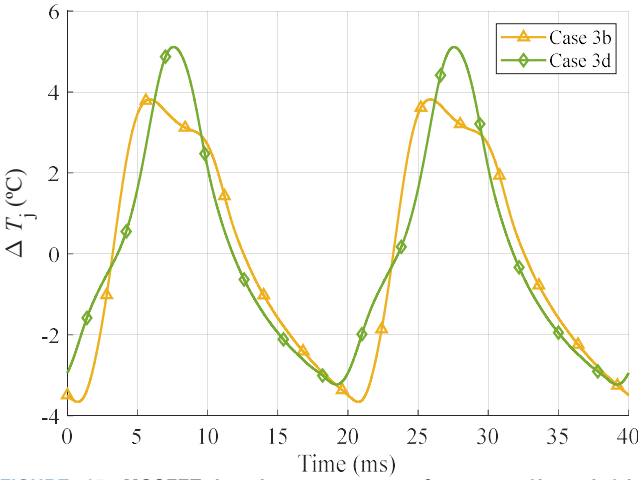

FIGURE 15. MOSFET junction temperature for cases 3b and 3d, calculated following the methodology proposed in Fig. 11. Refer to Table II for cases reference.

swings. The phase delay of the harmonic decomposition is crucial regarding the junction temperature swing.

VII. CONCLUSIONS

This paper proposes a comparative methodology to assess the impact of current imbalances and harmonic distortion on the semiconductor's reliability. The analysis has been done using a three-phase four-wire inverter. Still, the results can be extrapolated to other topologies.

In the paper, we have proved that the presence of unbalanced loads substantially distorts the reliability of the semiconductors, especially if some phases are overloaded to compensate for the loss of power in other phases.

The paper demonstrates that overloading more than 5 % two phases while the third one operates with 0 current is harmful to the semiconductor's reliability. A 20 % overload in two phases with the third phase operating with 0 current implies a 57 % reduction in reliability compared with a balanced load.

Furthermore, we proved that harmonic content in the load current substantially decreases the semiconductor's reliability.

A 30% of third harmonic content in the load current can reduce the semiconductor's reliability to half compared with a load without harmonic content.

Finally, the analysis shows that the harmonic content's phase delay is crucial in determining the semiconductor's reliability. Cases 3b and 3d have the same harmonic content but different phase delays, $\pi/2$ and $3\pi/2$. Both cases show similar peak current and similar power losses in magnitude. However, the different shape in the MOSFET power losses results in a different junction temperature swing and a substantially different semiconductor's reliability. Case 3d shows a $B10$ value 40 % lower than case 3b.

For all the reasons mentioned above, the reliability analyses of power converters for microgrids, PFCs, UPS, or active filters should not overlook these disturbances.

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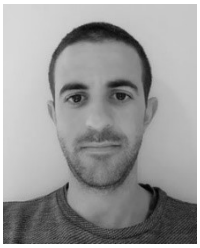

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