UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH
Escola Superior d'Enginyeries Industrial,
Aeroespacial i Audiovisual de Terrassa

Disseny i implementació d'un convertidor CC/CC per a una aplicació solar fotovoltaica

ANNEX 1: FULLS TÈCNICS

TREBALL FI DE GRAU

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Grau en Enginyeria Electrònica Industrial i Automàtica

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Índex

Normativa d'impressió per a la PCB (Castellà)

- El servicio de elaboración de circuitos impresos, consiste en el fresado de las pistas, corte del contorno y taladrado de los pads y vías a partir de archivos de diseño.
- Opcionalmente y de forma independiente, se ofrece el servicio de metalizado de placas mediante el cual se comunican por los taladros ambas capas del circuito. El circuito final, se entrega con una capa de barniz soldable antioxidante.
- Debido a las limitaciones del sistema, las placas vírgenes sobre las que se fresarán los circuitos son las disponibles en el mismo laboratorio de circuitos impresos a tal efecto (suministradas expresamente por el distribuidor del equipo).
- Para poder realizar el proceso de fresado, son necesarios los siguientes archivos provenientes del programa CAD de diseño de circuito impreso:
  - Archivos en formato GerberX de la(s) capa(s) del diseño.
  - Capa de contorno de placa (habitualmente denominada board o brd).
  - Archivo de taladros "Drills".

  Tan solo se garantiza que se puedan importar los archivos de los siguientes programas y versiones:

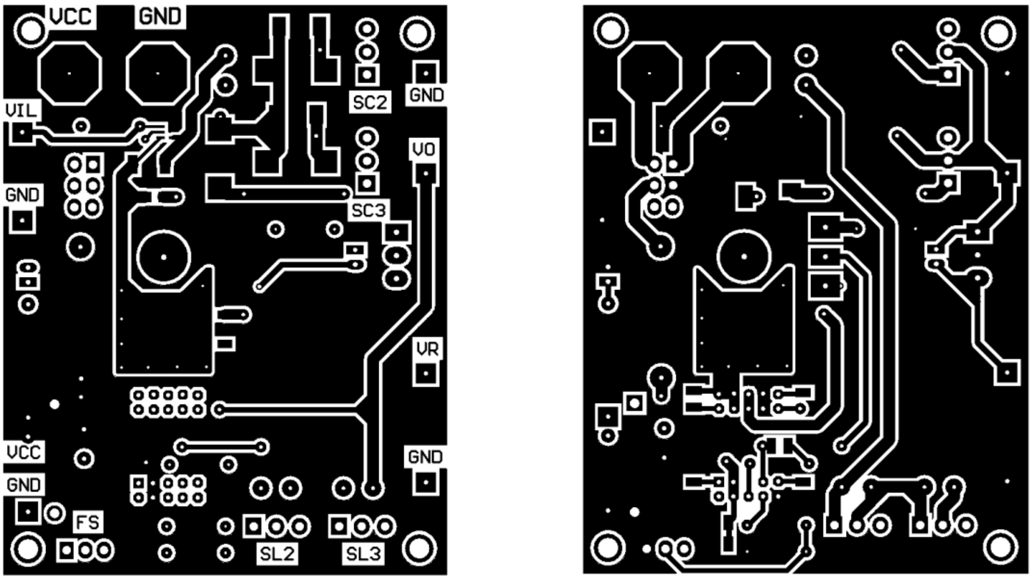
  - Protel, version DXP o superior.
  - Orcad, versión 9 o superior.
  - Ultiboard, versión 8 o superior.
- Mediante el sistema de fresado, es posible la realización de placas de circuito impreso de una o dos caras de tamaño máximo efectivo 270x210 mm.
- Salvo casos excepcionales, las zonas que no estén ocupadas por pistas, vías o pads deberán quedar cubiertas por cobre. Se recomienda el uso de planos de masa y/o alimentación.
- Los requerimientos de diseño para la elaboración de los Circuitos Impresos son:
  - Medidas de la placa en sistema métrico, para que los archivos se puedan importar correctamente.
  - Mínimo grosor de pistas o planos: Se recomienda grosor no inferior a 0.25mm con un mínimo absoluto de 0.15mm. Para diseños sin exigencias especiales de frecuencia o corriente se recomienda 0.6mm.
  - Mínima distancia entre pistas o entre planos y pistas: 0.3mm. Recomendado: 0.3mm.
  - Taladros recomendados: 0.6mm para vías, 1 mm para circuitos integrados formato DIL y componentes discretos, 1.2 mm para conectores tipo regleta y 3

mm para patas de sujeción. Hay que tener en cuenta que al metalizar los taladros (si es el caso), el grosor de las paredes interiores se reduce.

El número máximo de brocas a utilizar para un mismo diseño es 5.

- Se recomienda dejar el mayor grosor posible en los pads (existe la posibilidad de realizarlos ovalados) siempre respetando la distancia entre ellos (la misma que entre pistas).

- No se puede realizar serigrafiado (capa topsilk), a cambio, se puede grabar en la capa TOP sobre el plano de cobre. El grosor mínimo es el mismo que para las pistas.



Ejemplo de diseño de placa de circuito impreso. Izqda capa Top, dcha capa Bottom.

Solar Modules
Sun Plus

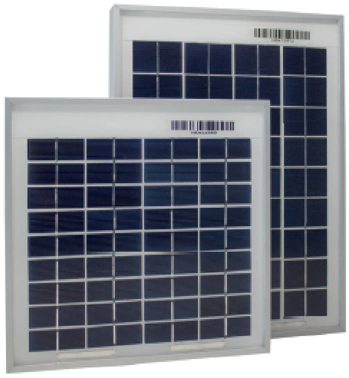
Solar Modules
310164, 310165, 310168 • 05/2019

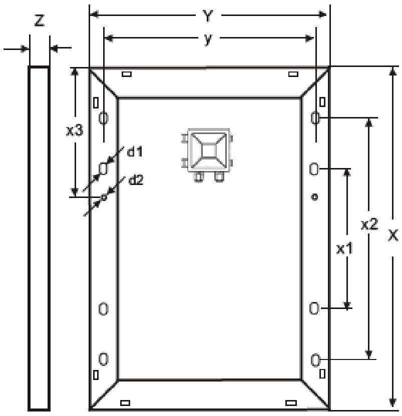
Phaesun Solar Modules are designed for industrial and professional applications using scratch resistant anodised aluminum with a twin wall frame. The junction box is borrowed from large sized modules and support a user friendly and outdoor proof field installation. Crystalline cells are sandwiched between strong tempered low iron solar glass sheets and double layered highly resistant foil.

Please find the technical data on the next page.

Phaesun Solarmodule Sun Plus sind für industrielle und professionelle Anwendungen ausgelegt und sind mit kratzfesten anodisierten doppelwandigen Aluminiumrahmen ausgestattet. Die Junction Box gleicht der bei großen Modulen verwendeten Box und erlaubt eine benutzerfreundliche und sichere Installation im Außenbereich. Kristalline Zellen werden von einer eisenarmen, starken Solarglasscheibe abgedeckt und einer doppelschichtigen hochwiderstandsfähigen Folie umschlossen.

Die technischen Daten finden Sie auf der nächsten Seite.





Technical Data		Technische Daten				Sun Plus 5	Sun Plus 10	Sun Plus 20
Systemvoltage		Systemspannung		(VDC)	[V]	12		
Power		Nennleistung		(Pmp)	[W]	5	10	20
Voltage at max. power		Spannung bei Max. Leistung		(Vmp)	[V]	16,8	17,0	17,0
Current at max. power		Strom bei Maximalleistung		(Imp)	[A]	0,3	0,59	1,18
Open circuit voltage		Leerlaufspannung		(Voc)	[V]	21,0	22,0	22,0
Short circuit voltage		Kurzschlussstrom		(Isc)	[A]	0,34	0,66	1,32
Max. tolerance		Max. Leistungstoleranz			[%]	+/−3%		
Max. system voltage		Max. Systemspannung			[V]	70		
Operating module temp.		Min. Betriebstemperatur			[°C]	−40 °C to +85		
Cells		Zellen				36 cells poly | 36 Zellen, polykristallin		
Front		Vorderseite				Tempered Low Iron Solar Glass | gehärtetes eisenarmes Solarglas		
Frame		Rahmen				Anodized Aluminum with Twin – Wall Profile | eloxierter Aluminium Hohlkammerrahmen		
Junction box protection		Anschlussdose Schutzklasse				IP65		
Dimension (l x w x h)		Abmessung (L x B x H)		(X/Y/Z)	[mm]	255 x 255 x 34	355 x 255 x 34	455 x 380 x 34
Mounting holes pitch		Befestigungslöcher Abstand		(x1/y/x2)	[mm]	150/226/–	200/226/–	330/351/–
Mounting hole Ø		Befestigungslöcher Ø				7 x 10	7 x 10	7 x 10
Weight		Gewicht			[kg]	1,0	1,4	2,2
Temperature coefficient	Power	Temperaturkoeffizient	Leistung		[%]	−0,43		
	Voc		Voc		[%]	−0,33		
	Isc		Isc		[%]	0,05		
Package		Verpackung				single | einzeln		
Certificates		Zertifikate				IEC 61215 (Design qualification and type approval), IEC 61730 (Module safety qualification), IEC 60068-2-68 (Test L: Dust and sand), IEC 61701 (Salt Mist corrosion)		
Article Number		Artikelnummer				310164	310165	310168

Datasheet

Sealed Lead-Acid Battery

General Purpose

537-5488(12V7.0Ah)

Specification

Cells Per Unit	6
Voltage Per Unit	12
Capacity	7.0Ah@20hr-rate to 1.80V per cell @25°C
Weight	Approx 2.2 kg
Max. Discharge Current	105 A (5 sec)
Internal Resistance	Approx 23m Ω
Operating Temp.Range	Discharge : -15~50°C (5~122°F) Charge : 0~40°C (32~104°F) Storage : -15~40°C (5~104°F)
Nominal Operating Temp. Range	25±3°C (77±5°F)
Float charging Voltage	13.5to 13.8VDC/unit Average at 25°C
Recommended Maximum Charging Current Limit	2.1 A
Equalization and Cycle Service	14.4to15.0 VDC/unit Average at 25°C
Self Discharge	The batteries can be stored for more than 6 months at 25°C. Self-discharge ratio less than 3% per month at 25°C. Please charge batteries before using.
Terminal	T1
Container Material	A.B.S. (UL94-HB) , Flammability resistance of UL94-V0 can be available upon request.

Applications

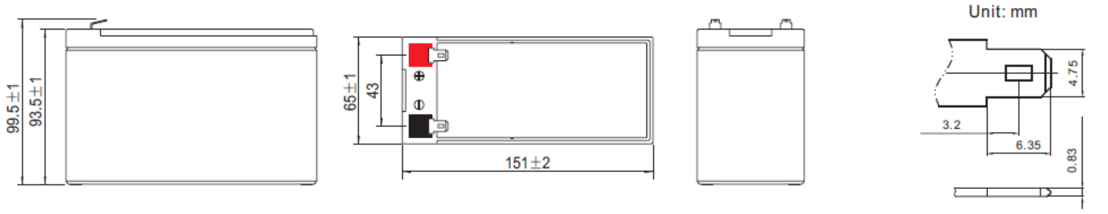
- *All purpose*
- *Uninterruptable Power Supply (UPS)*
- *Electric Power System (EPS)*
- *Emergency backup power supply*
- *Emergency light*
- *Railway signal*
- *Aircraft signal*
- *Alarm and security system*
- *Electronic apparatus and equipment*
- *Communication power supply*
- *DC power supply*
- *Auto control system*

Dimensions

Unit: mm Dimension:151 (L)×65 (W) ×99.5 (H)

T1 Terminal

Unit: mm



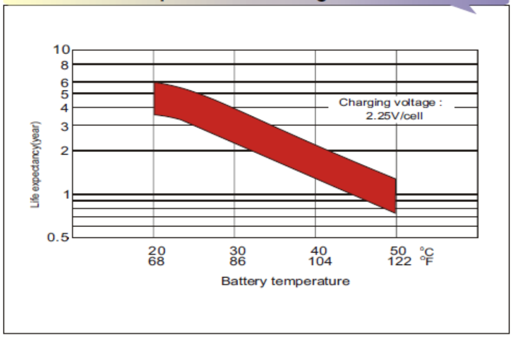
Constant Current Discharge Characteristics : A (25°C)

F.V/Time	5min	10min	15min	20min	30min	45min	1h	2h	3h	4h	5h	6h	8h	10h	20h
1.85V/cell	16.0	11.7	9.97	8.46	6.17	4.52	3.60	2.14	1.60	1.30	1.10	0.95	0.756	0.626	0.343
1.80V/cell	19.2	13.7	11.3	9.20	6.65	4.80	3.83	2.24	1.66	1.35	1.14	0.99	0.783	0.653	0.350
1.75V/cell	21.5	14.9	12.0	9.70	6.92	4.99	3.98	2.31	1.71	1.38	1.16	1.01	0.795	0.663	0.357
1.70V/cell	23.4	15.9	12.8	10.2	7.18	5.12	4.05	2.36	1.75	1.41	1.19	1.03	0.812	0.672	0.361
1.65V/cell	25.5	16.8	13.4	10.6	7.43	5.28	4.17	2.40	1.77	1.43	1.21	1.04	0.823	0.680	0.365
1.60V/cell	26.8	17.6	13.8	10.9	7.64	5.42	4.26	2.46	1.81	1.46	1.23	1.06	0.837	0.690	0.371

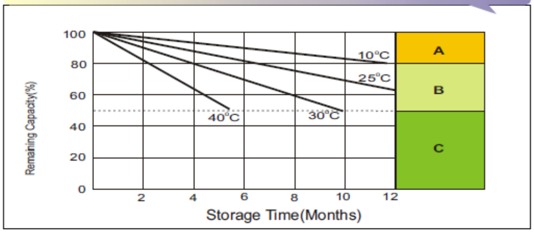
Constant Power Discharge Characteristics : W (25°C)

F.V/Time	5min	10min	15min	20min	30min	45min	1h	2h	3h	4h	5h	6h	8h	10h	20h
1.85V/cell	30.3	22.3	19.2	16.4	12.0	8.86	7.09	4.23	3.17	2.59	2.20	1.91	1.52	1.26	0.694
1.80V/cell	35.9	25.8	21.5	17.7	12.9	9.37	7.52	4.42	3.30	2.69	2.27	1.97	1.57	1.31	0.704
1.75V/cell	39.8	28.0	22.8	18.6	13.4	9.72	7.79	4.55	3.37	2.74	2.31	2.00	1.59	1.33	0.716
1.70V/cell	42.8	29.5	24.0	19.3	13.8	9.89	7.88	4.61	3.42	2.78	2.34	2.03	1.61	1.33	0.718
1.65V/cell	45.7	30.7	24.8	19.8	14.1	10.1	8.02	4.65	3.45	2.80	2.36	2.05	1.62	1.34	0.720
1.60V/cell	47.0	31.5	25.1	20.1	14.3	10.3	8.13	4.73	3.50	2.83	2.39	2.07	1.63	1.35	0.728

Effect of Temperature on Long Term Float Life



Self Discharge Characteristics

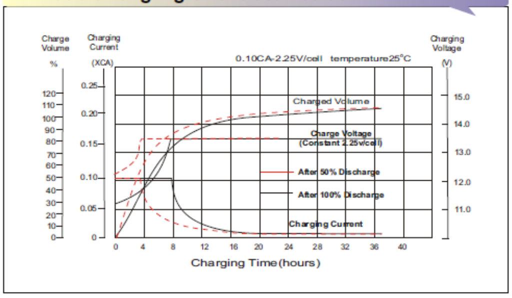


A No supplementary charge required
(Carry out supplementary charge before use if 100% capacity is required.)

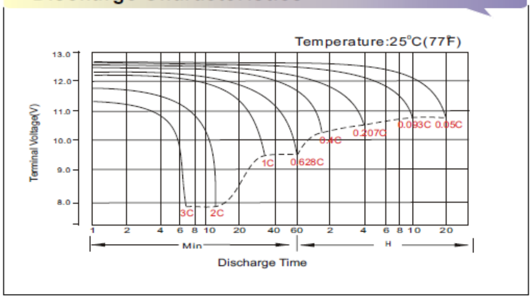
B Supplementary charge required before use.Optional charging way as below:
1.Charged for above 3 days at limted current 0.25CA and constant volatge 2.25V/cell.
2.Charged for above 20hours at limted current 0.25CA and constant volatge 2.45V/cell.
3.Charged for 8~10hours at limted current 0.05CA .

C Avoid this storage period unless regular Top charge.
Supplementary charge may often fail to recover the full capacity

Float Charging Characteristics



Discharge Characteristics



Available Capacity Subject to Temperature

Battery Type		-20℃	-10℃	0℃	5℃	10℃	20℃	25℃	30℃	40℃	45℃
AGM Battery	6V&12V	46%	66%	86%	89%	93%	98%	100%	102%	103%	105%

Discharge Current VS. Discharge Voltage

Final Discharge Voltage V/cell	1.80V	1.75V	1.60V
Discharge Current (A)	(A) ≤0.2C	0.2C< (A) <1.0C	(A) ≥1.0C

Charge the batteries at least once every six months, if they are stored at 25°C.

Charging Method:

Constant Voltage	-0.2Cx2h+2.4~2.45V/Cellx24h,Max. Current 0.3CA
Constant Current	0.1C until the voltage reaching 14.4V,then 0.1Cx4h

Maintenance & Cautions

Float Service:
◆It is recommended to check battery/Float voltage each month.
Equalisation charge:
◆Equalisation charging is recommended once every 3 to 6 months using.
◆Discharge 100% rated capacity.
◆Charge 2.35v/cell constant voltage, maximum 0.3CA 24hrs.
Cyclic Service:
◆Temperature compensation for varying temperatures:
-Charge voltage -3mV/Cell/degC from 25degC norm.
◆The service life of your battery will be affected by:
-The number of discharge cycles, depth of discharge, ambient temperature and charging voltage.

LT3652 y BQ2031

Power Tracking 2A Battery Charger for Solar Power

FEATURES

- **Input Supply Voltage Regulation Loop for Peak Power Tracking in (MPPT) Solar Applications**
- **Wide Input Voltage Range: 4.95V to 32V (40V Abs Max)**
- **Programmable Charge Rate Up to 2A**
- **User Selectable Termination: C/10 or On-Board Termination Timer**
- **Resistor Programmable Float Voltage Up to 14.4V Accommodates Li-Ion/Polymer, $LiFePO_4$, SLA Chemistries**
- **No V_{IN} Blocking Diode Required for Battery Voltages ≤ 4.2V**
- 1MHz Fixed Frequency
- 0.5% Float Voltage Reference Accuracy
- 5% Charge Current Accuracy
- 2.5% C/10 Detection Accuracy
- Binary-Coded Open-Collector Status Pins
- Thermally Enhanced 12-Lead 3mm × 3mm DFN and MSE Packages

APPLICATIONS

- Solar Powered Applications
- Remote Monitoring Stations
- $LiFePO_4$ (Lithium Phosphate) Applications
- Portable Handheld Instruments
- 12V to 24V Automotive Systems

DESCRIPTION

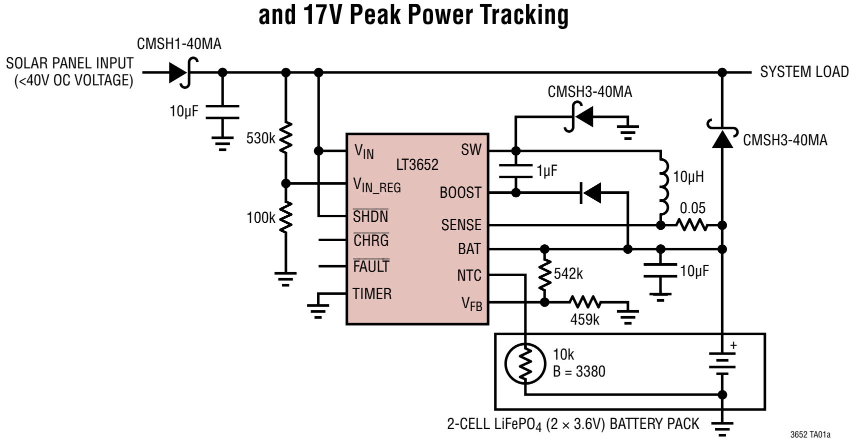
The LT®3652 is a complete monolithic step-down battery charger that operates over a 4.95V to 32V input voltage range. The LT3652 provides a constant-current/constant-voltage charge characteristic, with maximum charge current externally programmable up to 2A. The charger employs a 3.3V float voltage feedback reference, so any desired battery float voltage up to 14.4V can be programmed with a resistor divider.

The LT3652 employs an input voltage regulation loop, which reduces charge current if the input voltage falls below a programmed level, set with a resistor divider. When the LT3652 is powered by a solar panel, the input regulation loop is used to maintain the panel at peak output power.

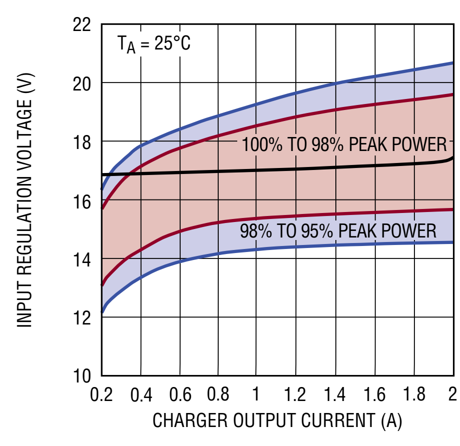
The LT3652 can be configured to terminate charging when charge current falls below 1/10 of the programmed maximum (C/10). Once charging is terminated, the LT3652 enters a low-current (85µA) standby mode. An auto-recharge feature starts a new charging cycle if the battery voltage falls 2.5% below the programmed float voltage. The LT3652 also contains a programmable safety timer, used to terminate charging after a desired time is reached. This allows top-off charging at currents less than C/10.

TYPICAL APPLICATION

2A Solar Panel Power Manager With 7.2V $LiFePO_4$ Battery and 17V Peak Power Tracking



Solar Panel Input Voltage Regulation, Tracks Max Power Point to Greater Than 98%



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Voltages:

V_{IN} 40V

V_{IN_REG}, $\overline{SHDN}$, $\overline{CHRG}$, $\overline{FAULT}$ .... V_{IN} + 0.5V, 40V

SW...40V

SW-V_{IN}...4.5V

BOOST ....SW+10V, 50V

BAT, SENSE...15V

BAT-SENSE .... –0.5V to +0.5V

NTC, TIMER, ...2.5V

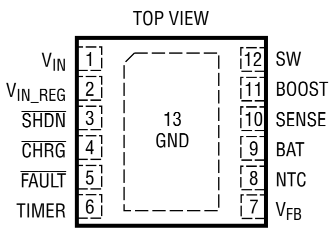
V_{FB} 5V

Operating Junction Temperature Range

(Note 2) .... –40°C to 125°C

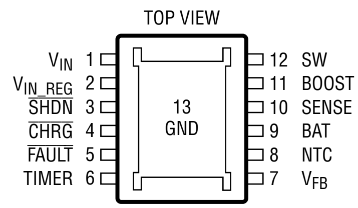
Storage Temperature Range.................. –65°C to 150°C

PIN CONFIGURATION



DD PACKAGE
12-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
12-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3652EDD#PBF	LT3652EDD#TRPBF	LFHT	12-Lead Plastic DFN 3mm × 3mm	–40°C to 125°C
LT3652IDD#PBF	LT3652IDD#TRPBF	LFHT	12-Lead Plastic DFN 3mm × 3mm	–40°C to 125°C
LT3652EMSE#PBF	LT3652EMSE#TRPBF	3652	12-Lead Plastic MSOP	–40°C to 125°C
LT3652IMSE#PBF	LT3652IMSE#TRPBF	3652	12-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 20V, Boost – SW = 4V, $\overline{SHDN}$ = 2V, V_{FB} = 3.3V, C_{TIMER} = 0.68µF.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	V_{IN} Operating Range V_{IN} Start Voltage	V_{BAT} = 4.2 (Notes 3, 4) V_{BAT} = 4.2 (Note 4)	● ●	4.95 7.5		32	V V
$V_{IN(OVLO)}$	OVLO Threshold OVLO Hysteresis	V_{IN} Rising	●	32	35 1	40	V V
$V_{IN(UVLO)}$	UVLO Threshold UVLO Hysteresis	V_{IN} Rising			4.6 0.2	4.95	V V
$V_{FB(FLT)}$	Float Voltage Reference	(Note 6)	 ●	3.282 3.26	3.3	3.318 3.34	V V
$\Delta V_{RECHARGE}$	Recharge Reference Threshold	Voltage Relative to $V_{FB(FLT)}$ (Note 6)			82.5		mV
$V_{FB(PRE)}$	Reference Precondition Threshold	V_{FB} Rising (Note 6)			2.3		V
$V_{FB(PREHYST)}$	Reference Precondition Threshold Hysteresis	Voltage Relative to $V_{FB(PRE)}$ (Note 6)			70		mV
$V_{IN\_REG(TH)}$	Input Regulation Reference	V_{FB} = 3V; V_{SENSE} – V_{BAT} = 50mV	●	2.65	2.7	2.75	V
I_{IN_REG}	Input Regulation Reference Bias Current	V_{IN_REG} = $V_{IN\_REG(TH)}$	●		35	100	nA
I_{VIN}	Operating Input Supply Current	CC/CV Mode, I_{SW} = 0 Standby Mode Shutdown ($\overline{SHDN}$ = 0)	●		2.5 85 15	3.5	mA µA µA
I_{BOOST}	BOOST Supply Current	Switch On, I_{SW} = 0, 2.5 < $V_{(BOOST-SW)}$ < 8.5			20		mA
I_{BOOST}/I_{SW}	BOOST Switch Drive	I_{SW} = 2A			30		mA/A
$V_{SW(ON)}$	Switch-On Voltage Drop	V_{IN} – V_{SW}, I_{SW} = 2A			350		mV
$I_{SW(MAX)}$	Switch Current Limit		●	2.5	3		A
$V_{SENSE(PRE)}$	Precondition Sense Voltage	V_{SENSE} – V_{BAT}; V_{FB} = 2V			15		mV
$V_{SENSE(DC)}$	Maximum Sense Voltage	V_{SENSE} – V_{BAT}; V_{FB} = 3V (Note 7)	●	95	100	105	mV
$V_{SENSE(C/10)}$	C/10 Trigger Sense Voltage	V_{SENSE} – V_{BAT}, Falling	●	7.5	10	12.5	mV
I_{BAT}	BAT Input Bias Current	Charging Terminated			0.1	1	µA
I_{SENSE}	SENSE Input Bias Current	Charging Terminated			0.1	1	µA
$I_{REVERSE}$	Charger Reverse Current I_{BAT} + I_{SENSE} + I_{SW}	V_{IN} = 0; V_{BAT} = V_{SENSE} = V_{SW} = 4.2V			1		µA
I_{VFB}	V_{FB} Input Bias Current	Charging Terminated			65		nA
I_{VFB}	V_{FB} Input Bias Current	CV Operation (Note 5)			110		nA
$V_{NTC(H)}$	NTC Range Limit (High)	V_{NTC} Rising	●	1.25	1.36	1.45	V
$V_{NTC(L)}$	NTC Range Limit (Low)	V_{NTC} Falling	●	0.27	0.29	0.315	V
$V_{NTC(HYST)}$	NTC Threshold Hysteresis	% of threshold			20		%
$R_{NTC(DIS)}$	NTC Disable Impedance	Impedance to ground	●	250	500		kΩ
I_{NTC}	NTC Bias Current	V_{NTC} = 0.8V	●	47.5	50	52.5	µA
$V_{\overline{SHDN}}$	Shutdown Threshold	Rising	●	1.15	1.2	1.25	V
$V_{\overline{SHDN}(HYST)}$	Shutdown Hysteresis				120		mV
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Input Bias Current				–10		nA
$V_{\overline{CHRG}}$, $V_{\overline{FAULT}}$	Status Low Voltage	10mA Load	●			0.4	V
I_{TIMER}	Charge/Discharge Current				25		µA
$V_{TIMER(DIS)}$	Timer Disable Threshold		●	0.1	0.25		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 20V, Boost – SW = 4V, $\overline{SHDN}$ = 2V, V_{FB} = 3.3V, C_{TIMER} = 0.68µF.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{TIMER}	Full Charge Cycle Timeout				3		hr
	Precondition Timeout				22.5		min
	Timer Accuracy		●	–10		10	%
f_O	Operating Frequency				1		MHz
DC	Duty Cycle Range	Continuous Operation	●	15		90	%

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3652EDD is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LT3652IDD specifications are guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: V_{IN} minimum voltages below the start threshold are only supported if (V_{BOOST}-V_{SW}) > 2V.

Note 4: This parameter is valid for programmed output battery float voltages ≤ 4.2V. V_{IN} operating range minimum is 0.75V above the programmed output battery float voltage ($V_{BAT(FLT)}$ + 0.75V). V_{IN} Start Voltage is 3.3V above the programmed output battery float voltage ($V_{BAT(FLT)}$ + 3.3V).

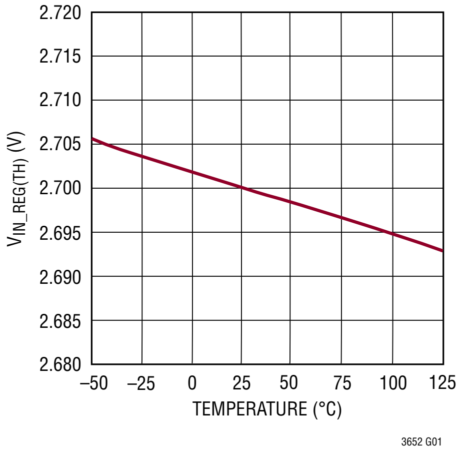
Note 5: Output battery float voltage ($V_{BAT(FLT)}$) programming resistor divider equivalent resistance = 250k compensates for input bias current.

Note 6: All V_{FB} voltages measured through 250k series resistance.

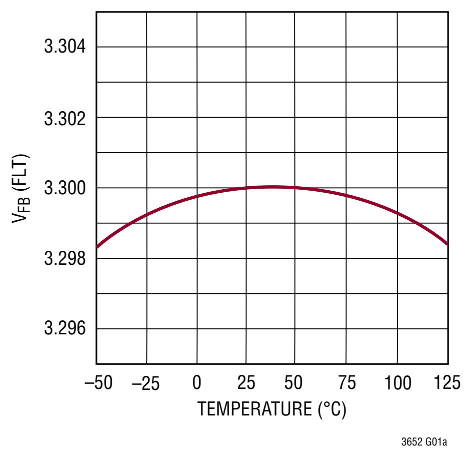
Note 7: $V_{SENSE(DC)}$ is reduced by thermal foldback as junction temperature approaches 125°C.

TYPICAL PERFORMANCE CHARACTERISTICS $T_J = 25°C$, unless otherwise noted.

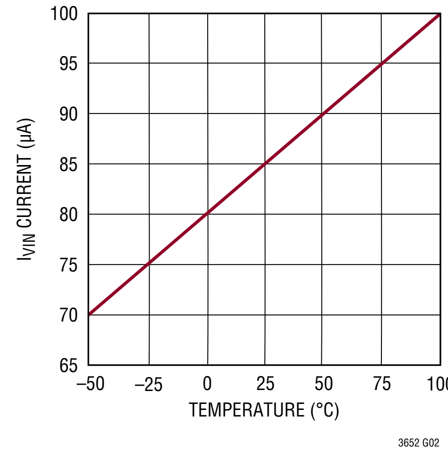
V_{IN_REG} Threshold vs Temperature: I_{CHG} at 50%



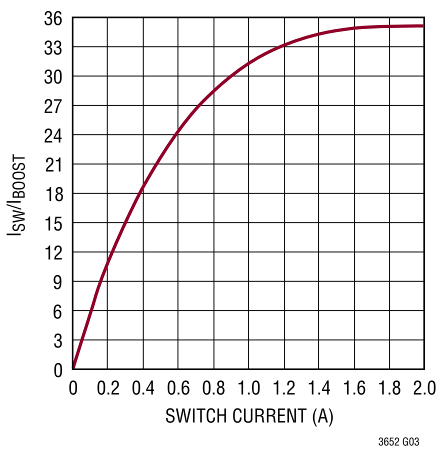
V_{FB} Reference Voltage vs Temperature



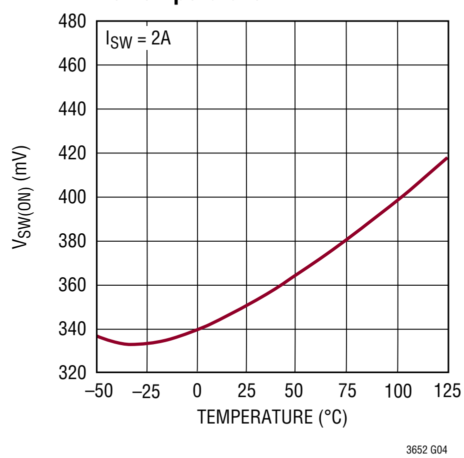
V_{IN} Standby Mode Current vs Temperature



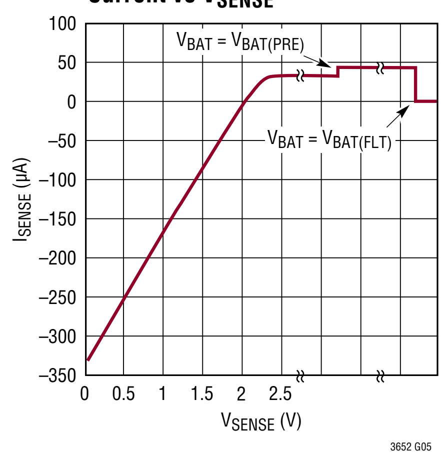
Switch Drive (I_{SW}/I_{BOOST}) vs Switch Current



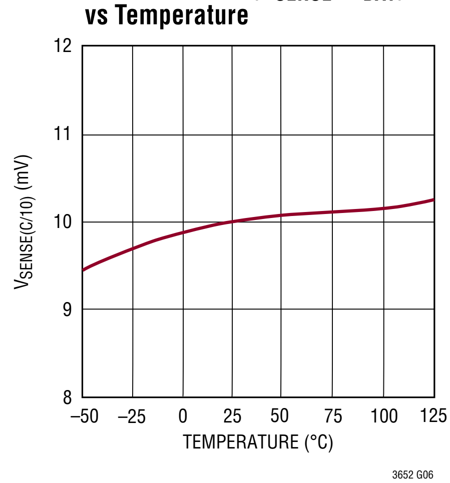
Switch Forward Drop ($V_{IN} – V_{SW}$) vs Temperature



CC/CV Charging; SENSE Pin Bias Current vs V_{SENSE}

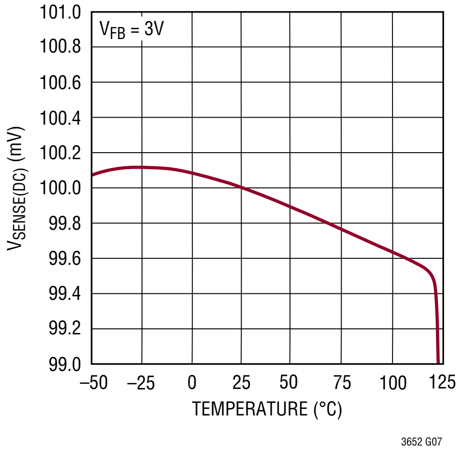


C/10 Threshold (V_{SENSE}–V_{BAT}) vs Temperature

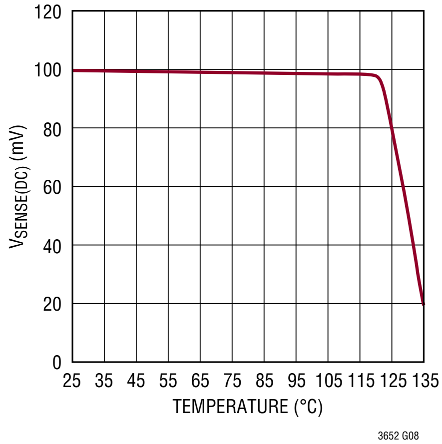


TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, unless otherwise noted.

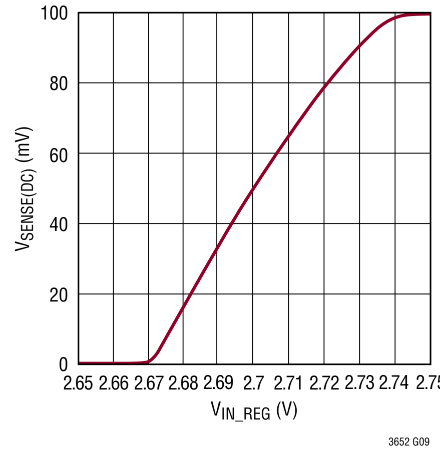
Maximum Charge Current (V_{SENSE}–V_{BAT}) vs Temperature



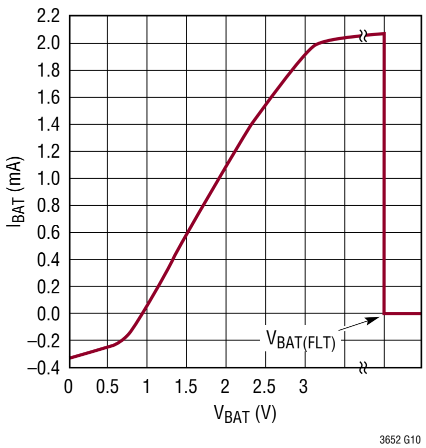
Thermal Foldback – Maximum Charge Current (V_{SENSE}–V_{BAT}) vs Temperature



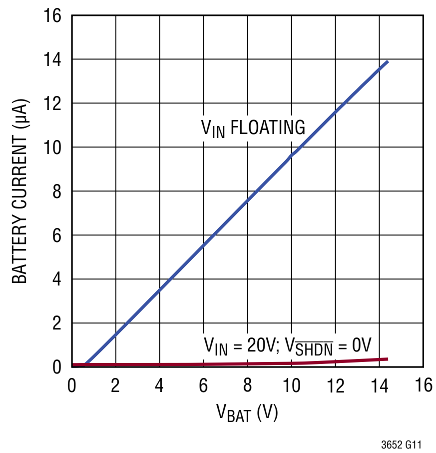
Maximum Charge Current (V_{SENSE}–V_{BAT}) vs V_{IN_REG} Voltage



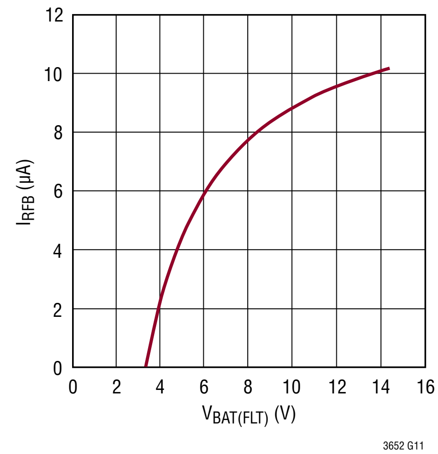
CC/CV Charging; BAT Pin Bias Current vs V_{BAT}



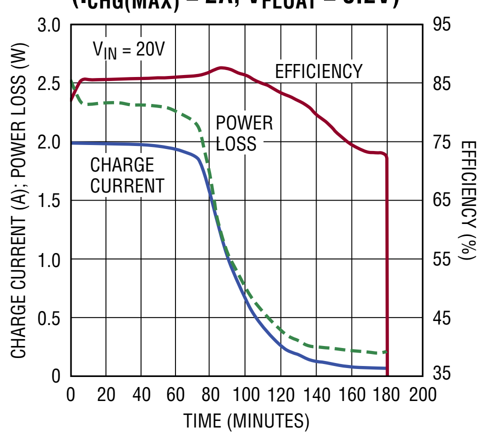
Battery Bias Current with Charger Disabled ($I_{BAT} + I_{SENSE} + I_{BOOST} + I_{SW}$)



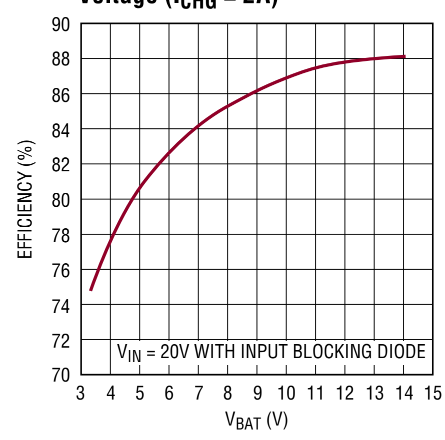
V_{FLOAT} Programming Resistor Current vs V_{FLOAT} for 2-Resistor Network



Charge Current, Efficiency, and Power Loss vs Time ($I_{CHG(MAX)} = 2A$; $V_{FLOAT} = 8.2V$)



Charger Efficiency vs Battery Voltage ($I_{CHG} = 2A$)



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PIN FUNCTIONS

V_{IN} (Pin 1): Charger Input Supply. V_{IN} operating range is 4.95V to 32V. V_{IN} must be 3.3V greater than the programmed output battery float voltage ($V_{BAT(FLT)}$) for reliable start-up. ($V_{IN} – V_{BAT(FLT)}$) ≥ 0.75V is the minimum operating voltage, provided ($V_{BOOST} – V_{SW}$) ≥ 2V. I_{VIN} ~ 85μA after charge termination.

V_{IN_REG} (Pin 2): Input Voltage Regulation Reference. Maximum charge current is reduced when this pin is below 2.7V. Connecting a resistor divider from V_{IN} to this pin enables programming of minimum operational V_{IN} voltage. This is typically used to program the peak power voltage for a solar panel. The LT3652 servos the maximum charge current required to maintain the programmed operational V_{IN} voltage, through maintaining the voltage on V_{IN_REG} at or above 2.7V. If the voltage regulation feature is not used, connect the pin to V_{IN}.

$\overline{SHDN}$ (Pin 3): Precision Threshold Shutdown Pin. The enable threshold is 1.2V (rising), with 120mV of input hysteresis. When in shutdown mode, all charging functions are disabled. The precision threshold allows use of the $\overline{SHDN}$ pin to incorporate UVLO functions. If the $\overline{SHDN}$ pin is pulled below 0.4V, the IC enters a low current shutdown mode where V_{IN} current is reduced to 15μA. Typical $\overline{SHDN}$ pin input bias current is 10nA. If the shutdown function is not desired, connect the pin to V_{IN}.

$\overline{CHRG}$ (Pin 4): Open-Collector Charger Status Output; typically pulled up through a resistor to a reference voltage. This status pin can be pulled up to voltages as high as V_{IN} when disabled, and can sink currents up to 10mA when enabled. During a battery charging cycle, if required charge current is greater than 1/10 of the programmed maximum current (C/10), $\overline{CHRG}$ is pulled low. A temperature fault also causes this pin to be pulled low. After C/10 charge termination or, if the internal timer is used for termination and charge current is less than C/10, the $\overline{CHRG}$ pin remains high-impedance.

$\overline{FAULT}$ (Pin 5): Open-Collector Charger Status Output; typically pulled up through a resistor to a reference voltage. This status pin can be pulled up to voltages as high as V_{IN} when disabled, and can sink currents up to 10mA when enabled. This pin indicates fault conditions during a battery charging cycle. A temperature fault causes this pin to be pulled low. If the internal timer is used for termination, a bad battery fault also causes this pin to be pulled low. If no fault conditions exist, the $\overline{FAULT}$ pin remains high-impedance.

TIMER (Pin 6): End-Of-Cycle Timer Programming Pin. If a timer-based charge termination is desired, connect a capacitor from this pin to ground. Full charge end-of-cycle time (in hours) is programmed with this capacitor following the equation:

$$t_{EOC} = C_{TIMER} \bullet 4.4 \bullet 10^6$$

A bad battery fault is generated if the battery does not achieve the precondition threshold voltage within one-eighth of t_{EOC}, or:

$$t_{PRE} = C_{TIMER} \bullet 5.5 \bullet 10^5$$

A 0.68μF capacitor is typically used, which generates a timer EOC at three hours, and a precondition limit time of 22.5 minutes. If a timer-based termination is not desired, the timer function is disabled by connecting the TIMER pin to ground. With the timer function disabled, charging terminates when the charge current drops below a C/10 threshold, or $I_{CHG(MAX)}/10$

V_{FB} (Pin 7): Battery Float Voltage Feedback Reference. The charge function operates to achieve a final float voltage of 3.3V on this pin. Output battery float voltage ($V_{BAT(FLT)}$) is programmed using a resistor divider. $V_{BAT(FLT)}$ can be programmed up to 14.4V.

The auto-restart feature initiates a new charging cycle when the voltage at the V_{FB} pin falls 2.5% below the float voltage reference.

The V_{FB} pin input bias current is 110nA. Using a resistor divider with an equivalent input resistance at the V_{FB} pin of 250k compensates for input bias current error.

Required resistor values to program desired $V_{BAT(FLT)}$ follow the equations:

$$R1 = (V_{BAT(FLT)} \bullet 2.5 \bullet 10^5)/3.3 \quad (\Omega)$$

$$R2 = (R1 \bullet 2.5 \bullet 10^5)/(R1 - (2.5 \bullet 10^5)) \quad (\Omega)$$

R1 is connected from BAT to V_{FB}, and R2 is connected from V_{FB} to ground.

PIN FUNCTIONS

NTC (Pin 8): Battery Temperature Monitor Pin. This pin is the input to the NTC (Negative Temperature Coefficient) thermistor temperature monitoring circuit. This function is enabled by connecting a 10kΩ, B = 3380 NTC thermistor from the NTC pin to ground. The pin sources 50µA, and monitors the voltage across the 10kΩ thermistor. When the voltage on this pin is above 1.36 (T < 0°C) or below 0.29V (T > 40°C), charging is disabled and the $\overline{CHRG}$ and $\overline{FAULT}$ pins are both pulled low. If internal timer termination is being used, the timer is paused, suspending the charging cycle. Charging resumes when the voltage on NTC returns to within the 0.29V to 1.36V active region. There is approximately 5°C of temperature hysteresis associated with each of the temperature thresholds. The temperature monitoring function remains enabled while the thermistor resistance to ground is less than 250k, so if this function is not desired, leave the NTC pin unconnected.

BAT (Pin 9): Charger Output Monitor Pin. Connect a 10µF decoupling capacitance (C_{BAT}) to ground. Depending on application requirements, larger value decoupling capacitors may be required. The charge function operates to achieve the programmed output battery float voltage ($V_{BAT(FLT)}$) at this pin. This pin is also the reference for the current sense voltage. Once a charge cycle is terminated, the input bias current of the BAT pin is reduced to < 0.1µA, to minimize battery discharge while the charger remains connected.

SENSE (Pin 10): Charge Current Sense Pin. Connect the inductor sense resistor (R_{SENSE}) from the SENSE pin to the BAT pin. The voltage across this resistor sets the average charge current. The maximum charge current ($I_{CHG(MAX)}$) corresponds to 100mV across the sense resistor. This resistor can be set to program maximum charge current as high as 2A. The sense resistor value follows the relation:

$$R_{SENSE} = 0.1/I_{CHG(MAX)}\ (\Omega)$$

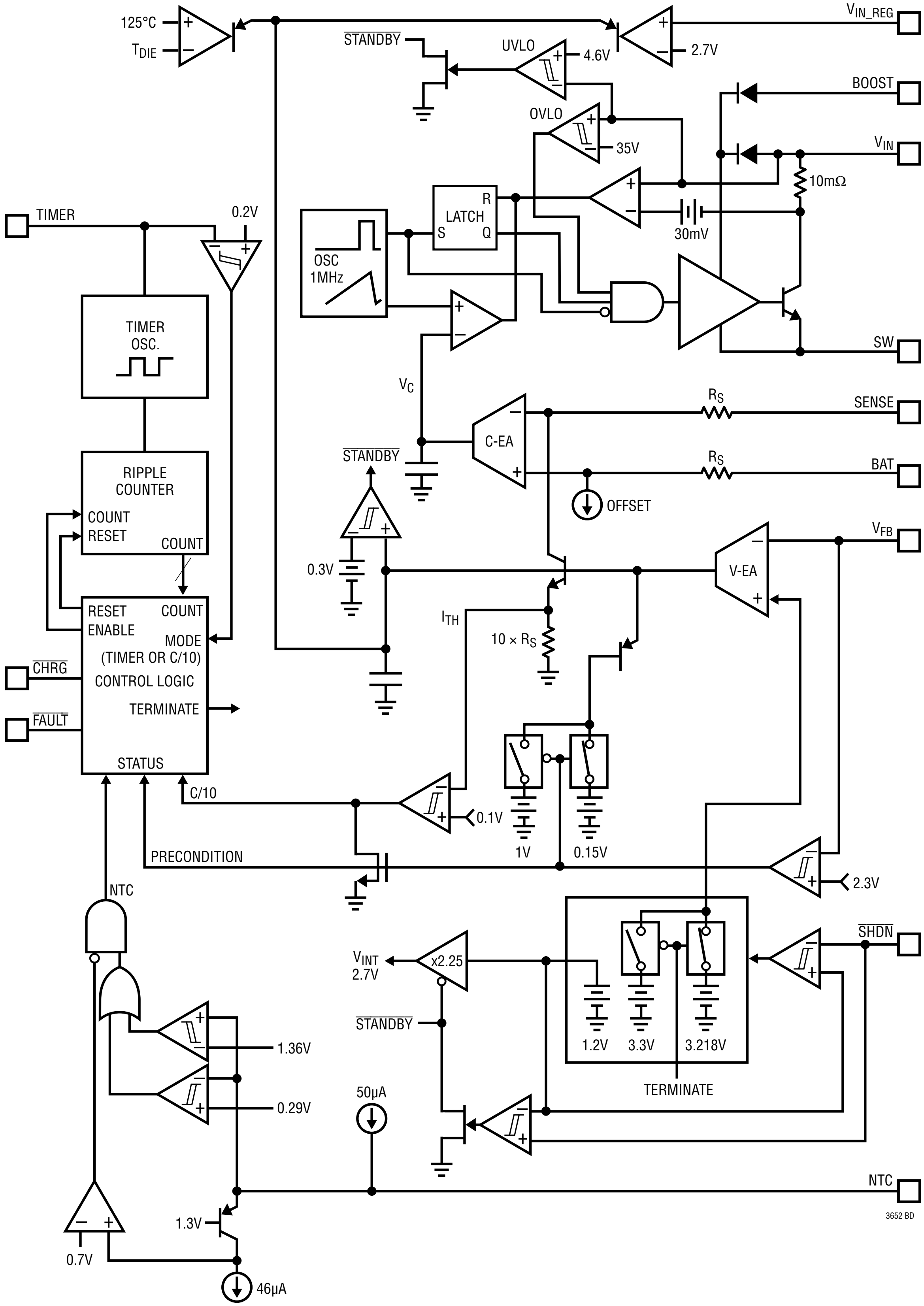
Once a charge cycle is terminated, the input bias current of the SENSE pin is reduced to < 0.1µA, to minimize battery discharge while the charger remains connected.

BOOST (Pin 11): Bootstrapped Supply Rail for Switch Drive. This pin facilitates saturation of the switch transistor. Connect a 1µF or greater capacitor from the BOOST pin to the SW pin. Operating range of this pin is 0V to 8.5V, referenced to the SW pin. The voltage on the decoupling capacitor is refreshed through a rectifying diode, with the anode connected to either the battery output voltage or an external source, and the cathode connected to the BOOST pin.

SW (Pin 12): Switch Output Pin. This pin is the output of the charger switch, and corresponds to the emitter of the switch transistor. When enabled, the switch shorts the SW pin to the V_{IN} supply. The drive circuitry for this switch is bootstrapped above the V_{IN} supply using the BOOST supply pin, allowing saturation of the switch for maximum efficiency. The effective on-resistance of the boosted switch is 0.175Ω.

GND (Pin 13): Ground Reference and Backside Exposed Lead Frame Thermal Connection. Solder the exposed lead frame to the PCB ground plane.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Overview

LT3652 is a complete monolithic, mid-power, multi-chemistry buck battery charger, addressing high input voltage applications with solutions that require a minimum of external components. The IC uses a 1MHz constant frequency, average-current mode step-down architecture.

The LT3652 incorporates a 2A switch that is driven by a bootstrapped supply to maximize efficiency during charging cycles. Wide input range allows operation to full charge from voltages as high as 32V. A precision threshold shutdown pin allows incorporation of UVLO functionality using a simple resistor divider. The IC can also be put into a low-current shutdown mode, in which the input supply bias is reduced to only 15µA.

The LT3652 employs an input voltage regulation loop, which reduces charge current if a monitored input voltage falls below a programmed level. When the LT3652 is powered by a solar panel, the input regulation loop is used to maintain the panel at peak output power.

The LT3652 automatically enters a battery precondition mode if the sensed battery voltage is very low. In this mode, the charge current is reduced to 15% of the programmed maximum, as set by the inductor sense resistor, R_{SENSE}. Once the battery voltage reaches 70% of the fully charged float voltage, the IC automatically increases maximum charge current to the full programmed value.

The LT3652 can use a charge-current based C/10 termination scheme, which ends a charge cycle when the battery charge current falls to one tenth of the programmed maximum charge current. The LT3652 also contains an internal charge cycle control timer, for timer-based termination. When using the internal timer, the IC combines C/10 detection with a programmable time constraint, during which the charging cycle can continue beyond the C/10 level to top-off a battery. The charge cycle terminates when a specific time elapses, typically 3 hours. When the timer-based scheme is used, the IC also supports bad battery detection, which triggers a system fault if a battery stays in precondition mode for more than one eighth of the total charge cycle time.

Once charging is terminated, the LT3652 automatically enters a low-current standby mode where supply bias currents are reduced to 85µA. The IC continues to monitor the battery voltage while in standby, and if that voltage falls 2.5% from the full-charge float voltage, the LT3652 engages an automatic charge cycle restart. The IC also automatically restarts a new charge cycle after a bad battery fault once the failed battery is removed and replaced with another battery.

The LT3652 contains provisions for a battery temperature monitoring circuit. This feature monitors battery temperature using a thermistor during the charging cycle. If the battery temperature moves outside a safe charging range of 0°C to 40°C, the IC suspends charging and signals a fault condition until the temperature returns to the safe charging range.

The LT3652 contains two digital open-collector outputs, which provide charger status and signal fault conditions. These binary-coded pins signal battery charging, standby or shutdown modes, battery temperature faults, and bad battery faults.

General Operation (See Block Diagram)

The LT3652 uses average current mode control loop architecture, such that the IC servos directly to average charge current. The LT3652 senses charger output voltage through a resistor divider via the V_{FB} pin. The difference between the voltage on this pin and an internal 3.3V voltage reference is integrated by the voltage error amplifier (V-EA). This amplifier generates an error voltage on its output (I_{TH}), which corresponds to the average current sensed across the inductor current sense resistor, R_{SENSE}, which is connected between the SENSE and BAT pins. The I_{TH} voltage is then divided down by a factor of 10, and imposed on the input of the current error amplifier (C-EA). The difference between this imposed voltage and the current sense resistor voltage is integrated, with the resulting voltage (V_C) used as a threshold that is compared against an internally generated ramp. The output of this comparison controls the charger's switch.

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The I_{TH} error voltage corresponds linearly to average current sensed across the inductor current sense resistor, allowing maximum charge current control by limiting the effective voltage range of I_{TH}. A clamp limits this voltage to 1V which, in turn, limits the current sense voltage to 100mV. This sets the maximum charge current, or the current delivered while the charger is operating in constant-current (CC) mode, which corresponds to 100mV across R_{SENSE}. The I_{TH} voltage is pulled down to reduce this maximum charge current should the voltage on the V_{IN_REG} pin falls below 2.7V ($V_{IN\_REG(TH)}$) or the die temperature approaches 125°C.

If the voltage on the V_{FB} pin is below 2.3V ($V_{FB(PRE)}$), the LT3652 engages precondition mode. During the precondition interval, the charger continues to operate in constant-current mode, but the maximum charge current is reduced to 15% of the maximum programmed value as set by R_{SENSE}.

When the charger output voltage approaches the float voltage, or the voltage on the V_{FB} pin approaches 3.3V ($V_{FB(FLT)}$), the charger transitions into constant-voltage (CV) mode and charge current is reduced from the maximum value. As this occurs, the I_{TH} voltage falls from the limit clamp and servos to lower voltages. The IC monitors the I_{TH} voltage as it is reduced, and detection of C/10 charge current is achieved when I_{TH} = 0.1V. If the charger is configured for C/10 termination, this threshold is used to terminate the charge cycle. Once the charge cycle is terminated, the $\overline{CHRG}$ status pin becomes high-impedance and the charger enters low-current standby mode.

The LT3652 contains an internal charge cycle timer that terminates a successful charge cycle after a programmed amount of time. This timer is typically programmed to achieve end-of-cycle (EOC) in 3 hours, but can be configured for any amount of time by setting an appropriate timing capacitor value (C_{TIMER}). When timer termination is used, the charge cycle does not terminate when C/10 is achieved. Because the $\overline{CHRG}$ status pin responds to the C/10 current level, the IC will indicate a fully-charged battery status, but the charger continues to source low currents into the battery until the programmed EOC time has elapsed, at which time the charge cycle will terminate. At EOC when the charging cycle terminates, if the battery did not achieve at least 97.5% of the full float voltage, charging is deemed unsuccessful, the LT3652 re-initiates, and charging continues for another full timer cycle.

Use of the timer function also enables bad-battery detection. This fault condition is achieved if the battery does not respond to preconditioning, such that the charger remains in (or enters) precondition mode after 1/8th of the programmed charge cycle time. A bad battery fault halts the charging cycle, the $\overline{CHRG}$ status pin goes high-impedance, and the $\overline{FAULT}$ pin is pulled low.

When the LT3652 terminates a charging cycle, whether through C/10 detection or by reaching timer EOC, the average current mode analog loop remains active, but the internal float voltage reference is reduced by 2.5%. Because the voltage on a successfully charged battery is at the full float voltage, the voltage error amp detects an over-voltage condition and I_{TH} is pulled low. When the voltage error amp output drops below 0.3V, the IC enters standby mode, where most of the internal circuitry is disabled, and the V_{IN} bias current is reduced to 85µA. When the voltage on the V_{FB} pin drops below the reduced float reference level, the output of the voltage error amp will climb, at which point the IC comes out of standby mode and a new charging cycle is initiated.

V_{IN} Input Supply

The LT3652 is biased directly from the charger input supply through the V_{IN} pin. This supply provides large switched currents, so a high-quality, low ESR decoupling capacitor is recommended to minimize voltage glitches on V_{IN}. The V_{IN} decoupling capacitor (C_{VIN}) absorbs all input switching

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ripple current in the charger, so it must have an adequate ripple current rating. RMS ripple current ($I_{CVIN(RMS)}$) is:

$$I_{CVIN(RMS)} \cong I_{CHG(MAX)} \bullet (V_{BAT}/V_{IN}) \bullet ([V_{IN}/V_{BAT}]-1)^{1/2},$$

where $I_{CHG(MAX)}$ is the maximum average charge current (100mV/R_{SENSE}). The above relation has a maximum at $V_{IN} = 2 \bullet V_{BAT}$, where:

$$I_{CVIN(RMS)} = I_{CHG(MAX)}/2$$

The simple worst-case of ½ • $I_{CHG(MAX)}$ is commonly used for design.

Bulk capacitance is a function of desired input ripple voltage (ΔV_{IN}), and follows the relation:

$$C_{IN(BULK)} = I_{CHG(MAX)} \bullet (V_{BAT}/V_{IN})/\Delta V_{IN}\ (\mu F)$$

Input ripple voltages above 0.1V are not recommended. 10µF is typically adequate for most charger applications.

Charge Current Programming

The LT3652 charger is configurable to charge at average currents as high as 2A. Maximum charge current is set by choosing an inductor sense resistor (R_{SENSE}) such that the desired maximum average current through that sense resistor creates a 100mV drop, or:

$$R_{SENSE} = 0.1/I_{CHG(MAX)}$$

where $I_{CHG(MAX)}$ is the maximum average charge current. A 2A charger, for example, would use a 0.05Ω sense resistor.

BOOST Supply

The BOOST bootstrapped supply rail drives the internal switch and facilitates saturation of the switch transistor. Operating range of the BOOST pin is 0V to 8.5V, as referenced to the SW pin. Connect a 1µF or greater capacitor from the BOOST pin to the SW pin.

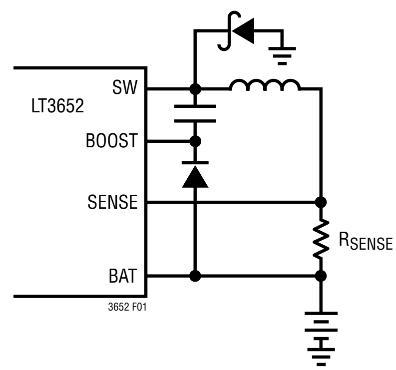

Figure 1. Programming Maximum Charge Current Using R_{SENSE}

The voltage on the decoupling capacitor is refreshed through a diode, with the anode connected to either the battery output voltage or an external source, and the cathode connected to the BOOST pin. Rate the diode average current greater than 0.1A, and reverse voltage greater than $V_{IN(MAX)}$.

To refresh the decoupling capacitor with a rectifying diode from the battery with battery float voltages higher than 8.4V, a >100mA Zener diode can be put in series with the rectifying diode to prevent exceeding the BOOST pin operating voltage range.

APPLICATIONS INFORMATION

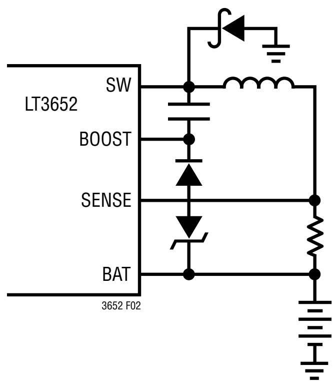

Figure 2. Zener Diode Reduces Refresh Voltage for BOOST Pin

V_{IN}/BOOST Start-Up Requirement

The LT3652 operates with a V_{IN} range of 4.95V to 32V, however, a start-up voltage requirement exists due to the nature of the non-synchronous step-down switcher topology used for the charger. If there is no BOOST supply available, the internal switch requires ($V_{IN} – V_{SW}$) ≥ 3.3V to reliably operate. This requirement does not exist if the BOOST supply is available and ($V_{BOOST} – V_{SW}$) > 2V.

When an LT3652 charger is not switching, the SW pin is at the same potential as the battery, which can be as high as $V_{BAT(FLT)}$. As such, for reliable start-up, the V_{IN} supply must be at least 3.3V above $V_{BAT(FLT)}$. Once switching begins and the BOOST supply capacitor gets charged such that ($V_{BOOST} – V_{SW}$) > 2V, the V_{IN} requirement no longer applies.

In low V_{IN} applications, the BOOST supply can be powered by an external source for start-up, eliminating the V_{IN} start-up requirement.

V_{BAT} Output Decoupling

An LT3652 charger output requires bypass capacitance connected from the BAT pin to ground (C_{BAT}). A 10µF ceramic capacitor is required for all applications. In systems where the battery can be disconnected from the charger output, additional bypass capacitance may be desired for visual indication for a no-battery condition (see the Status Pins section).

If it is desired to operate a system load from the LT3652 charger output when the battery is disconnected, additional bypass capacitance is required. In this type of application, excessive ripple and/or low amplitude oscillations can occur without additional output bulk capacitance. For these applications, place a 100µF low ESR non-ceramic capacitor (chip tantalum or organic semiconductor capacitors such as Sanyo OS-CONs or POSCAPs) from BAT to ground, in parallel with the 10µF ceramic bypass capacitor. This additional bypass capacitance may also be required in systems where the battery is connected to the charger with long wires. The voltage rating of C_{BAT} must meet or exceed the battery float voltage.

Inductor Selection

The primary criterion for inductor value selection in an LT3652 charger is the ripple current created in that inductor. Once the inductance value is determined, an inductor must also have a saturation current equal to or exceeding the maximum peak current in the inductor. An inductor value (L), given the desired amount of peak-to-peek inductor ripple current (ΔI_L) can be approximated using the relation:

$$L = \frac{\frac{10 \bullet R_{SENSE}}{\Delta I_L}}{I_{CHG(MAX)}} \bullet V_{BAT(FLT)} \bullet \left[1 - \frac{V_{BAT(FLT)}}{V_{IN(MAX)}}\right] \ (\mu H)$$

In the above relation, $V_{IN(MAX)}$ is the maximum operational voltage. Ripple current is typically set within a range of 25% to 35% of $I_{CHG(MAX)}$, so an inductor value can be determined by setting $0.25 < \Delta I_L/I_{CHG(MAX)} < 0.35$.

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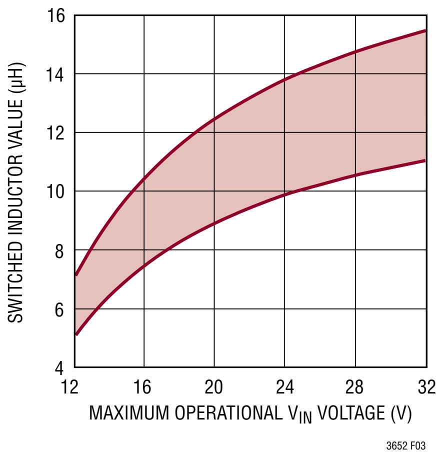

Figure 3. 7.2V at 1.5A Switched Inductor Values

Magnetics vendors typically specify inductors with maximum RMS and saturation current ratings. Select an inductor that has a saturation current rating at or above $(1+ \Delta I_{MAX}/2) \bullet I_{CHG(MAX)}$, and an RMS rating above $I_{CHG(MAX)}$. Inductors must also meet a maximum volt-second product requirement. If this specification is not in the data sheet of an inductor, consult the vendor to make sure the maximum volt-second product is not being exceeded by your design. The minimum required volt-second product is:

$$V_{BAT(FLT)} \bullet \left(1 - \frac{V_{BAT(FLT)}}{V_{IN(MAX)}}\right)(V \bullet \mu S)$$

Rectifier Selection

The rectifier diode from SW to GND, in a LT3652 battery charger provides a current path for the inductor current when the main power switch is disabled. The rectifier is selected based upon forward voltage, reverse voltage, and maximum current. A Schottky diode is required, as low forward voltage yields the lowest power loss and highest efficiency. The rectifier diode must be rated to withstand reverse voltages greater than the maximum V_{IN} voltage.

The minimum average diode current rating ($I_{DIODE(MAX)}$) is calculated with maximum output current ($I_{CHG(MAX)}$), maximum operational V_{IN}, and output at the precondition threshold ($V_{BAT(PRE)}$, or $0.7 \bullet V_{BAT(FLT)}$):

$$I_{DIODE(MAX)} > I_{CHG(MAX)} \bullet \frac{V_{IN(MAX)} - V_{BAT(PRE)}}{V_{IN(MAX)}} (A)$$

For example, a rectifier diode for a 7.2V, 2A charger with a 25V maximum input voltage would require:

$$I_{DIODE(MAX)} > 2A \bullet \frac{25V - 0.7(7.2V)}{25V}, \text{or}$$

$$I_{DIODE(MAX)} > 1.6A$$

Battery Float Voltage Programming

The output battery float voltage ($V_{BAT(FLT)}$) is programmed by connecting a resistor divider from the BAT pin to V_{FB}. $V_{BAT(FLT)}$ can be programmed up to 14.4V.

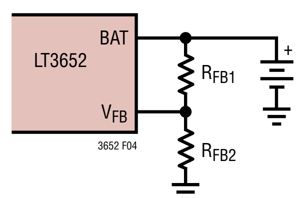

Figure 4. Feedback Resistors from BAT to V_{FB} Program Float Voltage

APPLICATIONS INFORMATION

Using a resistor divider with an equivalent input resistance at the V_{FB} pin of 250k compensates for input bias current error. Required resistor values to program desired $V_{BAT(FLT)}$ follow the equations:

$$R_{FB1} = (V_{BAT(FLT)} \cdot 2.5 \cdot 10^5)/3.3 \quad (\Omega)$$

$$R_{FB2} = (R_{FB1} \cdot (2.5 \cdot 10^5))/(R_{FB1} - (2.5 \cdot 10^5)) \quad (\Omega)$$

The charge function operates to achieve the final float voltage of 3.3V on the V_{FB} pin. The auto-restart feature initiates a new charging cycle when the voltage at the V_{FB} pin falls 2.5% below that float voltage.

Because the battery voltage is across the $V_{BAT(FLT)}$ programming resistor divider, this divider will draw a small amount of current from the battery (I_{RFB}) at a rate of:

$$I_{RFB} = 3.3/R_{FB2}$$

Precision resistors in high values may be hard to obtain, so for some lower $V_{BAT(FLT)}$ applications, it may be desirable to use smaller-value feedback resistors with an additional resistor (R_{FB3}) to achieve the required 250k equivalent resistance. The resulting 3-resistor network, as shown in Figure 5, can ease component selection and/or increase output voltage precision, at the expense of additional current through the feedback divider.

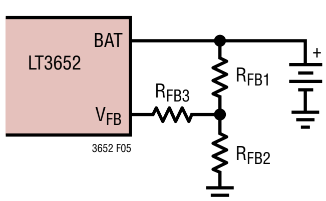

Figure 5. A Three-Resistor Feedback Network Can Ease Component Selection

For a three-resistor network, R_{FB1} and R_{FB2} follow the relation:

$$R_{FB2}/R_{FB1} = 3.3/(V_{BAT(FLT)} - 3.3)$$

Example:

For $V_{BAT(FLT)}$ = 3.6V:

R_{FB2}/R_{FB1} = 3.3/(3.6 - 3.3) = 11.

Setting divider current (I_{RFB}) = 10µA yields:

R_{FB2} = 3.3/10µA

R_{FB2} = 330k

Solving for R_{FB1}:

R_{FB1} = 330k/11

R_{FB1} = 30k

The divider equivalent resistance is:

$R_{FB1}||R_{FB2}$ = 27.5k

To satisfy the 250k equivalent resistance to the V_{FB} pin:

R_{FB3} = 250k – 27.5k

R_{FB3} = 223k.

Because the V_{FB} pin is a relatively high impedance node, stray capacitances at this pin must be minimized. Special attention should be given to any stray capacitances that can couple external signals onto the pin, which can produce undesirable output transients or ripple. Effects of parasitic capacitance can typically be reduced by adding a small-value (20pF to 50pF) feedforward capacitor from the BAT pin to the V_{FB} pin.

Extra care should be taken during board assembly. Small amounts of board contamination can lead to significant shifts in output voltage. Appropriate post-assembly board

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cleaning measures should be implemented to prevent board contamination, and low-leakage solder flux is recommended.

Input Supply Voltage Regulation

The LT3652 contains a voltage monitor pin that enables programming a minimum operational voltage. Connecting a resistor divider from V_{IN} to the V_{IN_REG} pin enables programming of minimum input supply voltage, typically used to program the peak power voltage for a solar panel. Maximum charge current is reduced when the V_{IN_REG} pin is below the regulation threshold of 2.7V.

If an input supply cannot provide enough power to satisfy the requirements of an LT3652 charger, the supply voltage will collapse. A minimum operating supply voltage can thus be programmed by monitoring the supply through a resistor divider, such that the desired minimum voltage corresponds to 2.7V at the V_{IN_REG} pin. The LT3652 servos the maximum output charge current to maintain the voltage on V_{IN_REG} at or above 2.7V.

Programming of the desired minimum voltage is accomplished by connecting a resistor divider as shown in Figure 6. The ratio of R_{IN1}/R_{IN2} for a desired minimum voltage ($V_{IN(MIN)}$) is:

$$R_{IN1}/R_{IN2} = (V_{IN(MIN)}/2.7) - 1$$

If the voltage regulation feature is not used, connect the V_{IN_REG} pin to V_{IN}.

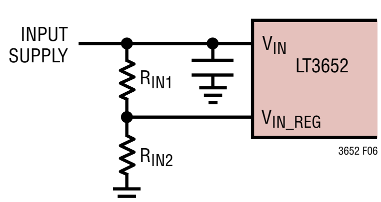

Figure 6. Resistor Divider Sets Minimum V_{IN}

MPPT Temperature Compensation

A typical solar panel is comprised of a number of series-connected cells, each cell being a forward-biased p-n junction. As such, the open-circuit voltage (V_{OC}) of a solar cell has a temperature coefficient that is similar to a common p-n diode, or about –2mV/°C. The peak power point voltage (V_{MP}) for a crystalline solar panel can be approximated as a fixed voltage below V_{OC}, so the temperature coefficient for the peak power point is similar to that of V_{OC}.

Panel manufacturers typically specify the 25°C values for V_{OC}, V_{MP}, and the temperature coefficient for V_{OC}, making determination of the temperature coefficient for V_{MP} of a typical panel straight forward.

The LT3652 employs a feedback network to program the V_{IN} input regulation voltage. Manipulation of the network makes for efficient implementation of various temperature compensation schemes for a maximum peak power tracking (MPPT) application. As the temperature characteristic for a typical solar panel V_{MP} voltage is highly linear, a

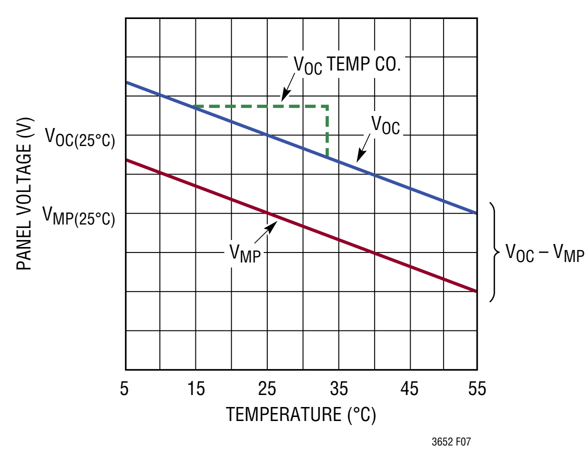

Figure 7. Temperature Characteristics for Solar Panel Output Voltage

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simple solution for tracking that characteristic can be implemented using an LM234 3-terminal temperature sensor. This creates an easily programmable, linear temperature dependent characteristic.

In the circuit shown in figure 8,

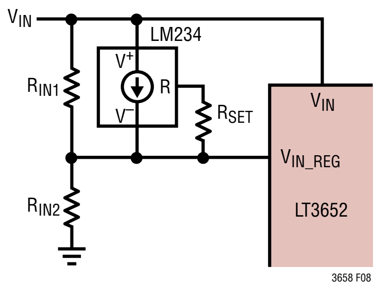

Figure 8. MPPT Temperature Compensation Network

$R_{IN1} = -R_{SET} \bullet (TC \bullet 4405)$, and

$R_{IN2} = R_{IN1}/(\{[V_{MP(25°C)} + R_{IN1} \bullet (0.0674/R_{SET})]/V_{IN\_REG}\} - 1)$

Where: TC = temperature coefficient (in V/°C), and $V_{MP(25°C)}$ = maximum power voltage at 25°C

For example, given a common 36-cell solar panel that has the following specified characteristics:

Open Circuit Voltage (V_{OC}) = 21.7V

Maximum Power Voltage (V_{MP}) = 17.6V

Open-Circuit Voltage Temperature Coefficient (V_{OC}) = –78mV/°C

As the temperature coefficient for V_{MP} is similar to that of V_{OC}, the specified temperature coefficient for V_{OC} (TC) of –78mV/°C and the specified peak power voltage ($V_{MP(25°C)}$) of 17.6V can be inserted into the equations to calculate the appropriate resistor values for the temperature compensation network in Figure 8. With R_{SET} equal to 1000Ω, then:

R_{SET} = **1k**

R_{IN1} = –1k • (–0.078 • 4405) = **344k**

R_{IN2} = 344k/({[17.6 + 344k • (0.0674/1k)]/2.7} – 1) = **24.4k**

Battery Voltage Temperature Compensation

Some battery chemistries have charge voltage requirements that vary with temperature. Lead-acid batteries in particular experience a significant change in charge voltage requirements as temperature changes. For example, manufacturers of large lead-acid batteries recommend a float charge of 2.25V/cell at 25°C. This battery float voltage, however, has a temperature coefficient which is typically specified at –3.3mV/°C per cell.

In a manner similar to the MPPT temperature correction outlined previously, implementation of linear battery charge voltage temperature compensation can be accomplished by incorporating an LM234 into the output feedback network.

For example, a 6-cell lead acid battery has a float charge voltage that is commonly specified at 2.25V/cell at 25°C, or 13.5V, and a –3.3mV/°C per cell temperature coefficient,

APPLICATIONS INFORMATION

or –19.8mV/°C. Using the feedback network shown in Figure 9, with the desired temperature coefficient (TC) and 25°C float voltage ($V_{FLOAT(25°C)}$) specified, and using a convenient value of 2.4k for R_{SET}, necessary resistor values follow the relations:

R_{FB1} = $-R_{SET}$ • (TC • 4405)

= –2.4k • (–0.0198 • 4405) = **210k**

R_{FB2} = R_{FB1} / ({[$V_{FLOAT(25°C)}$ + R_{FB1} • (0.0674/ R_{SET})]/ V_{FB}} – 1)

= 210k/({[13.5 + 210k • (0.0674/2.4k)]/3.3} – 1) = **43k**

R_{FB3} = 250k - R_{FB1}||R_{FB2}

= 250k – 210k||43k = **215k** (see the Battery Float Voltage Programming section)

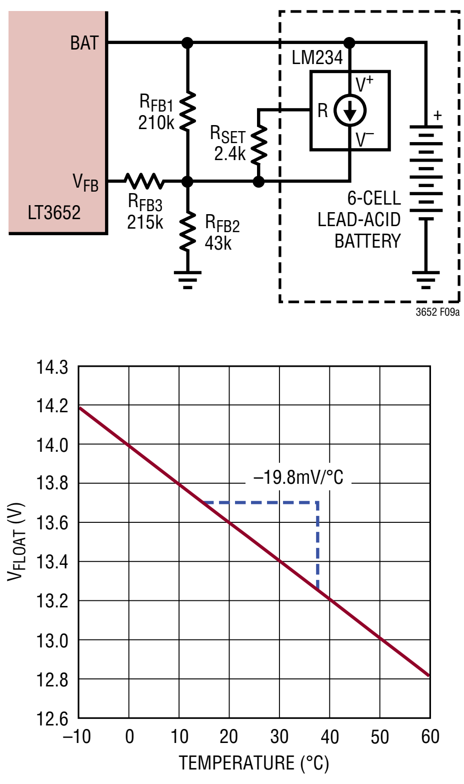

Figure 9. Lead-Acid 6-Cell Float Charge Voltage vs Temperature Has –19.8mV/°C Characteristic Using LM234 with Feedback Network

While the circuit in Figure 9 creates a linear temperature characteristic that follows a typical –3.3mV/°C per cell lead-acid specification, the theoretical float charge voltage characteristic is slightly nonlinear. This nonlinear characteristic follows the relation $V_{FLOAT(1\text{-}CELL)} = 4 \times 10^{-5} (T^2) - 6 \times 10^{-3}(T) + 2.375$ (with a 2.18V minimum), where T = temperature in °C. A thermistor-based network can be used to approximate the nonlinear ideal temperature characteristic across a reasonable operating range, as shown in Figure 10.

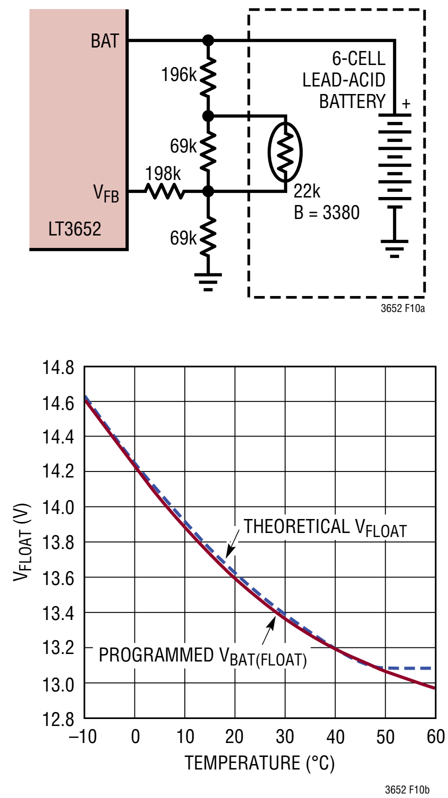

Figure 10. Thermistor-Based Temperature Compensation Network Programs V_{FLOAT} to Closely Match Ideal Lead-Acid Float Charge Voltage for 6-Cell Charger

APPLICATIONS INFORMATION

Status Pins

The LT3652 reports charger status through two open collector outputs, the $\overline{CHRG}$ and $\overline{FAULT}$ pins. These pins can accept voltages as high as V_{IN}, and can sink up to 10mA when enabled.

The $\overline{CHRG}$ pin indicates that the charger is delivering current at greater that a C/10 rate, or 1/10th of the programmed maximum charge current. The $\overline{FAULT}$ pin signals bad battery and NTC faults. These pins are binary coded, and signal following the table below, where *ON* indicates pin pulled low, and *OFF* indicates pin high-impedance:

STATUS PINS STATE		
$\overline{CHRG}$	$\overline{FAULT}$	CHARGER STATUS
OFF	OFF	Not Charging — Standby or Shutdown Mode
OFF	ON	Bad Battery Fault (Precondition Timeout/EOC Failure)
ON	OFF	Normal Charging at C/10 or Greater
ON	ON	NTC Fault (Pause)

If the battery is removed from an LT3652 charger that is configured for C/10 termination, a sawtooth waveform of approximately 100mV appears at the charger output, due to cycling between termination and recharge events, This cycling results in pulsing at the $\overline{CHRG}$ output. An LED connected to this pin will exhibit a blinking pattern, indicating to the user that a battery is not present. The frequency of this blinking pattern is dependent on the output capacitance.

C/10 Termination

The LT3652 supports a low-current based termination scheme, where a battery charge cycle terminates when the current output from the charger falls to below one-tenth of the maximum current, as programmed with R_{SENSE}. The C/10 threshold current corresponds to 10mV across R_{SENSE}. This termination mode is engaged by shorting the TIMER pin to ground.

When C/10 termination is used, a LT3652 charger will source battery charge current as long as the average current level remains above the C/10 threshold. As the full-charge float voltage is achieved, the charge current falls until the C/10 threshold is reached, at which time the charger terminates and the LT3652 enters standby mode. The $\overline{CHRG}$ status pin follows the charger cycle, and is high impedance when the charger is not actively charging.

When V_{BAT} drops below 97.5% of the full-charged float voltage, whether by battery loading or replacement of the battery, the charger automatically re-engages and starts charging.

There is no provision for bad battery detection if C/10 termination is used.

Timer Termination

The LT3652 supports a timer based termination scheme, in which a battery charge cycle is terminated after a specific amount of time elapses. Timer termination is engaged when a capacitor (C_{TIMER}) is connected from the TIMER pin to ground. The timer cycle EOC (T_{EOC}) occurs based on C_{TIMER} following the relation:

$$C_{TIMER} = T_{EOC} \bullet 2.27 \times 10^{-7} \qquad \text{(Hours)}$$

Timer EOC is typically set to 3 hours, which requires a 0.68µF capacitor.

The $\overline{CHRG}$ status pin continues to signal charging at a C/10 rate, regardless of what termination scheme is used. When timer termination is used, the $\overline{CHRG}$ status pin is pulled low during a charging cycle until the charger output current falls below the C/10 threshold. The charger continues to top-off the battery until timer EOC, when the LT3652 terminates the charging cycle and enters standby mode.

Termination at the end of the timer cycle only occurs if the charging cycle was successful. A successful charge cycle is when the battery is charged to within 2.5% of the

APPLICATIONS INFORMATION

full-charge float voltage. If a charge cycle is not successful at EOC, the timer cycle resets and charging continues for another full timer cycle.

When V_{BAT} drops below 97.5% of the full-charge float voltage, whether by battery loading or replacement of the battery, the charger automatically reengages and starts charging.

Preconditioning and Bad Battery Fault

A LT3652 has a precondition mode, where charge current is limited to 15% of the programmed $I_{CHG(MAX)}$, as set by R_{SENSE}. The precondition current corresponds to 15mV across R_{SENSE}.

Precondition mode is engaged while the voltage on the V_{FB} pin is below the precondition threshold (2.3V, or 0.7 • $V_{BAT(FLT)}$). Once the V_{FB} voltage rises above the precondition threshold, normal full-current charging can commence. The LT3652 incorporates 70mV of threshold hysteresis to prevent mode glitching.

When the internal timer is used for termination, bad battery detection is engaged. There is no provision for bad battery detection if C/10 termination is used. A bad battery fault is triggered when the voltage on V_{FB} remains below the precondition threshold for greater than 1/8 of a full timer cycle (1/8 EOC). A bad battery fault is also triggered if a normally charging battery re-enters precondition mode after 1/8 EOC.

When a bad battery fault is triggered, the charging cycle is suspended, so the $\overline{\text{CHRG}}$ status pin becomes high-impedance. The $\overline{\text{FAULT}}$ pin is pulled low to signal a fault detection.

Cycling the charger's power or $\overline{\text{SHDN}}$ function initiates a new charging cycle, but a LT3652 charger does not require a reset. Once a bad battery fault is detected, a new timer charging cycle initiates when the V_{FB} pin exceeds the precondition threshold voltage. During a bad battery fault, 0.5mA is sourced from the charger, so removing the failed battery allows the charger output voltage to rise and initiate a charge cycle reset. As such, removing a bad battery resets the LT3652, so a new charge cycle is started by connecting another battery to the charger output.

Battery Temperature Monitor and Fault

The LT3652 can accommodate battery temperature monitoring by using an NTC (negative temperature co-efficient) thermistor close to the battery pack. The temperature monitoring function is enabled by connecting a 10kΩ, B = 3380 NTC thermistor from the NTC pin to ground. If the NTC function is not desired, leave the pin unconnected.

The NTC pin sources 50μA, and monitors the voltage dropped across the 10kΩ thermistor. When the voltage on this pin is above 1.36V (0°C) or below 0.29V (40°C), the battery temperature is out of range, and the LT3652 triggers an NTC fault. The NTC fault condition remains until the voltage on the NTC pin corresponds to a temperature within the 0°C to 40°C range. Both hot and cold thresholds incorporate hysteresis that correspond to 5°C.

If higher operational charging temperatures are desired, the temperature range can be expanded by adding series resistance to the 10k NTC resistor. Adding a 0.91k resistor will increase the effective hot temperature to 45°C.

During an NTC fault, charging is halted and both status pins are pulled low. If timer termination is enabled, the timer count is suspended and held until the fault condition is relieved.

Thermal Foldback

The LT3652 contains a thermal foldback protection feature that reduces maximum charger output current if the IC junction temperature approaches 125°C. In most cases, on-chip temperatures servo such that any excessive temperature conditions are relieved with only slight reductions in maximum charger current.

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In some cases, the thermal foldback protection feature can reduce charger currents below the C/10 threshold. In applications that use C/10 termination (TIMER=0V), the LT3652 will suspend charging and enter standby mode until the excessive temperature condition is relieved.

Layout Considerations

The LT3652 switch node has rise and fall times that are typically less than 10nS to maximize conversion efficiency. The switch node (Pin SW) trace should be kept as short as possible to minimize high frequency noise. The input capacitor (C_{IN}) should be placed close to the IC to minimize this switching noise. Short, wide traces on these nodes also help to avoid voltage stress from inductive ringing. The BOOST decoupling capacitor should also be in close proximity to the IC to minimize inductive ringing. The SENSE and BAT traces should be routed together, and these and the V_{FB} trace should be kept as short as possible. Shielding these signals from switching noise with a ground plane is recommended.

High current paths and transients should be kept isolated from battery ground, to assure an accurate output voltage reference. Effective grounding can be achieved by considering switched current in the ground plane, and careful component placement and orientation can effectively steer these high currents such that the battery reference does not get corrupted. Figure 11 illustrates an effective grounding scheme using component placement to control ground currents. When the switch is enabled (loop #1), current flows from the input bypass capacitor (C_{IN}) through the switch and inductor to the battery positive terminal. When the switch is disabled (loop #2), the current to the battery positive terminal is provided from ground through the freewheeling Schottky diode (D_F). In both cases, these switch currents return to ground via the output bypass capacitor (C_{BAT}).

The LT3652 packaging has been designed to efficiently remove heat from the IC via the Exposed Pad on the backside of the package, which is soldered to a copper footprint on the PCB. This footprint should be made as large as possible to reduce the thermal resistance of the IC case to ambient air.

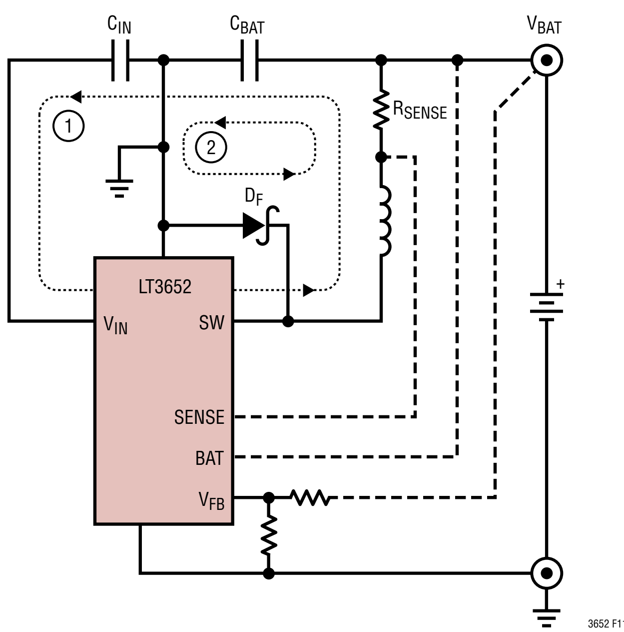
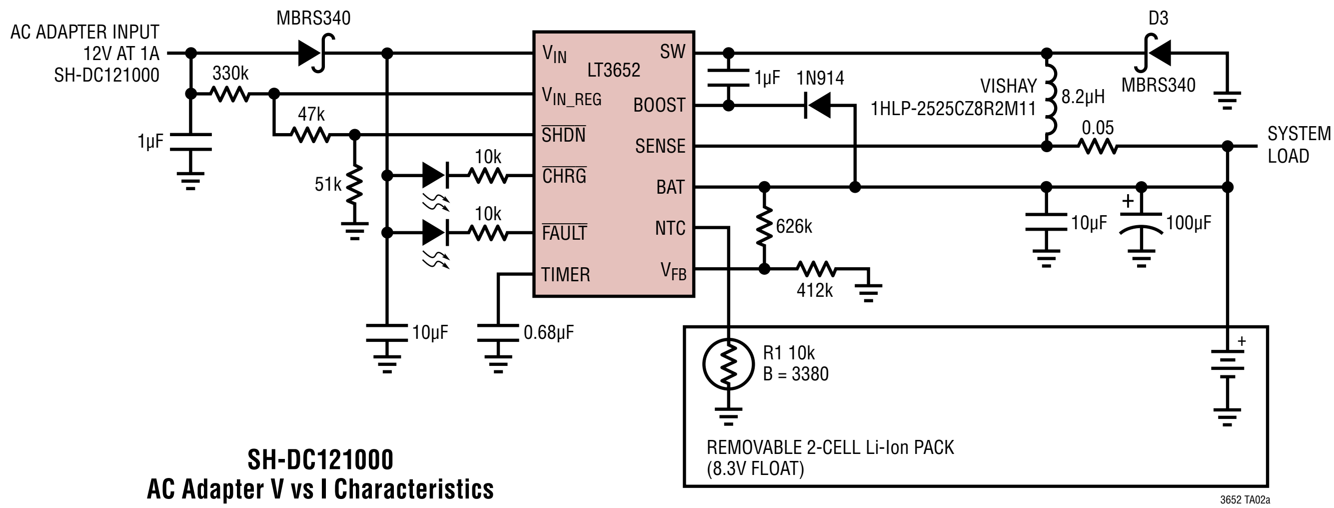


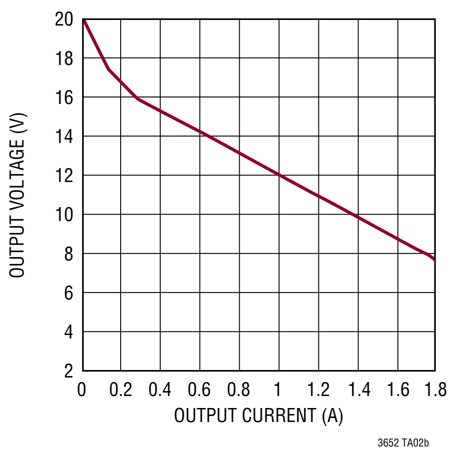
Figure 11. Component Orientation Isolates High Current Paths from Sensitive Nodes

TYPICAL APPLICATIONS

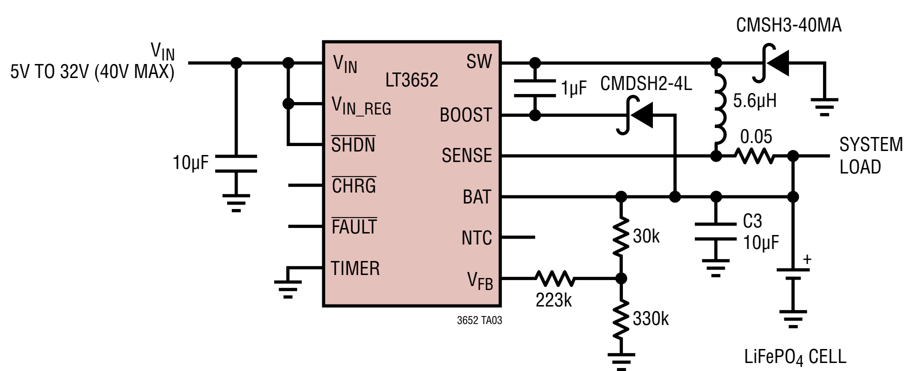
2-Cell Li-Ion Charger (8.3V at 2A) With 3 Hour Timer Termination Powered by Inexpensive 12V at 1A Unregulated Wall Adapter; V_{IN_REG} Loop Servos Maximum Charge Current to Prevent AC Adapter Output from Drooping Lower than 12V



SH-DC121000
AC Adapter V vs I Characteristics



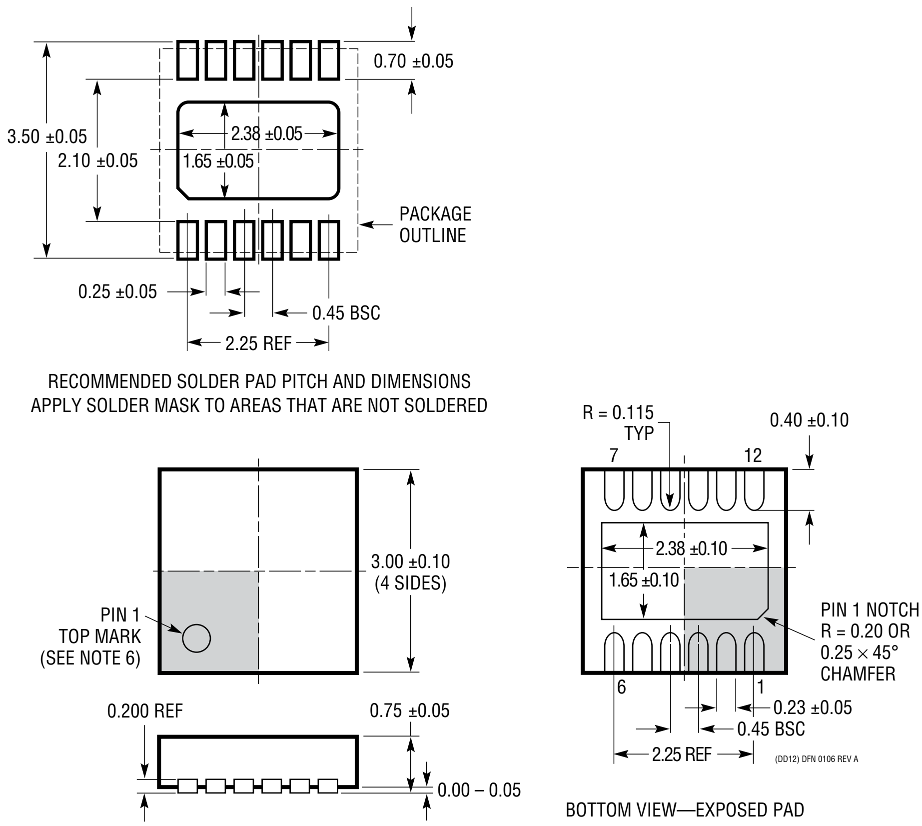
Basic 2A 1-Cell $LiFePO_4$ Charger (3.6V Float) With C/10 Termination



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT3652#packaging for the most recent package drawings.

DD Package
12-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1725 Rev A)

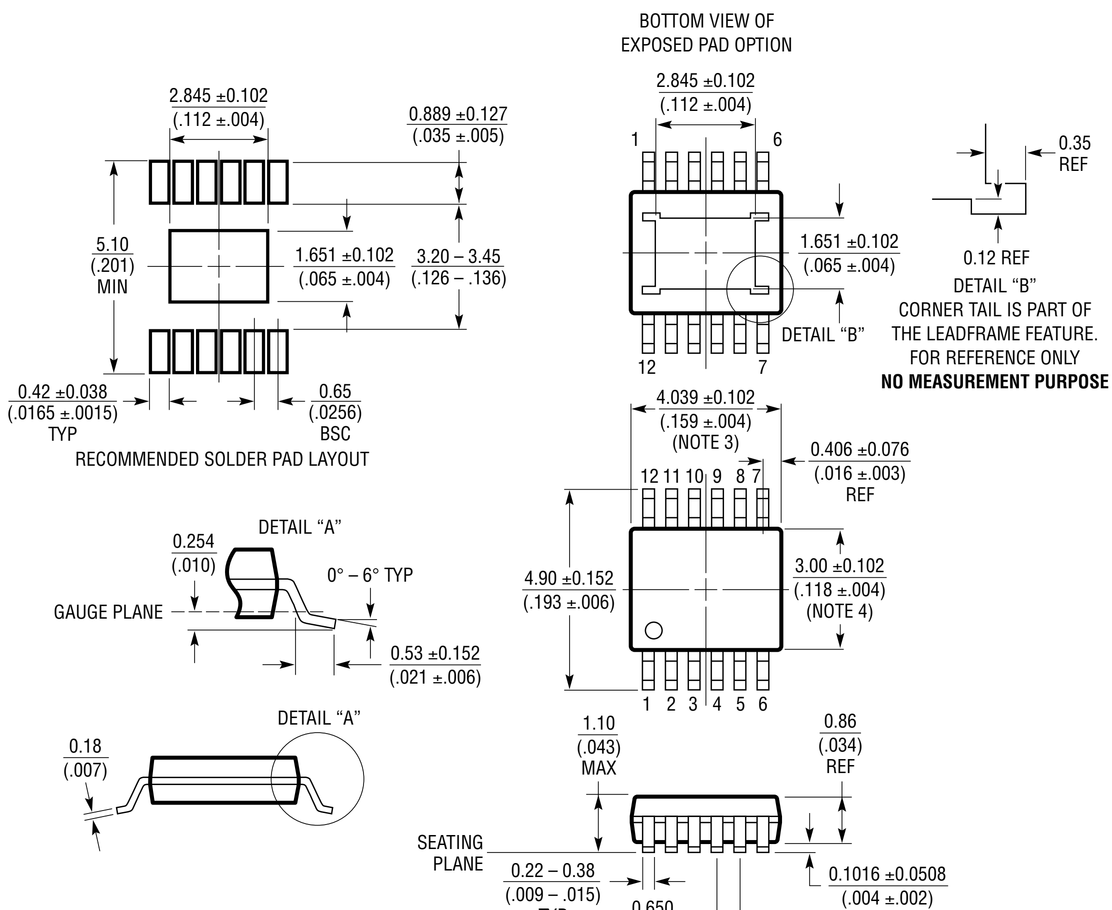


NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD AND TIE BARS SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT3652#packaging for the most recent package drawings.

MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev G)



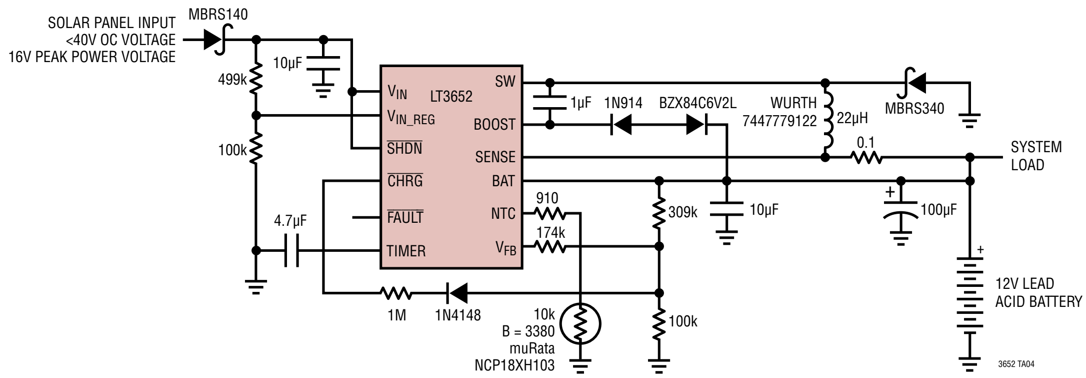
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	2/10	Add MSOP-12 Package	1, 2, 24
C	5/10	Corrected $\overline{SHDN}$ Pin Labels	3, 4
D	12/12	Removed reference to Nickel cell charging capability	1
		Added new Battery Bias Current curve	6
E	12/15	Enhanced Pin Configuration	2
		Added Note 2 to top of Electrical Characteristics	3, 4
		Enhanced Note 2	4
		Changed name of Pin 13	8
		Modified Inductor Selection section	13
		Modified Battery Float Voltage Programming equations	15

TYPICAL APPLICATION

1A Solar Panel Powered 3-Stage 12V Lead-Acid Fast/Float Charger; 1A Charger Fast Charges with CC/CV Characteristics Up to 14.4V; When Charge Current Falls to 0.1A Charger Switches to 13.5V Float Charge Mode; Charger Re-Initiates 14.4V Fast Charge Mode if Battery Voltage Falls Below 13.2V and Trickle Charges at 0.15A if Battery Voltage is Below 10V; 0°C to 45°C Battery Temperature Charging Range



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3650-8.2/LT3650-8.4	Monolithic 2A Switch Mode 2-Cell Li-Ion Battery Charger	Standalone, 9V ≤ V_{IN} ≤ 32V (40V Absolute Maximum), 1MHz, 2A Programmable Charge Current, Timer or C/10 Termination, Small and Few External Components, 3mm × 3mm DFN12 Package, –8.2 for 2 × 4.1V Float Voltage Batteries, –8.4 for 2 × 4.2V Float Voltage Batteries
LTC4001/LTC4001-1	Monolithic 2A Switch Mode Synchronous Li-Ion Battery Charger	Standalone, 4V ≤ V_{IN} ≤ 5.5V (6V Absolute Maximum, 7V Transient), 1.5MHz, Synchronous Rectification Efficiency >90%, Adjustable Timer Termination, Small and Few External Components, 4mm × 4mm QFN-16 Package –1 for 4.1V Float Voltage Batteries
LTC4002	Switch Mode Lithium-Ion Battery Charger	Standalone, 4.7V ≤ V_{IN} ≤ 24V, 500kHz Frequency, 3 Hour Charge Termination
LTC4006	Small, High Efficiency, Fixed Voltage, Lithium-Ion Battery Charger with Termination and Thermistor Sensor	Complete Charger for 3- or 4-Cell Li-Ion Batteries, AC Adapter Current Limit, 16-Pin Narrow SSOP Package
LTC4007	High Efficiency, Programmable Voltage Battery Charger with Termination	Complete Charger for 3- or 4-Cell Li-Ion Batteries, AC Adapter Current Limit, Thermistor Sensor and Indicator Outputs
LTC4008	4A, High Efficiency, Multi-Chemistry Battery Charger	Constant-Current/Constant-Voltage Switching Regulator Charger, Resistor Voltage/Current Programming, AC Adapter Current Limit and Thermistor Sensor and Indicator Outputs
LTC4012/LTC4012-1/ LTC4012-2/ LTC4012-3	4A, High Efficiency, Multi-Chemistry Battery Charger with PowerPath™ Control	PowerPath Control, Constant-Current/Constant-Voltage Switching Regulator Charger, Resistor Voltage/Current Programming, AC Adapter Current Limit and Thermistor Sensor and Indicator Outputs 1 to 4 Cell Li, Up to 18 Cell Ni, SLA and Supercap Compatible; 4mm × 4mm QFN-20 Package –1 Version for 4.1V Li Cells, –2 Version for 4.2V Li Cells, –3 Version has Extra GND Pin
LTC4015	Multichemistry Buck Battery Charger Controller with Digital Telemetry System	Multichemistry Li-Ion/Polymer, $LiFePO_4$, or Lead-Acid Battery Charger with Termination, Digital Telemetry System Monitors V_{BAT}, I_{BAT}, R_{BAT}, NTC Ratio (Battery Temperature), V_{IN}, I_{IN}, V_{SYSTEM}, Die Temperature, Coulomb Counter and Integrated 14-Bit ADC, Maximum Power Point Tracking, Wide Charging Input Voltage Range: 4.5V to 35V, Wide Battery Voltage Range: Up to 35V, 5mm × 7mm QFN-38 Package
LTC4020	55V Buck-Boost Multi-Chemistry Battery Charger	Wide Voltage Range: 4.5V to 55V Input, Up to 55V Output (60V Absolute Maximums), Synchronous Buck-Boost DC/DC Controller, Li-Ion and Lead-Acid Charge Algorithms, Input Voltage Regulation for High Impedance Input Supplies and Solar Panel Peak Power Operation, Low Profile (0.75mm) 38-Pin 5mm × 7mm QFN Package

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U-510 **Using the bq2031 to Charge Lead-Acid Batteries**

U-510 Using the bq2031 to Charge Lead-Acid Batteries

Description of Operation

The bq2031 has two primary functions: lead-acid battery charge control and switch-mode power conversion control. Figure 1 is a block diagram of the bq2031. The charge control circuitry is capable of a variety of full-charge detection techniques and supports three different charging algorithms. The Pulse-Width Modulator (PWM) provides control for high-efficiency current and voltage regulation.

Starting a Charge Cycle and Battery Qualification

When V_{CC} becomes valid (rises past its minimum value), the first activates battery temperature monitoring. Temperature is indicated by the voltage between the pins TS and SNS (V_{TEMP}). If the bq2031 finds the temperature out of range (or the thermistor is absent), it enters the Charge Pending State. In this state, all timers are suspended, charging current is kept off by MOD being held low, and the state is annunciated by LED_3 alternating high and low at approximately 1/6th second intervals.

Temperature checks remain active throughout the charge cycle. They are masked only when the bq2031 is in the Fault state (see below). When the temperature returns to the allowed charging range, timers are restarted (not reset) and the bq2031 returns to the state it was in when the temperature fault occurred.

When the thermistor is present and the temperature is within the allowed range, the bq2031 then checks for the presence of a battery. If the voltage between the BAT and SNS pins (V_{CELL}) is between the Low-Voltage Cut-Off threshold (V_{LCO}) and the High-Voltage Cut-Off (V_{HCO}), the bq2031 perceives a battery to be present and begins pre-charge battery qualification after a 500ms (typical) delay. If any new temperature or voltage faults occur during this time, the bq2031 immediately transitions to the appropriate state.

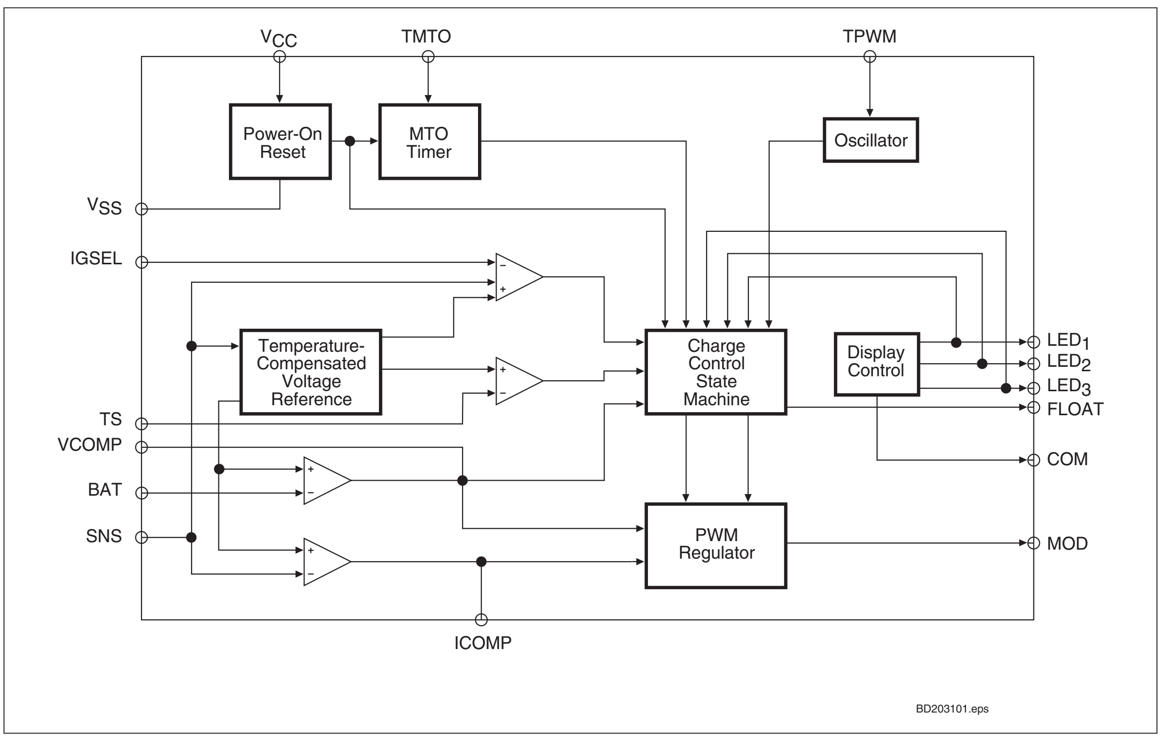

Figure 1. Block Diagram of the bq2031

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If V_{CELL} is less than V_{LCO} or above V_{HCO}, the bq2031 believes no battery is present and enters the Fault state; MOD is held low and LED_3 is turned on. This light gives the customer an indication that the charger is on, even though no battery is present. The bq2031 leaves the Fault state only if it sees V_{BAT} rise past V_{LCO} or fall past V_{HCO}, indicating a new battery insertion. If temperature is within bounds, there will again be a 500ms delay before battery qualification tests start.

Battery Qualification Tests

In test 1, the bq2031 attempts to regulate a voltage = V_{FLT} + 0.25V across the battery pack. The bq2031 monitors the time required for ISNS, the charging current, to rise to $I_{COND} = I_{MAX}/5$. If the current fails to rise to this level before the time-out period t_{QT1} expires (e.g., the battery has failed open), the bq2031 enters the Fault state, indicated by the LED_3 pin going high. Charging current is removed from the battery by driving the MOD pin low, and the bq2031 remains in this state until it detects the conditions to start a new charge cycle; the battery is replaced or V_{CC} is cycled off and then back on.

If test 1 passes, the bq2031 starts test 2 by attempting to regulate a charging current of I_{COND} into the battery pack. It monitors the time required for the pack voltage to rise above V_{MIN} (the voltage may already be over this limit). If the voltage fails to rise to this level before the time out period t_{QT2} expires (e.g., the battery has failed short), the bq2031 again enters the Fault state as described above. If test 2 passes, the bq2031 then begins fast (bulk) charging.

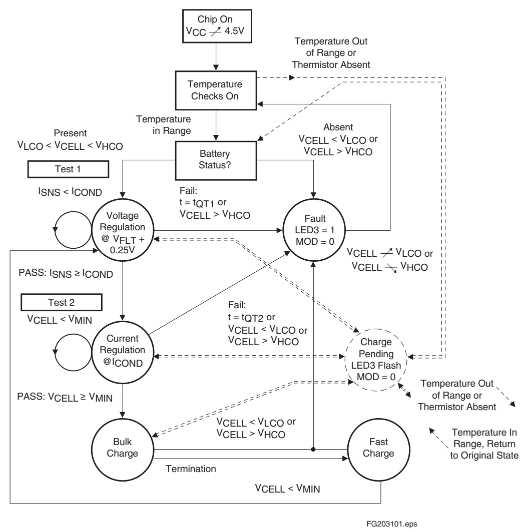

Figure 2. Cycle Start/Battery Qualification State Diagram

Fast Charging

The user configures the bq2031 for one of three fast charge and maintenance algorithms.

Two-Step Voltage (Figure 3)

This algorithm consists of three phases:

- Fast-Charge phase 1: The charging current is limited at I_{MAX} until the cell voltage rises to V_{BLK}.
- Fast-Charge phase 2: The charging voltage is regulated at V_{BLK} until the charging current drops below I_{MIN}.
- Maintenance phase: The charging voltage is regulated at V_{FLT}.

Two-Step Current (Figure 4)

This algorithm consists of two phases:

- Fast-Charge phase: The charging current is regulated at I_{MAX} until the cell voltage rises to V_{BLK} **or** the "Second Difference" of cell voltage drops below -8mV while V_{BAT} is over 2.0V. Second Difference is the accumulated differences between successive samples of V_{BAT}. The Second Difference technique looks for a negative change in battery voltage as the battery begins overcharging (see Figure 6).
- Maintenance phase: Fixed-width pulses of charging current = I_{COND} are modulated in frequency to achieve an average value of I_{MIN}. See Appendix A for implementation details.

Pulsed Current (Figure 5)

This algorithm consists of two phases:

- Fast-Charge phase: The charging current is regulated at I_{MAX} until the cell voltage rises to V_{BLK}.
- Maintenance phase: Charging current is removed until the battery voltage falls to V_{FLT}; charging current is then restored and regulated at I_{MAX} until the battery voltage once again rises to V_{BLK}. This cycle is repeated indefinitely.

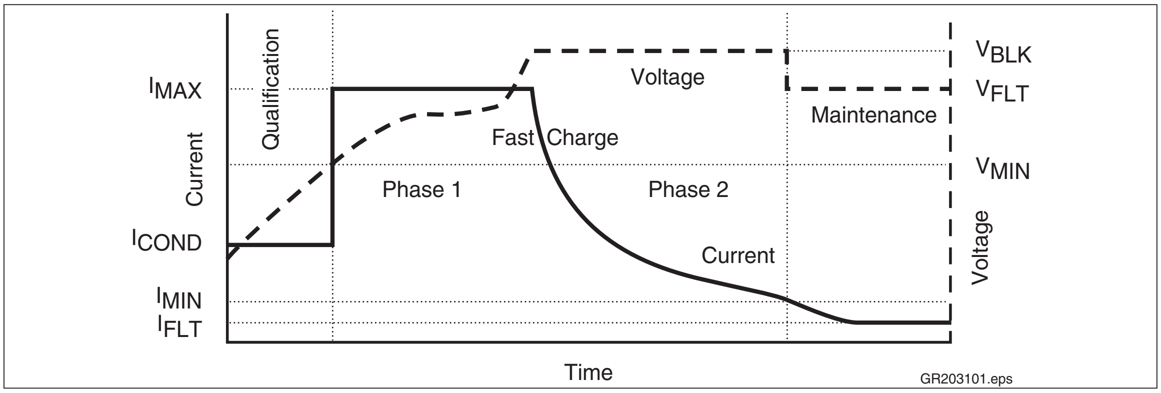

Figure 3. Two-Step Voltage Algorithm

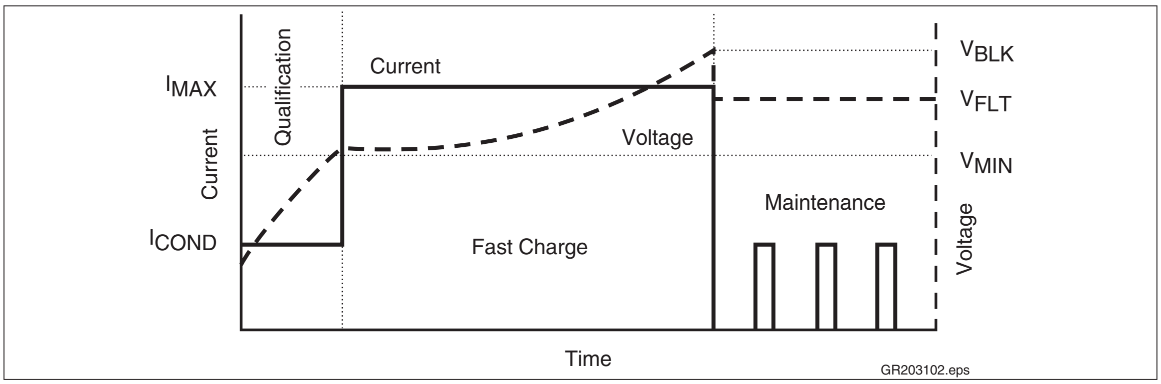

Figure 4. Two-Step Current Algorithm

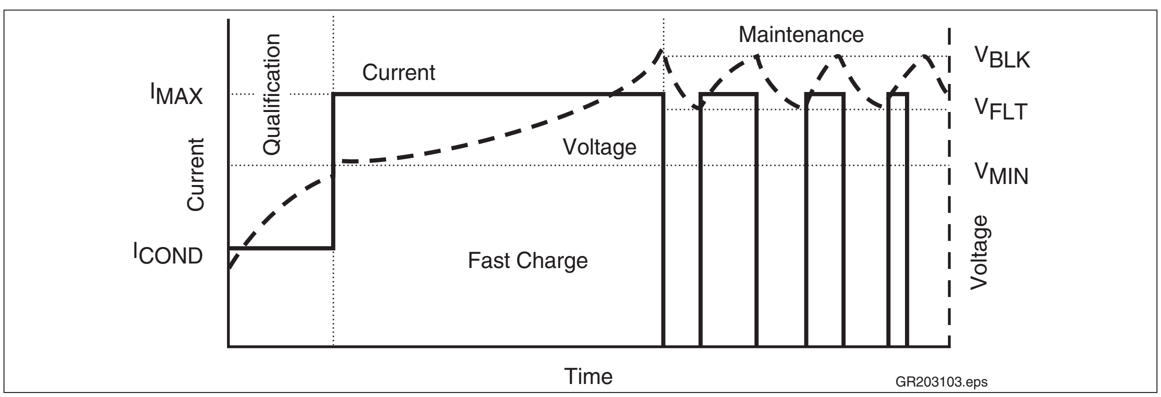

Figure 5. Pulsed Current Algorithm

Safety Time-Out

A safety timer limits the time the charger can spend in any phase of the charging cycle except maintenance. This Maximum Time-Out (MTO) timer is reset at the end of successful pre-charge qualification when the bq2031 begins fast charging1. If MTO times out before a fast charge termination criterion is met, the charging current is turned off (MOD driven low) and the bq2031 enters the Fault state exactly as if it had failed a pre-charge qualification test.

There is one exception. In the Two-Step Voltage algorithm, MTO is reset when the bq2031 transitions from the current-limited phase 1 to the voltage-regulated phase 2 of fast charging. If MTO expires while the bq2031 is still in phase 1, it does not enter the Fault state but instead transitions to maintenance phase.

During maintenance, the MTO timer is reset at the beginning of each new pulse in the Two-Step Current and Pulsed Current algorithms. It expires (and puts the bq2031 in the Fault state) only when the bq2031 beccomes "jammed" with a pulse stuck "on." The MTO timer is not active during the maintenance phase of the Two-Step Voltage algorithm.

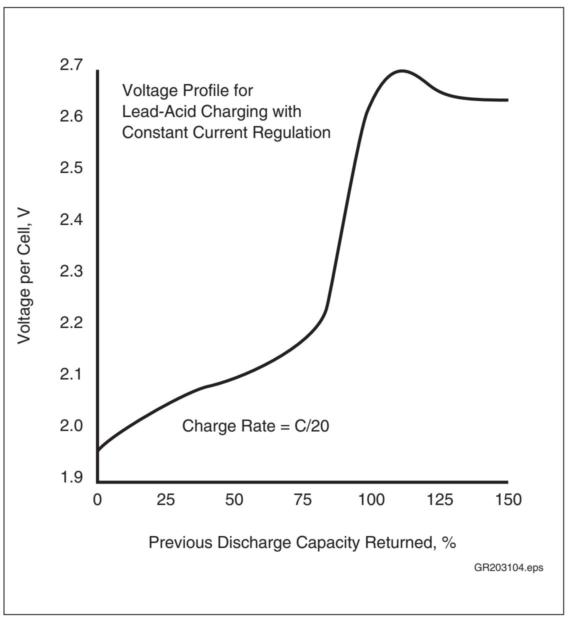

Figure 6. Voltage Roll-Off in Constant-Current Charging Profile

Hold-off Periods

Old age and/or abuse can create conditions in lead-acid batteries that may generate a large transient voltage spike when current-regulated charging is first applied. This spike could cause early termination in the fast charge algorithms by mimicking their voltage-based termination criteria. To prevent this, the bq2031 uses a "hold-off" period at the beginning of the fast charge phase. During this time, all voltage criteria are ignored except cutoff voltages. (Straying outside the range between V_{HCO} and V_{LCO} still causes the bq2031 to believe the battery has been removed, and the bq2031 enters the Fault state and shuts off charging current.) A hold-off period is also enforced during test 2 of pre-charge qualification for the same reason.

Configuration Instructions

Selecting Charge Algorithm and Display Mode

QSEL/LED_3, DSEL/LED_2, and TSEL/LED_1 are bi-directional pins with two functions: they are LED driver pins as outputs and programming pins for the bq2031 as inputs. The selection of pull-up, pull-down, or no pull resistor for these pins programs the charging algorithm on QSEL and TSEL per Table 1 and the display mode on DSEL per Table 2. The bq2031 forces the output driver on these bi-directional pins to their high-impedance state (as well as their common return output pin, COM) and latches the programming data sensed on the inputs when any one of the following three events occurs:

1. V_{CC} rises to a valid level.
2. The bq2031 leaves the Fault state.
3. The bq2031 detects battery insertion.

The LEDs go blank for approximately 0.75s. (typical) while new programming data is latched.

Figure 7 shows the bq2031 configured for the Two-Step Current algorithm and display mode 2.

Table 1. Programming Charge Algorithms

Charge Algorithms	QSEL	TSEL	Programmable Thresholds
Two-Step Voltage	L	H/L*	I_{MAX}, V_{BLK}, V_{FLT}
Two-Step Current	H	L	I_{MAX}, V_{BLK}, I_{MIN}
Pulsed Current	H	H	I_{MAX}, V_{BLK}, V_{FLT}

Note: * Set either high or low; do not float pin.

1 The MTO timer also resets at the beginning of the pre-charge qualification period. However, t_{QT1} or t_{QT2} (the qualification test time limits) expire and put the bq2031 in the Fault state before the MTO limit can be reached. The MTO timer is suspended while the bq2031 is in the Fault state, and is reset by the conditions that allow the bq2031 to exit that state.

Table 2. bq2031 Display Output Summary

Mode	Charge State	LED_1	LED_2	LED_3
DSEL = 0 (Mode 1)	Battery absent	Low	Low	High
	Pre-charge qualification	Flash*	Low	Low
	Fast charging	High	Low	Low
	Maintenance charging	Low	High	Low
	Charge pending (temperature out of range)	X	X	Flash*
	Fault	X	X	High
DSEL = 1 (Mode 2)	Battery absent	Low	Low	High
	Pre-charge qualification	High	High	Low
	Fast charge	Low	High	Low
	Maintenance charging	High	Low	Low
	Charge pending (temperature out of range)	X	X	Flash*
	Fault	X	X	High
DSEL = Float (Mode 3)	Pre-charge qualification	Flash*	Flash*	Low
	Battery absent	Low	Low	High
	Fast charge: current regulation	Low	High	Low
	Fast charge: voltage regulation	High	High	Low
	Maintenance charging	High	Low	Low
	Charge pending (temperature out of range)	X	X	Flash*
	Fault	X	X	High

Notes: 1 = V_{CC}, 0 = V_{SS}, X = LED state when fault occurred.
* Flash = $\frac{1}{6}$ sec. low, $\frac{1}{6}$ sec. high

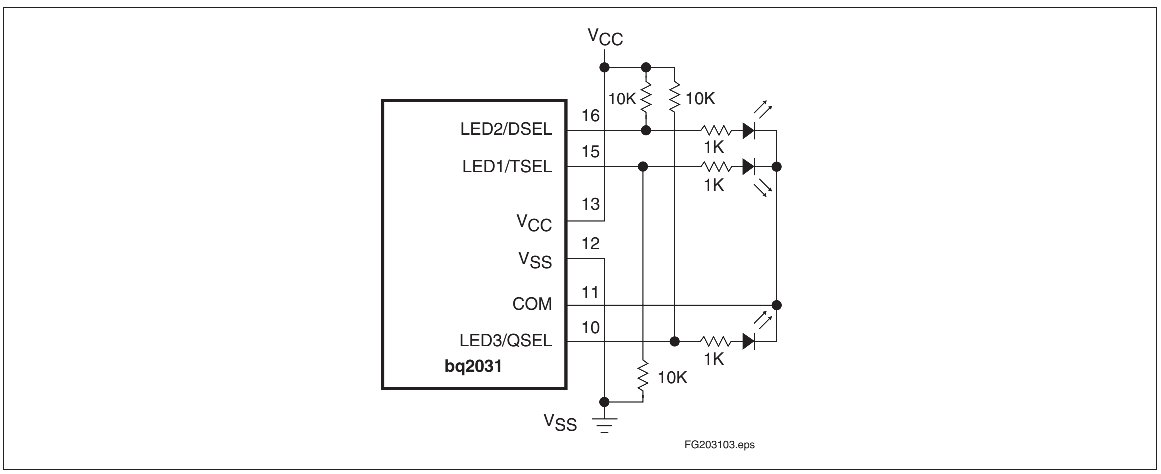

Figure 7. Configuring 10K Two-Step Current Algorithm and Display Mode Selection

Setting Voltage and Current Thresholds

Fixed Thresholds

The bq2031 uses the following fixed thresholds:

- **V_{HCO}**—High-Cutoff Voltage: V_{BAT} rising above this level is interpreted as battery removal, cutting off charging current. $V_{HCO} = 0.6 * V_{CC}$.
- **V_{LCO}**—Low-Cutoff Voltage: V_{BAT} dropping below this level is interpreted as battery removal, cutting off charging current. $V_{LCO} = 0.8V$.
- **V_{MIN}**—Minimum Voltage: Used in pre-charge qualification test 2. $V_{MIN} = 0.34 * V_{CC}$.
- **I_{COND}**—Conditioning Current: Used in the maintenance phase of the Two-Step Current algorithm and pre-charge qualification tests 1 and 2. $I_{COND} = I_{MAX}/5$. I_{MAX} is set by Equation 3.

Configurable Thresholds

The bq2031 uses the following configurable thresholds:

- **V_{BLK}**—Upper voltage limit during fast charge, typically specified by the battery manufacturers to be 2.45V–2.5V per cell @ 25°C.
- **V_{FLT}**—Minimum charge voltage required to compensate for the battery's self-discharge rate and maintain full charge on the battery. A value is usually recommended by the battery manufacturer.
- **I_{MAX}**—Fast charge current specified as a function of "C," the capacity of the battery in Ampere-hours (e.g., a charge rate of 1C for a 5Ah battery is 5A). Typical values range from $C/_{10}$ to C, although some battery vendors may approve higher charge rates.

V_{FLT}, V_{BLK}, and I_{MAX} are configured by the user when selecting resistor values for the battery voltage divider network (see Figure 8). V_{FLT} is set by RB1 and RB2 by:

Equation 1

$$\frac{RB1}{RB2} = \frac{(N * V_{FLT})}{2.2V} - 1$$

VBLK is determined by:

Equation 2

$$\frac{RB1}{RB2} + \frac{RB1}{RB3} = \left(\frac{N * V_{BLK}}{2.2}\right) - 1$$

I_{MAX} is determined by:

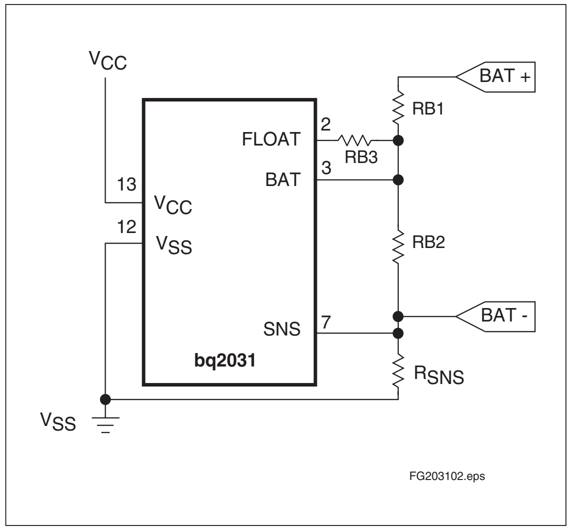

Figure 8. configuring the Battery Divider and Current Sense Circuit

Equation 3

$$I_{MAX} = \frac{0.250V}{R_{SNS}}$$

where:

- N = Number of series cells in the battery pack
- V_{FLT} = Value recommended by manufacturer
- V_{BLK} = Value recommended by manufacturer at 25°C. If you have selected the Two-Step Current algorithm and want Second Difference detection to be your primary fast charge termination criterion, use V_{BLK} = 2.75V.
- I_{MAX} = Desired maximum charge current

The bq2031 internal band-gap reference voltage at 25°C is 2.2V. This reference shifts with temperature at -3.9mV/°C to compensate for the negative temperature coefficient of lead-acid chemistry.

The total resistance presented by the divider between BAT+ and BAT- (RB1 + RB2) should be between 150kΩ and 1MΩ . The minimum value ensures that the divider network does not drain the battery excessively when the power source is disconnected. Exceeding the maximum value increases the noise susceptibility of the BAT pin.

An empirical procedure for setting the values in the resistor network is as follows:

1. Set RB2 to 49.9 kΩ (for 3 to 18 series cells).

2. Determine RB1 from equation 1 given V_{FLT}.
3. Determine RB3 from equation 2 given V_{BLK}.
4. Determine R_{SNS} from equation 3 given I_{MAX}.

Table 3 shows the results of these calculations at several example cell counts for V_{FLT} = 2.25V and V_{BLK} = 2.45V. 1% resistors are recommended.

Table 3. Example Resistor Values by Number of Cells

Number of Cells	RB1 (kΩ)	RB2 (kΩ)	RB3 (kΩ)
3	102.0	49.9	383.0
6	261.0	49.9	475.0
12	562.0	49.9	511.0
18	866.0	49.9	536.0

I_{MIN}—In the Two-Step Voltage algorithm, I_{MIN} is the level to which charging current must drop to terminate fast charge. In the Two-Step Current algorithm, it is the average value of pulsed current in the maintenance phase. I_{MIN} is a fraction of I_{MAX} programmed by the state of the pin IGSEL and the charging algorithm selected, per Table 4.

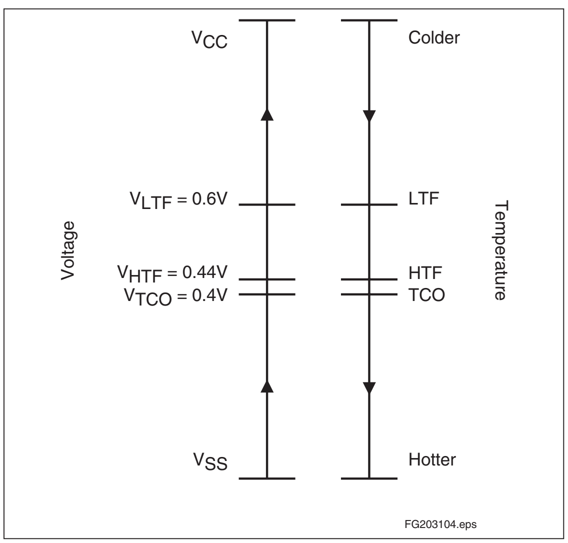

Figure 9. Voltage Equivalent of Current Thresholds

Table 4. Programming I_{MIN}

Two-Step Voltage		Two-Step Current	
IGSEL	I_{MIN}	IGSEL	I_{MIN}
L	I_{MAX}/10	L	I_{MAX}/10
H	I_{MAX}/20	H	I_{MAX}/20
Z	I_{MAX}/30	Z	I_{MAX}/40

Setting Temperature Thresholds

The bq2031 senses temperature by monitoring the voltage between the TS and SNS pins. The bq2031 assumes a Negative Temperature Coefficient (NTC) thermistor, so the voltage on the TS pin is inversely proportional to the temperature (see Figure 9). The temperature thresholds used by the bq2031 and their corresponding TS pin voltage are:

TCO—Temperature Cut-Off: Higher limit of the temperature range in which charging is allowed. $V_{TCO} = 0.4 * V_{CC}$.

HTF—High-Temperature Fault: Threshold to which temperature must drop after Temperature Cut-Off is exceeded before charging can begin again. $V_{HTF} = 0.44 * V_{CC}$

LTF—Low-Temperature Fault: Lower limit of the temperature range in which charging is allowed. $V_{LTF} = 0.6 * V_{CC}$.

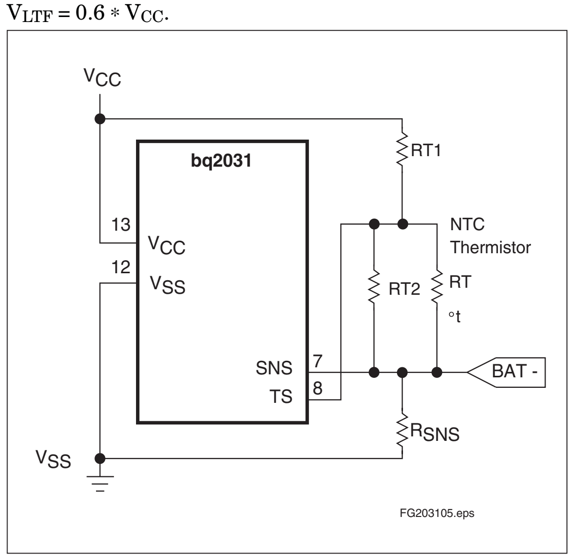

Figure 10. Configuring Temperature Sensing

A resistor-divider network must be implemented that presents the defined voltage levels to the TS pin at the desired temperatures (see Figure 10).

The equations for determining RT1 and RT2 are:

Equation 4

$$0.6 * V_{CC} = \frac{(V_{CC} - 0.250)}{1 + \frac{RT1 * (RT2 + R_{LTF})}{(RT2 * R_{LTF})}}$$

Equation 5

$$0.44 = \frac{1}{1 + \frac{RT1 * (RT2 + R_{HTF})}{(RT2 * R_{HTF})}}$$

where:

- R_{LTF} = Thermistor resistance at LTF
- R_{HTF} = Thermistor resistance at HTF

TCO is determined by the values of RT1 and RT2. 1% resistors are recommended. As an example, the resistor values for several temperature windows computed for a Philips 2333-640-63103 thermistor are shown in Table 5.

Table 5. RT1 and RT2 Values for Temperature Thresholds

LTF (°C)	HTF (°C)	TCO (°C)	RT1 (kΩ)	RT2 (kΩ)
0	45	47	3.57	7.50
5	45	47	3.65	8.66
–5	50	52	2.74	5.36

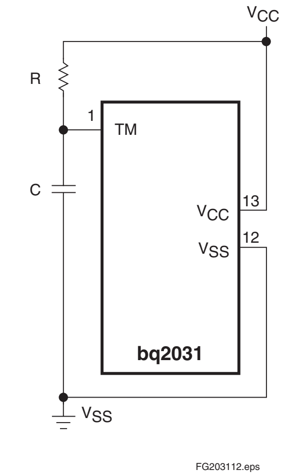

Figure 11. RC Network for Setting MTO

Disabling Temperature Sensing

Temperature sensing may be disabled by removing the thermistor and RT1, and using a value of 100kΩ for RT1 and RT2.

Setting Timers

The user sets the Maximum Time-Out (MTO) value. All other timing periods used in the bq2031 are fixed as fractions of MTO (see Table 6). MTO is set by an R-C network on the TMTO pin as shown in Figure 11.

Table 6. Timing Parameters

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{MTO}	Maximum Time Out range	1	-	24	hours
t_{QT1}	Qualification time-out test 1	-	$0.02t_{MTO}$	-	-
t_{QT2}	Qualification time-out test 2	-	$0.16t_{MTO}$	-	-
t_{DV}	$-\Delta^2V$ termination sample frequency	-	$0.008t_{MTO}$	-	-
t_{HO1}	Qualification test 2 hold-off period	-	$0.002t_{MTO}$	-	-
t_{HO2}	Bulk-charge hold-off period	-	$0.015t_{MTO}$	-	-

The equation for MTO is:

Equation 6

$$\text{MTO (in hours)} = 0.5 * R * C$$

where R is in kΩ and C is in µF. The value for C must not exceed 0.1µF.

Example: An MTO of 5 hours is set by R = 100kΩ and C = 0.1µF

Switch-Mode Power Conversion

The bq2031 incorporates the necessary PWM control circuitry to support switch-mode voltage and current regulation.

Figure 12 shows a functional block diagram of a switch-mode buck topology converter using the bq2031. The battery voltage is divided down to a per-cell equivalent value at the BAT pin. During voltage regulation, the voltage on the BAT pin (V_{BAT}) is regulated to the internal band-gap reference of 2.2V at 25°C (with a temperature drift of -3.9 mV/°C). The charge current through the inductor L is sensed across the resistor R_{SNS}. During current regulation, the bq2031 regulates the voltage on the SNS pin (V_{SNS}) to a temperature-compensated reference of 0.250V.

The passive components C_I on the I_{COMP} pin, R_V and C_V on the V_{COMP} pin, and C_F across the high side of the battery voltage divider form the phase compensation network for the current and voltage control loops, respectively. The diodes (Db1 and Db2) serve to prevent battery drain when VDC is absent, while the pull-up resistor (R_P) is used to detect battery removal. The resistor R_S, typically a few tens of mΩ, is optional and depends on the battery impedance and the resistance of the battery leads to and from the charger board.

Pulse-Width Modulator

The bq2031 incorporates two PWM circuits, one for each control loop (voltage and current, see Figure 13). Each PWM circuit runs off a common saw-tooth waveform (V_S) whose time-base is controlled by a timing capacitor (CPWM) on the TPWM pin.

The relationship between CPWM and the switching frequency (F_S) is given by :

Equation 7

$$F_S = \frac{0.1}{C_{PWM}} \text{ kHz}$$

where CPWM is in µF.

Each PWM loop starts with a comparator whose positive terminal is driven by V_S. The negative terminal is driven by the output of an Operational Transconductance Amplifier (OTA) which, with the compensation network connected via V_{COMP} or I_{COMP}, generates the control signal V_C. The OTA characteristics are: R_O = 250kΩ; G_M = 0.42m-mho; gain bandwidth = 80MHz. The output of each comparator, along with the ramp waveform (V_S), is used to generate a pulse-width modulated waveform at a constant frequency on the MOD output. Figure 14 shows the relationship of MOD with V_C and V_S.

The MOD output swings rail-to-rail and can source and sink 10mA. It is used to control the drive circuitry of the switching transistor.

The pulse-width modulated square-wave signal on the MOD pin is synchronized to the internal sawtooth ramp signal. The ramp-down time (T_D) is fixed at approximately 20% of the ramp time-period (T_P). This limits the maximum duty-cycle achievable to approximately 80%. See Figure 14.

Example: At a switching frequency of F_S = 100kHz, T_D = 2µs.

Inductor Selection

The inductor selection criteria for a DC-DC buck converter vary depending on the charging algorithm used. For the Two-Step Current and Pulsed Current charge algorithms, the inductor equation is:

Equation 8

$$L = \frac{(N * V_{BLK} * 0.5)}{F * \Delta I}$$

where:

- N = Number of cells
- V_{BLK} = Bulk voltage per cell, in volts
- F_S = Switching frequency, in Hertz
- ΔI = Ripple current at I_{MAX}, in amperes

The ripple current is usually set between 20–25% of I_{MAX}.

Example: A 6-cell SLA battery is to be charged at I_{MAX} = 2.75A in a buck topology running at 100kHz. The V_{BLK} threshold is set at 2.45V per cell and the charger is configured for Pulsed Current mode. Assuming a ripple = 25% of I_{MAX}, the inductor value required is:

Equation 9

$$L = \frac{(6 * 2.45 * 0.5)}{(100000 * 0.6875)} = 107\mu H$$

The inductor formula for the Two-Step Voltage charge algorithm is dictated by the inductor current, which must remain continuous down to I_{MIN} during Fast Charge phase 2 (voltage regulation phase).

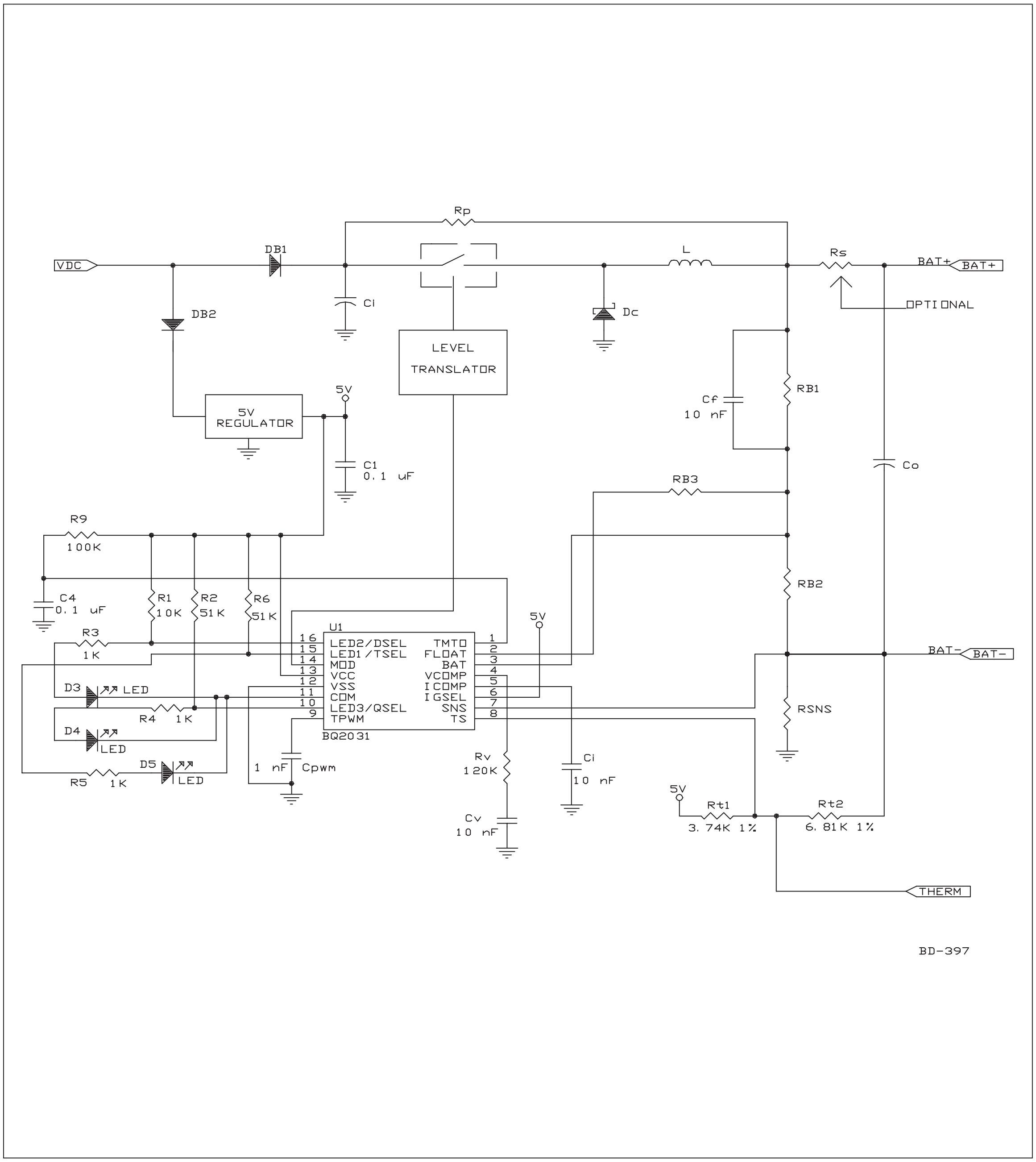

Figure 12. Functional Diagram of a Switch-Mode Buck Regulator Lead-Acid Charger Using the bq2031

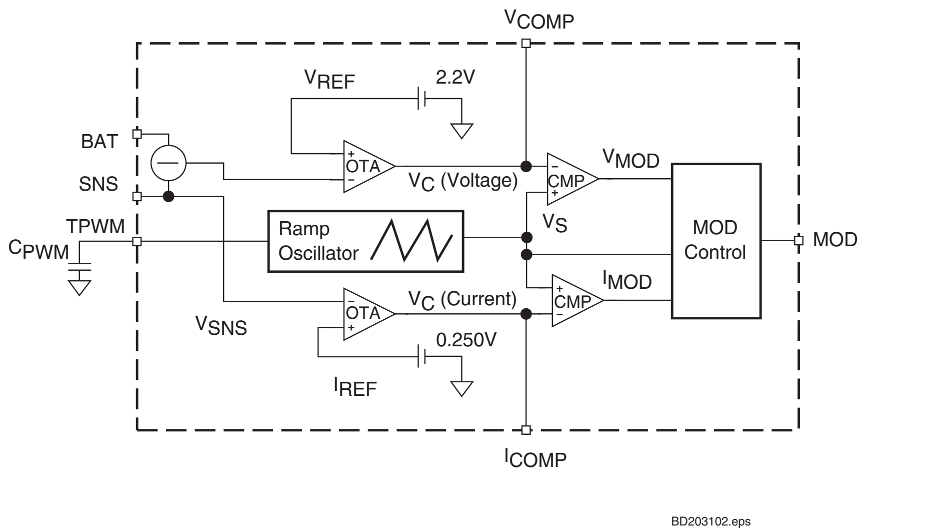

Figure 13. Block Diagram of the bq2031 PWM Control Circuitry

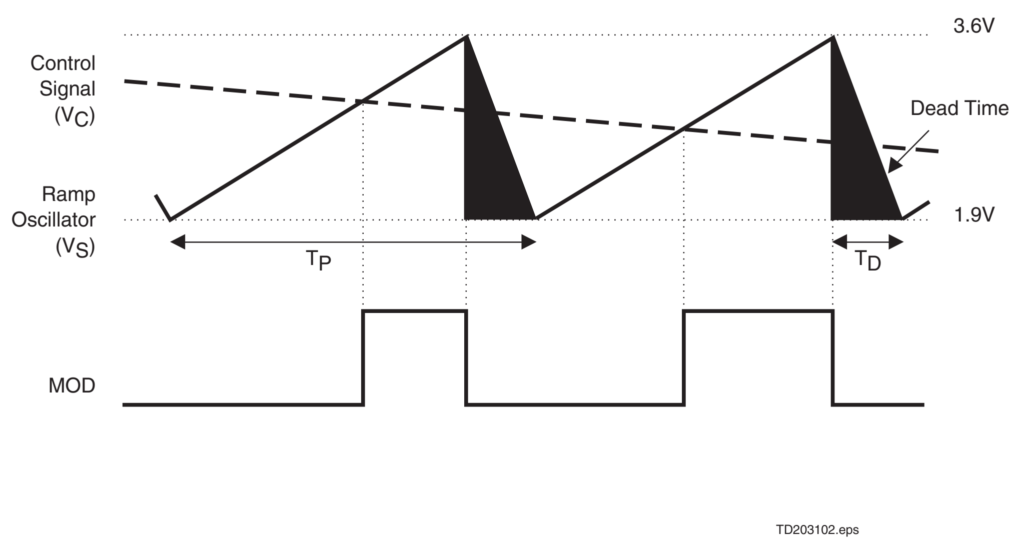

Figure 14. Relationship of MOD Output to Sawtooth Waveform V_S and Control Signal V_C

Equation 10

$$L = \frac{N * V_{BLK} * 0.5}{F_S * 2 * I_{MIN}}$$

Example: A 6-cell SLA battery is to be charged at I_{MAX} = 2.75A in a buck topology running at 100kHz. The V_{BLK} threshold is set at 2.45V per cell and the charger is configured for Two-Step Voltage mode, with I_{MIN} = I_{MAX}/20. The inductor value required is:

Equation 11

$$L = \frac{6 * 2.45 * 0.5}{(100000 * 2 * 0.1375)} = 267\mu H$$

Phase Compensation

For buck-mode switching applications, the suggested component values shown in Figure 12 are good starting points. More details on the calculations used in this program are available in the application note entitled "Switch-Mode Power Converson Using the bq2031." For assistance with other power supply topologies, contact one of our field application engineers.

Miscellaneous Issues

V_{CC} Supply

The V_{CC} supply provides bq2031 power and serves as the reference voltage for all temperature sense thresholds (V_{LTF}, V_{HTF}, and V_{TCO}) and the battery voltage thresholds V_{HCO} and V_{MIN}. The timer thresholds (MTO and its derivatives) are trimmed within 5% of the typical value with V_{CC} = 5V.

The V_{BLK} and V_{FLT} thresholds are set from an external divider network powered by the battery. These thresholds are referenced to an internal band-gap reference, and the accuracy of voltage regulation will not be adversely affected by variation in V_{CC}. The current regulation threshold (I_{MAX}) is referenced to a temperature compensated reference and is also unaffected by V_{CC}.

DC Power Supply

The DC power supply voltage (V_{DC}) for a switch-mode application must satisfy the following criterion:

Equation 12

$$V_{DC} = (N * V_{BLK} * 1.2) + 2$$

where:

- N = Number of cells
- V_{BLK} = Bulk voltage threshold per cell

Logical Control of Charging

Charge Inhibit

An inhibit input may be implemented by connecting the cathode of a small-signal diode to the TS pin. A CMOS logic-level "1" applied to the anode of the diode then functions as an inhibit input, by driving the temperature sense voltage out of its allowed range and simulating an under-temperature condition. The bq2031 enters the Charge Pending state, shutting off charging current (driving MOD low) and suspending all timers. When the Inhibit signal is allowed to float, the bq2031 returns to its previous state (as long as the temperature is still within the allowed range). The bq2031 restarts (but does not reset) its timers, and the suspended charge cycle resumes at the point where it stopped.

Reset

A logical Reset signal for the bq2031 can be created in a manner similar to the Charge Inhibit input described above. Instead of being connected to the T_S pin, however, the diode is connected to the BAT input. In this configuration, a logic "1" on the diode drives V_{BAT} above V_{HCO}, simulating battery removal. The bq2031 enters the Fault state and waits to see a battery insertion; V_{BAT} rising past V_{LCO} or falling past V_{HCO}. Removing the logic "1" from the diode creates this transition (as long as a battery is still present), and the bq2031 starts a new charge cycle.

Caution: To avoid damage to the bq2031, always keep the voltage applied to the anode of the diode below V_{CC} for either the Charge Inhibit or Reset implementations.

Layout Guidelines

Printed circuit board layout must adhere to the following guidelines to minimize noise injection on the high-impedance pins (BAT, V_{COMP}, I_{COMP}, and SNS).

1. Use a single-point grounding technique such that the isolated small-signal ground path and the high-current power ground path return to the power supply ground.
2. The charging path components and traces must be isolated from the voltage and current feedback small signal paths.
3. 0.1µF and 10µF decoupling capacitors must be placed close to the V_{CC} pin. This also helps to prevent voltage dips while the bq2031 is driving the LEDs.
4. A 100pF capacitor, if used for coupling the BAT and SNS pins, must be placed close to those pins.
5. The compensation network on I_{COMP} and V_{COMP} must be placed close to their respective pins.

6. Minimize loop area in paths with high pulsating currents.

Battery Removal Detection

The bq2031 interprets V_{BAT} rising past V_{HCO} or falling past V_{LCO} as battery removal, and the bq2031 enters the Fault state until a new battery insertion is seen. The battery removal transitions are precluded during periods of voltage regulation unless circuitry (e.g., a pull-up to V_{DC}) is provided to pull V_{BAT} out of the "battery present" range.

Voltage regulation occurs during phase 2 of the Two-Step Voltage fast charge algorithm and in battery qualification test 1 which precedes all three algorithms. The time-out period of this test (= 0.02 * MTO) is at least 1.2 minutes and may be as long as 28.8 minutes. Unless waiting through this period before detecting battery removal is acceptable, the pull-up is required in the purely current regulated algorithms as well. A diode should also be installed in the path of the pull-up to prevent the power supply from draining the battery when the supply is turned off. Refer to resistor R12 and diode D3 in the example design in Figure 15.

This pull-up creates a background trickle charge current to the battery that can be minimized by minimizing the voltage overhead; that is, the voltage difference between the V_{DC} supply and the battery stack.

Load-Only Operation

The bq2031 supports the case in which the charger must supply the load in the absence of a battery, provided the load can pass the two pre-charge qualifications tests (draw current of at least I_{COND} when regulated at V_{FLT} + 0.25V and maintain voltage of at least V_{MIN} when regulated at I_{COND}). Further, the load must not create conditions that cause fast charge termination or it must be able to tolerate the conditions of maintenance regulation for the charge algorithm selected. This is regulation at V_{FLT} in the case of the Two-Step Voltage algorithm or constant or hysteretic pulsed current supply in the case of the Two-Step Current and Pulsed Current algorithms, respectively. This can be a problem for intermittent loads unless circuitry is provided to maintain these conditions during the low-load or no-load periods.

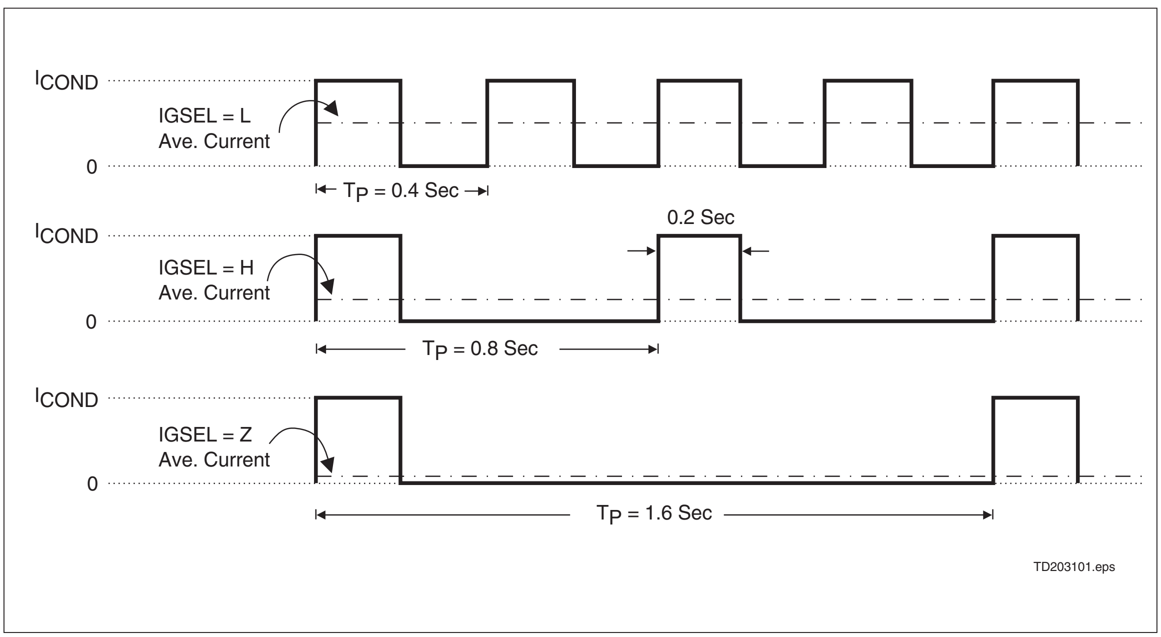

Figure 15. Implementation of Fixed-Pulse Maintenance Charge

Back-up Supply Regulation

To protect the system from damage during periods of fast charge voltage regulation, the bq2031 regulates to I_{MAX} if the current tries to rise above that level, and has an absolute current limit of 1.25 * I_{MAX}. Similarly, during periods of fast charge current regulation, the bq2031 enforces a V_{BLK} upper limit on voltage, and regulates to V_{BLK} if the voltage tries to rise above this level. During the maintenance phase, the bq2031 regulates to V_{FLT} and I_{COND} during periods of current or voltage regulation, respectively.

Applications Example: Single-Ended Buck Charger

For an application example, please see the DV2031S1 data sheet and schematic.

Appendix A: Implementation Details of Pulsed Maintenance Charging

Two-Step Current Algorithm

Maintenance charging in the Two-Step Current Algorithm is implemented by varying the period (TP) of a fixed current (I_{COND} = I_{MAX}/5) and duration (0.2 second) pulse to achieve the configured average maintenance current value. See Figure 16.

Maintenance current can be calculated by:

Equation 14

$$\text{Maintenance current} = \frac{((0.2) * I_{COND})}{T_P} = \frac{((0.04) * I_{MAX})}{T_P}$$

where TP is the period of the waveform in seconds.

Table 7 gives the values of TP programmed by IGSEL.

Table 7. Fixed-Pulse Period by IGSEL

IGSEL	T_P (s)
L	0.4
H	0.8
Z	1.6

Revision History

Charge No.	Page No.	Description	Nature of Change
1	4, 5	Renamed	Figure 7 was: Pulsed Current; Is: Two-Step Current
1	6, 8	Changed values in Equations 3 and 4	Was: 0.275V; is now 0.250V
1	9	Under Switch-Mode Power Conversion	Changed value, was: 0.275V; is now 0.250V
1	11	Figure 13 changed	Block diagram has been reconfigured. VC was 0.275V; us biw 0.250V
1	13	Applications Example changed	Changed to: For an application example, please see the DV2031S1 datasheet and schmatic
1	14	Figure 15. Example Schematic of a Single-Ended Buck Topology Charger	Deleted
1	15	Table 7. Parts List for Single-Ended Buck Charger	Deleted
2	8	Equation 4	Was: -0.275 Is: -0.250
2	9	Temperature-compensated reference	Was: 0.275V Is: 0.250V
2	12	Equation 12	Was: V_{DC} = (N * V_{BLK}) + 3V Is: V_{DC} = (N * V_{BLK} * 1.2) + 2
3	12	Clarify description for phase compensation	

Notes: Change 1 = April 1997 B changes from Dec. 1995.
Change 2 = Oct. 1997 C changes from April 1997 B.

IMPORTANT NOTICE