NEUTRAL-POINT-CLAMPED DC–AC POWER CONVERTERS

1. INTRODUCTION

Direct current–alternating current (DC–AC) power converters control the power flow between a DC system and an AC system through the control of some of the interface electrical variables. As shown in Figure 1, the power converter interfaces both systems through a set of wires (z_{DC} and z_{AC}). The wire voltages (with reference to any given node) and currents of each interconnection can be arranged into vectors $\mathbf{v}_X(t)$ and $\mathbf{i}_X(t)$, and the inner product of these two vectors defines the power flowing between system X and the power converter. The power converter interacts with each system receiving as an input $\mathbf{v}_X$ or $\mathbf{i}_X$ and delivering as an output $\mathbf{i}_X$ or $\mathbf{v}_X$. In a *voltage-source* DC–AC converter, the DC system forces $\mathbf{v}_{DC}$. On the other hand, in a *current-source* DC–AC converter, the DC system forces $\mathbf{i}_{DC}$. The main function of the power converter is to guarantee the transfer of energy between the DC and AC systems with the suitable voltages and currents for every system. The power flow can be unidirectional or bidirectional. When the power flows from the DC side to the AC side (positive P_{DC} and P_{AC}), the converter is said to operate in *inverter mode*. When the power flows from the AC side to the DC side (negative P_{DC} and P_{AC}), the converter is said to operate in *rectifier mode*.

Conventional voltage source DC–AC power converters are configured with the basic building block depicted in Figure 2: a single-pole double-throw (SPDT) switch that allows the connection of the AC terminal to any of the two available DC-link terminals (DC_1 and DC_2). Figure 2a and b show the AC terminal connected to DC_2. This connection is indicated with a solid circle in the symbol of Figure 2b. Variable $s_{AC} \in \{1, 2\}$ indicates the switch position. The block receives as inputs the positive DC-link voltage v_{DC} (typically forced by a capacitor) and the bidirectional AC-side current i_{AC} (typically forced by an inductor). The block produces as outputs the AC terminal voltage v_{AC} and the DC-link currents i_{DC1} and i_{DC2}. Voltage v_{AC} is a binary or two-level voltage waveform that essentially contains a main sinusoidal component with some distortion. Currents i_{DC1} and i_{DC2} essentially contain a main DC component with some distortion. The SPDT switch of Figure 2 can be implemented, as shown in Figure 3, with a simple arrangement of power semiconductor devices and without the need of passive energy storage components such as capacitors and inductors. This arrangement, known as a *half-bridge leg*, is made up of two series-connected voltage-unidirectional current-bidirectional single-pole single-throw (SPST) switches. Each SPST switch consists of one controlled switch and an antiparallel diode. The controlled switch can be either a transistor or a thyristor: typically, a power metal-oxide-semiconductor field-effect transistor (MOSFET), an insulated-gate bipolar transistor (IGBT), or an integrated-gate commutated thyristor (IGCT). The state of both switches is governed by the binary switch control signal s, generating the two switching states of the half-bridge leg outlined in Table 1. When $s = 0$, the bottom switch is *on* and the upper switch is *off*. When $s = 1$, the bottom switch is *off* and the upper switch is *on*. Figure 3b and c show the current path through the leg in both switching states with both possible i_{AC} current directions (positive i_{AC} shown in blue and negative i_{AC} shown in red). The dotted lines indicate the additional current path when the controlled switch is bidirectional in current (e.g., MOSFET). The antiparallel diodes are necessary for two reasons. On one hand, they provide a current path in the reverse direction in both switching states when the switch is unidirectional in current (e.g., IGBT). On the other hand, they also provide a flow path for i_{AC} when both switches are *off*. This is a brief switching state that occurs during leg switching state transitions, due to the blanking time introduced between the turn-off of a switch and the turn-on of the other switch. The introduction of this blanking time is necessary to avoid the possibility of a DC-link short circuit (both switches *on*) as a consequence of switch transition delay tolerances.

The SPDT switch of Figure 2 can be used to configure voltage-source two-level single-phase and multiphase DC–AC converters, as shown in Figure 4. The converters are made up of one or more legs and feature bidirectional power flow. For the sake of simplicity, the multiphase case considers an AC system with isolated neutral. This is the most common case in practice.

The concept of multilevel conversion, which consists in synthesizing AC voltages with more than two voltage levels, was first introduced in the early 1970s (1, 2). But it was not until the late 1970s and early 1980s that the first members of the neutral-point-clamped (NPC) converter family, one of the three basic multilevel converter families (NPC, flying capacitor, and cascaded H-bridge) (3), were originally presented (4–9). NPC DC–AC converters, also designated as full-semiconductor multipoint-clamped converters, constitute an extension of the two-level case to a higher number of levels through the replacement of the SPDT switches by single-pole multiple-throw (SPMT) switches, depicted in Figure 5. The SPMT switches, which are implemented through an arrangement of power semiconductor devices without passive energy storage components, enable the possible connection of the AC terminal to more than two DC-link terminals. The inner DC-link terminals, from DC_2 to DC_{n-1}, where n is the number of levels, are designated as the *neutral points*, although this term is sometimes reserved for the middle inner point (odd n). The voltage across adjacent DC-link points is a portion of the DC-link voltage, usually equal to $v_{DC}/(n-1)$. The multiple DC-link points are provided by the DC system. They are often generated by a capacitor voltage divider across the DC-link; that is, a series connection of capacitors across the DC-link. Although, as it will be seen in the next section, the leg topologies include a larger number of power semiconductor components compared with the two-level case, involving an increased control complexity, the availability of multiple DC-link terminals brings a set of advantages:

1. For a given semiconductor device technology, higher converter DC-link voltage and power ratings, since the power devices only have to block a portion of the total DC-link voltage, typically.

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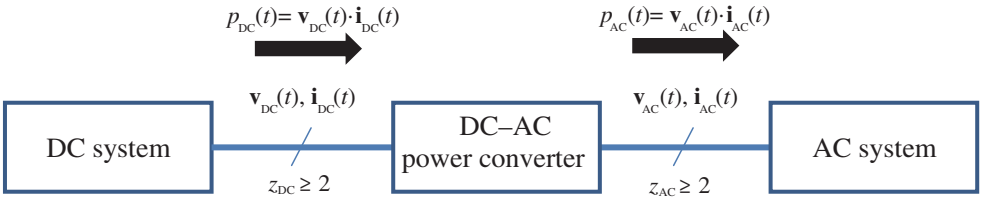


Figure 1. General diagram of a DC–AC power conversion system. The arrows indicate the positive direction of the power flow.

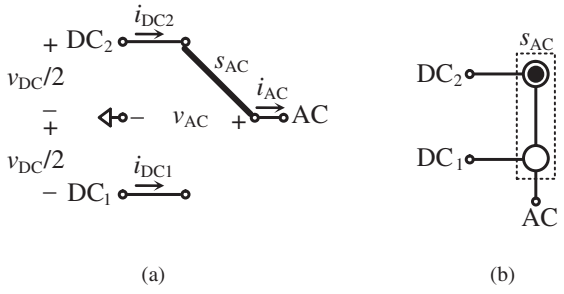


Figure 2. Functional building block of a conventional two-level voltage-source DC–AC converter: single-pole double-throw (SPDT) switch. (a) Symbol 1. (b) Symbol 2.

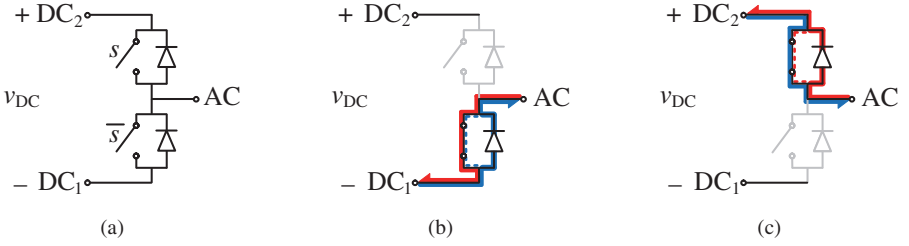


Figure 3. Implementation of the SPDT switch as a two-level half-bridge leg. The current path is shown in blue for positive i_{AC} and in red for negative i_{AC}. (a) Topology. (b) $s_{AC} = 1$. (c) $s_{AC} = 2$.

Table 1. Switching States of a Two-Level Half-Bridge Leg

s_{AC}	AC terminal connection to	s	v_{AC}
1	DC_1	0	$-v_{DC}/2$
2	DC_2	1	$+v_{DC}/2$

2. Better overall system performance, since the availability of multiple voltage levels at the DC-link may allow a more efficient control of the power flow between systems. For instance, in battery-powered systems, the multilevel converter may aid in the balancing of the battery packs, simplifying the task and reducing the losses produced by the battery management system. In power generation applications from photovoltaic arrays, the multiple voltage levels allow to operate the different photovoltaic arrays at their maximum power point, even if partial shading occurs (10).
3. Inherent reduction of v_{AC} voltage harmonic distortion, leading to lower required filter size, weight, and filter losses.
4. Inherent reduction of switching losses, because switching transitions take place at lower blocking voltage levels and with lower voltage-rated devices featuring better relative switching performance.
5. Wider loss spreading among devices, leading to reduced global heat sink requirements.
6. Better leg fault-tolerance capacity, since the failure of one device does not necessarily lead to a full leg shutdown, as is the case of the two-level topology of Figure 3a.
7. Lower v_{AC} dv/dt.
8. Lower converter AC-side common-mode voltage.
9. Lower electromagnetic noise.

Although NPC DC–AC converters have been mainly applied to date in high-power medium-voltage applications, they can also be competitive at lower power and voltage ratings (11–13). In most occasions, they have been applied with three levels. Two main application fields can be identified as follows:

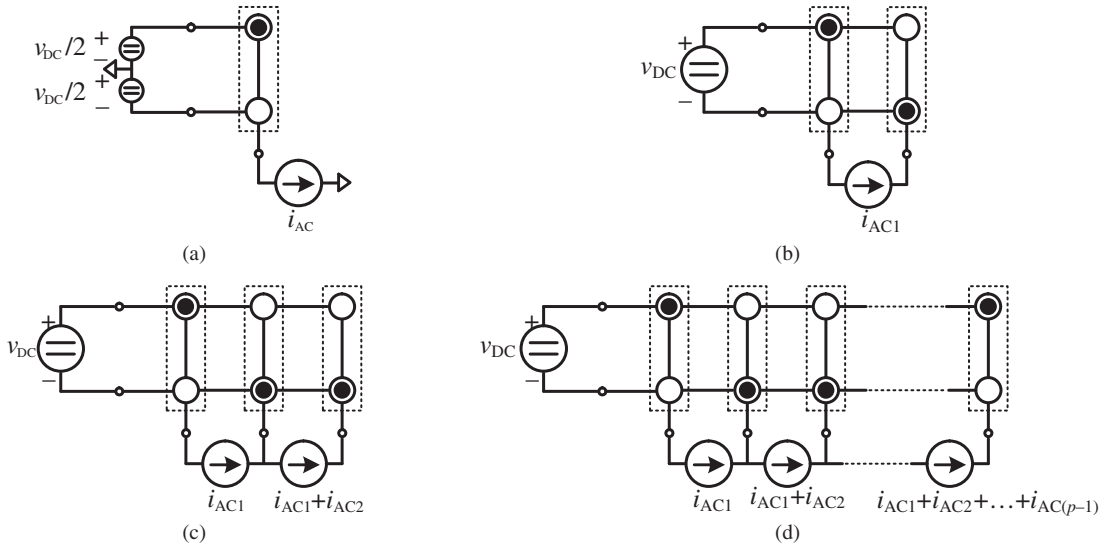


Figure 4. Voltage-source two-level DC–AC converter configurations. (a) Single phase with one leg. (b) Single phase with two legs. (c) Three phase with three legs. (d) p-phase with p legs ($p > 3$).

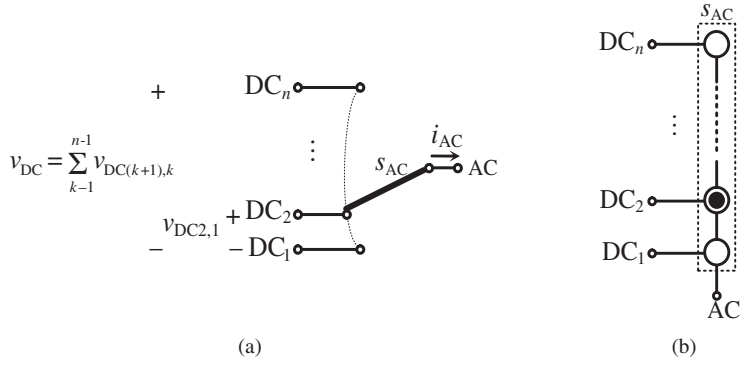


Figure 5. Functional building block of an n-level voltage-source NPC DC–AC converter: single-pole multiple-throw (SPMT) switch. (a) Symbol 1. (b) Symbol 2.

1. *AC motor drives*: Both in industrial processes (fans, pumps, blowers, compressors, conveyors, laminators, mills, extruders, crushers, gas turbine starters, mixers, mine hoists, etc.) for the oil, gas, metals, mining, water, chemical, industries and in transportation applications (train, ship, automobile, etc.).
2. *Generation, transmission, and distribution of electrical energy*: Grid interfacing of renewable energy sources like wind power and photovoltaics, active filters, static compensators, dynamic voltage restorers, universal power flow controllers, uninterruptible power supplies, and so on.

This article reviews the fundamentals of multilevel multiphase NPC DC–AC power converters. Section 2 presents the main leg topologies. Subsequently, Section 3 discusses the leg switching states enabling all possible leg positions. In Section 4, the set of all possible converter switching states and their standard representation in the converter space vector diagram is systematically derived, starting from the simplest converter (single-phase single-leg) up to the most complex converter with an arbitrary number of phases. Once the converter states have been characterized, Section 5 introduces the most common converter control approaches. In Section 6, the article presents the DC-link capacitor voltage balance problem and the different approaches to solve it. Finally, the article is concluded in Section 7 with a brief discussion of the future research directions.

2. TOPOLOGIES

This article focuses on NPC DC–AC converters with bidirectional power flow capability. In the following, the four main leg topologies of these converters are presented. Other topologies are also possible as a modification or combination of these basic topologies.

The most complete leg topology is the active clamped or transistor clamped, depicted in Figure 6 (14, 15). It is built from a pyramidal connection of two-level half-bridge legs. As a result, the topology is built from a combination of

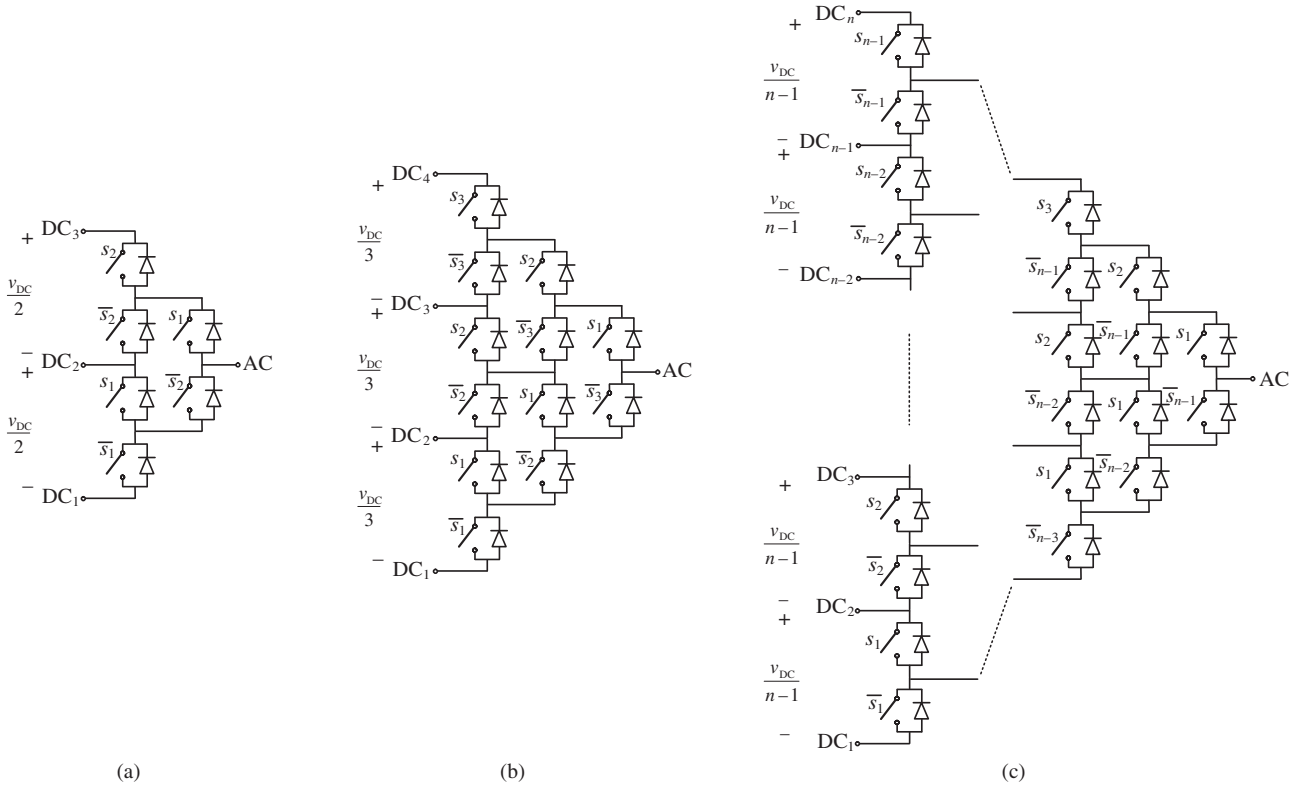


Figure 6. Multilevel active-clamped (transistor-clamped) topology. (a) Three levels. (b) Four levels. (c) n levels.

voltage-unidirectional and current-bidirectional SPST switches, each formed by a controlled switch and an antiparallel diode. The voltage rating of all switches and diodes is the same and corresponds to a blocking voltage of $v_{DC}/(n-1)$. This blocking voltage value can be inherently guaranteed by the topology for all devices through a proper operating principle. In addition, in the connection of the AC terminal to the inner DC-link points, the topology offers several possible flow paths for the current, which confers the topology certain degree of redundancy.

If the inner switches from the active-clamped topology are removed, the passive-clamped or diode-clamped topology results, depicted in Figure 7 (16). Again, all power semiconductor components have the same voltage rating corresponding to a blocking voltage of $v_{DC}/(n-1)$. However, this blocking voltage value cannot be inherently fully guaranteed by the topology for all components, and some additional blocking-voltage balancing circuitry may be required (16). In addition, the removal of the inner switches also eliminates the redundancy in the possible current paths.

Both the active-clamped and passive-clamped topologies contain a large number of components. The number of switches and diodes of each topology are indicated in Table 2. However, the number of components can be reduced at the expense of increasing the voltage rating of some devices beyond $v_{DC}/(n-1)$. This is the case of the reduced active-clamped and passive-clamped topologies presented in Figure 8 ([4,9,17]), and Figure 9 (5–9), respectively. Figure 8 corresponds to the reduced version of Figure 6. However, the voltage rating of switches and diodes now depends on the device position. In particular, the top and bottom switch-diode pairs have to withstand a blocking voltage equal to v_{DC}, which is the same value as in a two-level leg. Figure 9 corresponds to the reduced version of Figure 7. In this case, the blocking voltage of switches remains equal to $v_{DC}/(n-1)$ and only the blocking voltage of certain diodes increase. This is the most popular topology in the literature.

3. LEG SWITCHING STATES

Regardless of the selected leg topology, each NPC leg is functionally equivalent to a SPMT switch, as depicted in Figure 5. Each of the n possible SPMT switch positions (leg positions) is associated with at least one *leg switching state*, which corresponds to a particular combination of *on* and *off* states of the leg controlled power switches. These switching states are typically defined with the aid of $n-1$ binary switch control signals $(s_1, s_2, \ldots, s_{n-1})$ and their complementary values $(\overline{s}_1, \overline{s}_2, \ldots, \overline{s}_{n-1})$. The assignment of control signals to all switches is presented in Figures 6–9. A value of the control signal equal to 0 indicates that the corresponding switch is in the *off* state and a value equal to 1 indicates that the switch is *on*. A set of n switching states generating all possible leg positions can be then defined with a thermometric code in terms of the switch control signals, as shown in Table 3. Variable $s_{AC} \in \{1, 2, \ldots, n\}$ indicates the SPMT switch position. The voltage of the AC terminal with reference to the midpoint of the DC-bus for

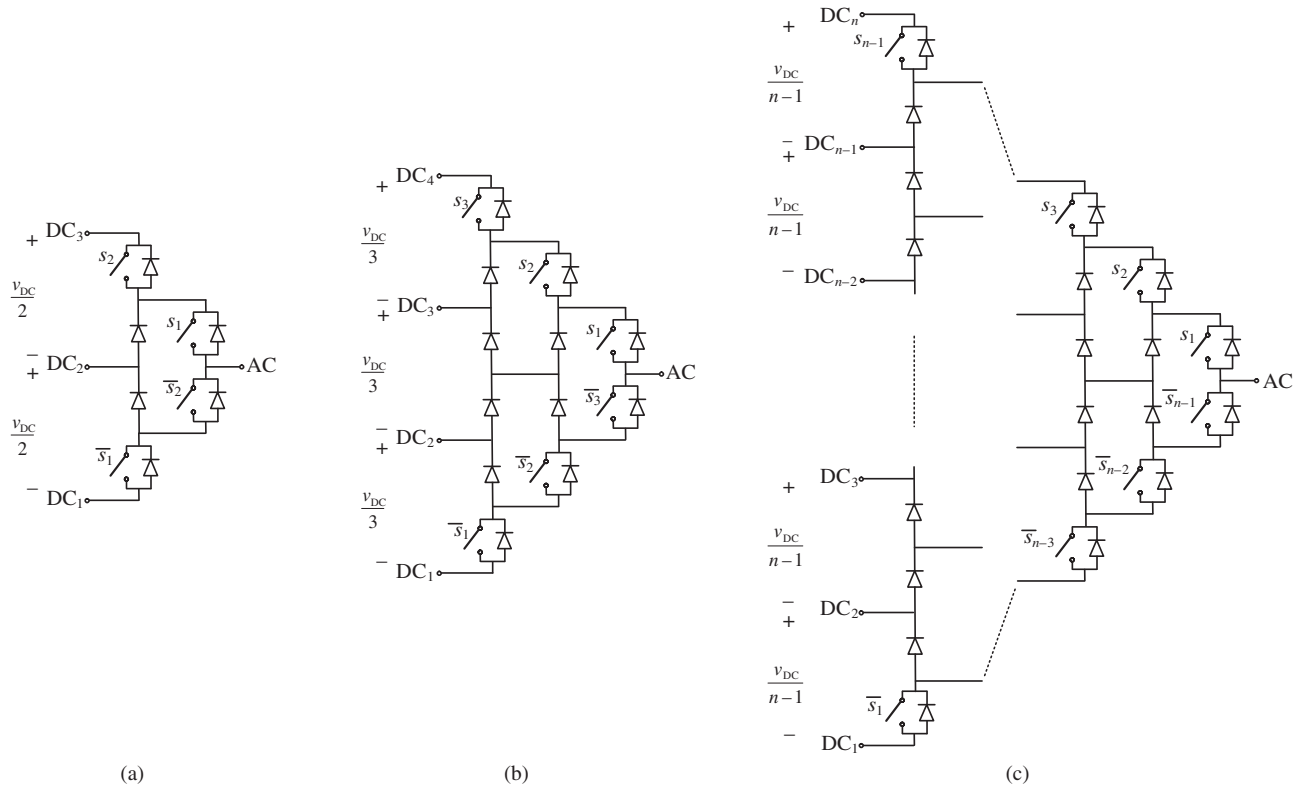


Figure 7. Multilevel passive-clamped (diode-clamped) topology. (a) Three levels. (b) Four levels. (c) n levels.

Table 2. Number of Power Semiconductor Devices of Each n-Level Leg Topology

	Active clamped	Passive clamped	Reduced active clamped	Reduced passive clamped
Switches	$n\cdot(n-1)$	$2\cdot(n-1)$	$2\cdot(n-1)$	$2\cdot(n-1)$
Diodes	$n\cdot(n-1)$	$n\cdot(n-1)$	$2\cdot(n-1)$	$2\cdot(2n-3)$

each leg switching state can be expressed in terms of variable s_{AC} or the switch control signals as

$$v_{AC} = \frac{v_{DC}}{n-1}\cdot(s_{AC}-1) - \frac{v_{DC}}{2} = \frac{v_{DC}}{n-1}\cdot\sum_{k=1}^{n-1} s_k - \frac{v_{DC}}{2} \qquad (1)$$

In the case of the multilevel active-clamped topology, Table 3 and the switch control signal assignment of Figure 6 enable all possible parallel current paths for the connection of the AC terminal to each inner DC-link terminal. However, other switching states are also possible to implement these connections, involving only a subset of the *on* devices defined with Table 3 and Figure 6. The set of switching states generating the same leg position are regarded as *redundant* leg switching states.

Figures 10–12 illustrate the three switching states of the three-level case in all four possible topologies. In Figure 10, it can be observed how the multilevel active-clamped topology inherently guarantees a blocking voltage of all the *off*-state devices (shown in gray) equal to $v_{DC}/2$. This is not fully guaranteed in the diode-clamped topology. With reference to Figure 11a and c, it can be seen that the blocking voltage of the *off*-state SPST switches connected to the AC terminal can, in principle, reach values above $v_{DC}/2$ if the corresponding clamping diode is not forward biased. In the reduced active-clamped topology (Figure 12), two devices present a blocking voltage equal to $v_{DC}/2$ and two devices present a blocking voltage equal to v_{DC}. Thus, the reduction in power semiconductor devices comes at the expense of increased voltage ratings.

Figures 10–12 also illustrate the i_{AC} current paths in all switching states, for both positive i_{AC} (blue) and negative i_{AC} (red). In general, the current flows through one possible path of two power semiconductor devices in series. There are, however, two exceptions to this rule. In the active-clamped topology, two parallel current paths are available in the connection to the neutral point (Figure 10b) in both current directions. In the reduced active-clamped topology (T-type), the current flows through only one device in two switching states (Figure 12a and 12c).

For a proper leg operation, switching state transitions should occur changing only one switch control signal at a time; that is, between adjacent leg positions (between $s_{AC} = k$ and $s_{AC} = k+1$). Trying to directly switch between nonadjacent leg positions may lead to device blocking voltages exceeding the intended values. These switching

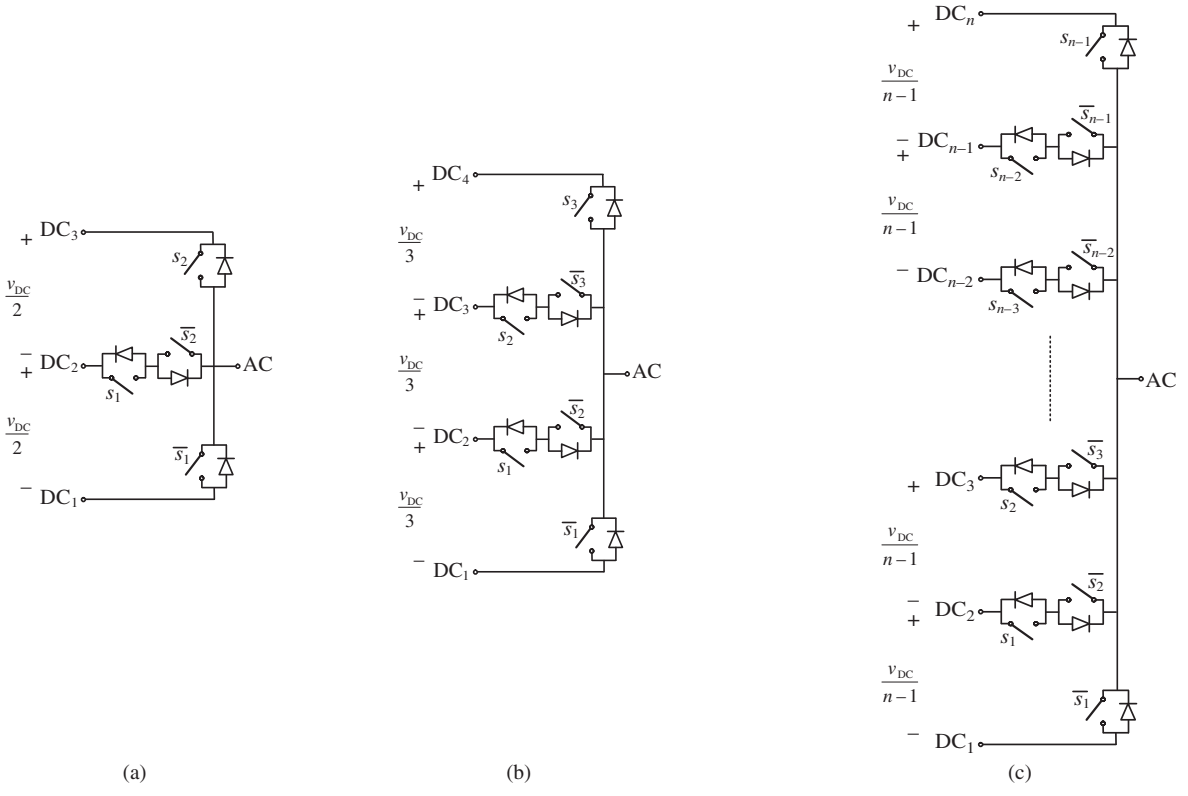


Figure 8. Reduced multilevel active-clamped (transistor-clamped) topology, also known as neutral-point piloted. (a) Three levels (T-type). (b) Four levels (π-type). (c) n levels.

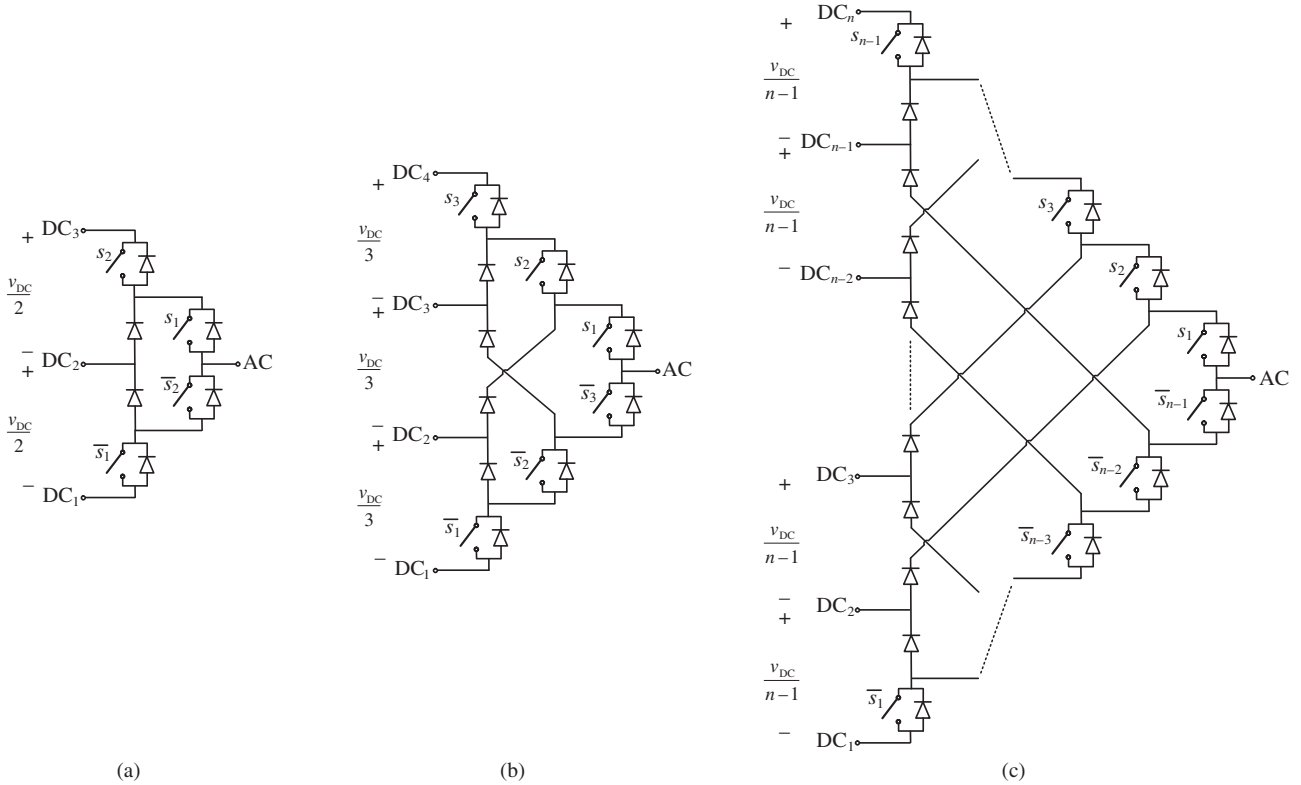


Figure 9. Reduced multilevel passive-clamped (diode-clamped) topology. (a) Three levels. (b) Four levels. (c) n levels.

Table 3. Switching States of an n-Level NPC Half-Bridge Leg

s_{AC}	AC terminal connection to	s_1	s_2	s_3	...	s_k	...	s_{n-2}	s_{n-1}	v_{AC}
1	DC_1	0	0	0	...	0	...	0	0	$-v_{DC}/2$
2	DC_2	1	0	0	...	0	...	0	0	$v_{DC}\cdot(3-n)/(2\cdot(n-1))$
3	DC_3	1	1	0	...	0	...	0	0	$v_{DC}\cdot(5-n)/(2\cdot(n-1))$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
k	DC_k	1	1	1	...	0	...	0	0	$v_{DC}\cdot(2k-1-n)/(2\cdot(n-1))$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
$n-1$	DC_{n-1}	1	1	1	...	1	...	1	0	$v_{DC}\cdot(n-3)/(2\cdot(n-1))$
n	DC_n	1	1	1	...	1	...	1	1	$+v_{DC}/2$

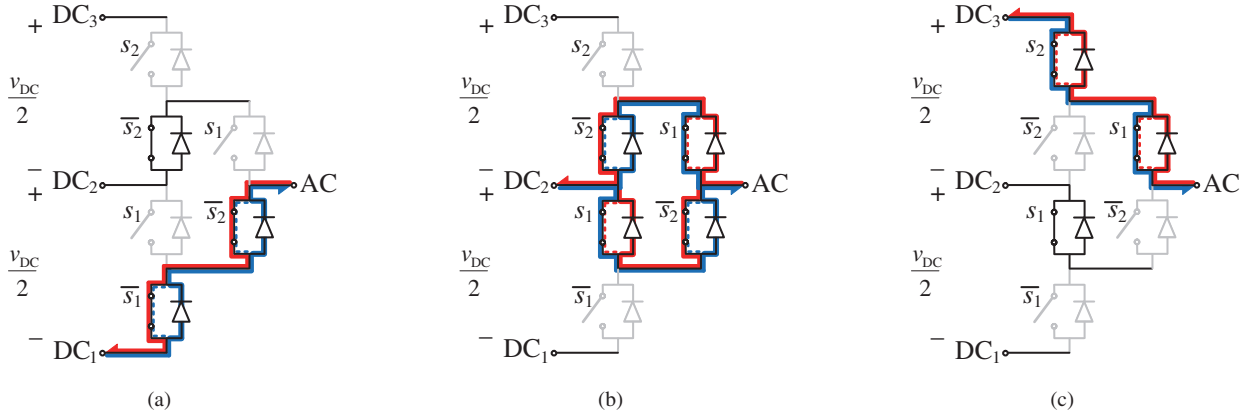


Figure 10. Switching states in the three-level active-clamped NPC topology. (a) $s_{AC}=1$. (b) $s_{AC}=2$. (c) $s_{AC}=3$.

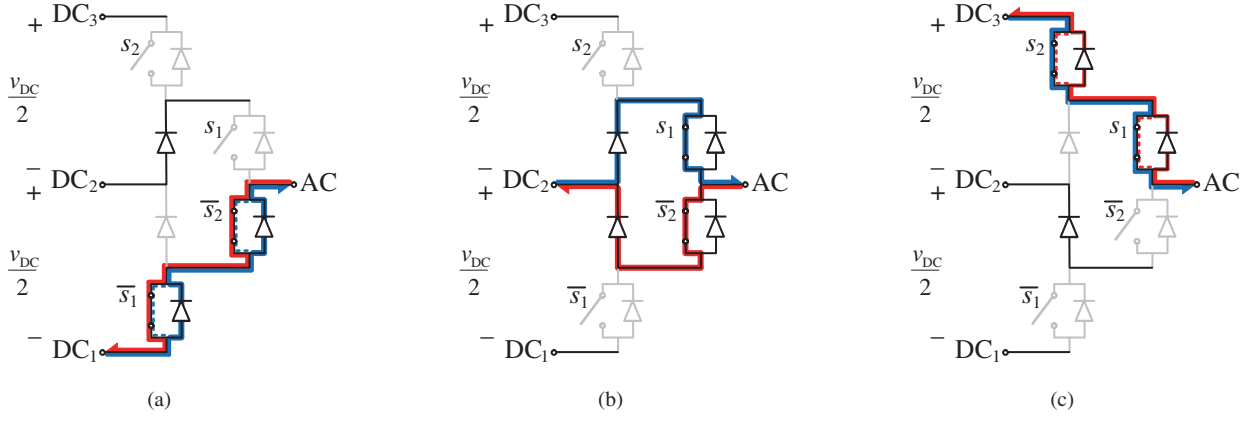


Figure 11. Switching states in the three-level diode-clamped NPC topology. (a) $s_{AC}=1$. (b) $s_{AC}=2$. (c) $s_{AC}=3$.

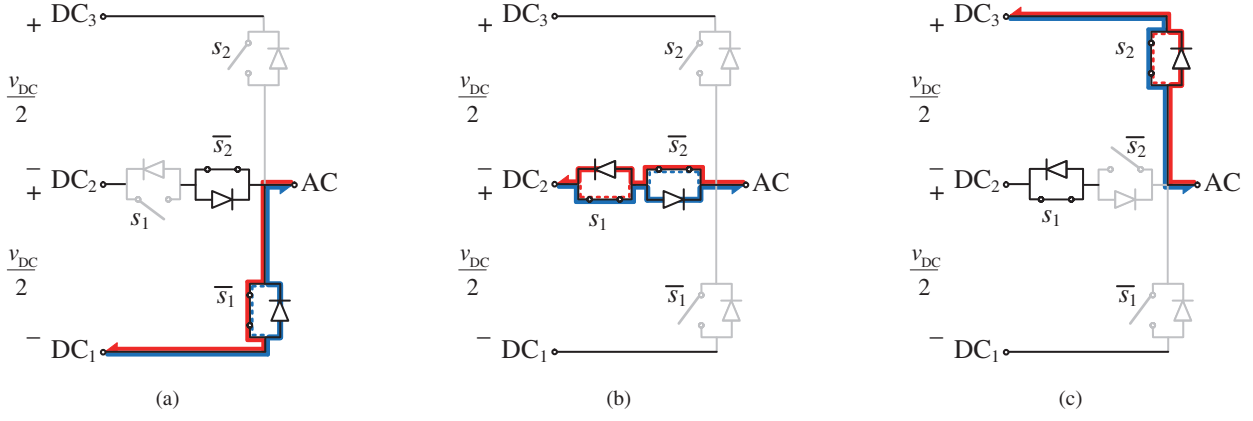


Figure 12. Switching states in the T-type NPC topology. (a) $s_{AC}=1$. (b) $s_{AC}=2$. (c) $s_{AC}=3$.

state transitions involve the turn-off of at least one switch and the turn-on of at least one switch. To prevent short circuits across DC-link terminals, turn-off transitions should precede turn-on transitions.

4. CONVERTER SWITCHING STATES

Similar to the two-level case, the NPC legs can be used to configure voltage-source multilevel single-phase and multiphase DC–AC converters, as shown in Figure 13. The converters are made up of one or more legs and feature bidirectional power flow. Each leg is functionally equivalent to a SPMT switch with n positions associated with the n leg switching states. Each particular combination of converter leg positions defines a *converter switching state*, which can be designated as (s_{AC1}, s_{AC2}, . . . , s_{ACp}). A converter featuring p n-level legs will therefore present n^p switching states. Each converter switching state produces a combination of leg AC terminal voltages: v_{AC1}, v_{AC2}, . . . , and v_{ACp}, whose values can be calculated from the leg positions s_{AC} according to equation 1. These AC terminal voltages can be then assigned to the coordinates of a vector in an orthogonal p-dimensional space, $\mathbf{V} = [v_{AC1}, v_{AC2}, \ldots, v_{ACp}]$, generating a vectorial representation of the converter switching states known as the converter *space vector diagram* (SVD). The SVD is simply a very convenient mathematical tool to represent all possible converter AC-terminal voltage states. In the following, the SVD of the different converters depicted in Figure 13 will be presented.

4.1. Single-Phase Single-Leg Converter

In this simple case, the converter features only one leg and the resulting SVD is unidimensional. Figure 14 shows the corresponding SVD for three levels, four levels, and the general n-level case. The n leg switching states produce n vectors. Figure 14 represents the tips of these vectors with a small circle along the normalized v_{AC} axis, according to the associated v_{AC} value.

4.2. Single-Phase Two-Leg Converter

In this case, the converter features two legs and the resulting SVD is bidimensional. Figure 15 shows the corresponding SVD for three levels, four levels, and the general n-level case. The vector associated with a given switching state is

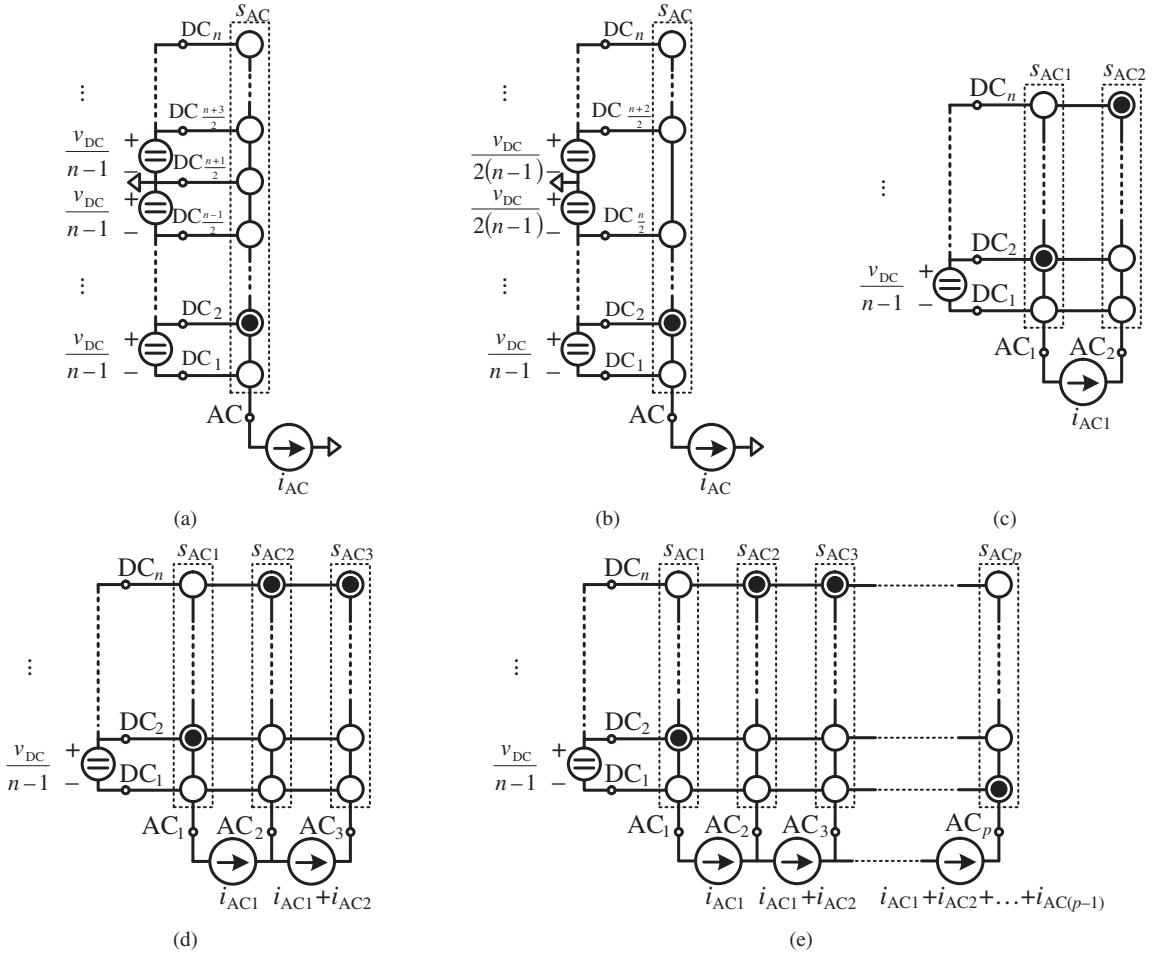


Figure 13. Voltage-source multilevel DC–AC converter configurations. (a) Single-phase with one leg (odd n). (b) Single-phase with one leg (even n). (c) Single phase with two legs. (d) Three-phase with three legs. (e) p-phase with p legs ($p > 3$).

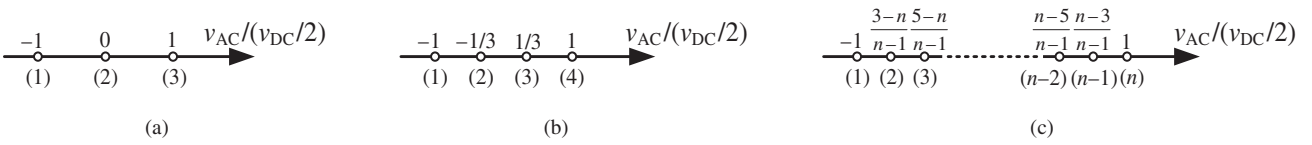


Figure 14. Space vector diagram (SVD) of a single-phase single-leg converter. The converter switching states are designated as (s_{AC}). (a) Three levels. (b) Four levels. (c) n levels.

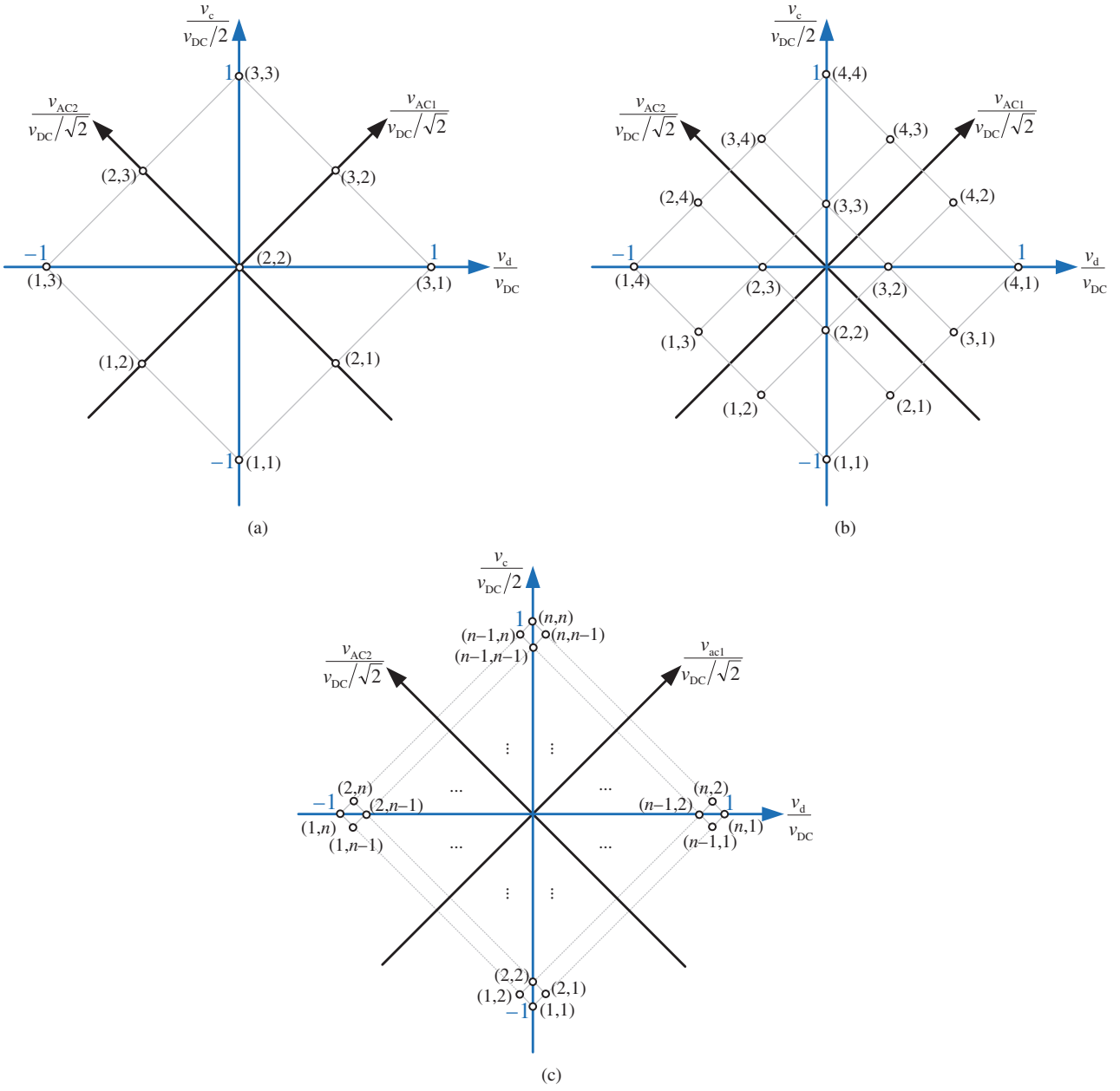


Figure 15. SVD of a single-phase two-leg converter. The converter switching states are designated as (s_{AC1}, s_{AC2}). (a) Three levels. (b) Four levels. (c) n levels.

determined assigning the corresponding AC terminal voltages (v_{AC1} and v_{AC2}), with a convenient normalizing factor, to an orthogonal frame (black axes in Figure 15). These vectors can also be expressed in other frames. A particularly interesting frame is the one formed by the two orthogonal blue axes of Figure 15. One of the axes is in the [1,1] direction, corresponding to the common-mode voltage

$$v_c = \frac{v_{AC1} + v_{AC2}}{2} \tag{2}$$

The second axis, orthogonal to the first, corresponds to the differential-mode voltage

$$v_d = v_{AC1} - v_{AC2} \tag{3}$$

Thus, the coordinates of the vectors in this new frame are proportional to the v_c and v_d associated with each vector. This is particularly convenient and informative, since it allows decoupling the effects of the voltage vector on the AC system. The main variables under control (such as the AC phase current) are only affected by v_d. Common-mode voltage v_c only modifies the average AC system voltage with reference to the DC-link. The effect of v_c on the AC system may be relevant (e.g., may induce bearing currents in AC motors), but it is often a secondary effect, and does not affect the main system functionality. For this reason, a simplified unidimensional version of the SVD is often presented, with all vectors projected to the v_d axis, as shown in Figure 16. From a differential-mode point of view, the converter presents $2n-1$ vectors, where some of these vectors have several associated switching states. The set of switching states associated with a given vector are designated as *redundant* converter switching states. For instance, in Figure 16a, switching states (1,1), (2,2), and (3,3) are redundant states producing a zero differential-mode voltage.

4.3. Three-Phase Three-Leg Converter

An analogous procedure can be followed to derive the SVD for a three-phase three-leg converter. In this case, the converter features three legs and the resulting SVD is tridimensional. The vector associated with a given switching state is determined assigning the corresponding AC terminal voltages (v_{AC1}, v_{AC2}, and v_{AC3}) with the same normalizing factor as in Figure 15 $\left(v_{DC}/\sqrt{2}\right)$ to the three axes of an orthogonal frame. Direction [1, 1, 1] defines the common mode axis, where the common mode voltage is defined as

$$v_c = \frac{v_{AC1} + v_{AC2} + v_{AC3}}{3} \tag{4}$$

The plane perpendicular to [1, 1, 1] is the differential-mode plane, defined by two independent axes corresponding to two independent differential-mode voltages. For instance,

$$\begin{aligned} v_{d1} &= v_{AC1} - v_{AC2} \\ v_{d2} &= v_{AC2} - v_{AC3} \end{aligned} \tag{5}$$

The projection of all vectors to the differential plane is of major interest, since this projection determines the contribution of each vector to generate differential-mode voltages. For this reason, the simplified two-dimensional SVD diagram of Figure 17 is often used for three-phase three-leg converters, avoiding the complexity of a three-dimensional representation. This simplified SVD contains $\left(1+6\cdot\sum_{k=1}^{n-1}k\right)$ vectors distributed in $n-1$ hexagonal rings (18). The number of redundant switching states increases from the outer to the inner hexagonal rings.

In some applications, the neutral point of the three-phase AC system is not isolated but somehow connected to the DC-link. In this case, the applied common-mode voltage becomes relevant, since it determines a nonnegligible common-mode current through the AC system, and the full tridimensional SVD is necessary to properly represent all relevant converter voltage states.

4.4. *p*-Phase *p*-Leg Converter

In the case of a p-phase converter with p legs, where $p > 3$, a p-dimensional SVD is generated. Direction [1, 1, . . . , 1] again corresponds to the common mode voltage axis, where

$$v_c = \frac{\sum_{k=1}^{p} v_{ACk}}{p} \tag{6}$$

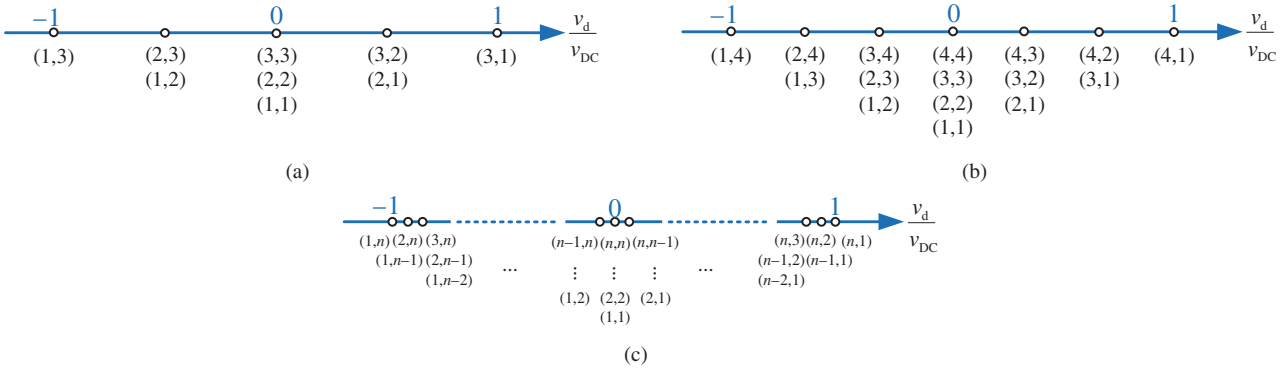


Figure 16. Simplified SVD of a single-phase two-leg converter with only differential-mode information. (a) Three levels. (b) Four levels. (c) n levels.

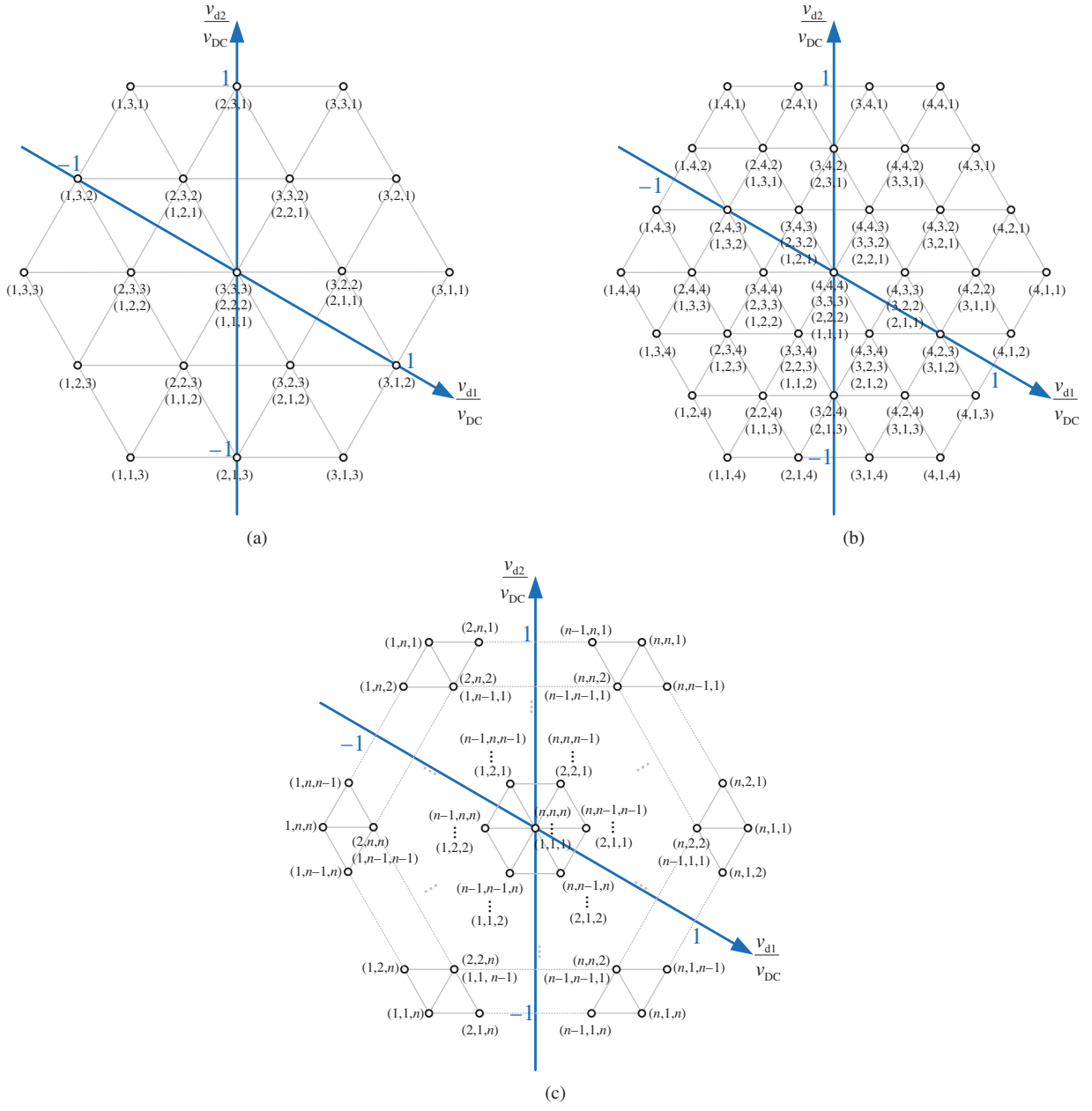


Figure 17. Simplified SVD of a three-phase three-leg converter with only differential-mode information. Converter switching states are designated as (s_{AC1}, s_{AC2}, s_{AC3}). (a) Three levels. (b) Four levels. (c) n levels.

The hyperplane perpendicular to the common-mode axis is the differential-mode hyperplane, defined by $p-1$ independent axes corresponding to $p-1$ independent differential-mode voltages. For instance,

$$v_{dk} = v_{ACk} - v_{AC(k+1)}; \quad k \in \{1, 2, \cdots, p-1\} \tag{7}$$

Although the graphical representation of this case becomes complex, the vectors can be easily represented and manipulated algebraically.

5. CONTROL STRATEGIES

As seen previously, an NPC DC–AC converter presents a number of converter switching states. A suitable sequence of such switching states needs to be determined to guarantee the desired power flow and the proper operation of the DC and AC subsystems. This sequence is determined by the converter control, understanding here control in a broad sense.

There are several control strategies applicable to NPC DC–AC converters that can be classified into two categories:

1. Strategies that determine the sequence of converter switching states in order to synthesize a given reference AC voltage, as a first step to reach the system main control goals.
2. Strategies that select the converter switching states most convenient to directly reach the system main control goals.

The next two subsections present the most common control strategies under each category.

5.1. Strategies Synthesizing a Reference AC Voltage

In the first category, the reference AC voltage is defined by the desired voltage for each converter leg AC terminal. Let us designate these voltages as $v^*_{AC1}, v^*_{AC2}, \ldots, v^*_{ACp}$, for a p-leg converter. These reference voltages define the so-called *reference voltage vector* $\mathbf{V}^*$ in the converter SVD. As discussed earlier, in an AC system with isolated neutral, only the differential-mode component of the converter-generated AC voltage affects the main AC-system electrical performance. Thus, only the differential-mode component of the reference vector is usually defined. This differential-mode component can be obtained in closed-loop control structures as the outcome of processing the error in the system control variables with proportional-resonant compensators (using stationary coordinates) or with proportional-integral compensators (using rotating coordinates). This is accomplished in the same manner as in a conventional two-level DC–AC converter.

In a single-phase system with one or two legs, the differential-mode component of the reference vector is a single coordinate along the normalized v_d axis. In steady state, this coordinate can be usually expressed as

$$\frac{v^*_d}{v_{DC}} = m \cdot \sin(\omega t) \tag{8}$$

where m is the so-called *modulation index* and ω is the angular frequency. Thus, $\mathbf{V}^*$ is a pulsating vector with amplitude m along the normalized v_d axis.

In a three-phase system with three legs, the differential-mode component of the reference vector is defined with two coordinates along the normalized v_d axes. In steady state, these coordinates can be usually expressed as

$$\begin{aligned} \frac{v^*_{d1}}{v_{DC}} &= m \cdot \sin(\omega t) \\ \frac{v^*_{d2}}{v_{DC}} &= m \cdot \sin\left(\omega t - \frac{2\pi}{3}\right) \end{aligned} \tag{9}$$

Thus, $\mathbf{V}^*$ is a rotating vector with constant length m along the differential-mode plane.

The strategies under this category approximate or synthesize the reference vector through a sequence of switching states. The approximation is performed from the reference vector trajectory over consecutive time intervals, while each strategy considers a different time span for these intervals.

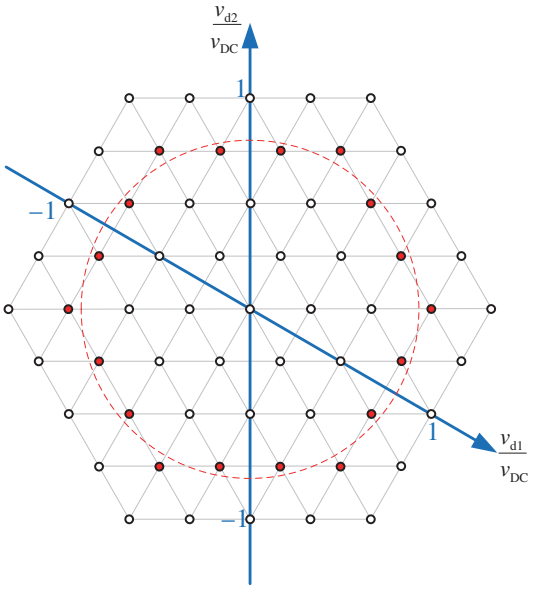


Figure 18. Space vector control in a five-level three-phase converter.

Space Vector Control. In *space vector control* or *nearest-vector control*, the reference vector is approximated on an instantaneous basis. At every point in time, the vector closest to the reference vector is selected. Figure 18 illustrates this strategy in a five-level three-phase converter. The steady-state circular reference vector trajectory is shown in dashed red. The closest space vector is selected at every point in time to approximate the reference vector. The different selected vectors along the trajectory are highlighted in red. If a common-mode voltage component of the reference vector is also specified, then, besides the SVD implementation approach, this strategy can also be implemented on a per leg basis through selecting the leg AC terminal voltage closest to the reference voltage, as illustrated in Figure 19. In this case, the strategy receives the name of *nearest-level control*.

In this strategy, the synthesized AC voltage contains a nonnegligible error at the fundamental component and

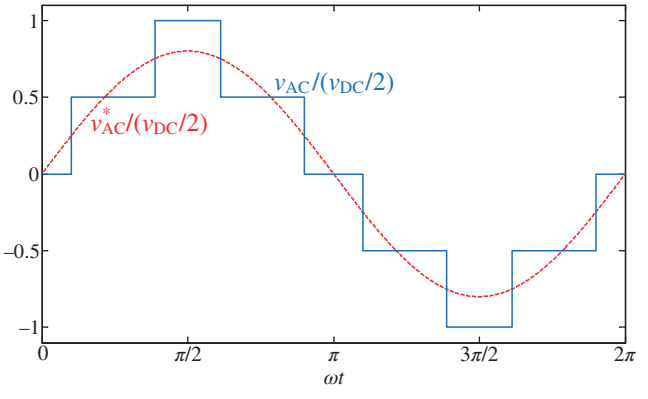


Figure 19. Nearest-level control in one leg of a five-level converter ($m = 0.8$).

contains low-frequency harmonic components, featuring a slightly increased total harmonic distortion (THD) and spread harmonic spectra compared with other control strategies. The error at the fundamental component decreases as the number of levels increases, since a denser SVD is available. Therefore, this strategy is usually applied in converters with a large number of levels.

Space Vector Modulation. In *space vector modulation* (SVM), a time span much smaller than the fundamental period, the so-called *switching period* (T_s), is defined. The reference vector is then approximated in every subsequent switching period, on average, through a sequence of converter space vectors

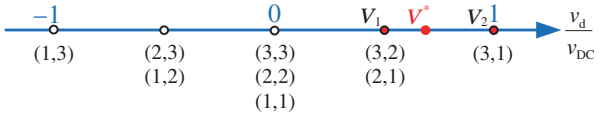
$$\frac{1}{T_s} \cdot \int_{k \cdot T_s}^{(k+1)T_s} \mathbf{V}^* \cdot dt = \sum_x \frac{T_x}{T_s} \cdot \mathbf{V}_x \tag{10}$$

where k and x are positive integers, $\mathbf{V}_x$ is one of the selected space vectors and T_x is the dwell time of $\mathbf{V}_x$ over the switching cycle. These dwell times should verify

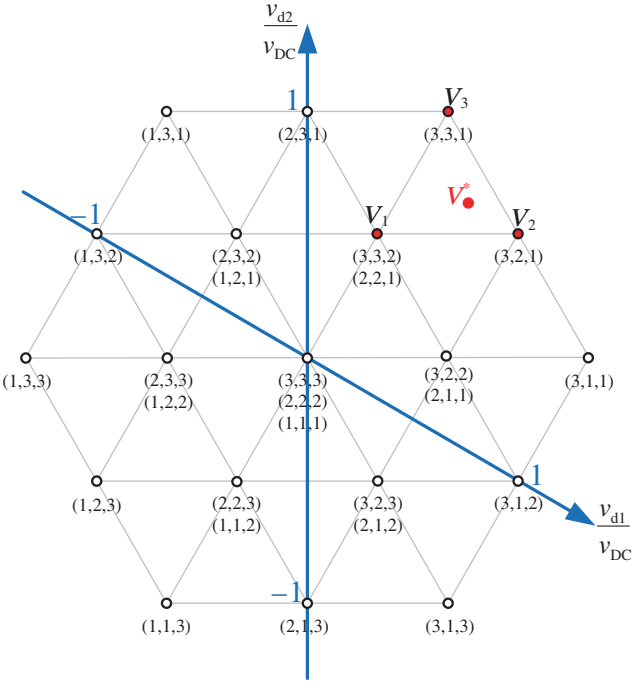
$$\sum_x T_x = T_s \tag{11}$$

To minimize the number of switching transitions, the minimum possible number of space vectors is often selected; that is, two vectors in single-phase converters, three vectors in three-phase converters, and so on. In addition, in order to minimize the error (harmonic distortion) in approximating the reference vector, those vectors closest to $\mathbf{V}^*$ are usually selected. Figure 20 illustrates the typical vector selection in a single-phase two-leg converter and in a three-phase three-leg converter. In Figure 20a, the nearest two vectors ($\mathbf{V}_1$ and $\mathbf{V}_2$) defining the segment where $\mathbf{V}^*$ is located are selected. In Figure 20b, the nearest three vectors ($\mathbf{V}_1$, $\mathbf{V}_2$, and $\mathbf{V}_3$) defining the triangle where $\mathbf{V}^*$ is located are selected. In case one of the selected vectors presents several associated redundant converter switching states, any combination of redundant switching states can be selected to implement such vector, by splitting the corresponding vector dwell time among all employed switching states. The final sequence of converter switching states applied over the switching cycle to approximate the reference vector is arranged to minimize the number of leg switching-state transitions.

Despite its apparent complexity, SVM strategies can be often implemented through the comparison of one or more modulating signals with one or more triangular carrier signals per leg. For example, Figure 21 shows the sinusoidal modulating waveform and two level-shifted carriers per leg used to implement a basic strategy known as sinusoidal pulse width modulation (PWM) in a three-level converter. The n-level case requires one sinusoidal modulating waveform and $n-1$ level-shifted carriers per leg. The modulating signals of all legs are phase-shifted $2\pi/p$, where p is the number of legs. A value of the carrier-to-modulating signal frequency ratio equal to an odd integer of the number of legs leads to a reduced line-to-line AC voltage harmonic distortion. At every point in time, the leg position is $s_{AC} = 1+y$, where y is the number of carriers below the



(a)



(b)

Figure 20. Typical vector selection in SVM to approximate the reference vector in a switching cycle. (a) Nearest two vectors in a single-phase two-leg converter. (b) Nearest three vectors in a three-phase three-leg converter.

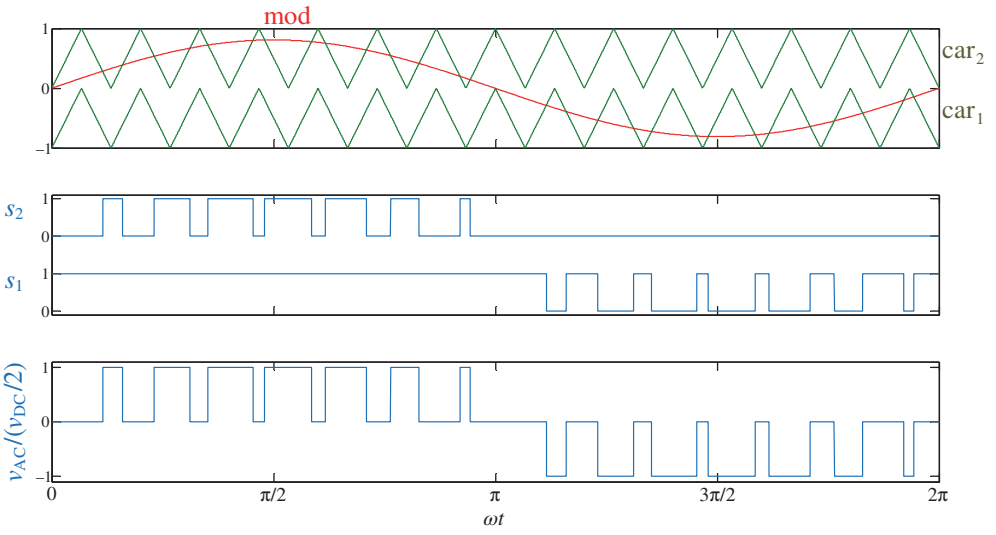


Figure 21. Sinusoidal PWM strategy in a three-level DC–AC converter: per leg modulating and carrier signals, switch control signals, and the resulting leg AC voltage ($m = 0.7$).

modulating signal. The switch control signals s_1, s_2, . . . , s_{n-1} can be directly obtained through the comparison of the modulating signal with each of the carriers. The sinusoidal PWM strategy is a specific SVM strategy employing the minimum number of nearest vectors (nearest two vectors in single-phase converters, nearest three vectors in three-phase converters, etc.) with the added constraint that the switching-cycle average common-mode voltage is equal to zero. This constraint restricts the maximum peak fundamental line–line voltage achievable in three-phase converters in the linear modulation range to $\left(\sqrt{3}/2\right)V_{\mathrm{DC}}$. Adding a common-mode voltage allows increasing this maximum peak voltage to V_{DC}, as in the case of Figure 22, corresponding to a nearest-three-vector strategy for a three-level three-phase converter, with an added normalized common-mode voltage equal to

$$\mathrm{mod}_c = -\frac{\mathrm{mod}_{\max} + \mathrm{mod}_{\min}}{2} \tag{12}$$

where $\mathrm{mod}_{\max}$ and $\mathrm{mod}_{\min}$ are the maximum and minimum values of the three original sinusoidal modulating signals, respectively.

Other values of the common-mode voltage are also possible, which correspond to other nearest-three-vector strategies. If at a given switching cycle, the added common-mode voltage forces that one modulating signal reaches its maximum or minimum values (1 or −1), then the

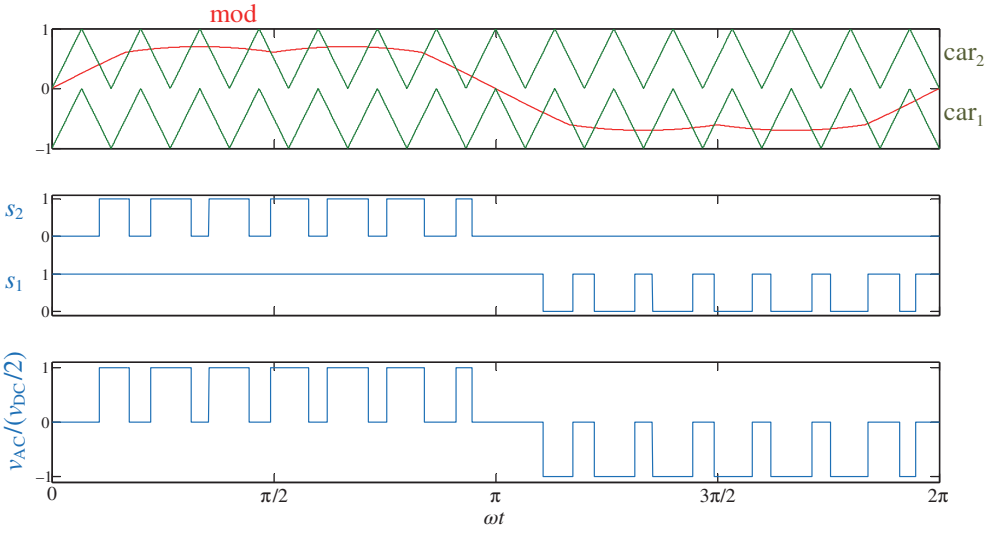


Figure 22. Carrier-based implementation of a specific nearest-three-vector SVM with maximum line-to-line voltage in the linear modulation range for a three-level three-phase converter ($m = 0.7$).

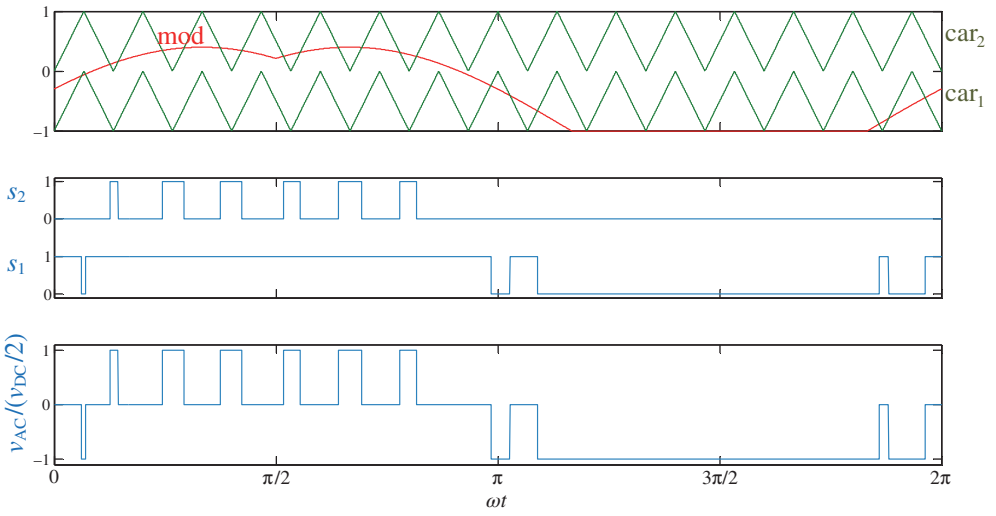


Figure 23. Carrier-based implementation of a specific nearest-three-vector discontinuous SVM for a three-level three-phase converter ($m = 0.7$).

corresponding leg stops switching, reducing the number of switching transitions and associated losses. The strategies presenting this feature are typically designated as *discontinuous* PWM strategies. Compared with *continuous* PWM strategies, the number of switching transitions is reduced at the expense of increasing the AC voltage harmonic distortion (18). Figure 23 presents a simple example of discontinuous PWM strategy, where an offset has been added to all three original sinusoidal modulation signals in order to clamp, at every point in time, the minimum modulating signal to −1.

Programmed Pulse Width Modulation. In the *programmed PWM* approach, a sequence of space vectors is selected to approximate the reference vector trajectory over a full fundamental cycle, where the reference vector has been conformed with balanced and sinusoidal reference differential voltages. For simplicity, the vector sequence produces the same voltage waveform but phase-shifted in all leg AC terminals. This leg AC terminal voltage waveform usually presents quarter-wave symmetry. Figure 24 shows an example of such voltage waveform in the case of a three-level converter. The N independent switching angles (α_k) over the first quarter represent the degrees of freedom available to shape the converter AC voltage. One of the degrees of freedom is used to adjust the fundamental component amplitude, and the remaining can be used for different purposes. A typical objective consists on

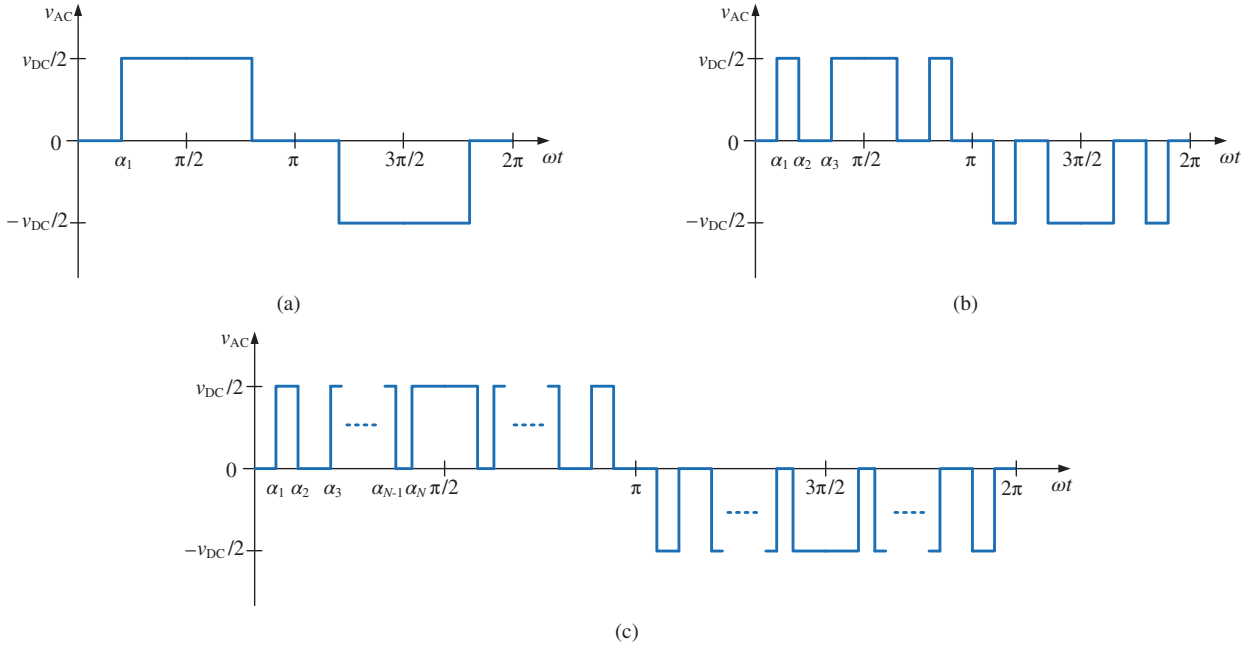


Figure 24. Three-level leg AC voltage pattern with quarter-wave symmetry. (a) One independent switching angle leading to three-level *staircase modulation*. (b) Three independent switching angles. (c) General case with N independent switching angles.

eliminating $N-1$ harmonics, leading to a technique known as *selective harmonic elimination* (19). A system of N nonlinear equations in terms of trigonometric functions of the switching angles results from imposing a specific fundamental component amplitude and the elimination of $N-1$ harmonics. This system of equations usually needs to be solved offline using numerical methods. In addition, there may not be solution, there might be one solution, or there might be several solutions. This implies an increased complexity compared with the previous methods. On the other hand, since the time span for the approximation is a full line cycle, this strategy usually leads to closed-loop controls with limited dynamical performance (20).

The available degrees of freedom can also be employed to mitigate a number of harmonics rather than eliminating them, leading to a technique known as *selective harmonic mitigation*. This is of interest to meet regulations where certain harmonic amplitude is allowed, and thus, it is not necessary to fully eliminate them. The degrees of freedom can also be used to minimize the waveform total harmonic distortion, and so on.

5.2. Other Strategies

In the following, the two most common strategies that select the converter switching states most convenient to directly reach the system main control goals, without the need to operate with a reference AC voltage, are briefly described.

Hysteresis Control. In *hysteresis control*, a value over time of the target control variable is specified, together with a suitable hysteresis band. Whenever the measured control variable surpasses the hysteresis band limit, a new converter switching state is selected in order to keep the control variable within the band. This converter switching state is kept until the control variable hits the upper or lower limit again. This is the type of control used in *direct torque control* (motor drive application) and *direct power control* (grid-connected inverter application). The main drawback of this control strategy is its inherent variable switching frequency and disperse harmonic spectrum unless a variable hysteresis band is used.

Predictive Control. In *finite-control-set model predictive control*, a cost function dependent on the converter switching states is defined based on a system mathematical model. Then, in every successive switching or sampling cycle, the cost function is evaluated for every converter switching state and the converter switching state that minimizes the cost function is selected. This strategy also inherently leads to a variable switching frequency and spread harmonic spectrum, although several modifications of the technique allow palliating this effect.

6. DC-LINK CAPACITOR VOLTAGE BALANCING

Whenever the DC-link of an NPC converter is configured with a capacitor voltage divider (i.e., a series connection of capacitors), an inherent problem of this topology emerges: the DC-link capacitor voltage balancing. The connection of the converter legs to the inner DC-link points involves the injection of inner DC-link currents that modify the capacitor voltage balance. This is illustrated in the case of a three-level converter in Figure 25a. The inner DC-link current i_{DC2} is directly proportional to the derivative of the capacitor voltage unbalance as

$$\begin{aligned} i_{DC2} &= i_{Cu2} - i_{Cd2} = C \cdot \frac{dv_{DC3,2}}{dt} - C \cdot \frac{dv_{DC2,1}}{dt} \\ &= C \cdot \frac{d\left(v_{DC3,2} - v_{DC2,1}\right)}{dt} = C \cdot \frac{dv_{unb2}}{dt} \end{aligned} \tag{13}$$

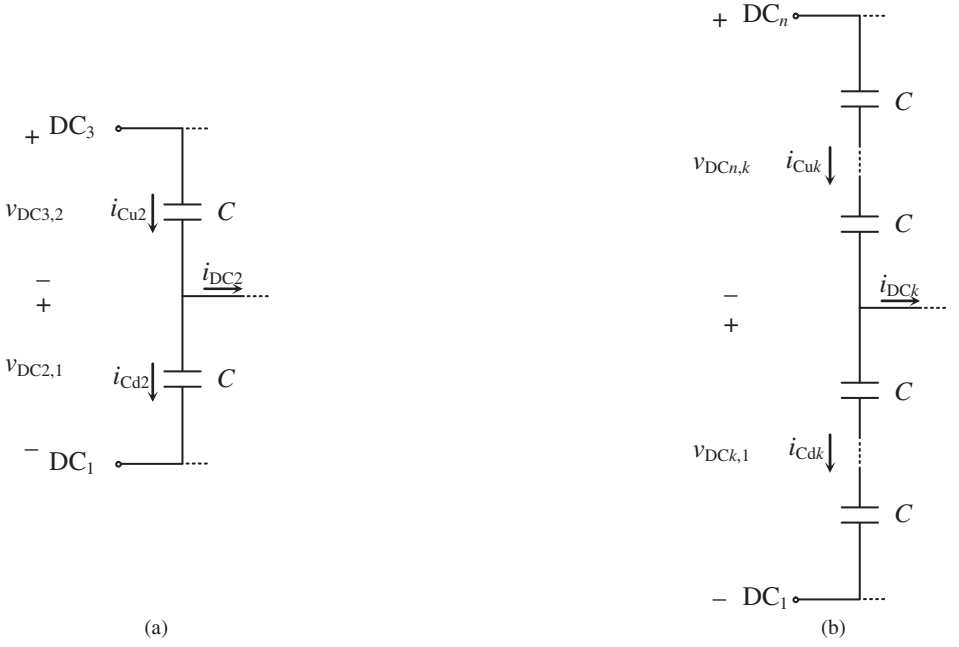


Figure 25. Effect of inner DC-link current on DC-link capacitor voltage balance. (a) Three-levels. (b) General n-level case.

The extension to the general n-level case is illustrated in Figure 25b, where the k-th DC-link current is proportional to the derivative of the unbalance between two normalized partial DC-link voltages according to

$$\begin{aligned} i_{\mathrm{DC}k} &= i_{\mathrm{Cu}k} - i_{\mathrm{Cd}k} = \frac{C}{n-k} \cdot \frac{\mathrm{d}v_{\mathrm{DC}n,k}}{\mathrm{d}t} - \frac{C}{k-1} \cdot \frac{\mathrm{d}v_{\mathrm{DC}k,1}}{\mathrm{d}t} \\ &= C \cdot \frac{\mathrm{d}\left(\frac{v_{\mathrm{DC}n,k}}{n-k} - \frac{v_{\mathrm{DC}k,1}}{k-1}\right)}{\mathrm{d}t} = C \cdot \frac{\mathrm{d}v_{\mathrm{unb}k}}{\mathrm{d}t}. \end{aligned} \tag{14}$$

Under a preexisting capacitor voltage balance condition, this balance will be lost unless zero instantaneous inner DC-link currents can be forced. This is not usually feasible, since the connection of the converter legs to the inner DC-link points in general involves non-zero instantaneous inner DC-link currents. However, if zero average inner DC-link currents (i.e., zero net charge drawn from the inner DC-link points) can be guaranteed over a given period of time, a balanced condition will be regained at the end of this period. This will keep the average capacitor voltages balanced (more precisely, this occurs if the capacitor voltages at the beginning of the averaging period match their average values or if capacitor voltage ripple can be neglected). Thus, the main condition to maintain capacitor voltage balance is stated as forcing all average inner DC-link currents equal to zero. The period of time considered for the averaging can vary from a switching cycle to a full line cycle or beyond. The longer the period of time, the higher the required capacitance to keep the voltage ripple within the desired limit.

The solutions to the capacitor voltage balancing problem can be classified as hardware and software solutions. Hardware solutions consist of adding additional hardware to guarantee the balance. Within this category, one solution consists of adding balancing circuits that generate an inner DC-link current that compensates the current produced by the NPC converter. Another solution consists of operating in a back-to-back converter configuration, where the inner DC-link current introduced by both converters into the common DC link compensate each other.

Software solutions consist of defining a converter control that guarantees average inner DC-link currents equal to zero. To illustrate the simple three-level case, Figure 26 indicates within square brackets the neutral-point current associated with each switching state for the single-phase and three-phase cases. The converter control should produce a sequence of switching states that guarantees capacitor voltage balance. In nearest vector SVM, this can be accomplished thanks to the different effect that redundant switching states have on capacitor voltage balance. In every switching cycle, the most convenient combination of redundant switching states is selected to force a zero neutral-point current, on average over the switching cycle. However, although this approach guarantees DC-link capacitor voltage balance in the three-level single-phase case over the full converter operating conditions, this is not true in the three-level three-phase case: for high modulation indexes and low AC-side power factors, the balancing in every switching cycle is not possible, leading to capacitor voltage oscillations at three times the fundamental frequency (i.e., capacitor voltage balance is achieved on average over one third of a fundamental cycle). For a number of levels higher than three in nearest vector SVM, the difficulty in achieving capacitor voltage balancing increases and some of the capacitor voltages collapse under a wide operating range. In a single-phase

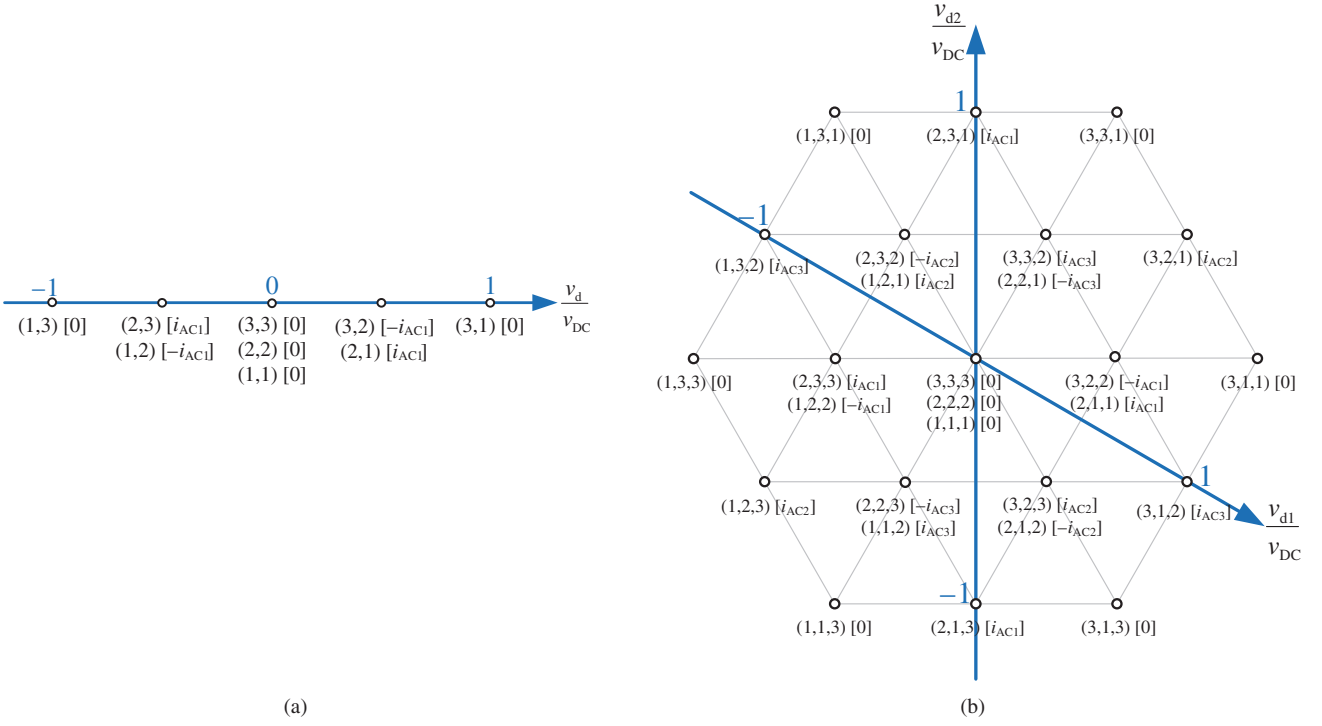


Figure 26. Three-level SVD with indication of the neutral-point current associated with each switching state. (a) Single-phase two-leg converter. (b) Three-phase three-leg converter.

two-leg converter with more than three levels, the unfeasible region at least includes (21)

$$m > \frac{2}{\pi \cdot |\cos(\phi)|} = \frac{0.637}{|\cos(\phi)|} \tag{15}$$

where ϕ is the displacement angle between the fundamental component of the leg AC voltage v_{AC} and leg AC current i_{AC}. In a three-phase three-leg converter with more than three levels, the unfeasible balance region at least includes (21)

$$m > \frac{\sqrt{3}}{\pi \cdot |\cos(\phi)|} = \frac{0.551}{|\cos(\phi)|} \tag{16}$$

Thus, it can be concluded that the operation under nearest-vector SVM is in general not feasible for a wide operating range of a single NPC DC–AC converter with a DC-link passively configured through a series connection of capacitors.

Nevertheless, other SVM strategies can be conceived to overcome the capacitor voltage balance problem over the full operating range. This is the case of so-called *virtual* SVM strategies. A new set of space vectors, the *virtual vectors*, is defined as a linear combination of certain switching states. Each virtual vector features a zero neutral-point current in average over the switching cycle. Therefore, if the reference vector is synthesized with these virtual vectors, the capacitor voltage balance will be guaranteed in every switching cycle. Figure 27 shows a possible set of virtual vectors in the first sextant of a three-level three-phase converter SVD (22). The remaining sextants are analogous due to symmetry. In every switching cycle, the reference vector is approximated with the three virtual vectors defining the triangle where the reference vector is located, as illustrated in Figure 27. The duty cycle assigned to each virtual vector is then evenly distributed among the associated converter switching states. For the sake of simplicity, this virtual SVM can also be carrier-based implemented. In the three-level three-phase case, two modulating waveforms per leg are compared with a single triangular carrier, as depicted in Figure 28. At every point in time, the leg position is $s_{AC} = 1 + y$, where y is the number

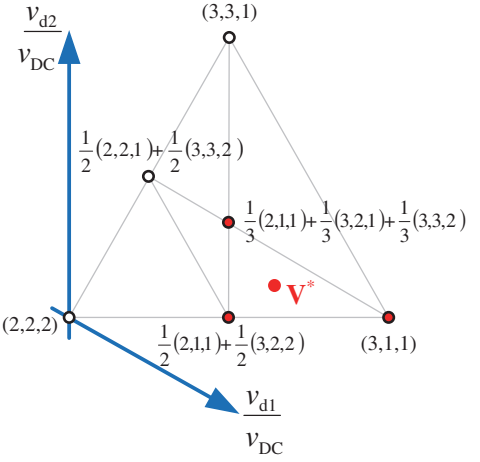


Figure 27. Virtual vectors for the first sextant of the SVD of a three-level three-phase converter.

of modulating waveforms below the carrier. The leg switch control signals can also be easily obtained from the comparison of the modulating waveforms with the carrier. Control signal s_1 is obtained from the comparison of mod_1 with the carrier. Control signal s_2 is obtained from the comparison of mod_2 with the carrier. The virtual SVM and its carrier-based implementation can be easily extended to converters with any number of levels and phases (23), enabling control strategies that guarantee capacitor voltage balance in every switching cycle for all operating conditions, although at the expense of an increased number of switching transitions and AC voltage harmonic distortion compared with nearest-vector SVM. Therefore, the operation of NPC DC–AC converters with any number of DC levels and AC phases is feasible in the full operating range with a DC-link passively formed by a series connection of capacitors. In the general n-level multiphase case, the carrier-based implementation of virtual SVM strategies can be performed with $n-1$ modulating waveforms and one carrier per leg.

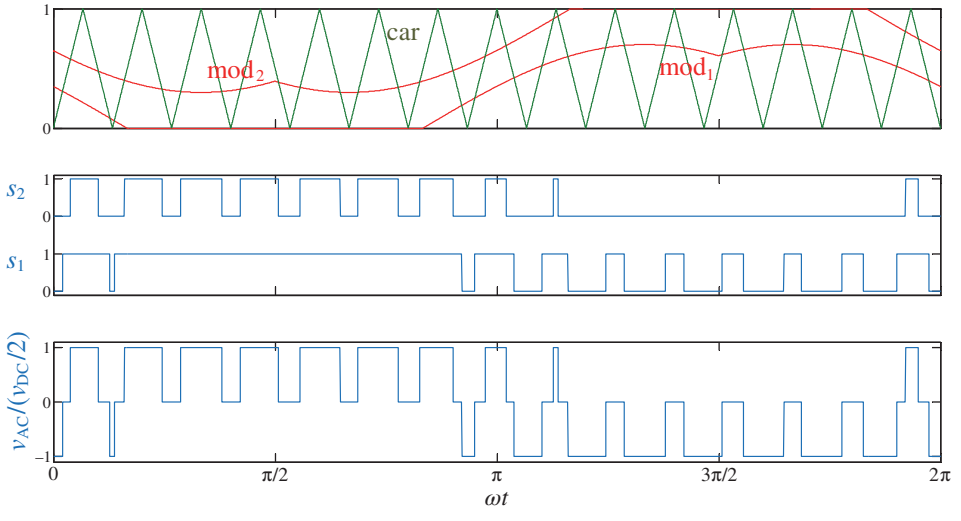


Figure 28. Carrier-based implementation of the virtual-vector SVM defined in Figure 27 ($m = 0.7$).

7. CONCLUSION

This article has reviewed the fundamentals of multilevel multiphase NPC DC–AC power converters: active- and passive-clamped leg topologies, converter topologies, leg switching states, converter switching states, and main control strategies together with a discussion of the DC-link capacitor voltage balancing problem and the different approaches to solve it. Compared with other multilevel topologies, NPC converters offer the potential advantage of a higher power density, since the converter legs do not require bulky passive components storing energy (inductors or capacitors), and the DC-link formed by a series connection of capacitors is shared by all converter legs.

To fully exploit this potential advantage and to improve the performance of these converters, further research is needed to determine, for each application, optimal leg configurations (including the selection of homogeneous or heterogeneous power semiconductor devices within each leg), suitable integration techniques to implement these legs, optimal leg switching states, optimal transitions between switching states, and optimal control strategies, all with the objectives of achieving higher power density, higher efficiency, reducing the converter harmonic distortion, achieving DC-link capacitor voltage balancing, improving the converter reliability, and extending the converter fault-tolerance capacity. An important challenge related to many of the above objectives is to achieve an even distribution of power losses through the leg structure.

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LIST OF ABBREVIATIONS

AC	alternating current
DC	direct current
IGBT	insulated-gate bipolar transistor
IGCT	integrated-gate commutated thyristor
MOSFET	metal-oxide-semiconductor field-effect transistor
NPC	neutral-point clamped
PWM	pulse width modulation
SPDT	single-pole double-throw
SPMT	single-pole multiple-throw
SPST	single-pole single-throw
SVD	space vector diagram
SVM	space vector modulation.

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