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Effects of clock deviations on the performance of microgrids based on virtual synchronous generators

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Abstract

An inverter-based microgrid is a small-scale power network governed by a distributed control system. In this system, the nodes are the digital controllers of the power inverters, normally located at separate points within the microgrid. A relevant issue is that these controllers operate at different frequencies due to inherent clock deviations in the local hardware oscillators. This paper evaluates the effects of these clock deviations on the performance of microgrids equipped with inverters that emulate the operation of synchronous machines. A systematic procedure is presented to derive steady-state expressions of the inverter active power and microgrid frequency as a function of clock drift rates. This procedure is applied to swing and governor equations of the virtual synchronous generators, revealing the mechanism that allows clock drifts to be absorbed, making their presence negligible. In addition, it allows recognising the controllers that should never be implemented in a distributed control system, since they cause an unsatisfactory behaviour that can even lead to a blackout in the microgrid. Therefore, the relevance of this study is the identification of the control schemes that are most sensitive to clock drifts, which makes it easier to choose the most suitable control implementation for a particular application. Furthermore, technical guidelines are reported to help researchers on developing control solutions more robust to clock drifts. In this study, the theoretical results are validated by experimental tests in a laboratory microgrid.

1 | INTRODUCTION

Power inverters are essential elements in microgrids. They are responsible for integrating energy sources by injecting the active and reactive power demanded by the control system. In this mode of operation, the inverters are known as grid-feeding inverters [1]. Conversely, as grid-forming inverters, they are responsible for interfacing storage devices to ensure adequate energy reserved in the system. In addition, in this mode of operation, they participate in the frequency control of the microgrid by collaborating in the power balance between generation and demand [2]. In the literature, there are two families of grid-forming inverters: the first one with inverters that base their operation on the droop method and, the second one with inverters that emulate the operation of synchronous machines. Some attempts have been made to find the equivalence between both

families with good results for the basic control implementations [3, 4]. Nowadays, the current trends in droop control are the development of distributed approaches for both frequency regulation and economic dispatch [5, 6]. In virtual synchronous generator (VSG) control, an emerging topic is the improvement of system inertia in order to satisfy the frequency transient-response requirements [7]. These different trends have motivated the development of both families along separate path, giving rise to algorithms with different compensators for droop and VSG control schemes [5–7].

As described above, the control schemes determine the mode of operation of inverters, as grid-feeding or grid-forming. These schemes are programmed in computing devices, mainly digital signal processors (DSP). These devices internally run with control signals synchronized by a crystal-based hardware oscillator. In this situation, clock drifts are unwanted variations in

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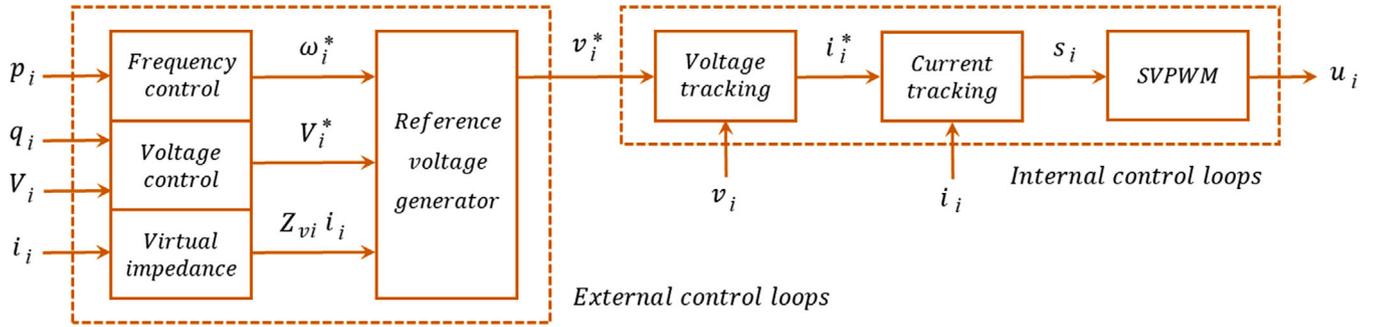


FIGURE 1 Control system of a grid-forming inverter

the oscillator frequency measured over time [8]. Due to clock drifts, slightly different clock frequencies are noticed in distributed DSPs [8]. Typical clock drift rates for these computing devices are less than about 20 parts per million (ppm) [9]. This small deviation causes different effects in microgrids. In grid-feeding inverters, the effect is negligible since the injected active and reactive powers coincide with their references. Therefore, the power supplied by the energy sources is independent of the clock drifts of the distributed DSPs. The main reason for this desired behaviour is that grid-feeding inverters do not participate in the regulation of the grid frequency [1]. In droop-based grid-forming inverters which interface energy sources, the impact is unequal. In systems equipped with only primary control layers, the droop method provides an accurate frequency and power sharing even in the presence of clock drifts [10, 11]. Conversely, the operation of the microgrid deteriorates in some cases when secondary control layers are activated for the reduction of steady-state errors in voltage and frequency in droop-based inverters. The worst cases identified correspond to inverters that do not use the communication system for secondary control purposes [12]. In particular, large deviations in steady-state power sharing were noticed in this scenario for droop-controlled grid-forming inverters subject to clock drifts, as reported in [13]. A partial solution to this problem, valid only for high-load conditions, was presented in [14]. The study in [13] also revealed that frequency and power sharing was good enough for communication-based secondary control schemes.

Focusing on VSG grid-forming inverters, it is worth mentioning that the impact of clock drifts on these inverters has not been studied in the literature. As noted above, the compensators used in the new algorithms of droop and VSG control are clearly different today [5–7]. That is why the impact of clock drifts on droop control (as in [12–14]) and VSG control (as in this paper) should be studied separately. Therefore, the novelty of this paper is the study of the clock drift effects on microgrids equipped with VSG grid-forming inverters. The four contributions of the study are

- (i) A classification of VSG schemes in three control families according to the response to clock drifts.
- (ii) A systematic procedure to derive theoretical expressions that characterize the performance of the microgrid in steady-state as a function of the clock drifts.

- (iii) A framework for identifying the mechanisms that allow clock drifts to be absorbed by control schemes.
- (iv) A set of technical guidelines to develop robust control schemes to clock drifts.

The rest of the paper is organised as follows: Section 2 reviews the control schemes of the VSG inverters according to the compensators used in the swing and governor equations. Section 3 models the control schemes as a function of the clock drift rates and derives the steady-state expressions of the active power and frequency. This section includes technical guidelines to develop robust solutions to clock drifts. Section 4 validates the theoretical study with experimental results in a laboratory microgrid. Section 5 is the conclusion.

2 | CONTROL SCHEMES OF VSG INVERTERS

Figure 1 shows the control system of a grid-forming inverter [1]. The subscript i in the variables denotes the number of the VSG inverter, going from 1 to n , being n the total number of VSG inverters in the microgrid. The system in Figure 1 is a cascading combination of external and internal control loops with specific control objectives. External control loops regulate the angular frequency ω_i and the amplitude V_i of the output voltage of inverter i by sharing the active p_i and reactive q_i powers supplied by the inverter [2, 5]. A virtual impedance Z_{vi} is included in the external control loops to improve both inverter controllability and online limitation of the inverter output current i_i [15, 16]. Internal control loops ensure fast tracking of both reference voltage v_i^* and reference current i_i^* with a typical transient response of approximately 100 times faster than external control loops [1]. The reference voltage for the voltage tracking loop v_i^* is generated by the reference angular frequency ω_i^* , reference amplitude V_i^* and the virtual impedance. Finally, the space-vector pulse-width modulator (SVPWM) generates the driving pulses of the inverter switches u_i from the duty cycle signals s_i provided by the current tracking loop.

Grid-forming inverters operate as synchronous generators when swing and governor equations are implemented in the frequency control block of Figure 1. Typical compensators used in

TABLE 1 Compensators in VSG inverters

Swing	Governor	Comm.-based	References
P	P	no	[17–20]
P	D	no	[21, 22]
P	I	no	[23, 24]
P	PI	no	[25, 26]
P	LPF(P)	no	[27–33]
P	LPF(PD)	no	[34]
P	LPF(PI)	no	[35, 36]
D	LPF(P)	no	[37]
D	LPF(PI)	no	[38]
P	C	yes	[39, 40]

these equations are listed in Table 1. In the swing equation, the damping effect in the active power is often emulated using a proportional (P) controller of the frequency error [17–36]. In some studies, a derivative (D) controller is used to accelerate the transient response of the virtual generator [37, 38]. Both P and D compensators introduce a steady-state frequency error when the governor equation is not equipped with an integral compensator [4, 23–26]. In the governor equation, the basic compensators are considered first, including P, D, integral (I), and proportional-integral (PI) [17–26]. The use of a low-pass filter at the output of a P, PD or PI compensator, hereafter referred to as LPF(P), LPF(PD) or LPF(PI), provides a degree of freedom in the design of these controllers and facilitates the achievements of their dynamic specifications [27–38]. All the compensators presented so far use only locally measured signals, which makes VSG inverters operate without communications. However, microgrid performance improves considerably with the exchange of locally measured signals between distributed controllers, as reported in [39, 40]. These last two studies are based on using the consensus (C) compensator in the governor equation, which requires the communication service for control purposes; see Table 1.

Table 2 shows the swing and governor equations with the particular implementation of each compensator. In these equations, the variables are written as a function of the local time t_i . On the one hand, the swing equation is responsible for providing virtual inertia to the inverter by emulating the operation of the synchronous machine. To achieve this end, it calculates the reference angular frequency ω_i^* as the integral of a linear combination of the errors in active power and angular frequency, where P_i^* is the reference active power and p_i the active power; see Table 2. The control parameters in these equations are the nominal angular frequency ω_0 , the inertia factor J_i and the damping factor D_i . Note the different role that D_i plays in the swing equations. It is a proportional gain in the equation with P compensator while it is a derivative gain in the equation with D compensator. On the other hand, the governor equation provides frequency control by calculating the reference active power that each inverter must supply. In Table 2, the implementation of the compensators P, D, I, PI, LPF(P), LPF(PD), LPF(PI), and C for the governor equation is shown. For these compensators, the control parameters are the proportional k_{Pj} , derivative k_{Dj} and integral k_{Ij} gains of the compensators, the low-pass-filter cut-off frequency ω_{LPFj} and the gain of the C compensator k_{Cj} . Note that almost all compensators use integral terms, including I, PI, LPF(P), LPF(PD), LPF(PI) and C. In this regard, it is worth mentioning that the LPF(PI) compensator has a double integral, with the output of the frequency error integral as an input to a second integral that provides the value of the reference power; see Table 2. In addition, in the C compensator, the input of the integral term is a combination of two terms: the frequency error and a weighted sum of the reference active powers. This second term is introduced to improve the power sharing between VSG inverters [39, 40]. As indicated in Table 1, the C compensator is the only one that uses control signals received by the communication service. In particular, it receives each P_j^*/D_j signal at a transmission rate of T_r . In this signal, j can take the values from 1 to n and $j \neq i$.

The presented control system has its computing devices located at separate points within the microgrid. The challenge with this control system is the presence of distributed integrals

TABLE 2 Compensators for swing and governor equations in VSG inverters

Equation	Compensator	Implementation
Swing	P	$\omega_i^*(t_i) = \omega_0 + \frac{1}{J_i \omega_0} \int (P_i^*(t_i) - p_i(t_i) + D_i(\omega_0 - \omega_i^*(t_i))) dt_i$
Swing	D	$\omega_i^*(t_i) = \omega_0 + \frac{1}{J_i \omega_0} \int (P_i^*(t_i) - p_i(t_i) + D_i \frac{d(\omega_0 - \omega_i^*(t_i))}{dt_i}) dt_i$
Governor	P	$P_i^*(t_i) = k_{Pj}(\omega_0 - \omega_i^*(t_i))$
Governor	D	$P_i^*(t_i) = k_{Dj} \frac{d(\omega_0 - \omega_i^*(t_i))}{dt_i}$
Governor	I	$P_i^*(t_i) = k_{Ij} \int (\omega_0 - \omega_i^*(t_i)) dt_i$
Governor	PI	$P_i^*(t_i) = k_{Pj}(\omega_0 - \omega_i^*(t_i)) + k_{Ij} \int (\omega_0 - \omega_i^*(t_i)) dt_i$
Governor	LPF(P)	$P_i^*(t_i) = \omega_{LPFj} \int (k_{Pj}(\omega_0 - \omega_i^*(t_i)) - P_i^*(t_i)) dt_i$
Governor	LPF(PD)	$P_i^*(t_i) = \omega_{LPFj} \int (k_{Pj}(\omega_0 - \omega_i^*(t_i)) + k_{Dj} \frac{d(\omega_0 - \omega_i^*(t_i))}{dt_i} - P_i^*(t_i)) dt_i$
Governor	LPF(PI)	$P_i^*(t_i) = \omega_{LPFj} \int (k_{Pj}(\omega_0 - \omega_i^*(t_i)) + k_{Ij} \int (\omega_0 - \omega_i^*(t_i)) dt_i - P_i^*(t_i)) dt_i$
Governor	C	$P_i^*(t_i) = k_{Ij} \int (\omega_0 - \omega_i^*(t_i)) + k_{Cj} \sum_{j=1}^n (\frac{P_j^*(t_i)}{D_j} - \frac{P_i^*(t_i)}{D_i}) dt_i$

that are calculated locally with computing devices with clock drifts [41]. This problem is analysed and discussed in detail in next section.

3 | THEORETICAL ANALYSIS

The four contributions of this paper are listed at the end of Section 1. All these contributions are presented in this section through a theoretical analysis of the microgrid.

3.1 | Model considering a global reference time

The analysis is based on considering a global time t for all the computing devices of the VSG inverters. Each local time can be expressed in terms of the global time as [10]

$$t_i = d_i t, \quad (1)$$

where d_i is defined as the clock drift rate. Ideally, $d_i = 1$. However, in practice, small deviations around this ideal value are noticed. In this study, the limits for the DSPs used in the laboratory microgrid are [9]

$$1 - 20 \text{ ppm} < d_i < 1 + 20 \text{ ppm}. \quad (2)$$

The assumptions for the analysis are listed below:

- (i) The frequency control loop forces the inverter to exactly follow the reference angular frequency $\omega_i(t_i) = \omega_i^*(t_i)$. In terms of global time, the angular frequency is written as [10]

$$\omega_i(t_i) = \frac{2\pi}{T_i} = \frac{2\pi}{d_i T} = \frac{\omega_i(t)}{d_i}, \quad (3)$$

where T_i and T are the periods of the sinusoidal signals (voltages and currents) of inverter i expressed in local and global times, respectively. Therefore, it is also true that

$$\omega_i^*(t_i) = \frac{\omega_i(t)}{d_i}. \quad (4)$$

- (i) The power balance equation relates the total power generated by the energy sources P_G , the total power in the loads P_L , the total power losses P_{loss} and the total power supplied by the storage devices. In this equation, this last term can be written as the contribution of the power supplied by each VSG inverter p_i . In this way, the power balance equation is expressed as

$$P_G + \sum_{i=1}^n p_i = P_L + P_{loss}. \quad (5)$$

- (ii) The properties of the communication system are ideal, so time delays and packet losses are considered negligible when analysing the effect of clock drifts on microgrid performance. Of course, these properties are important in the analysis of the dynamic response of the microgrid. For instance, excessive time delays in the communication network can lead the system to instability [41–43]. However, as shown below, the impact of clock drifts is identified in the theoretical analysis of the steady-state operation, that is, when all the variables involved remain in their equilibrium point. In this state, the assumption about the communication system presented in this point is valid, as reported previously in [10] and [11].

3.2 | Steady-state active power and frequency

Clock drifts move the position of the poles of the closed-loop system almost imperceptibly [12, 13]. Therefore, the impact of clock drifts must be analysed in steady-state operation. A systematic procedure to derive the steady-state expressions of the active power supplied by the VSG inverters $P_{i,ss}$ and the microgrid frequency ω_{ss} is presented below:

- (i) Write all the swing and governor equations as a function of the global time t by inserting (1) and (4) in the equations listed in Table 2.
- (ii) Particularize the above equations for steady state. Note that all VSG inverters operate at the same frequency

$$\omega_{i,ss} = \omega_{ss}. \quad (6)$$

because the steady-state frequency is a global variable in a power system [2, 5].

- (i) In steady state, the input of the integral term of a well-regulated system is 0 [44]. Apply this principle to the steady-state swing and governor equations obtained in the previous step. Following this principle, two set of equations as a function of $P_{i,ss}^*$, $P_{j,ss}^*$ and ω_{ss} are obtained

$$P_{i,ss} = f_{swi} \left(P_{i,ss}^*, \omega_{ss} \right), \quad (7)$$

$$P_{i,ss}^* = f_{gov} \left(P_{j,ss}^*, \omega_{ss} \right), \quad (8)$$

where f_{swi} and f_{gov} denote swing and governor equations, respectively. In other words, the steady-state values of the active power $P_{i,ss}$ and its reference $P_{i,ss}^*$ rely on the microgrid frequency ω_{ss} and the reference power of the other inverters $P_{j,ss}^*$. A special situation is observed in the governor equations using I and PI compensators. In these equations, the input of the integral term is the frequency error only; see Table 2. The same is true for the inner integral of the governor equation with the LPF(PI) compensator. In these three cases, the input of the integral term cannot be 0 in steady-state since the left-side of (9)

TABLE 3 Steady-state microgrid angular frequency

Family	Swing	Governor	Steady-state angular frequency ω_{ss}
1	P	P	$(\omega_0 \sum_{j=1}^n (D_j + k_{Pj}) - P_L - P_{loss} + P_G) / \sum_{j=1}^n \left(\frac{D_j + k_{Pj}}{d_j} \right)$
1	P	D	
1	P	LPF(P)	
1	P	LPF(PD)	
1	D	LPF(P)	
2	P	I	$\omega_0 \sum_{j=1}^n (k_{Ij} d_j) / \sum_{j=1}^n (k_{Ij})$
2	P	PI	
2	P	LPF(PI)	
2	D	LPF(PI)	
3	P	C	$\omega_0 \sum_{j=1}^n \left(\frac{1}{k_{Cj}} \right) / \sum_{j=1}^n \left(\frac{1}{k_{Cj} d_j} \right)$

TABLE 4 Steady-state active power supplied by the VSG inverters as a function of the clock drift rates

Family	Steady-state active power $P_{i,ss}$
1	$(P_L + P_{loss} - P_G) / \sum_{j=1}^n \left(\frac{D_j + k_{Pj}}{D_j + k_{Pj}} \right) \left(\frac{d_j}{d_j} \right) + \omega_0 (D_i + k_{Pi}) \left(1 - \sum_{j=1}^n (D_j + k_{Pj}) / \sum_{j=1}^n \left(\frac{D_j + k_{Pj}}{d_j} \right) \right)$
2	$(P_L + P_{loss} - P_G) / \sum_{j=1}^n \left(\frac{k_{Ij}}{k_{Ij}} \right) + \omega_0 \left(d_i - \sum_{j=1}^n (k_{Ij} d_j) / \sum_{j=1}^n (k_{Ij}) \right) \left(\frac{D_i + k_{Pi} + d_i k_{Pi}}{d_i} \right)$
3	$(P_L + P_{loss} - P_G) / \sum_{j=1}^n \left(\frac{D_j}{D_j} \right) + \frac{\omega_0 D_i}{nk_{Ci}} \left(1 - \sum_{j=1}^n \left(\frac{nk_{Ci}}{k_{Cj} d_j} \right) / \sum_{j=1}^n \left(\frac{1}{k_{Cj} d_j} \right) \left(1 + \frac{1}{nk_{Ci}} - \sum_{j=1}^n \left(\frac{D_j}{d_j} \right) / \sum_{j=1}^n \left(\frac{D_j}{d_j} \right) \right) \right)$

cannot be 0 simultaneously for all DSPs. The reason of this is that, in practice, the clock drift rates are different ($d_1 \neq d_2 \neq \dots \neq d_n$)

$$\omega_0 - \frac{\omega_{ss}}{d_i} \neq 0. \quad (9)$$

Note that (9) is obtained by inserting (4) and (6) in the integral term of the compensators in Table 2 with frequency error only; see the governor equations with I, PI and LPF(PI) compensators. Consequently, the output of these integral terms increase or decrease continuously over time depending on the sign of $\omega_0 - \omega_{ss}/d_i$

$$k_{Ii} \int \left(\omega_0 - \frac{\omega_{ss}}{d_i} \right) dt = k_{Ii} \left(\omega_0 - \frac{\omega_{ss}}{d_i} \right) t. \quad (10)$$

This situation is not repeated in the rest of governor equations with integral terms, that is, compensators LPF(P), LPF(PD) and C. In these three cases, the input of the integral is a linear combination of the frequency error and another term that depends on the reference power; see Table 2. This second term absorbs the impact of clock drifts, giving a very small error in active power, as will be seen in the next subsection. For this reason, the active power is properly regulated with LPF(P), LPF(PD) and C compensators, even though they use distributed integral terms. In other words, these compensators prevent the

continuous increase or decrease of the active power over time produced by clock drifts.

(i) Particularize the power balance equation for steady state

$$P_G + \sum_{j=1}^n P_{i,ss} = P_L + P_{loss}. \quad (11)$$

(ii) Solve the system of Equations (7), (8) and (11) for $P_{i,ss}$ and ω_{ss} .

Tables 3 and 4 show the results of applying this procedure to the VSG control schemes listed in Table 2.

4 | DISCUSSION

From the above analysis, VSG control schemes are classified in three families, which are defined in the left column of Table 3. The control schemes of each family share the same expressions of frequency and active power in steady state, as shown in Tables 3 and 4. Therefore, the elements of each family have a common response to clock drifts. Below is a discussion of the impact of clock drifts on these families.

As shown in Table 3, in family 1, the microgrid frequency deviates from the nominal value depending on the power

TABLE 5 Steady-state active power for $d_i = 1$

Family	Steady-state active power $P_{i,ss}$
1	$(P_L + P_{loss} - P_G) / \sum_{j=1}^n \left(\frac{D_j + k_{Ij}}{D_j + k_{Ij}} \right)$
2	$(P_L + P_{loss} - P_G) / \sum_{j=1}^n \left(\frac{k_{Ij}}{k_{Ij}} \right)$
3	$(P_L + P_{loss} - P_G) / \sum_{j=1}^n \left(\frac{D_j}{D_j} \right)$

balance. The compensators of this family produce this deviation, because they are not based on integral terms of the frequency error; see Table 2. In this family, the deviation is insignificant only when generation and consumption coincide, that is, $P_G = P_L + P_{loss}$. This condition is only possible in generators with a load following control strategy [45]. In microgrids with energy storage devices, this strategy is not advantageous and, therefore, this situation is not considered in this study. Consequently, notable frequency deviations are normally expected in family 1 when generation is higher than consumption or vice versa. However, in families 2 and 3, the frequency is independent of power balance, as shown in Table 3. This is because the compensators in these families use integral terms of the frequency error.

Active power has two terms in all families; see Table 4. The term on the left depends on the power balance, as expected for the correct distribution of power among grid-forming inverters. The term on the right is an offset produced by clock drifts. In fact, this offset disappears in the ideal situation where $d_i = 1$, for $i = 1, \dots, n$. Table 5 shows the steady-state active power in this situation. In this case, the only difference between families is that power sharing depends on different control parameters. This is not an important issue because the design of these parameters can be done in such a way that the same behaviour is achieved in the three families.

Returning to the discussion of the offset term in the active power, it is worth mentioning that in families 1 and 3 this term is negligible. In other words, the expressions in Tables 4 and 5 for families 1 and 3 nearly coincide. This point can be easily verified with a numerical example using the data presented in next section for the laboratory microgrid. However, for family 2, the offset is directly dependent on time through the term (see Table 4)

$$\omega_0 \left(d_i - \sum_{j=1}^n (k_{Ij} d_j) / \sum_{j=1}^n (k_{Ij}) \right) k_{Ii} t = \omega_0 e_i k_{Ii} t, \quad (12)$$

where e_i is an error defined between the clock drift rate d_i and an averaged term that takes into account the clock drift rate of all DSPs and the integral gains of the governor equations. The expression in (12) causes the active power to increase (if e_i is positive) or decrease (if e_i is negative) continuously, being the dominant term of the active power injected by the inverters belonging to family 2. From a practical point of view, this behaviour will inevitably lead to the shutdown of the inverters when they reach the limit for the maximum power, prob-

ably causing a blackout in the microgrid. Consequently, the control schemes of family 2 cannot be used in this application. It is worth mentioning that this practical problem was not previously reported in the operation of VSG inverters in microgrids.

4.1 | Technical guidelines to develop robust control schemes to clock drifts

Distributed integrals calculated using local DSPs can cause performance problems in networked control systems. This a common phenomenon formulated in a general framework in [44]. In microgrids, problems in droop-based grid-forming inverters arise in frequency regulation when the input of the distributed integrals is only based on the frequency error [12–14]. This phenomenon is observed again in this paper in the study of VSG grid-forming inverters; see the compensators I, PI and LPF(PI) in Table 2.

Several state-of-the-art control schemes alleviate this problem. The easiest way to do this is by using a low-pass filter, as in LPF(P) and LPF(PD) compensators. These implementations include the reference active power as an additional input to the integral, which absorbs the deviations caused by the clock drifts. A more sophisticated solution is the communication-based C compensator that uses the reference active power of the other inverters to compensate for practical differences between them.

Current research on VSG inverters focuses on improving the inertia of microgrids. New control schemes are needed to meet stringent transient response specifications. In this scenario, robustness is achieved by implementing distributed integrals with a combination of input terms that includes the frequency error and other terms responsible for absorbing the effects of clock drifts. The choice of these additional terms will mark the performance of the distributed control system. This study can be a guide for the synthesis of these new control schemes.

5 | EXPERIMENTAL VALIDATION

The theoretical results of this study can be summarised as

- (i) The active powers of VSG inverters with control schemes classified in family 2 diverge over time.
- (ii) The active powers of VSG inverters with control schemes classified in families 1 and 3 coincide in steady state.

In this section, these results are experimentally validated with tests conducted in a laboratory microgrid.

5.1 | Laboratory microgrid

Figure 2 shows the diagram of the laboratory microgrid. The grid-forming converters are represented as voltage sources and are connected to nodes 1 and 2 through a transformer. In these converters, the primary source is a DC source (Amrel, SPS800-19), which emulates the battery banks BAT1 and BAT2. The

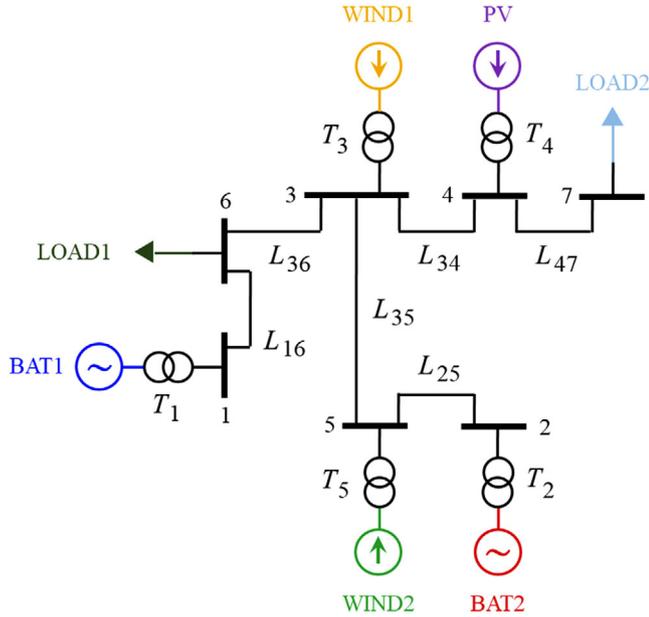


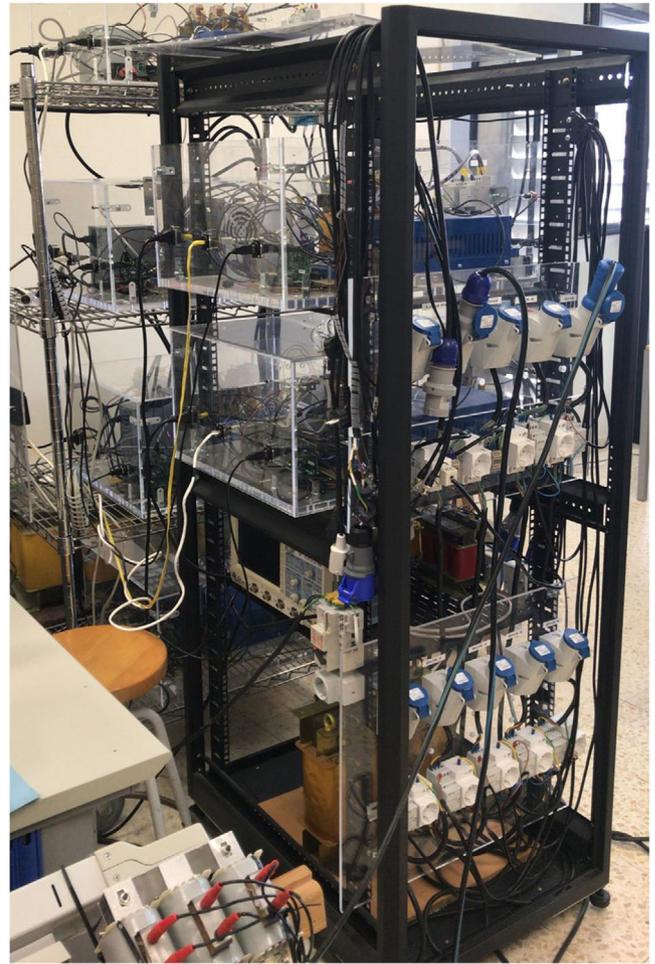
FIGURE 2 Diagram of the laboratory microgrid (the colour of each element identifies its experimental waveforms in Figures 4–8)

grid-feeding converters are represented as current sources and are connected to nodes 3, 4 and 5 also through a transformer. These converters were programmed to imitate the operation of wind ($WIND1$ and $WIND2$) and photovoltaic (PV) generators. Two loads are connected to nodes 6 and 7. The described setup is suitable for evaluating the impact of clock drifts in inverter-based microgrids [10–12]. The clock drift problem occurs in the distributed DSPs that control each of the five inverters considered. Primary sources can be emulated as in this setup or using real wind and PV sources, but in no case will they have an effect on the operation of the DSPs. Therefore, clock drift effects on microgrid response are independent of the nature of the primary sources.

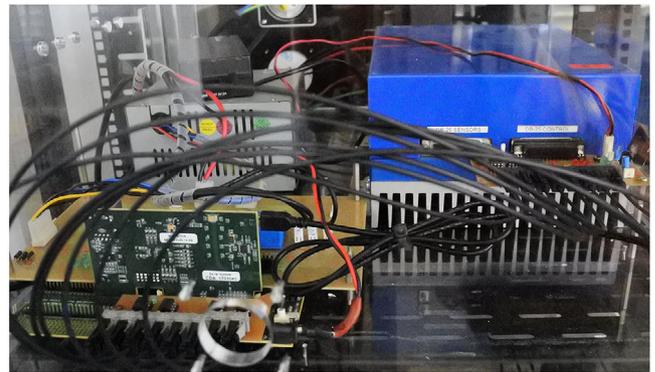
Figure 3 shows two photos with the complete microgrid setup and a detailed view of some components. The inverters were built with three-phase IGBT full-bridge configurations (Guasch, MTL-CBI0060F12IXHF); see blue boxes in Figure 3. Each inverter was controlled with a dual-core DSP, which is formed by a C28 control processor and a M3 communication processor (TI, Concerto F28M36P63C); see the vertical green card on the left side of Figure 3b. For control purposes, the communication among M3 processors was done through an Ethernet link with User Datagram Protocol (UDP)/Internet Protocol (IP). For monitoring purposes, the communication of the M3 processors with the supervisory personal computer was performed with Transmission Control Protocol (TCP)/IP.

5.2 | Details on the control implementation

The control system in Figure 1 was programmed in the C28 processors of the grid-forming inverters. The frequency control was implemented with the swing and governor equations shown



a



b

FIGURE 3 Photo of the laboratory microgrid. (a) Complete setup, (b) detail of one DSP, sensing board, and inverter

in Table 2. The voltage control is based on generating the reference voltage amplitude as follows [20]

$$V_i^*(t_i) = V_0 + k_{V_i} \int (-q_i(t_i) + E_i(V_0 - V_i(t_i))) dt_i, \quad (13)$$

where V_i is the amplitude of the inverter output voltage and V_0 its nominal value, q_i the reactive power supplied by the inverter, E_i the damping factor of the reactive power, and k_{V_i} the gain of the integral compensator. Note that (13) is

TABLE 6 Nominal values of the microgrid components

Symbol	Quantity	Nominal value
V_0	Phase-to-neutral voltage	155 V (peak)
ω_0	Angular frequency	2π 60 rad/s
V_{DC}	DC voltage at battery side	400 V
Z_1	Impedance of transformer T_1	$0.50 + j 0.38 \Omega$
Z_2	Impedance of transformer T_2	$1.95 + j 0.68 \Omega$
Z_3, Z_4, Z_5	Impedance of transformers T_3, T_4 and T_5	$1.13 + j 0.23 \Omega$
Z_{16}, Z_{35}, Z_{47}	Impedance of lines L_{16}, L_{35} and L_{47}	$0.04 + j 0.75 \Omega$
Z_{25}, Z_{34}, Z_{36}	Impedance of lines L_{25}, L_{34} and L_{36}	$0.02 + j 0.30 \Omega$
T_s	Sampling and switching period	100 μ s
T_r	Transmission period	100 ms
J_1, J_2	Inertia of swing equation	0.27 Ws/(rad/s) ²
D_1, D_2	Damping of swing equation	500 W/(rad/s)
k_{p1}, k_{p2}	Proportional gain of governor equation	1000 W/(rad/s)
k_{i1}, k_{i2}	Integral gain of governor equation	50 W/rad
$\omega_{L_{PF1}}, \omega_{L_{PF2}}$	Low-pass-filter cut-off frequency of governor equation	2π 1.2 rad/s
k_{C1}, k_{C2}	Consensus gain of governor equation	50
E_1, E_2	Damping of voltage equation	100 A
k_{V1}, k_{V2}	Integral gain of voltage equation	$0.2 (\text{As})^{-1}$
Z_{v1}, Z_{v2}	Virtual impedance	$j 3.77 \Omega$

similar to the swing equation with P compensator shown in Table 2, but in the voltage/reactive-power channel instead of the frequency/active-power channel. The reference voltage in Figure 1 was generated as [15]

$$v_i^*(t_i) = V_i^*(t_i) \sin(\omega_i^*(t_i) t_i) - Z_{vi} i_i(t_i), \quad (14)$$

where $Z_{vi} = \omega_i L_{vi}$ is the virtual impedance and L_{vi} is the virtual inductance. With the presented control schemes for frequency and voltage control, a dominant inductive impedance is needed to ensure controllability, which is achieved by the proper design of the virtual inductance L_{vi} [16]. The internal control loops in Figure 1 were programmed in stationary reference frame with proportional-resonant (PR) compensators. This choice is based on the excellent voltage and current tracking properties of these compensators for reference sinusoidal signals operating at fundamental frequency [1].

In grid-feeding inverters, the current tracking loop was also programmed in stationary reference frame using PR compensators. The reference current for this loop was calculated as [1]

$$i_i^*(t_i) = \frac{P_i^*(t_i)}{V_i(t_i)} v_i(t_i), \quad (15)$$

where v_i is the output voltage and V_i its amplitude. In (15), the reference power $P_i^*(t_i)$ is particularized for the wind and PV generators included in Figure 2 as P_{WIND1}^* , P_{WIND2}^* , and P_{PV}^* , respectively.

TABLE 7 Clock drift rates of DSPs for VSG inverters

DSPs	d_1	d_2
Pair 1	$1 - 12.7$ ppm	$1 + 15.2$ ppm
Pair 2	$1 - 12.7$ ppm	$1 + 11.3$ ppm
Pair 3	$1 - 12.7$ ppm	$1 + 6.6$ ppm
Pair 4	$1 - 12.7$ ppm	$1 + 0.9$ ppm

5.3 | Values of the microgrid components

Table 6 lists the nominal values of the microgrid components, including microgrid voltage and frequency, DC voltage at battery side, parasitic elements of transformers and power lines, sampling, switching and transmission periods, and control parameters of grid-forming inverters (with subscripts 1 and 2).

The experimental results presented in the next sections were obtained using several pairs of DSPs. These pairs were formed by always keeping the same DSP for inverter 1 and changing the DSP device for inverter 2. In this way, a rich set of practical experiences was achieved due to the different clock drift rates for DSP2.

5.4 | Measurement of clock drift rates

Table 7 lists the clock drift rates measured for the four pairs of DSPs considered. The test performed to measure these drift rates is described below.

The clock of the DSP for the PV inverter is considered the global time in the microgrid. The drift rates of the other five DSP clocks refer to this global time. In the test, the inverters and M3 processors were disabled. C28 processors were programmed to generate a pulse each 100 μ s. The number of pulses was counted for 10,000 s in the DSP devices under test (DUT) using the C28 processor via hardware interrupts. The process was repeated four times to obtain an averaged number of pulses for each processor ($N_{i,DUT}$) in order to compensate random delays. Based on (1), the clock drift rates were calculated as

$$d_i = \frac{N_{i,DUT}}{N_{PV}}, \quad (16)$$

where N_{PV} was the average number of pulses counted in the DSP for the PV inverter.

5.5 | Numerical example for family 2 control schemes

This subsection discusses some issues about family 2 control schemes with a numerical example. The analysis focuses on family 2 because it is the only family with active powers that continuously increase or decrease over time (see Table 4). In the example, a constant generation and demand is considered with $P_G = 2.5$ kW and $P_L = 3.83$ kW, respectively. The power losses are $P_{loss} = 0.17$ kW.

For family 2, the expressions for frequency and power were collected in Tables 3 and 4. By replacing the numerical values of the previous paragraph and those of Table 6 in these expressions, the resulting equations are

$$P_{1,ss} = 750 - 60\pi (d_2 - d_1) k_{I1} \left(\frac{1000 + D_1}{k_{I1} d_1} + t \right), \quad (17)$$

$$P_{2,ss} = 750 + 60\pi (d_2 - d_1) k_{I2} \left(\frac{1000 + D_2}{k_{I2} d_2} + t \right), \quad (18)$$

$$f_{i,ss} = f_0 \frac{d_1 + d_2}{2} \approx 60 \text{ Hz}. \quad (19)$$

In (17)–(19), the damping factors D_i , the integral gains of governor equations k_{Ii} , and the clock drift rates d_i are kept as variables to discuss their impact on the performance of family 2 control schemes.

Individual powers of the batteries ($P_{1,ss}$ and $P_{2,ss}$) diverge in time because their expressions depend on t , as seen in (17) and (18). This is a problem in family 2 control schemes that cannot be alleviated with high damping factors D_i as might initially be considered. In fact, the effect of D_i on $P_{i,ss}$ is to change its initial value at $t = 0$, but D_i has no influence on the $P_{i,ss}$ term that evolves over time, being its slope $\Delta P_{i,ss}(t)$

$$\Delta P_{i,ss}(t) = \pm 60\pi (d_2 - d_1) k_{Ii}, \quad (20)$$

and, therefore, cannot cancel it. Note that the individual power of the batteries is constant only if $d_1 = d_2$, which is not the case in real applications (see Table 7), or with $k_{Ii} = 0$, which is also not possible for the control schemes of family 2.

However, the total power supplied by the batteries $P_{BAT,ss} = P_{1,ss} + P_{2,ss}$ is constant and independent of the clock drift rates. By replacing the values of D_i and k_{Ii} in (17) and (18), the power $P_{BAT,ss}$ is written as

$$P_{BAT,ss} = 1500 - 90000\pi \frac{(d_2 - d_1)^2}{d_1 d_2}. \quad (21)$$

Even considering the largest possible difference between d_1 and d_2 , that is, 40 ppm according to (2), the second term on the right-hand side of (21) is negligible. Therefore, $P_{BAT,ss} \approx 1.5$ kW. Note that, with this result, the power balance equation in (5) holds. Hence, power generation coincides with power demand, as desired. The fact that the power balance is fulfilled in steady state makes the frequency of the microgrid constant, as announced in (19), even if the power of each battery separates over time.

5.6 | Design of the experiments

The objective of the experiments is to validate the theoretical results summarised at the beginning of Section 4. As shown in previous subsection, the slopes $\Delta P_{i,ss}(t)$ are very small for control schemes in family 2. Therefore, the experiments should last long enough so that the difference between the powers of the VSG inverters can be clearly appreciated. For this purpose, all figures with experimental results have a duration of 600 s.

In the experiments, the two VSG inverters are turned on at the same time to share load power collaboratively. In any case, since clock drifts are a physical property of crystal-based hardware oscillators, this property (which is intrinsic to distributed DSPs) is not influenced by the inverter power-up sequence.

In the following subsections, the theoretical results will be evaluated in several generation scenarios and using DSP devices with different clock drift rates.

5.7 | Experimental validation of family 2 schemes in a scenario with constant generation and demand

The theoretical discussion in Section 4.5 is validated by experimental results. The constant generation and demand scenario is: $P_G = 2.5$ kW, $P_L = 3.83$ kW and $P_{loss} = 0.17$ kW. Figure 4 shows measured active powers and frequencies using the DSPs considered in Table 7. The important point in this figure is that active powers diverge, as predicted by (17) and (18). In addition, the slopes of the active powers are different in each subfigure in which DSPs with different clock drift rates are used. Note that the slopes are reduced from Figure 4a to Figure 4d as the

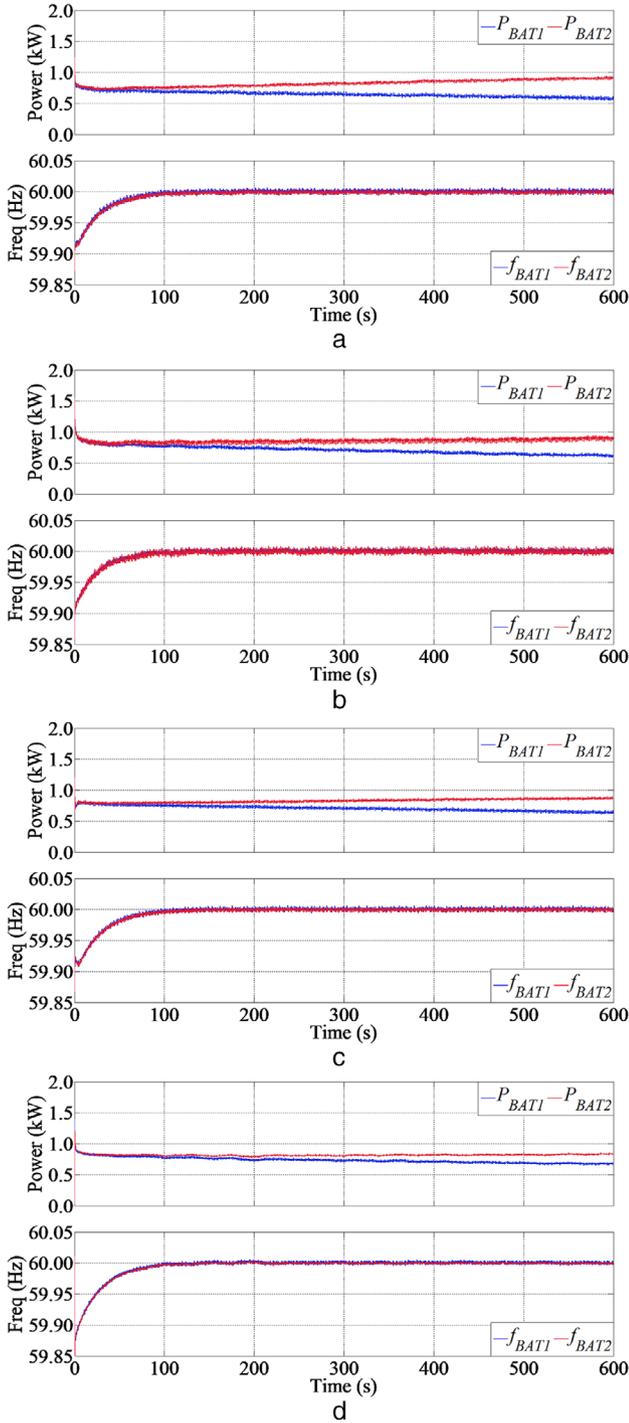


FIGURE 4 Experimental results for control family 2 in constant generation and demand scenario for the considered DSPs. (a) Pair 1, (b) pair 2, (c) pair 3, (d) pair 4. The tested scheme was the one with P and PI compensators in swing and governor equations, respectively

difference between the clock drift rates $d_2 - d_1$ is also reduced; see Figure 4 and Table 7.

Figure 5 shows the measurements for non-nominal values of D_i and κ_{fi} using the pair of DSPs 1. Comparing Figures 4a and 5a, it is clear that changes in D_i are almost negligible on the slopes of the active powers, as predicted by (20). In addition,

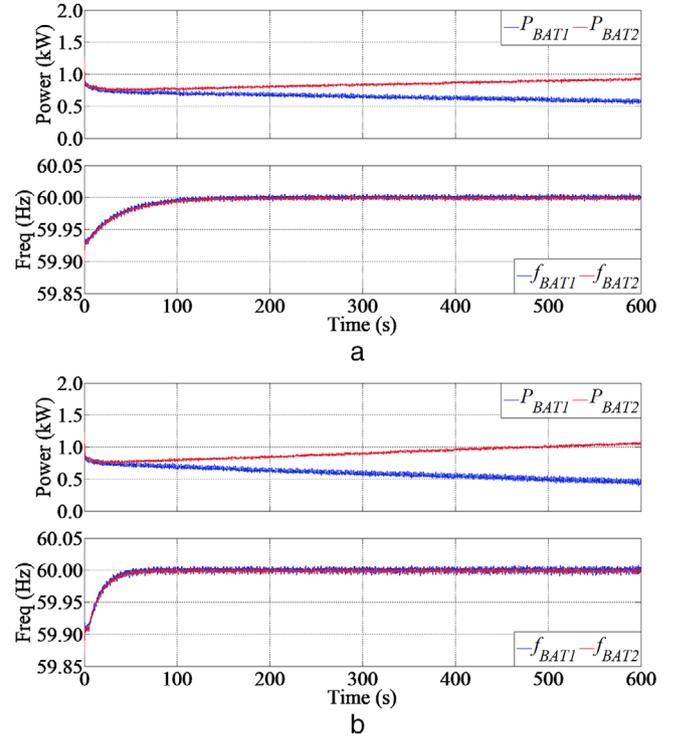


FIGURE 5 Experimental results for control family 2 in constant generation and demand scenario for non-nominal control gains. (a) $D_i = 1000$ W/(rad/s), (b) $\kappa_{fi} = 100$ W/rad. The tested scheme was the one with P and PI compensators in swing and governor equations, respectively

comparing Figures 4a and 5b, it is clear that the slopes increase as κ_{fi} increases. This effect was also theoretically predicted by (20).

The experimental results presented in this subsection correspond to the control scheme with P and PI compensators in swing and governor equations. The transient response of the rest of control schemes in family 2 shows a very similar behaviour in this test condition. For this reason, these additional transient responses have been omitted in this paper.

5.8 | Experimental validation in a scenario with variable generation and demand

This subsection evaluates the operation of the three control families in a realistic scenario with variable generation and demand. Figure 6 shows the power supplied by the wind and PV generators, and the power consumed by the loads. Figure 7 shows the active powers and frequencies of the VSG inverters governed by the three control families using the pair of DSPs 1. In families 1 and 2, the results correspond to the control schemes specified at the bottom of the figure. Practically the same results were obtained with the rest of schemes of these families.

From Figure 7, it is clear that the effects of clock drifts are negligible in control families 1 and 3. In both families, the powers supplied by the VSG inverters coincide; see the top of Figures 7a and 7c. In each control family, the operating

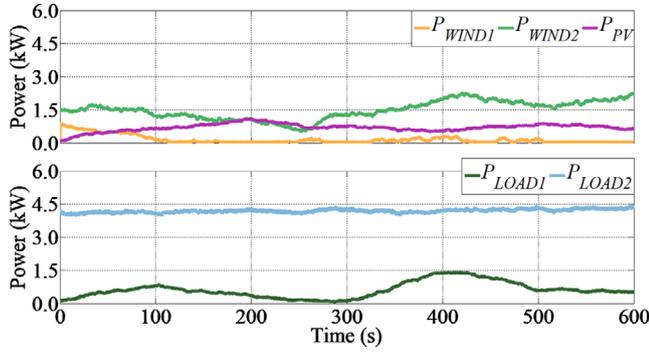


FIGURE 6 Power in generation (top) and loads (bottom) in variable generation and demand scenario

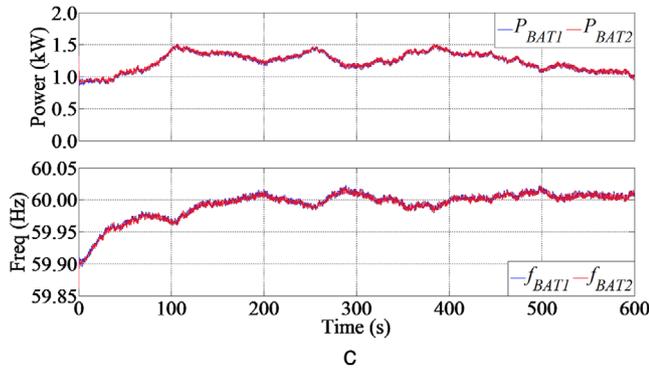
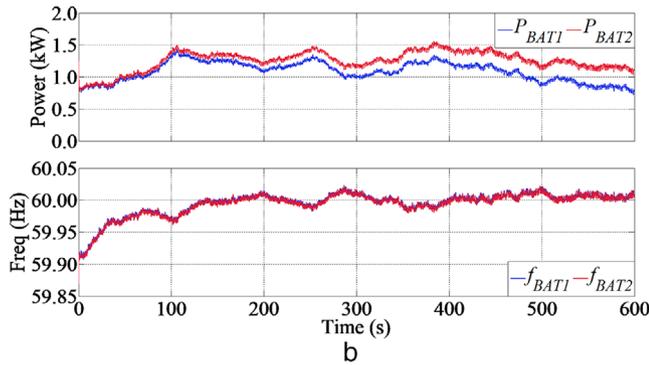
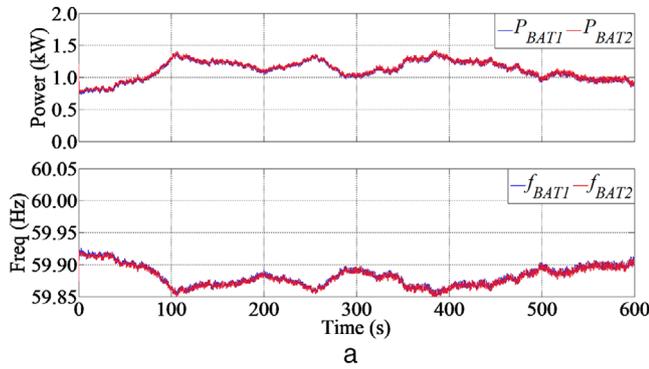


FIGURE 7 Experimental results in variable generation and demand scenario for the pair of DSPs 1. (a) Control family 1, (b) Control family 2, (c) Control family 3. Families 1 and 2 use a P compensator in the swing equation and a P and PI compensator in the governor equation, respectively

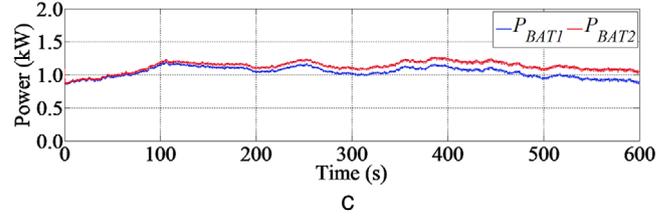
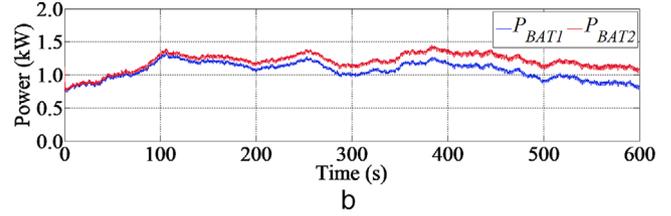
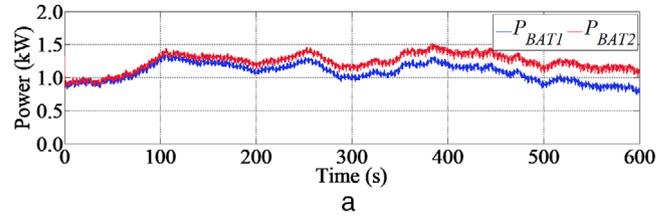


FIGURE 8 Experimental results in variable generation and demand scenario for control family 2. (a) Pair 2, (b) Pair 3, (c) Pair 4. The tested scheme was the one with a P and PI compensators in swing and governor equations, respectively

frequencies of the VSG inverters also coincide; see the bottom of Figures 7a and 7c. In fact, in family 1, the frequencies deviate from the nominal value according to the supplied active power. However, in family 3, the frequencies move slightly around 60 Hz due to the integral action of the governor equation.

In family 2, the operating frequencies are similar to those in family 3; see the bottom of Figures 7b and 7c. This similar behaviour is because of the integral term in the governor equation is dominant in the frequency dynamics. However, the active powers are separating as time progresses, as shown in the top of Figure 7b. This fact is a direct consequence of the different clock drifts in the local hardware oscillators of the pair of DSPS 1, as predicted by (17) and (18).

The test was repeated with the pairs of DSPs 2, 3 and 4. For control families 1 and 3, the results were nearly identical as those shown in Figures 7a and 7c. For control family 2, it was observed that the active powers diverged over time with lower slopes compared to the results in Figure 7b. The results are shown in Figure 8. Note that the slopes decreased as the difference between the clock drift rates ($d_2 - d_1$) decreased. This phenomenon was already observed in Figure 4 with constant generation and demand. In this test, it is found that the phenomenon is repeated for the scenario with variable generation and demand.

6 | CONCLUSION

In this paper, a classification of VSG inverters in three control families has been presented. Family 1 and 3 control schemes

provide excellent power sharing and frequency regulation. However, family 2 control schemes produce unsatisfactory performance due to clock drifts in the hardware oscillators of the distributed DSPs. Although the total power delivered by VSG inverters is constant in this family, individual powers diverge over time. This impact of clock drifts will inevitably lead to the shutdown of the inverters when they reach the limit of the maximum power. The properties of these three control families have been experimentally validated in a laboratory microgrid. In the test, several generation scenarios and DSP devices with different clock drift rates have been considered.

The development of novel VSG control schemes is an open topic for further research. The technical guidelines provided in this paper are valuable in designing robust control schemes to clock drifts.

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