Common Mode Response Effects in Differential Measurements

Gemma Hornero, Óscar Casas and Ramon Pallàs Areny

Abstract— In differential measurements, before digitized, the signal is conditioned by a differential or fully differential circuit which output depends on both the differential- and common-mode input voltages. Differential signals carry the desired information but common-mode voltages are a nuisance and their contribution to the output signal becomes an interference which is usually evaluated from the ratio between the respective gains for the differential- and common-mode input voltages, Common-Mode Rejection Ratio (CMRR). Usually, only the modulus of the CMRR is specified for IC differential. In this paper we demonstrate that the common-mode response depends on component tolerance and can be band-pass with gain peaking and positive phase shifts inside differential signal passband. Tolerances as low as ±0.01% cannot prevent phase shifts close to +90º. The presence of positive phase shifts in the common-mode gain can be suspected whenever the modulus of the CMRR decreases for frequencies below the -3 dB bandwidth of the differential gain but cannot be appraised from that modulus alone. Surprisingly, a high CMRR at low frequencies can worsen that effect. Therefore, common-mode effects in differential circuits can be evaluated only from the separate description of the response to differential and common-mode inputs signals.

Index Terms— Differential measurements, differential signal conditioners, common mode response, common mode gain, common mode voltage

1. INTRODUCTION

Differential measurements involve differential sensors, Wheatstone or ac bridges with sensors in one, two or four arms or sensors (and their conditioners) in separate places and connected to a differential amplifier [1], for example for current, high-voltage or biopotential measurement [2]. Differential or pseudo-differential voltages also arise in four-terminal impedance measurements, and in difference measurements at large, for example in thermal standards of power, to minimize common mode effects in tilt measurements and to reduce interference due to ground loops [3].

Differential signal conditioners can process the voltage difference between two nodes even if none of them is connected to signal ground. Therefore, any undesired voltage simultaneously added to both nodes will ideally be cancelled out upon subtracting their respective voltages.

In practice, however, each of the two voltages is processed (amplified, filtered) before subtracting them. The consequence is that unless both voltages undergo identical processing before being subtracted, the final result will depend not only on their difference but also on their average value, termed *common-mode voltage*, v_c. In circuits with differential input and single-ended output, the output voltage contributed by the input common-mode voltage is described by the so-called common-mode gain G_c and the ratio between the differential-mode gain G_d and G_c, termed Common-Mode Rejection Ratio (CMRR) [4], [5], is the most common parameter to describe the effect of v_c because the circuit output can be written as

$$V_o(s) = G_d(s) \cdot V_d(s) + G_c(s) \cdot V_c(s) \tag{1}$$

and for low-frequency signals we have

$$v_o = G_d\left(v_d + \frac{G_c}{G_d} v_c\right) = G_d\left(v_d + \frac{v_c}{\mathrm{CMRR}}\right). \tag{2}$$

Therefore, a very high CMRR minimizes the output contribution of low-frequency v_c as compared

to that of v_d.

Nevertheless, the assumptions that lead from Eq. (1) to Eq. (2) hold true only if v_d and v_c have the same frequency and G_d and G_c are real numbers, *i.e*. they do not contribute any phase shift. Obviously, this is not always the case because, on the one hand, v_d is the signal of interest and v_c can be, say, an interference of unknown frequency. On the other hand, G_d is designed to be constant in the frequency band of interest whereas G_c results from component mismatches and depends on circuit topology. Often, the only information available about G_c is that inferred from the CMRR and G_d. Since only the modulus but not the phase characteristic of CMRR is specified or measured, it turns out that G_c can be estimated only at very low frequency where CMRR is constant and its phase is presumed to be zero (or 180°). But for ac signals, $G_c \times v_c$ could drive the ensuing stage into a nonlinear region, the transient response could be much longer than the one attributable to the differential-mode response, G_c could be unstable in spite of G_d being stable, and a voltage with uncontrolled phase angle could add up to the desired output. None of these undesired effects can be predicted from G_d and the modulus of CMRR.

In fully differential amplifiers, Eq. (2) also holds if G_d is replaced by G_{DD} (differential-to-differential gain) and G_c by G_{DC} (common-mode-to-differential gain), so that now CMRR = G_{DD}/G_{DC} [4]. Therefore, the same comments above relative to G_c apply to G_{DC}. For example, the possible instability of a very common fully-differential amplifier due to G_{DC} was reported long ago [6] and the lengthy transient responses due to G_{DC} have also been studied for some fully differential filters [7].

In this paper we analyze the common-mode gain of differential circuits built by subtracting the outputs of two equal single-ended circuits, and describe their response to common-mode input signals. First, circuit models are obtained for the frequency response to common-mode signals and

that response is later experimentally assessed. The results should provide a better understanding of the effects of input common-mode signals and lead to stronger design criteria for high-performance differential signal conditioners.

2. Common Mode Gain of Differential Circuits

An expeditious way of designing a differential circuit is by subtracting the output voltages of two equal single-ended circuits, as shown in Fig. 1. This is often the case, for example, when the two voltages to be subtracted are obtained at separate places and each voltage is amplified before being subtracted in a central data acquisition unit. If both circuits have a first-order low pass response,

$$G_1(s) = G_1 \frac{\omega_1}{s+\omega_1} \tag{3a}$$

$$G_2(s) = G_2 \frac{\omega_2}{s+\omega_2} \tag{3b}$$

then the differential output voltage due to a common-mode input voltage $v_c = (v_1 + v_2)/2$ is

$$V_o(s) = V_{oH}(s) - V_{oL}(s) = V_C\left[G_2(s) - G_1(s)\right] \tag{4}$$

hence the common-mode-to-differential gain is [4]

$$G_{DC}(s) = G_2(s) - G_1(s) = G_2 \frac{\omega_2}{s+\omega_2} - G_1 \frac{\omega_1}{s+\omega_1} \tag{5}$$

and $G_{DC}(0) = G_2 - G_1 = \Delta G$.

If we assume that both the dc gain and the corner frequencies of the two single-ended circuits are mismatched because of manufacturing tolerances t_G and t_ω, respectively, then in a worst case condition we have

$$\begin{aligned} G_1 &= G_a(1 - t_G) \\ G_2 &= G_a(1 + t_G) \end{aligned} \tag{6}$$

and, initially,

$$\begin{aligned}\omega_1 &= \omega_a\left(1-t_\omega\right)\\ \omega_2 &= \omega_a\left(1+t_\omega\right)\end{aligned} \tag{7}$$

where G_a is the average dc gain and ω_a is the average angular corner frequency. Therefore, $G_1 < G_a < G_2$ and $\omega_1 < \omega_a < \omega_2$. If Eq. (6) and Eq. (7) are introduced into Eq. (5), the result is

$$G_{DC}\left(s\right) = 2G_a\omega_a\left(t_G+t_\omega\right)\frac{s+\omega_a\dfrac{t_G\left(1-t_\omega^2\right)}{t_G+t_\omega}}{\left(s+\omega_1\right)\left(s+\omega_2\right)} \tag{8}$$

that can be rewritten as

$$G_{DC}\left(s\right) = G_a\omega_a\left(\frac{\Delta G}{G_a}+\frac{\Delta\omega}{\omega_a}\right)\frac{s+\omega_{zc}}{\left(s+\omega_1\right)\left(s+\omega_2\right)} \tag{9}$$

where $\Delta G = G_2 - G_1 = 2G_a t_G$, $\Delta\omega = \omega_2 - \omega_1 = 2\omega_a t_\omega$, and

$$\omega_{zc} = \omega_a\frac{t_G\left(1-t_\omega^2\right)}{t_G+t_\omega} = \omega_a\frac{1-t_\omega^2}{1+t_\omega/t_G}\,. \tag{10}$$

Therefore, ω_{zc} will be different from zero whenever $t_G \neq 0$ and proportional to the average corner frequency but independent from the dc gain. Since t_G and t_ω in Eq. (7) are both positive, then from Eq. (10) it follows $\omega_{zc} < \omega_1, \omega_2$ whenever $t_G < 1$, which is usually the case, and the larger the ratio t_ω/t_G, the lower will ω_{zc} be, *i.e.*, it will fall well inside the differential circuit passband.

According to Eq. (9), the mismatch between two first-order low-pass systems leads to a band-pass response for G_{DC} that at ω_{zc} raises by 3 dB with respect to $G_{DC}(0) = \Delta G$, stops raising below ω_1, and starts decreasing below ω_2. Therefore, G_{DC}(s) will have a maximum between ω_1 and ω_2 that will increase with increasing $\Delta\omega$, hence t_ω. By equating to zero the first derivative of the modulus of Eq. (9), it is found that the maximum occurs at

$$\omega_{\max} = \sqrt{\sqrt{\omega_{zc}^4 - \omega_{zc}^2\left(\omega_1^2 + \omega_2^2\right) + \omega_1^2\omega_2^2} - \omega_{zc}^2} \tag{11}$$

and, for small ω_{zc}, we have $\omega_{\max} \approx (\omega_1\omega_2)^{1/2} = \omega_g$, the geometric mean of ω_1 and ω_2. The maximal gain relative to the dc gain is

$$\frac{\left|G_{DC}\right|_{\max}}{\left|G_{DC}(0)\right|} = \left(1 + \frac{t_\omega}{t_G}\right)\frac{\omega_a\sqrt{\omega_{\max}^2 + \omega_{zc}^2}}{\sqrt{\omega_{\max}^2 + \omega_1^2\sqrt{\omega_{\max}^2 + \omega_2^2}}} \tag{12}$$

which increases with t_ω/t_G hence for smaller ω_{zc}. If ω_{zc} is small enough, then the maximal gain is

$$\left|G_{DC}\right|_{\max} \approx G_a\left(t_G + t_\omega\right) \tag{13}$$

meaning that dc gain and corner frequency tolerance effects add each other. The phase characteristic of G_{DC} will be positive from below ω_{zc} up to some frequency between ω_1 and ω_2 hence within the passband of the differential gain.

For $\omega_{\max}$ to be real, the radicand in Eq. (11) must be positive, which leads to the conditions

$$\omega_1^2\omega_2^2 > \omega_{zc}^2\left(\omega_1^2 + \omega_2^2\right) \tag{14}$$

and

$$\left(t_G + t_\omega\right)^2 > 2t_G^2\left(1 + t_\omega^2\right). \tag{15}$$

Solving for t_ω yields

$$t_\omega > \frac{t_G}{1 - 2t_G^2}\left(\sqrt{2}\sqrt{1 - t_G^2} - 1\right) \tag{16}$$

that for $t_G << 1$ can be simplified into $t_\omega > (\sqrt{2} - 1)t_G \approx 0.4t_G$, meaning that G_{DC} peaking is determined by corner frequency mismatch relative to dc gain mismatch.

For matched dc gains ($t_G = 0$), $G_1 = G_2 = G_a$, we have $\omega_{zc} = 0$ and Eq. (9) reduces to

$$G_{DC}(s)\big|_{t_G=0} = G_a\frac{\left(\omega_2 - \omega_1\right)s}{\left(s + \omega_1\right)\left(s + \omega_2\right)} \tag{17}$$

which implies a positive phase response from dc up to frequencies above ω_1, which is a wider range than that when $t_G \neq 0$. The maximal gain occurs now at ω_g and its value is $G_a t_\omega$, obviously smaller than that when $t_G \neq 0$ Eq. (13).

If the two corner frequencies are matched instead, $\omega_1 = \omega_2$ ($t_\omega = 0$), then we have $\omega_{zc} = \omega_a = \omega_1 = \omega_2$, $\omega_{max} = 0$ and Eq. (9) simplifies to

$$G_{DC}(s)\big|_{t_\omega=0} = (G_2 - G_1)\frac{\omega_a}{s+\omega_a} \tag{18}$$

which is a low-pass response hence has negative phase shift. Therefore, corner frequency mismatch yields the worst G_{DC} because it makes G_{DC} to increase inside the differential gain passband and can contribute positive phase shifts in a system which differential-mode response is low pass hence has negative phase shift for differential signals. This can be especially dangerous in ac measurements where in-phase and quadrature components must be separately processed, for example in complex impedance measurements.

If gain tolerances are those in Eq. (6), *i.e.* $G_1 < G_a < G_2$, but the tolerances of the angular corner frequency are such that

$$\begin{aligned} \omega_1 &= \omega_a(1+t_\omega) \\ \omega_2 &= \omega_a(1-t_\omega) \end{aligned} \tag{19}$$

i.e. $\omega_1 > \omega_a > \omega_2$, then Eq. (9) should be replaced by

$$G_{DC}(s) = G_a\omega_a\left(\frac{\Delta G}{G_a} - \frac{\Delta\omega}{\omega_a}\right)\frac{s+\omega'_{zc}}{(s+\omega_1)(s+\omega_2)} \tag{20}$$

where

$$\omega'_{zc} = \omega_a\frac{t_G(1-t_\omega^2)}{t_G - t_\omega} = \omega_a\frac{1-t_\omega^2}{1-t_\omega/t_G}. \tag{21}$$

Now, whenever $t_G < t_\omega$, $G_{DC}(s)$ will be negative and have a positive zero in the complex plane, which added to the two negative poles in the denominator amount to a maximum 270° phase shift.

For the particular cases with matched dc gains ($t_G = 0$) or corner frequencies ($t_\omega = 0$), the results are the same obtained before, *i.e.* Eq. (17) and Eq. (18) respectively.

If $t_G = t_\omega = t$, which implies matched gain-bandwidth products, $G_1\omega_1 = G_2\omega_2$, then, from Eq. (5), the result is

$$G_{DC}(s)\Big|_{t_G=t_\omega=t} = G_a\omega_a\left(1-t^2\right)\frac{\omega_2-\omega_1}{(s+\omega_1)(s+\omega_2)} \tag{22}$$

which is an overdamped second-order low-pass response hence shows negative phase shift and no gain peaking.

The differential gain is also affected by gain and corner frequency mismatches as we have [4]

$$G_{DD}(s) = \frac{G_1(s)+G_2(s)}{2} = \frac{1}{2}\left(\frac{G_1\omega_1}{s+\omega_1}+\frac{G_2\omega_2}{s+\omega_2}\right) \tag{23}$$

and considering tolerances as in Eq. (6) and Eq. (7), it results

$$G_{DD}(s) = G_a\omega_a\left(1+t_Gt_\omega\right)\frac{s+\omega_{zd}}{(s+\omega_1)(s+\omega_2)} \tag{24}$$

wherein

$$\omega_{zd} = \omega_a\frac{1-t_\omega^2}{1+t_Gt_\omega} \tag{25}$$

which, for t_G, $t_\omega < 1$, it implies $\omega_1 < \omega_{zd} < \omega_a < \omega_2$, and $\omega_{zd} > \omega_{zc}$. Therefore, the effect of mismatches is here a reduced gain and phase shift between ω_1 and ω_2 but otherwise the expected first-order low-pass response is obtained. Dividing Eq. (24) by Eq. (9) yields

$$\text{CMRR} = \frac{G_{DD}(s)}{G_{DC}(s)} = \frac{1+t_Gt_\omega}{2\left(1+t_\omega/t_G\right)}\frac{s+\omega_{zd}}{s+\omega_{zc}} \tag{26}$$

and CMRR(0) = $G_a/\Delta G$, which is quite plausible. Since, from Eq. (25) and Eq. (10) (or Eq. (21)),

$\omega_{zd} > \omega_{zc}$, ω'_{zc}, CMRR will decrease by 3 dB with respect to CMRR(0) at ω_{zc} and will stay constant up to a frequency a bit higher than ω_{zd} provided the first-order model for each channel in Fig. 1 is still valid at those frequencies. Coincidentally, this is the specified variation of the CMRR with frequency for the INA121 instrumentation amplifier (later used in this work). Since all data sheets of IC instrumentation amplifiers show that CMRR decreases starting at frequencies well below the corner frequency for the differential gain, this means that the common-mode gain starts to increase at low frequencies, the same as for the differential circuit in Fig. 1 in cases Eq. (9), Eq. (17) and Eq. (20), that is, whenever the corner frequencies or the gain-bandwidth products are mismatched, because when $t_\omega = 0$ or $t_G = t_\omega$ the common mode response is low-pass (Eq. (18) or Eq. (22), respectively).

Table I summarizes the above scenarios for G_{DC}. Subtracting the outputs from two mismatched first-order low-pass circuits yields a common-mode-to-differential gain with band-pass or low-pass frequency response when the two corner frequencies are mismatched, and a first-order low-pass response if only dc gains are mismatched. If the corner frequency mismatch is larger than about 40% of the gain mismatch, then the band-pass response Eq. (9) has gain peaking and positive phase angle inside the differential passband, starting at relatively low frequency. If the corner frequency mismatch is smaller than about 40% of the mismatch between dc gains, then G_{DC} is first-order, low-pass. If gain-bandwidth products are matched, then G_{DC} is second-order low-pass Eq. (22). Since the conditions $t_\omega = 0$ and $t_G = t_\omega$ are quite improbable, and dc gain tuning yields $t_G = 0$, we will have $t_\omega > t_G$, so that we can expect a band-pass response for G_{DC} to be quite common.

3. Experimental Design

The mathematical model above has been assessed by implementing the circuit in Fig. 1 with two single-ended amplifiers which outputs are subtracted by measuring their difference with an

accurate instrumentation amplifier (INA121P), differential gain $G = 6$ (Fig. 2), connected to an 8-bit Digital Storage Oscilloscope (TDS5054). Phase shift was measured from the time interval between sine wave peaks on the oscilloscope. The circuit was supplied at ±15 V. First, the common mode gain G_c for the INA121P instrumentation amplifier was measured from 1 Hz to 10 kHz by applying a 10 V sine wave input in common mode. Below 80 Hz, the output signal was too small to reliably measure the phase shift. The module of G_c increased from 1.4×10^{-4} at 1 Hz (CMRR ≈ 92 dB) to 1.6×10^{-4} at 10 Hz (CMRR ≈ 91 dB) and 5.4×10^{-3} at 10 kHz (CMRR ≈ 60 dB). These values fall between the specified CMRR for the INA121P for $G = 10$, (minimum 91 dB, typical 100 dB at low frequencies, and 75 dB typical at 10 kHz) and $G = 1$ (between 78 dB to 86 dB at low frequencies and 50 dB typical at 10 kHz). The measured phase shift for G_c was 90° for frequencies below 3 kHz, decreasing to 85º at 10 kHz, and 0º at 320 kHz. With these G_c values, and a 1 V common mode input voltage, the instrumentation amplifier contribution to the output signal is from 150 μV for frequencies below 100 Hz to 5.4 mV maximum at 10 kHz. Note that this behavior for G_c is the same obtained above for the case $t_G \neq 0$, $t_\omega > 0.4\ t_G$, Eq. (26), in spite that the INA121P does not certainly comprise two separate single-ended stages which outputs are subtracted.

Next, several resistors and capacitors were measured and specific units were selected to implement four different scenarios that could arise in practice because of component tolerances. Table II shows those four cases. Case 1 and Case 2 differ only in C value. Case 3 and Case 4 involve the same components but the positions of C and C' are interchanged.

The circuit parameters corresponding to the component values in Table II are shown in Table III. Cases 1 and 2 have different t_ω/t_G (less than 0.4 in Case 1, larger than 0.4 in Case 2), but otherwise $G_2 > G_1$ and $\omega_2 > \omega_1$ in both cases. Cases 3 and 4 have $G_2 > G_1$ and similar t_ω/t_G but ω_2

$> \omega_1$ in Case 3 and $\omega_2 < \omega_1$ in Case 4.

4. Experimental Results and Discussion

Fig. 3 shows the modulus (top) and phase (bottom) of G_{DC} in Cases 1 and 2. Theoretical values correspond to the solid and broken lines and experimental results, after discounting the gain of the instrumentation amplifier in Fig. 2, are triangles (Case 1) or squares (Case 2). At low frequencies, G_{DC} should be close to $\Delta G = 0.4$ in both cases and the asymptotes in Fig. 3 are -8 dB (= 0.4) for the modulus, and 0° for the phase, as expected. Case 1 leads to a low-pass response because $t_\omega/t_G = 0.055 < 0.4$ (Table I). Case 2, however, with $t_\omega/t_G = 2.5 > 0.4$ should result in a band-pass response with gain peaking and positive phase shift. The modulus in Fig. 3 shows obvious gain peaking, which cannot belong to an underdamped second-order low-pass system because the transfer function has two distinct negative poles. The phase characteristic shows positive values hence actually corresponds to a band-pass system Eq. (9). The maximal gain is at about 100 Hz, the corner frequency of the differential response, and the ratio $G_{DC(max)}/G_{DC(0)}$ is 1.75 (4.87 dB), *i.e*. very close to the theoretical values: 96 Hz (from Eq. (11)) and 1.82 (5.23 dB) (from Eq. (12)), respectively. The zero (f_{zc}) in the numerator of G_{DC} is close to one third of f_a, as expected. At 10 kHz, G_{DC} is less than -40 dB. If the input voltage is 1 V, the output voltage of the instrumentation amplifier is about 60 mV, so the 5.4 mV due to the common mode voltage of the INA121P instrumentation amplifier is less than 10 % of the 60 mV. For frequencies below 1 kHz this deviation is less than 0.1 % in all cases studied.

From Eq. (10), to obtain a G_{DC} with band-pass response and a very noticeable gain peak it should be $t_\omega/t_G >> 1$ and this can result from a large t_ω, a small t_G, or both. Cases 3 and 4 have a small t_G (0.3 %) and a large t_ω (about 19 %) hence fulfill that condition. G_{DC} in Case 3 ($G_2 > G_1, \omega_2 > \omega_1$) is given by Eq. (9) whereas G_{DC} in Case 4 ($G_2 > G_1, \omega_2 < \omega_1$) is given by Eq. (20). Since

$t_\omega/t_G >> 1$, the modulus of Eq. (9) and (20) should be very close and $G_{DC}(0) = 0.003$ (- 50 dB), but the phase characteristic should be very different because of the different sign for ω_{zc} and ω'_{zc} in Eq. (10) and Eq. (21), respectively. Fig. 4 (left) shows that both modulus are about the same and $G_{DC}(1\text{ Hz}) = -22.5$ dB and decreases with frequency, which is compatible with the expected $G_{DC}(0) \approx -50$ dB. Moreover, Eq. (11) and Eq. (12) predict $\omega_{max} = 570$ rad/s ($f_{max} = 91$ Hz) and $G_{DC(max)}/G_{DC(0)} = 32.20$ (= 30 dB), respectively, and in Fig. 4 we have $f_{max} = 90$ Hz, and $G_{DC(max)}/G_{DC(1\text{ Hz})} \approx 17$ (≈ 25 dB), which are in good agreement with those predictions. Further, f_{zc} is much lower than in Case 2. Therefore, whereas $t_\omega/t_G >> 1$ yields a large gain peaking, if t_G is small then $G_{DC}(0)$ is so small that $G_{DC(max)}$ is a bit larger than 1 and, since $G_a \approx 10$, the result is a poor CMRR < 20 dB. Therefore, tuning the dc gain of each channel in order to match $G_1 = G_2$ will reduce $G_{DC}(0)$, which is advantageous at low frequencies, but at the cost a gain peak close to $G_a t_\omega$ and, according to Eq. (17), large positive phase shifts at frequencies well below the corner frequency of the differential mode response. Similar behaviors of the common mode response to those presented in Fig. 4 had been previously observed experimentally in differential circuits [13]. It was known that the cause was the tolerance of the design resistances, but they had not been modeled and quantified theoretically.

The agreement between theoretical predictions and experimental results for G_{DC} is good enough for the equations above to be used to estimate G_{DC}, and CMRR, for usual tolerance values for gain and corner frequency in order to assess their impact. Table IV shows three different cases, all with 0.01 % dc gain tolerance, which is very good. In case A, $t_\omega = 10$ %, which can easily result, for example, from capacitor tolerance in passive filters, yields a zero in G_{DC} near 1 Hz that makes it to increase from -54 dB to 0 dB at 21 Hz, with a phase shift of 85° at this frequency. As a result, CMRR decreases from 74 dB at dc to 17 dB at 1 kHz, and maximal phase shift of -86° at 30 Hz.

Therefore, CMRR can be considered a real number only well below 1 Hz! Increasing the dc gain by 10 (G_a = 100, case B), worsens $G_{DC}(0)$ from -54 dB to -34 dB, and consequently $G_{DC,max}$ from 0 dB to 20 dB, but the other parameters remain the same. This worsening of G_{DC} is a direct consequence of the use of two separated stages which only interconnection is through signal ground. If the dc gain is kept at 100 but t_ω is improved to 1 %, then t_ω/t_G becomes 10 times smaller and the effect is an upwards shift of the zero of G_{DC} to 9.9 Hz and, whereas $G_{DC}(0)$ remains at -34 dB, $G_{DC,max}$ is now only 0 dB and CMRR at 1 kHz improves by 20 dB. Nevertheless, the maximal phase shift of G_{DC} is 74°, hence considerable, and the maximal phase shift of CMRR is -79° at 96 Hz, still well below 1 kHz.

A further reduction of t_ω while G_a is kept at 10, as in case A, should improve everything with respect to case A, exception made of $G_{DC}(0)$ and CMRR(0). Case D in Table IV shows that improving t_ω by 100 increases f_{zc} by about 90, $G_{DC(max)}$ and CMRR at 1 kHz by about 40 dB, and $f(\phi_{DC(max)})$ by 170 Hz, which are all beneficial, and decreases $\phi_{DC(max)}$ by 43°, which is also good. Nevertheless, CMRR(0) is still poor for the excellent tolerances (0.01°% for the gain and 0.1°% for the corner frequency, and the 43° phase shift for G_{DC} at 191 Hz, hence well below the circuit passband (1 kHz) can contribute major errors in the imaginary part of complex quantities if the common-mode voltage is relatively large as compared to the differential-mode voltage.

It could be argued that since the circuit in Fig. 2 comprises independent stages for each input signal, and it is well known that this yields a very poor CMRR [8], high-performance differential signal conditioners, and integrated circuits in particular, should rely on better topologies that avoid common-mode gain peaking and positive phase shifts. However, that topology is very common in differential measurements with distant sensors. With respect to differential integrated circuits, in [9], for example, the common-mode gain of the classic μA741 op amp was assumed to have a

single pole (at the same frequency as the differential gain) and a single zero and the measured CMRR modulus actually showed a “low-pass” variation with frequency (due to the zero of the common-mode gain). No information about the phase characteristic was provided. Similarly, a detailed study of CMOS operational transconductance amplifiers showed that their common-mode gain had the same dominant pole of the differential gain and two zeros, so that “the CMRR frequency response is basically determined by two poles which correspond to the two zeros of the common-mode gain.” [10]. The agreement between simulations and calculations in [10] were excellent. The amplifier in [5] shows a common-mode gain with a pole and a zero, and a CMRR that decreases about 20 dB/decade. Therefore, if the CMRR for differential circuits, integrated or not, decreases inside the -3 dB bandwidth of the differential gain, this means that the common-mode gain increases inside that frequency band, yet this gain cannot be deducted from the modulus of the CMRR, even if the frequency dependence of the differential gain is known in detail, so that its subtleties remain hidden to the user. As a result, CMRR calculations for cascaded differential stages that assume that this parameter is a real number within the frequency band of the differential signal being amplified [11] [12] cannot be directly applied inside all the differential amplifier passband.

Furthermore, for fully-differential circuits built from separated stages like that in Fig. 1, the differential to common-mode gain is $G_{CD}(s) = G_{DC}(s)/4$ [4]. Therefore, the effects of the input differential signal on the output common mode signal are qualitatively the same described for G_{DC} in Section II. This implies that the output common-mode signal comprises the input common mode signal amplified by $G_{CC}(s)$ (= $G_{DD}(s)$) [4], plus the input differential signal converted into common-mode output through $G_{CD}(s)$, with its band-pass or low-pass response. Consequently, the ensuing stage will need to tackle a larger common mode signal than the input stage, amplified

because of $G_{CC}(s)$, and distorted, because of $G_{CD}(s)$.

5. Conclusions

The deleterious effects of common-mode signals in differential measurements cannot be predicted from the CMRR modulus because this parameter is not a transfer function but the quotient of two transfer functions, namely the differential-mode and the common-mode gains. Consequently, that prediction needs the gain and phase characteristic of the common-mode gain, hence these should be specified or measured. Otherwise, a flat CMRR (in decibels) in a given frequency band, for example, could be wrongly interpreted as a real number when in fact it is a complex quantity with a phase that cannot be predicted from the modulus and that deviates from 0° well below the corner frequency of the differential mode gain.

Since the common-mode gain arises from component mismatching due to fabrication tolerances, and these are worse for passive discrete components, high-performance differential signal conditioners should not involve separate signal chains for each of the two signals to be processed and eventually subtracted, like the circuit in Fig. 1. Component tuning can help in improving the dc performance but at the cost of worsening ac performance. Multi-channel systems, in particular, wherein component tuning is unfeasible, should avoid circuit topologies that make the common-mode response to depend on passive component matching. Since the common-mode gain increase, when present, starts inside the circuit passband, designing a corner frequency much higher than the signal bandwidth could alleviate the problem but at the cost of increased noise bandwidth.

Common-mode gain in IC differential components such as op amps and instrumentation amplifiers may not obey the equations obtained for the circuit in Fig. 2, where mismatched passive components determine the common mode gain. Nevertheless, the qualitative conclusions about the results of subtracting two dissimilar first-order transfer functions apply whatever the circuit

topology. Therefore, by measuring the common-mode gain, Table I can be used to identify the source and relevance of the mismatch.

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Figures and tables

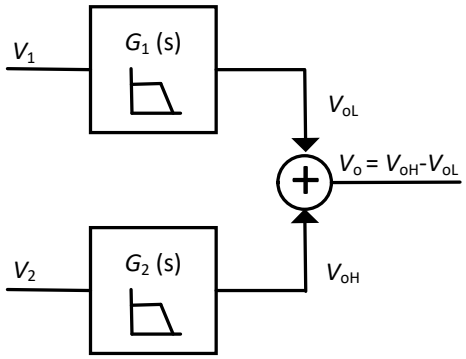

Fig. 1. Differential circuit built by subtracting the output voltages of two single-ended circuits.

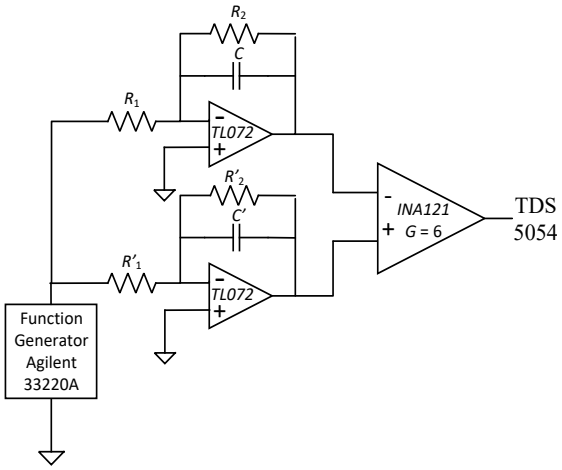

Fig. 2. Differential amplifier built by subtracting the output voltages of two single-ended amplifiers that are mismatched because of component tolerance.

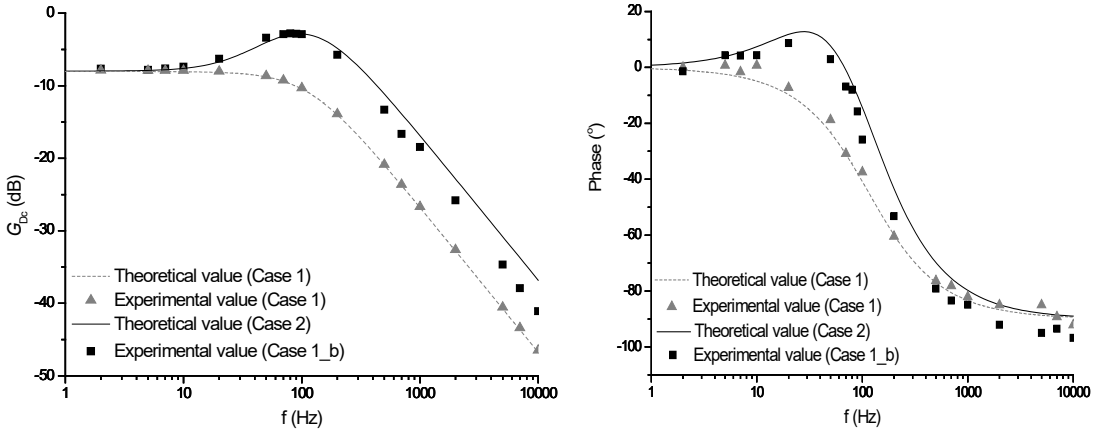

Fig. 3. G_{DC} modulus (left) and phase (right) for Cases 1 and 2 in Table III. Case 1: $G_2 > G_1$ and $t_\omega << t_G$; Case 2: $G_2 > G_1$ and $t_\omega >> t_G$.

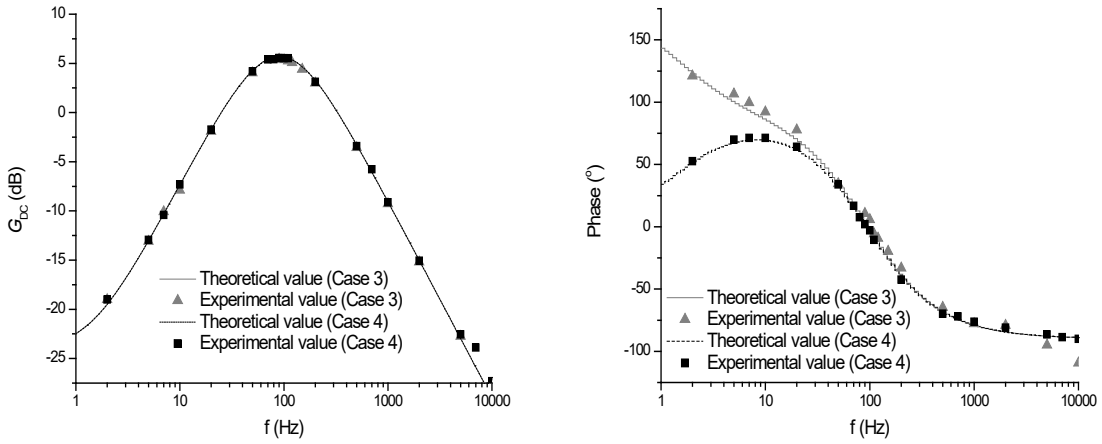

Fig. 4. G_{DC} modulus (left) and phase (right) for Cases 3 and 4 in Table III. Case 3: $G_2 < G_1$ and $\omega_2 > \omega_1$; Case 4: $G_2 < G_1$ and $\omega_2 < \omega_1$. In both cases, $t_\omega >> t_G$.

TABLE I
COMMON-MODE GAIN TRANSFER FUNCTIONS DEPENDING ON MISMATCHES

$G_2 > G_1$ $\omega_2 > \omega_1$ $\omega_2 < \omega_1$*	$t_G \neq 0$	$t_G = 0$
$t_\omega \neq 0$		**Band-pass response** (17)
$t_\omega > 0.4t_G$	**Band-pass response** (9)* (20) Gain peaking $\lvert G_{DC}\rvert_{max} \approx G_a(t_G + t_\omega)$ (13) $\phi > 0$ from ω_{zc} up to past ω_1	
$t_\omega < 0.4t_G$	**Low-pass response** (9) $\lvert G_{DC}(\omega)\rvert \leq \Delta G$ $\phi < 0$	Gain peaking $\lvert G_{DC}\rvert_{max} = G_a t_\omega$ $\phi > 0$ up to past ω_1
$t_\omega = 0$	**Low pass response** (18) $\phi < 0$	$G_{DC} = 0$
$G_1\omega_1 = G_2\omega_2$	Second-order, **low-pass response** (22) $\phi < 0$	

TABLE II
COMPONENTS FOR THE CIRCUIT IN FIG. 2 IMPLEMENTATIONS

	Case 1	Case 2	Case 3	Case 4
R_1/kΩ	10.35	10.35	9.91	9.91
R_2/kΩ	99.71	99.71	99.30	99.30
R_1'/kΩ	9.91	9.91	9.87	9.87
R_2'/kΩ	99.35	99.35	99.60	99.60
C/nF	14.57	16.06	14.59	21.30
C'/nF	14.59	14.59	21.30	14.59

TABLE III
CIRCUIT PARAMETERS FOR THE COMPONENT VALUES IN TABLE II

	Case 1	Case 2	Case 3	Case 4
G_1	9.63	9.63	10.03	10.03
G_2	10.03	10.03	10.09	10.09
G_a	9.83	9.83	10.06	10.06
ΔG	0.40	0.40	0.06	0.06
t_G/%	2	2	0.3	0.3
f_1/Hz	109.53	99.39	75.02	109.45
f_2/Hz	109.78	109.78	109.78	75.25
f_a/Hz	109.65	104.59	92.40	92.35
Δf/Hz	0.25	10.39	34.76	34.20
$\Delta\omega$/rad/s	1.57	65.28	218.38	214.88
t_ω/%	0.11	5	18.8	18.5
t_ω/t_G	0.055	2.50	62.70	61.70
f_{zc}/Hz	103.69	29.83	1.50	1.87

TABLE IV
ESTIMATED G_{DC} AND CMRR FOR DIFFERENT GAINS AND TOLERANCES

	Case A	Case B	Case C	Case D
G_a	10	100	100	10
t_G/%	0.01	0.01	0.01	0.01
f_a/kHz	1	1	1	1
t_ω/%	10	10	1	0.1
t_ω/t_G	1000	1000	100	10
f_{zc}/Hz	0.99	0.99	9.90	90.91
$G_{DC}(0)$/dB	-54	-34	-34	-54
$G_{DC(max)}$/dB	0	20	0	-39
$\phi_{DC(max)}$/°	85	85	74	43
$f(\phi_{DC(max)})$/Hz	21	21	76	191
CMRR(0)/dB	74	74	74	74
$CMRR_{1\ kHz}$/dB	17	17	37	56
$\phi_{CMRR(max)}$/°	-86	-86	-79	-56
$f(\phi_{CMRR(max)})$/Hz	30	30	96	305