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Aging in CMOS RF Linear Power Amplifiers: An Experimental Study

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Abstract— An extensive experimental analysis of the hot carrier injection (HCI) and bias temperature instability (BTI) aging effects on RF linear power amplifiers (PA) is presented in this paper. Two different 2.45-GHz PA topologies have been implemented in a CMOS 65-nm technology, one based on a classical common-source (CS) and choke inductor, another one based on a complementary current-reuse (CR) circuit, both of them producing similar gain and output 1-dB compression point (P_{-1dB}). These circuits have been stressed to produce accelerated aging degradation, by applying increasing supply (V_{DD}) voltages, or increasing RF input powers (P_{IN}). The degradation on the transistor parameters (threshold voltage and mobility), DC bias point (I_{DC} current) and RF performance (gain, matching, compression point) have been simultaneously measured. This has allowed to observe how the reduced transistor degradation in CR PA results in a higher robustness in its RF parameters, compared to CS PA circuit. The equivalent root-mean square (RMS) voltages have been proposed as an observable metric to assess the combined DC+RF stress in a PA circuit. This has been applied to a semi-analytical model, providing comprehension of the link between the conditions under which a circuit is operated, the degradation of the transistor parameters, and the effects on the DC current and RF performance.

I. Introduction

Designers of integrated circuits (IC) need to consider an increasing number of variability phenomena as technology scales down. In addition to the classical manufacturing variability, circuit reliability requires to contemplate effects that appear during circuit lifetime, such as the aging degradation [1]. In RF transceivers, the power amplifier (PA) circuit is particularly prone to suffer aging effects, given the large voltages appearing at device terminals. Introducing aging prediction in an IC design flow is now becoming possible with specific models and the tools developed by major CAD vendors [2], [3]. But besides simulation tools, circuit designers need a basic understanding of how circuit performance is degraded as a consequence of transistor degradation, and how this degradation is related to the circuit operating conditions. With that understanding, designers can take the wise decisions that would minimize aging effects –including select among circuit topologies–, which then can be verified with the aid of software tools.

Aging is the result of different physical phenomena: Hot Carrier Injection (HCI), Bias Temperature Instability (BTI), Time-Dependent Dielectric Breakdown (TDDB), and Electro-Migration (EM). Major reliability concerns in PA circuits are related to TDDB and EM effects, because of their potential to produce catastrophic failures derived from the large voltage and current spikes common in wireless transmitters. On the contrary, HCI and BTI produce a progressive circuit degradation, and attract increasing interest. HCI was first observed in old 2 μm technologies [4] and since then it has received considerable modeling efforts [5], [6]. HCI originates from high-energy carriers that become trapped in the oxide or create interface states, thus associated to the existence of high lateral electric fields. BTI phenomena also creates oxide and interface traps, but in this case because of the vertical electric fields in the oxide. MOS operating conditions (biasing) will thus determine the dominance of HCI or BTI phenomena. One remarkable characteristic of BTI is that part of the device degradation is recovered when the stress is removed, while another fraction becomes permanent [7], [8], [9]. The reported consequence of both HCI and BTI effects is an increase of the device threshold voltage V_{TH}, and a decrease of the saturation current I_{DS} [5], [10].

Previous works have evaluated experimentally the aging degradation of RF PA circuits, but some in the context of switched operation (class-E) [11], [12], and only a few analyzed linear PAs (class A or AB) [13], [14], [15]. In these works, aging is observed

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as a function of time but only in one or a few stress situations. To obtain insight on how circuit aging is related to the DC bias and the RF signal, measurements for different DC and RF stress situations should be obtained. In [16], [17] the HCI degradation on individual NMOS transistors was experimentally measured under DC or combined DC+RF stress, but then the effects on circuit RF metrics were estimated by means of simulation, using fresh and aged transistor parameters. All these experimental works have analyzed aging on the same conventional PA topology –an NMOS loaded with a choke inductor–, while aging effects in other circuit solutions have only been evaluated through simulation analysis [18].

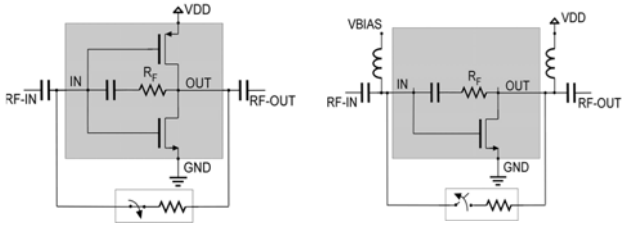
This work presents an experimental study to analyze the aging degradation specifically produced by HCI and BTI phenomena, in linear RF PA circuits implemented in a 65 nm CMOS technology. We have designed a simple test circuit that allows to observe individual transistor aging together with degradation of RF circuit metrics, in two representative basic PA topologies. Results will show a drastic difference in terms of aging robustness between these two topologies. The analysis performed demonstrates the reasons of that difference, and we propose and validate a simple model to relate the combined DC +RF voltages to the degradation measured. This model allows to estimate transistors aging in other amplifier topologies, and consequently, the circuit performance degradation. This paper is an extension of [19], [20], with significant extended experimental measurements, and deeper analysis, modeling and discussion of the degradations observed.

The PA circuits, measurement set-up and aging experiments are described in Section II. Section III focusses on the aging measured on the individual transistors, for each circuit topology and different stress conditions. The effect of that aging on the DC bias point of the PAs is described in Section IV. An analysis using a simple model allows to relate the DC current degradation to the effects measured on the MOS parameters, and how these are related to the circuit operating conditions. Finally, Section V shows the degradation observed on the RF gain, matching, and compression point, and justifies the differences between both PA circuits.

II. Experiment Description

A. Power Amplifier Circuits

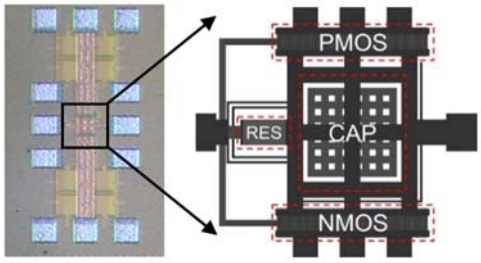
An IC containing test circuits has been designed specifically for this experimentation, according to the following requirements: (*i*) circuits should provide reasonable performance as RF PA, including input and output matching for measurement with a Network Analyzer; (*ii*) all transistor terminals should be accessible, in order to allow individual transistor characterization; (*iii*) they should be flexible in terms of configurability or frequency of operation; and (*iv*) the circuit must stand large currents/voltages produced in stress conditions, necessary to accelerate aging effects. All these requisites led to the design of a single circuit, which allows to be configured as two different PA topologies. In both cases, the resulting PAs are nominally operated as class-A, and provide broadband amplification up to 8 GHz. The first PA topology (named CR PA, Fig 1(a)) is a self-biased complementary current-reuse amplifier. An off-chip resistance provides self-biasing, which sets the DC operating point. The second topology (named CS PA, Fig. 1(b)) consists of a conventional NMOS in common-source configuration loaded with a choke inductor. In this configuration, the PA operating point is controlled externally through the gate voltage. The off-chip resistive feedback and the V_{DD} connection of the PMOS transistor are disabled to create this CS configuration. On the contrary, the off-chip choke inductor and the input DC bias connection are disabled in the CR configuration. An on-chip *RC* feedback network guarantees broadband input and output impedance matching in both configurations [20].



a) b)

Fig. 1. Scheme of the (a) current-reuse –CR– and (b) common-source –CS– power amplifier circuits measured. Greyed region indicates the components integrated in the IC, while the rest are implemented off-chip.

An IC containing several instances of the above described circuit has been manufactured in a CMOS 65 nm technology. A photograph and a simplified layout of the test structure are shown in Fig 2(a) and Fig 2(b) respectively. Transistors have been dimensioned with the objective to maximize the individual stress while fulfilling EM rules, rather than pursuing performance optimization. Both NMOS and PMOS transistors are *W/L* = 180µm/60nm (45 fingers), and designed to stand DC currents up to 100 mA. The transistors, the *RC* network and decoupling capacitors are integrated together with a 4×GSG pad structure for direct on-chip measurements in a probe station, occupying an area of 700 µm × 250 µm.



a) b)

Fig. 2. (a) IC photograph of the configurable PA, terminals accessible with four GSG pad structures. (b) Detail of the layout.

Table I reports the characteristics of both PA circuit topologies in nominal conditions. Note in the CS configuration, the DC gate voltage is selected the same value as that produced in the CR configuration V_{IN} = V_{OUT} = 520 mV. Both topologies provide similar performance in terms of gain, compression point and impedance matching at the frequency of 2.45 GHz, with the CR PA being more power-efficient, as otherwise expected.

TABLE I
NOMINAL PERFORMANCE OF THE PA CIRCUITS

	CR PA (NMOS+PMOS)	CS PA (NMOS+Lchoke)
V_{DD}	1.2 V	1.2 V
V_{IN_DC}	520mV (=V_{OUT_DC})	520 mV
I_{DC}	7.3 mA	10.3 mA
S_{21} @ 2.45GHz	10.3 dB	8.9 dB
S_{11} @ 2.45GHz	-8.5 dB	-8.1 dB
S_{22} @ 2.45GHz	-10.4 dB	-9.4 dB
$P_{-1dB,OUT}$	5 dBm	5.3 dBm
PAE @ P_{-1dB}	33.7%	26%

B. Measurement Set-up and Procedure

A measurement-stress-measurement procedure has been followed to induce and observe aging degradation in both PA configurations: first, complete characterization of fresh –before stress– amplifier and transistors is done; second, aging process is accelerated by operating the circuit in stressed conditions during a given time; and finally, complete characterization of the aged amplifier and transistors is repeated. This procedure has been repeated for different stress conditions, each time starting with a new fresh circuit. The time elapsed between the second and third steps in this measurement procedure was large enough to guarantee that the recovery process in BTI was completed, thus only the effects of the permanent BTI, and those of HCI, were observed [8], [9].

The experimental setup is shown in Fig. 3. A Vector Network Analyzer (VNA) is used to characterize the RF performance of the circuit as well as to provide RF stress. Besides, a Semiconductor device Parameter Analyzer (SPA) with Source Monitor Units (SMU) is used for DC characterization (of both circuit and transistors) as well as to provide circuit DC biasing and supply voltages during stress. Two external bias-T provide connection of the input and output terminals to the VNA and to the external resistive feedback or SPA. The IC is unpackaged, and PA input and output are contacted with GSG coplanar passive probes. The effect of all these cables and bias-T has been deembedded, both in the RF measurements and at DC (including contact resistances). During measurements, the ICs were glued to a thermally conductive support in order to minimize self-heating and allow temperature control. Further details on the measurement setup and procedure can be found in [20].

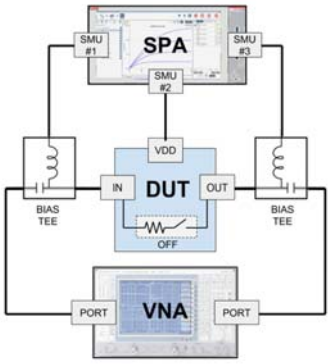


Fig. 3. Diagram of the experimental set-up. The SPA provides both DC biasing during circuit operation and also allows DC characterization (of PA circuit and individual transistors). The VNA provides RF power during stress, and also is required for characterization of RF circuit performance.

C. Description of the Stress Experiments

Different combinations of DC and RF stress have been applied to the PA circuits. The DC stress consists of supplying a V_{DD} voltage well above the nominal 1.2 V value, while the RF stress consists in simultaneously applying a 2.45 GHz tone to its input. Most of the measurements presented in this paper are presented as two experiments, summarized in Table II. In Experiment 1, the same DC stress conditions are applied (same V_{DD}), while the input power of the RF stress component took values from a small -20 dBm value, to a significant +10 dBm. This was the maximum power for which the circuits behaved as linear amplifiers and showed progressive increased degradation. In Experiment 2, the same RF P_{IN} = 6 dBm was applied to all the samples, while the DC stress was changed by applying different V_{DD} supply voltages. Nominal stress time is 30 minutes in all these cases. Remark that changing V_{DD} or P_{IN} does *not* mean a continuous sweep during stress, but each stress situation (each combination of V_{DD} and P_{IN} values) was applied during 30 minutes, on a different fresh circuit sample. Besides these two reference experiments, a few other measurements consisted of one-hour stress interrupted at regular time intervals, which allowed intermediate measurements and obtain I_{DC} degradation trends as a function of time.

TABLE II

SUMMARY OF AGING EXPERIMENTS PERFORMED ON THE PA CIRCUITS

	Experiment 1 Aging dependence on the RF component	Experiment 2 Aging dependence on the DC component
CR PA topology	V_{DD} = 2.8 V RF $P_{IN} \in$ {-20, +10} dBm	$V_{DD} \in$ {2.0, 2.8} V RF P_{IN} = +6 dBm
CS PA topology	V_{DD} = 2.2 V RF $P_{IN} \in$ {-20, +10} dBm	$V_{DD} \in$ {1.8, 2.4} V RF P_{IN} = +6 dBm

During the different stress situations, the transistor junctions are forced to strong voltage swings, resulting in electrical fields that enable BTI and HCI aging mechanisms. Fig. 4 plots the V_{GS} and V_{DS} voltages experienced by the transistors in both PA circuits during Experiments 1 and 2, obtained from simulations of the IC together with models of the external components. The RMS of the total voltage is represented, since it captures the contribution of both DC and RF components, and provides a better correlation to the observed degradation than the peak voltages. In fact, this metric is used in Section III as input to a semi-empirical model to predict transistor degradation. It must be noted that, while accelerated stress obviously also increases the drain current (up to 100 mA in the extreme cases), we have not observed a coherent correlation between the currents monitored and the measured degradations.

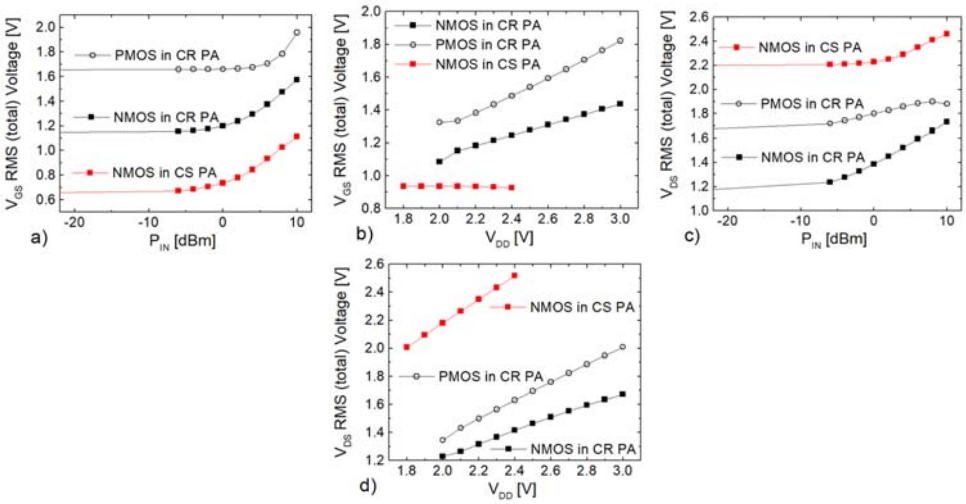


Fig. 4. Expected V_{GS} and V_{DS} voltages experienced by the transistors in both PA circuits during Experiments 1 and 2, obtained from circuit simulations.

As otherwise expected, simulations predict that transistors in the CR circuit are exposed to larger V_{GS} voltages during the stress (V_{DD} was increased above the nominal value during stress, while gate bias voltage in the CS circuit remained the same). On the contrary, the NMOS transistor in the CS PA circuit will be exposed to larger V_{DS} voltages than the transistors in the CR PA circuit. Therefore, it is expected that both PA circuits, although producing similar overall performance as shown in Table I, will experience important operation differences that will trigger differently the BTI and HCI effects.

III. Measurements of Aging in MOSFETs

A. NMOS and PMOS Degradation with DC and RF Stress

As a consequence of the stress applied, transistor characteristics are progressively degraded. For illustrative purposes, Fig. 5 depicts the $I_D(V_{GS})$ curves of the NMOS and PMOS transistors of the CR PA circuit, measured after several interruptions in a one-hour stress, in this case for a DC stress condition of V_{DD} = 3 V and RF input power P_{IN} = 6 dBm. Aging modifies the DC transistor characteristics, shifting the curves to higher voltages –V_{TH} increase– and reducing the slope –mobility decrease–. A first observation is that, although the stress intervals are increased following a potential law, curves are approximately equally spaced. This means aging degradation is dominantly produced in the first instants of circuit operation, which is consistent with classical models [4]. A second observation is that, although both transistors are stressed with similar voltages –in fact, larger V_{GS} and V_{DS} in the PMOS, see Fig. 4–, the effects on the NMOS transistor are significantly more important that those suffered by the PMOS device.

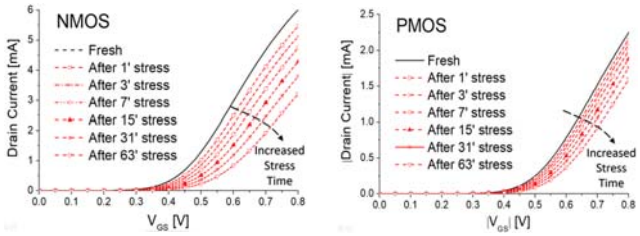


Fig. 5. Degradation of the characterisc $I_D(V_{GS})$ curves @ V_{DS} = 50 mV, of the NMOS and PMOS transistors of the CR PA, after increasing stress times. Stress conditions are V_{DD} = 3.0 V together with a RF 2.45 GHz tone of P_{IN} = 6 dBm.

While BTI degradation is conventionally more important in PMOS transistors (NBTI), HCI produces stronger degradation in NMOS [1]. This difference related to HCI is mainly attributed to the shorter mean-free path of holes in PMOS transistors [4], which can be related to the different carrier mobility. The lower HCI degradation of PMOS short-channel transistors compared to NMOS has been verified experimentally under constant DC stress [22]. Our observations then suggest that HCI is probably the dominant degradation mechanism produced in our circuits, which will be later endorsed with other observation.

In order to evaluate quantitatively the MOS transistor degradation under different stress conditions, threshold voltage V_{TH} and mobility μ have been extracted from the above $I_D(V_{GS})$ curves in the ohmic region. A least-squares algorithm was used to

determine the V_{TH} and μ_0 values that minimize the error between measurements and the simple MOS model in the triode region (1) with mobility degradation [23], after deembedding source and drain voltage drop in the measurement setup.

$$I_D = \frac{\mu_0 \cdot C_{ox}}{1+\theta(V_{GS}-V_{TH})}\frac{W}{L}\left[(V_{GS}-V_{TH})V_{DS}-\frac{V_{DS}^2}{2}\right] \qquad (1)$$

Fig. 6 plots the variation observed in these parameters, for the NMOS and PMOS transistors of the CR PA, after Experiments 1 and 2. Results show that the degradations of both V_{TH} and μ parameters of the NMOS are significantly larger than those of the PMOS, as expected from observation of Fig. 5. Most interestingly, it can be seen how a large DC stress alone (V_{DD} = 2.8 V but small P_{IN}) or large RF stress alone (P_{IN} = 6 dBm but small V_{DD}) do not produce significant degradation of the transistor parameters. On the contrary, degradation shows only after the combination of DC+RF stress. Also the amount of degradation produced by changing V_{DD} or P_{IN} is similar. These observations denote similar relevance of the DC and RF components in the aging degradation, in agreement with some previous simulation [24] and experimental [13] works.

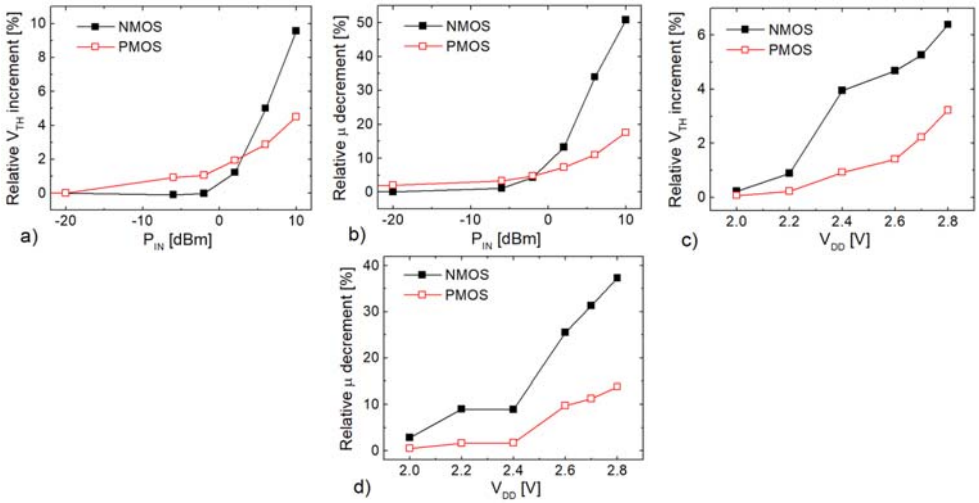


Fig. 6. Extracted variation of V_{TH} –(a) and (c)– and mobility μ –(b) and (d)– after 30 min. of stress in Experiments 1 and 2. Comparison between degradation of the NMOS (solid) vs. that of the PMOS (hollow) in the CR PA topology.

B. NMOS Degradation vs. PA Circuit

The same experiments done on the CR PA topology (aging vs. RF stress component and aging vs. DC stress component) are now repeated for the second CS PA configuration. Note in this case the single NMOS transistor sees the V_{DD} voltage directly applied to its drain terminal, thus smaller DC stress values are selected for this topology (see Table II). The power of the input tone producing the RF stress component is the same in both circuit topologies, for each of the experiments.

Fig. 7 compares the degradation observed, for each stress combination, on the V_{TH} and mobility of the NMOS transistor in each of the circuit topologies. Remember this NMOS device is physically identical in both PA circuits. It can be observed how, for the same applied stress, the NMOS transistor in the CS PA suffers significant stronger degradation than in the CR PA. Compare for example the degradation after V_{DD} = 2.4 V and P_{IN} = +6 dBm (Fig. 7(c) and 7(d)): the NMOS in the CS PA suffers degradation of V_{TH} and μ of 10.3% and 54.4% respectively, which reduce to 3.9% and 8.9% for the NMOS in the CR PA circuit. Even with negligible RF signal (P_{IN} = –20 dBm), the NMOS in the CS PA is significantly degraded (degradation of V_{TH} and μ of 3.9% and 25.8% respectively) while the NMOS in the CR PA suffers practically no degradation.

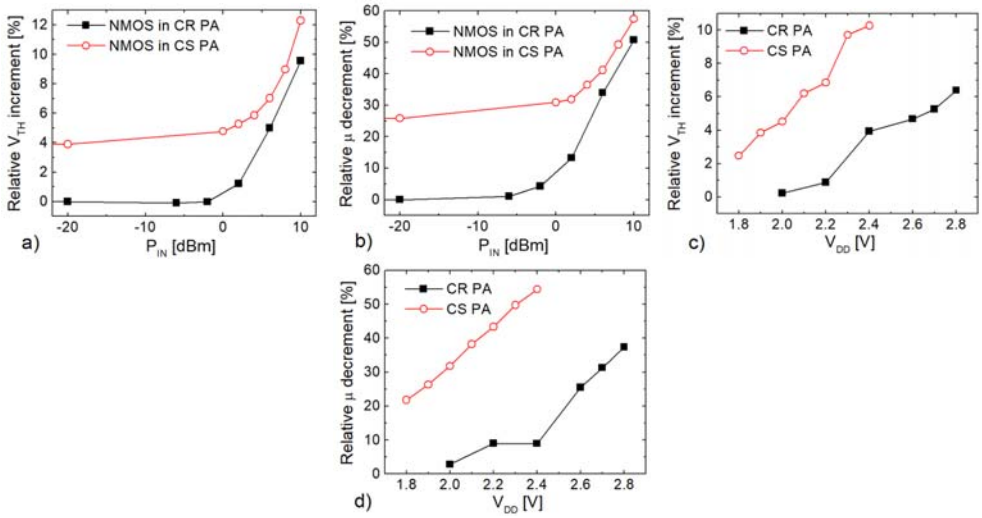


Fig. 7. Extracted variation of V_{TH} –(a) and (c)– and mobility μ –(b) and (d)– after 30 minutes of stress in Experiments 1 and 2. Comparison between degradation of the NMOS in the CR PA topology (solid) vs. that of the NMOS in the CS PA topology (hollow).

C. Modeling Transistor Degradation Produced with DC + RF Stress

Nowadays, most PDKs (Process Design Kits) for nanometer technologies include MOS parameters for complex aging models. Circuit designers then can use specific simulation tools [25] to predict the performance of a circuit after years of operation, when degraded as a consequence of HCI and BTI effects. Although these complex models can provide accuracy, simple models are preferred to obtain fast, handy estimations, but most important, to provide intuitive relationships helpful to the circuit designer. We propose in this section to validate a simple procedure to relate DC and RF operating conditions to the circuit degradation observed.

Analytical models to predict HCI and BTI degradation were derived in [6], [9], which were later simplified to the compact expressions (2), (3), consisting of a potential time law multiplied by exponential dependences on the lateral and vertical electrical fields [1]:

$$\Delta V_{TH,HCI} \propto e^{\alpha_{HCI1}E_{ox}} e^{-\frac{\alpha_{HCI2}}{E_{lat}}} t^{n_{HCI}} \qquad (2)$$

$$\Delta V_{TH,BTI,permanent} \propto e^{\alpha_{BTI1}V_{GS}} e^{-\frac{E_a}{k_B T}} t^{n_{BTIp}} \qquad (3)$$

The exponent in the time-potential law is a constant, as discussed in [4]. These expressions were further simplified in [18] as simple exponential dependences on the V_{GS} and V_{DS} applied voltages. These resulting models are simple enough for handy estimation, but were only validated in DC situations. Ignoring the RF stress contribution to aging degradation is not an option outside the small-signal regime, as evident from the measurements in our PA circuits. Time-integration can be used to account for the signal stress component [17], but this prevents usage for hand calculations. As a compromise between accuracy and simplicity, we propose to use the RMS [1] V_{GS} and V_{DS} voltages in the transistor as a metric that captures the combined DC and RF stress producing aging degradation. These equivalent voltages can be easily obtained from a simple transient simulation of the circuits. Then, a simple and intuitive prediction of the threshold voltage degradation can be obtained from simple exponential dependences on V_{GS} and V_{DS} RMS voltages,

$$\Delta V_{TH} = \beta_1 \cdot e^{\alpha_1 V_{GS,rms} + \alpha_2 V_{DS,rms}} \cdot t^{n1} \qquad (4)$$

where β_1, α_1 and α_2 are technology-dependent parameters. An equivalent expression is proposed to estimate the degradation of the $\mu \cdot C_{ox}$ parameter:

$$\Delta \mu \cdot C_{ox} = \beta_2 \cdot e^{\alpha_3 V_{GS,rms} + \alpha_4 V_{DS,rms}} \cdot t^{n2} \qquad (5)$$

The aging degradation observed in the NMOS transistors in our circuits has been compared against the RMS voltage dependence expressed in (4), (5). Simulation of the CR and CS PA circuits in the different stress situations in Experiments 1 and

[1] RMS of total voltage including both DC and AC components.

2 allowed to obtain the RMS values of the V_{GS} and V_{DS} voltages in the transistor terminals, represented in Fig. 4. Then we have empirically extracted values for α_i and $\beta_i \cdot t^n$ coefficients (with t = 1800 s) that would best fit the predictions in (4), (5) to the measured degradations. Fig. 8 compares the measured degradation on the threshold voltage (Fig. 7(a) and 7(c)) against the model prediction (4). The plot also includes other stress combinations (V_{BIAS} and V_{DD} values) different to those of the V_{DD} and P_{IN} sweeps. A strong correlation between model predictions and experimental results is observed, validating the method proposed to produce first-hand estimations.

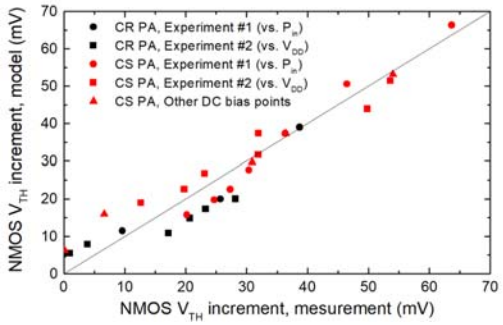


Fig. 8. V_{TH} degradation measured (X-axis) vs. model prediction (Y-axis). Measurements include Experiments 1 and 2 in both the CR and CS PA circuits (values in Fig. 7), and also other stress situations for different V_{IN_DC} and V_{DD} values in the CS circuit. Model prediction as of (4), where voltages are RMS values obtained from circuit simulations (Fig. 4).

The process has been repeated to fit the measured degradation of mobility (Fig. 7(b) and 7(d)) to expression (5) (assume C_{ox} remains constant). Fig. 9 shows how the prediction based on simulated RMS voltage now shows even better correlation to the measured aging, despite the situations analyzed include two different PA circuits, at different bias points, different DC and RF stress conditions, with the same technology-dependent parameters.

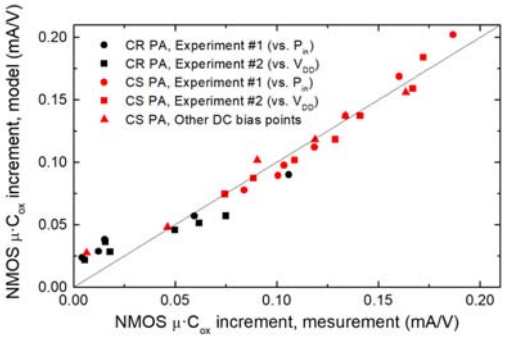


Fig. 9. $\mu \cdot C_{ox}$ degradation measured (X-axis) vs. model prediction (Y-axis). Measurements include Experiments 1 and 2 in both the CR and CS PA circuits (values in Fig. 7), and also other stress situations for different V_{IN_DC} and V_{DD} values in the CS circuit. Model prediction as of (5), where voltages are RMS values obtained from circuit simulations (Fig. 4).

Fig. 8 and 9 then validate the relationship between equivalent RMS voltages in the transistor terminals, and the progressive degradation produced as a consequence of HCI and BTI effects. Note this is in contrast to other reliability degradation issues in PAs, which may be triggered by occasional transient events.

IV. Bias Point Sensitivity to MOSFET Aging

A. DC Circuit Degradation

The degradations in the threshold voltage and mobility of the MOS transistors in both PA configurations produce a modification of the bias point in these circuits, which will ultimately impact their RF response. This section presents the measurements of the degradation suffered in the DC bias point of the CR and CS PA circuits, for each of the experiments described in Section II.B. For the CR PA configuration, which is self-biased, both the DC current I_{DC}, and the DC voltage $V_{INV} = V_{IN\_DC} = V_{OUT\_DC}$ are measured, while for the CS PA configuration, where DC voltages are set externally, only the I_{DC} current is evaluated. Nominal values for these parameters before aging is produced are detailed in Table I.

The degradations measured after 30 minutes of accelerated stress for each of the experiments are plotted in Fig. 10. It can be observed how the dependences with the DC (V_{DD}) or RF (P_{IN}) stress components follow qualitatively those of the MOS parameters in Fig. 7. In particular, the strong difference in aging degradation between the two circuit topologies becomes evident

now. For example, after being stressed with V_{DD} = 2.4 V and P_{IN} = 6 dBm, the I_{DC} current in the CS PA suffers a 65% decrease, while the CR PA stressed in the same conditions during the same time only experiences a 12% degradation.

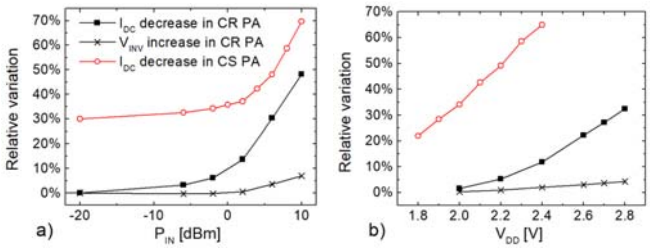


Fig. 10. Degradation of the DC bias point in the CR and CS amplifers after 30 minutes of accelerated stress in the experiments detailed in Table II. Decrease of the DC current is plot, and also the variation of DC voltage in the CR circuit.

Besides being more robust in terms of I_{DC} decrease, the CR PA experiences a very small variation in the DC input-output voltage. This is a consequence of the complementary effects of the NMOS and PMOS transistor degradations in this circuit. For a DC analysis, the CR PA can be viewed as a voltage divider. The consequence of the aging degradation is an increase in the drain-source channel resistance of both transistors, but since the degradation in the PMOS device is smaller than that of the NMOS (Fig. 6), the result is a small increase in the DC intermediate voltage.

While all the measurement results presented so far are obtained after a 30-minutes stress, it is interesting to experimentally observe how the degradation evolves after increasing stress times. To obtain this time dependence, the stress applied to each circuit sample was stopped at regular intervals, and intermediate MOSFET and circuit characterizations were done at those instants. These time measurements have been done for only one of the experiments in Table II: V_{DD} dependence (Experiment 2). The bias point (I_{DC} current) degradation on the CR PA circuit observed as a function of the stress time is plotted in Fig. 11. For a better reading, time is plotted in a log scale, since most degradation is produced in the first minutes. Note for example how, when stressed with V_{DD} = 3.0 V, one minute is enough to produce a 10% degradation in the I_{DC} current of the CR PA. Fig. 11 shows a power-law time degradation of I_{DC}, with time exponent $n \approx 0.43$. Note this is consistent with the models for the V_{TH} degradation produced by HCI and permanent BTI aging phenomena [4], [6], [9], as well as the prediction proposed in (4), (5).

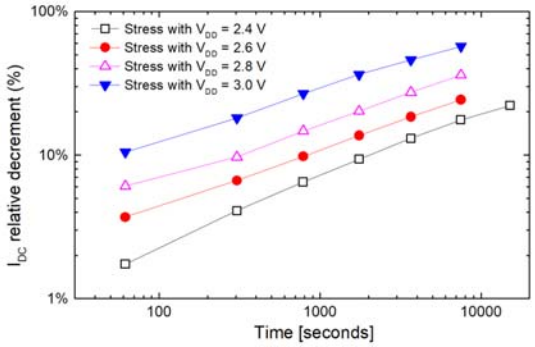


Fig. 11. Degradation of the DC bias point in the CR PA as a function of the stress time, for different DC stress conditions and P_{IN} = 6 dBm. Note the degradations in Fig. 7 correspond to an stress time of 1800 s in this plot.

B. Predicting DC Circuit Degradation Produced by NMOS Aging

The predictions of V_{TH} and mobility degradation offered by (4) and (5) can be used to predict analytically the impact on the bias point in simple circuits. Furthermore, this can provide insight into how transistor aging translates into circuit degradation.

Drain current for an NMOS in the saturation region can be approximated as

$$I_{DC} = \frac{\mu_0 C_{ox}}{2}\frac{W}{L}\frac{\left(V_{GS}-V_{TH}\right)^2}{1+\theta\left(V_{GS}-V_{TH}\right)}\left(1+\lambda V_{DS}\right) \qquad (6)$$

where λ is the channel length modulation factor, and ϑ models the mobility degradation produced with strong electrical fields [23]. Assuming moderate aging degradations of V_{TH} and μ_0, and neglecting the possible degradations suffered by C_{ox}, λ and θ parameters, the variation produced in I_{DC} as a consequence of aging can be approximated as

$$\Delta I_{DC} \approx \frac{\partial I_{DC}}{\partial \mu_0}\Delta\mu_0 + \frac{\partial I_{DC}}{\partial V_{TH}}\Delta V_{TH} \qquad (7)$$

Inserting (6) into (7), the relative degradation of the drain current can be expressed in function of the relative variations of the threshold voltage and mobility as:

$$\frac{\Delta I_{DC}}{I_{DC}} = \frac{\Delta \mu_0}{\mu_0} + \left[\frac{3\theta \cdot V_{TH}}{1+\theta(V_{GS}-V_{TH})} - \frac{V_{TH}}{(1+\theta(V_{GS}-V_{TH}))(V_{GS}-V_{TH})} \right] \frac{\Delta V_{TH}}{V_{TH}} \quad (8)$$

Observe how this expression can be evaluated from the nominal models parameters in the saturation region, and from the V_{TH} and mobility degradations estimated using (4), (5). We have produced this evaluation for the CS PA circuit, and compared it against the measured I_{DC} degradation measured after 30 min. of stress, represented in Fig. 10. The comparison of the prediction using (4), (5), and (8) against measurements is shown Fig. 12, for each of the Experiments 1 and 2, and also for other arbitrary stress situations (different V_{IN_DC} and V_{DD}). It can be observed how the simple model prediction provides a useful estimation of the combined effect of a DC and RF stress on the aging degradation of the PA circuit.

Besides quantitative estimation, (8) can be used to provide an intuitive understanding of the relationship between DC bias current and transistor degradation. According to the first term in this equation, mobility degradation is directly translated to degradation of I_{DC} current. On the contrary, the variation of the threshold voltage has a lesser impact on I_{DC}, because the V_{TH} degradation is small compared to that of the mobility (Fig. 7), but also because of the two subtracted terms in (8). In the predictions represented in Fig. 12, the contribution of the ΔV_{TH} term in (8) was always below 10% of the total result. Therefore, mobility degradation is the dominant contributor to the DC current degradation in these experiments, and this explains the similarity between the I_{DC} and μ degradations in the CS PA (Fig.7(b) compared to Fig.10(a); Fig.7(d) compared to Fig.10(b)). While many works in the literature focus on modeling only the V_{TH} degradation as a consequence of aging phenomena [6], [26], the above observation highlights the need to observe and model the effects on the mobility [14].

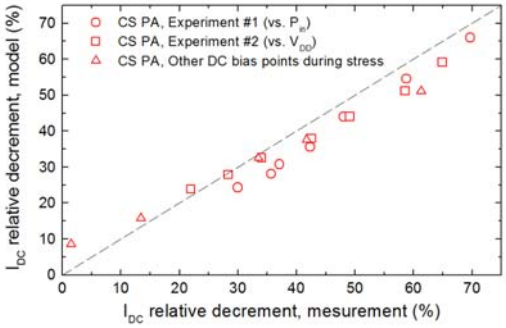


Fig. 12. DC current degradation in the CS PA, measurements (X-axis) vs. model prediction (Y-axis). Measurements include Experiments 1 and 2 (values in Fig. 7), and also other stress situations for different V_{IN_DC} and V_{DD} values. Model prediction as of (8), where V_{TH} and μ degradations have been estimated using (3) and (4).

Equation (5) proposes that it is possible to estimate the mobility degradation from a linear combination of RMS drain and gate voltages during the stress. From the experimental measurements in the 65 nm transistors, the linear coefficients $\alpha_3 = 1.07$ and $\alpha_4 = 1.79$ were extracted. Although these values point to a higher impact of the V_{DS} voltages on the transistor degradation, drain voltage is not necessarily the reason of the trends observed in the different experiments in this work. For example, observing the RMS voltages in Fig. 4 for the CS PA circuit, $V_{DS,rms}$ increases only moderately after increasing P_{IN}, since the PA enters into compression (peak V_{DS} voltages saturate, in fact). On the contrary, the $V_{GS,rms}$ voltage almost doubled when increasing P_{IN} from -20 to +10 dBm. In contrast, the degradation of the CS PA observed in Experiment 2 (increased V_{DD} values) is fully related to the increase of $V_{DS,rms}$ voltage, as far as the gate voltage remains unchanged. The models proposed thus allow to establish comparisons between different operating conditions accounting for both the DC and AC (RF) contributions. But also, allow to compare the expected aged performance of different circuit solutions. Applied to the circuits measured in this work, the model explains how the lower V_{DS} voltages in the MOS transistors of the CR PA produce a lower degradation of this circuit, compared to the CS PA. This conclusion can be extended to other similar circuit solutions (e.g. cascode [27]).

V. Aging Degradation of PA RF Performance

The experimental study of aging degradation experienced by the CR and CS PA circuits has been completed by characterizing their RF response. S-parameters have been measured in each of the experiments, before and after stress, together with the 1-dB compression point.

A. Aging effects on the Gain

In class-A operation, the reduction of the DC current observed in Section IV directly degrades the transistors transconductance g_m, and thus the amplification provided by the CR and CS PA circuits. Fig. 13 plots the variation observed in the small-signal gain parameter S_{21}, measured at 2.45 GHz frequency, after each of the experiments in Table II. As expected, the gain degradation as a function of the DC and RF stresses (V_{DD} and P_{IN}, respectively) follows the general trends observed for the I_{DC} current variations in Fig. 10. But a close comparison of Fig. 10 and Fig. 13 reveals that the degradation of the CR PA circuit, compared to that of the CS PA, is even lower when observed in terms of gain. To get more insight in this comparison, the relative degradation of S_{21} parameter (now in linear units) is plotted against the relative degradation of the DC current, for all the experiments represented in Fig. 10 and 13. The resulting plot is shown in Fig. 14. It can be observed how linear relationships between DC current variations and gain variations are observed, irrespective of the type of stress (DC or RF) that has produced that degradation. But remarkably, the different slopes indicate that the bias current degradation affects more importantly the gain in the CS PA, than the gain of the CR PA. The gain in the CR PA is contributed by the small-signal transconductances of both NMOS and PMOS (g_{mN} and g_{mP}, respectively), while the gain in the CS depends only on the NMOS. As observed in Section III.A, the degradation of the PMOS transistor is smaller than that of the NMOS, for a given stress situation. Therefore, degradation of g_{mP} is lower than that of g_{mN}. The circuit with a gain contributed by both g_{mN} and g_{mP} will be thus less sensitive to degradation of the DC current than a circuit where the gain depends entirely on g_{mN}. This explains the different sensitivity of the gain to DC current variation in the CR and CS PAs, shown in Fig. 14.

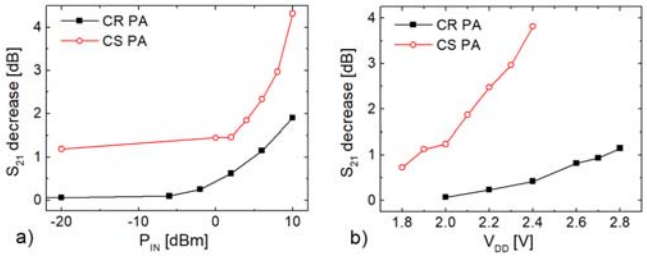


Fig. 13. Degradation of the S_{21} gain parameter at 2.45 GHz, in the CR and CS amplifers after 30 minutes of accelerated stress in the experiments in Table II.

The above discussion allows to conclude that the CR PA topology is more robust against aging, compared to a more conventional CS topology, because of a double reason. On one side, for the same DC bias and RF input, the current-reuse topology produces lower V_{DSrms} voltages in the transistors, which result in lower transistor aging, and thus lower degradation of the DC current. But besides that, the gain of CR circuit happens to be less sensitive to DC current variations than the gain of the CS topologies. As a result of this, the effects of aging on the amplification (and thus output power) in a CR PA are largely smaller than in a CS topology. Lifetime of these circuits extrapolated to nominal supply (V_{DD} = 1.2 V) was estimated in [19]: while in the CS PA a gain degradation of 3 dB would be produced after approximately only 3 years, it would take in the order of 100 years in the CR PA.

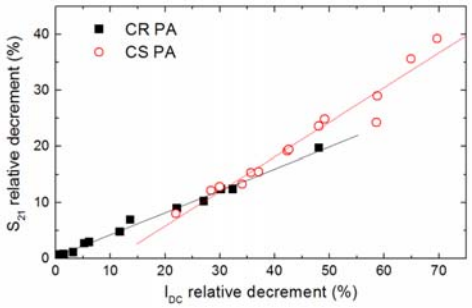


Fig. 14. Degradation of the S_{21} gain parameter at 2.45 GHz, in the CR and CS amplifers, related to the DC current degradation after 30 minutes of accelerated stress in the experiments detailed in Table II. Points are the experimental measurements (Fig. 10 and Fig. 13), while lines are interpolated linear trend laws for each amplifier.

B. Aging effects on matching

In the CR and CS PA circuits designed in this work, broadband impedance matching is obtained with the addition of shunt-feedback (R_F in Fig. 1). Therefore, from basic circuit analysis, gain degradation is expected to affect severely the matching parameters. Fig. 15 shows the measured value of the S_{11} parameter at 2.45 GHz, after the different stress experiments. As

predicted, the shunt-feedback solution degrades matching following a close correlation to the gain degradation in Fig. 13. Similar trends were obtained for the S_{22} parameter. This particular experiment illustrates how an amplifier with acceptable matching (see nominal values in Table I) can turn into a mismatched amplifier as a consequence of aging phenomena.

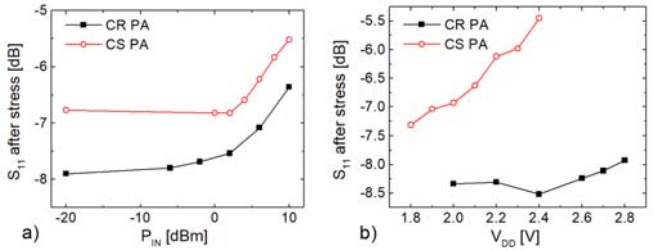


Fig. 15. S_{11} at 2.45 GHz, in the CR and CS amplifers after 30 minutes of accelerated stress in the experiments in Table II.

C. Effect of the circuit temperature

Maximum output power delivered by the test PA circuits is slightly beyond the ~5 dBm compression point, and this is a relatively low power compared to high-end 2.45 GHz PAs delivering ~30 dBm. While a few dBm P_{OUT} is reasonable in low-end PA's, a differential aspect at higher power levels is the temperature increase produced by self-heating effects. In our experimental set-up, self-heating effects were minimized since the ICs were glued with conductive epoxy to a metal support directly attached to the chuck, thus providing excellent thermal dissipation. Still, we want to investigate how the gain degradation is affected when the stress is produced at increasing temperatures. For that purpose, we used a thermo-chuck to apply increasing temperatures to the circuits. The same stress was applied to both PA configurations, V_{DD} = 2.8 V and P_{IN} = 6 dBm, with interruptions after 6, 30 and 60 minutes. The gain performance of the circuits was characterized after each of these interruptions.

The measured evolution of the gain after increasing stress times is plot in Fig. 16, for the different temperatures. A first observation is that at time zero, gain reduces as a consequence of the temperature increase. Both threshold voltage and mobility decrease with temperature, which produces complementary effects on the DC current [28]. Because of the strong effect of the mobility, the result in our circuits is a current reduction. The gain degradation is lower in the CR PA topology, because of the lower temperature sensitivity of the PMOS, and the reduced gain dependence on the DC current, as discussed in Section V.A.

After applying accelerated stress, gain degradation is produced, stronger in the CS circuit in coherence with measurements in Fig. 13. Interestingly enough, the initial differences observed at increasing temperatures tend to vanish as stress time increases, leading to approximately the same degraded gain values after one hour of stress. Results thus indicate that no significant differences on the RF gain performance resulting after aging degradation are expected by operating our circuits at higher temperatures.

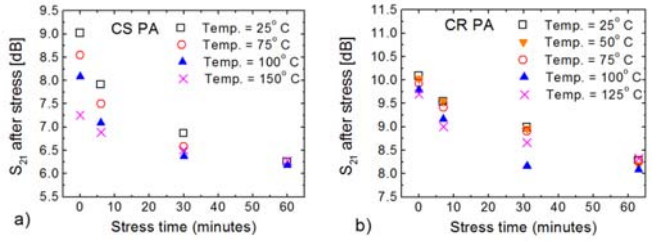


Fig. 16. S_{21} time evolution, measured at nominal V_{DD} = 1.2 V, after accelerated stress at increasing temperatures. (a) Measurements on the CS PA topology and (b) on the CR PA circuit topologies.

D. Aging effects on the Compression Point

While the experiments above have evidenced the better robustness of the CR PA in terms of gain and matching degradation, its PMOS+NMOS structure may look prone to suffer linearity degradation. Contrary to this intuition, the nominal (fresh) output-referred compression point of this circuit is only slightly (0.3 dB) worse than that of the CS PA. We have measured how this compression in the CR PA is degraded as a consequence of the aging produced after each of the experiments in Table II. Results in Fig. 17 show that, while aging degrades the output-referred compression point, the degradation produced is moderate, 0.6 dB in the worst case. Note that, since the S_{21} degradation is stronger (more than 1 dB, in the worst case), the input-referred compression point is actually increased (the PA can allow more input power to reach compression). The variations experienced in P_{-1dB} are anyhow small, and show that the CR PA solution is not disadvantageous in this respect.

In order to improve robustness against aging variability, self-healing techniques have been proposed in CS-based PA topologies in order to adaptively adjust the transistor bias after sensing the output power [29], [30]. Being a self-biased amplifier, such approach cannot be directly applied to the CR PA. Instead, gain loss should be compensated by increasing the power coming from pre-amplification stages, namely P_{IN} in our measured PA circuit. Results in Fig. 17 show that this a feasible approach, as far as output compression remains slightly affected by the aging degradation.

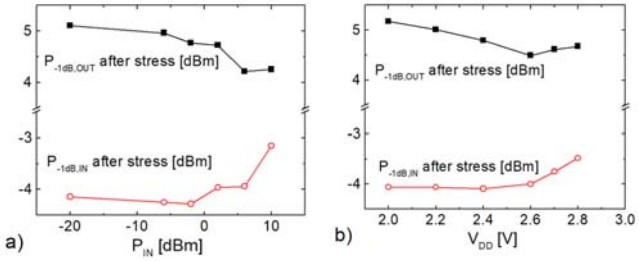


Fig. 17. Output-referred (back squares) and Input-referred (red circles) 1-dB compression point in the CR amplifier after 30 minutes of accelerated stress in the experiments in Table II.

E. Aging effects on the power efficiency

The power added efficiency (PAE) has been evaluated after each of the stress experiments in the CR PA circuit, and the results are represented in Fig. 18. The moderate degradation of the compression point, compared to the current degradation, results in a counter-intuitive moderate increase of the PAE after aging. Note that more input power is required to reach P_{-1dB} after stress (Fig. 17), while transistor threshold voltages have increased. This will decrease the transistors conduction angle (at compression, the circuit operates as class-AB) thus allowing increased efficiency, for the same output power.

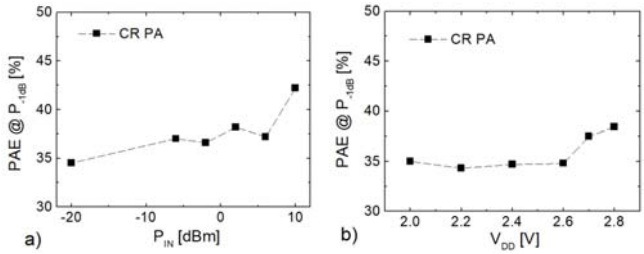


Fig. 18. Power Added Efficiency (*PAE*) of the CR amplifier, measured at the 1-dB compression point after 30 minutes of accelerated stress in the experiments in Table II.

F. Aging dependence on the frequency of the RF stress

Since one of the observations in this work is the importance of the RF stress component, we have finally evaluated the aging degradation as a function of the frequency of this RF stress component. The analysis has been done only in the CR PA, stressed at V_{DD} = 2.8 V and P_{IN} = +6 dBm during 30 min. The degradation of the gain parameter (S_{21}) and output-referred compression point ($P_{-1dB,OUT}$) measured at the PA operation frequency of 2.45 GHz is plotted in Fig. 19, in both cases together with the frequency response of the PA (before stress). Results show that the degradation effects decrease as frequency of the RF stress is increased, following roughly the same trend as the frequency response of the PA circuit. While the same V_{DD} and RF input power were applied at all frequencies, the RF output swings decrease as the PA gain decreases at high frequencies, thus producing less degradation.

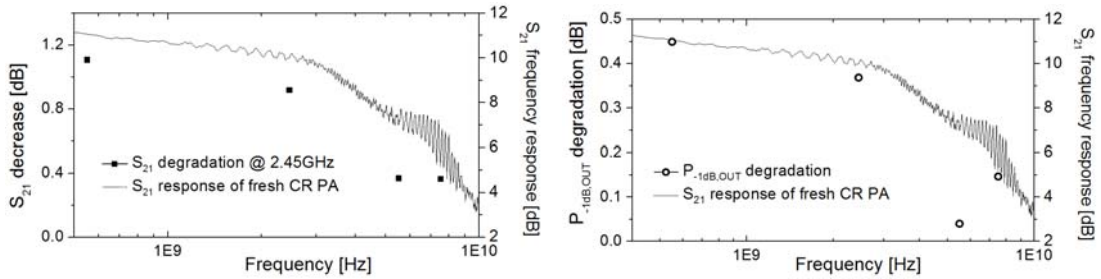


Fig. 19. Degradation of S_{21} (top) and $P_{-1dB,OUT}$ (bottom) at 2.45 GHz in the CR PA, produced by RF stress at different frequencies (symbols). Stress condition was V_{DD} = 2.8 V and P_{IN} = 6 dBm. Superposed (continous line) is the frequency response of the PA before the stress.

VI. Conclusion

The results of an experimental study to observe and comprehend the aging produced in linear RF PA circuits have been presented. A circuit has been designed in a 65 nm CMOS technology, that allows to be externally configured as two different representative PA topologies, one based on current-reuse, and one common-source loaded with choke inductor. Both topologies produce similar PA performance at 2.45 GHz. Aging effects produced by HCI and BTI have been measured at both transistor and circuit level after different experiments of accelerated stress. Experiments have evidenced the importance of the RF signal on the PA aging: variations produced after increasing V_{DD} voltage well above the nominal 1.2 V value were negligible if no RF signal was applied, while important degradation was observed after adding a RF signal component.

Measurements have shown how aging produces important degradation of MOS mobility and threshold voltage parameters, being the mobility the most affected. MOSFET degradation results in reduction of the DC current in the PA circuit, and simple models have allowed to relate this DC current variation dominantly to the mobility degradation of the NMOS transistors. We have proposed the equivalent RMS voltage in transistor terminals as a compact and intuitive metric to relate combined DC+RF stress to the aging degradation, which has been validated against experimentation. Our simple compact model has been used to identify the smaller equivalent voltage at the drain terminals of the transistors in a CR PA topology as the main responsible for its fairly better robustness against aging, compared to a classical CS solution.

As a consequence of the smaller bias point degradation, the aging impact on the PA gain at 2.45 GHz is radically smaller in a CR circuit than in an equivalent implementation based on a CS topology. Besides, it has been observed that PMOS transistors suffer significantly smaller degradation than NMOS ones, which also contributes to the smaller degradation of the CR PA gain. The better robustness of the CR PA also results in a better matching robustness, while we have shown that output compression is not significantly degraded. Finally, we have observed how the impact of the RF stress component decreases at high frequencies, in correlation with the PA frequency response.

References

[1] E. Maricau and G. Gielen, *Analog IC reliability in nanometer CMOS*. New York: Springer-Verlag, 2013.

[2] T. Guo, J. Xie, "A complete reliability solution: reliability modeling, applications, and integration in analog design environment", in *3rd Sino MOS-AK Workshop*, Beijing, China, 2018.

[3] B. Tudor *et al*, "MOS device aging analysis with HSPICE and CustomSim", Synopsys Inc., 2011. [Online] Available: http://www.synopsys.com/content/dam/synopsys/verification/white-papers/mosra-wp.pdf

[4] C. Hu *et al.,* "Hot-electron-induced MOSFET degradation—Model, monitor, and improvement," *IEEE Trans. Electron Devices*, vol. 32, no. 2, pp. 375-385, Feb. 1985.

[5] X. Li, J. Qin and J. B. Bernstein, "Compact modeling of MOSFET wearout mechanisms for circuit-reliability simulation," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 1, pp. 98-121, Mar. 2008.

[6] E. Maricau *et al.*, "An analytical model for hot carrier degradation in nanoscale CMOS suitable for the simulation of degradation in analog IC applications," *Microelectronics Reliability*, vol. 48, no 8-9, pp. 1576-1580, 2008.

[7] B. Kaczer *et al.*, "Ubiquitous relaxation in BTI stressing—New evaluation and insights," in *44th IEEE Int. Reliability Physics Symp. (IRPS)*, Phoenix, AZ, USA, 2008, pp. 20-27.

[8] N. Ayala, J. Martin-Martinez, R. Rodriguez, M. Nafria and X. Aymerich, "Unified characterization of RTN and BTI for circuit performance and variability simulation," *European Solid-State Device Research Conf. (ESSDERC)*, Bordeaux, France, 2012, pp. 266-269.

[9] E. Maricau and G. Gielen, "NBTI model for analogue IC reliability simulation," *Electronics Letters*, vol. 46, no. 18, pp. 1279-1280, Sep. 2010.

[10] E. Amat *et al.*, "Competing degradation mechanisms in short-channel transistors under channel hot-carrier stress at elevated temperatures," *IEEE Trans. Device Mater. Rel.*, vol. 9, no. 3, pp. 454-458, Sep. 2009.

[11] L. Larcher *et al.*, "Oxide breakdown after RF stress: Experimental analysis and effects on power amplifier operation," in *44th IEEE Int. Reliability Physics Symp. (IRPS)*, San Jose, CA, USA, 2006, pp. 283-288.

[12] C. D. Presti *et al.*, "Degradation mechanisms in CMOS power amplifiers subject to radio-frequency stress and comparison to the DC case," in *45th IEEE Int. Reliability Physics Symp. (IRPS)*, Phoenix, AZ, USA, 2007, pp. 86-92.

[13] C. H. Liu *et al.,* "DC and RF degradation induced by high RF power stresses in 0.18-µm nMOSFETs," *IEEE Trans. Device Mater. Rel.*, vol. 10, no. 3, pp. 317-323, Sep. 2010.

[14] T. Quémerais *et al.*, "Hot-carrier stress effect on a CMOS 65-nm 60-GHz one-stage power amplifier," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp.927-929, Sep. 2010.

[15] T. Quemerais, L. Moquillon, J. Fournier, P. Benech and V. Huard, "Design-in-reliable millimeter-wave power amplifiers in a 65-nm CMOS Process," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 4, pp. 1079-1085, Apr. 2012.

[16] C. Yu and J. S. Yuan, "Electrical and temperature stress effects on class-AB power amplifier performances," *IEEE Trans. Electron Devices*, vol. 54, no. 6, pp. 1346-1350, Jun. 2007.

[17] L. Negre *et al.*, "Reliability characterization and modeling solution to predict aging of 40-nm MOSFET DC and RF performances induced by RF stresses," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp.1075-1083, May 2012.

[18] S. Mahato and G. Gielen, "Impact of transistor aging on RF low noise amplifier performance of 28nm technology: Reliability assessment," in *IEEE 20th Int. Conf. Electronics, Circuits, and Systems (ICECS),* Abu Dhabi, UAE, 2013, pp. 413-416.

[19] X. Aragones *et al*., "Aging in CMOS RF linear power amplifiers: experimental comparison and modeling," in *IEEE Int. Symp. Circuits and Systems (ISCAS)*, Sapporo, Japan, 2019.

[20] R. Rodriguez et al., "Experimental monitoring of aging in CMOS RF linear power amplifiers: correlation between device and circuit degradation," in *2020 IEEE Int. Reliability Physics Symp. (IRPS)*, Dallas, TX, USA, 2020.

[21] E. Barajas *et al*., "Design of a broadband CMOS RF power amplifier to establish device-circuit aging correlations," in *2017 Int. Conf. Microelectronic Test Structures (ICMTS)*, Grenoble, France, 2017.

[22] E. Amat *et al*., "Channel hot-carrier degradation in pMOS and nMOS short channel transistors with high-k dielectric stack", *Microelectronic Engineering*, vol. 87, no 1, pp. 47-50. 2010.

[23] Willy M.C. Sansen, *Analog design essentials*. Springer, 2006.

[24] M. Ruberto *et al*., "Consideration of age degradation in the RF performance of CMOS radio chips for high volume manufacturing," *2005 IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, Long Beach, CA, USA, 2005, pp. 549-552.

[25] Zhang L., Chan M., Ma C., "Reliability-aware device modeling and implications on circuit aging simulations", *TechConnect Briefs*, vol. 4, pp. 299-303, May 2016.

[26] K. Joshi, S. Mukhopadhyay, N. Goel and S. Mahapatra, "A consistent physical framework for N and P BTI in HKMG MOSFETs," *2012 IEEE Int. Reliability Physics Symp. (IRPS)*, Anaheim, CA, USA. 2012.

[27] E. Xiao *et al*., "Analysis and modeling of LNA circuit reliability," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, 2005, pp. 69- 72.

[28] I. M. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits," *IEEE Trans. Circuits Syst. I Fundam. Theory and Appl.*, vol. 48, no. 7, pp. 876-884, Jul. 2001.

[29] J. Y. Liu, R. Berenguer and M. F. Chang, "Millimeter-wave self-healing power amplifier with adaptive amplitude and phase linearization in 65-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 5, pp. 1342-1352, May 2012.

[30] J. S. Gaggatur, I. Raja and G. Banerjee, "On-chip non-intrusive temperature detection and compensation of a fully integrated CMOS RF power amplifier," in *30th Int. Conf. on VLSI Design*, Hyderabad, India, 2017, pp. 21-26.

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