CHAPTER 28

LOW DROP-OUT VOLTAGE REGULATOR AS A CANDIDATE TOPOLOGY FOR PHOTOVOLTAIC SOLAR FACILITIES

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Abstract

This chapter presents a design for a 4.5-*V*, 450-*mA* low drop-out (LDO) linear voltage regulator based on a two-stage cascode operational transconductance amplifier (OTA) as an error amplifier for photovoltaic solar DC-DC regulation. The aforementioned two-stage OTA is designed with a cascode current mirroring technique to boost the output impedance. The proposed OTA has a DC gain of 101 dB under no load condition.

The designed reference voltage included in the LDO regulator is provided by a band gap reference with the temperature coefficient (T_γ) of 0.025 *mV/ºC*. The proposed LDO regulator has a maximum drop-out voltage of 0.5 *V* @ 450 *mA* of load current, and has a worst case power supply rejection ratio (PSRR) of [54.5 *dB*, 34.3 *dB*] @ [100 *Hz*, 10 *kHz*] in full load conditions. All the proposed circuits were designed using CMOS technology. The design was checked in order to corroborate its performance for a wide range of input voltages. We found that the circuit design worked well meeting all the initial specification requirements.

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Introduction

Virtually all power supplies employ semiconductors to provide a regulated output voltage. If the supply has an AC input, it is rectified to become a DC voltage. A power DC-DC integrated circuit (IC) converter accepts a DC input and produces a DC output or controls external power output semiconductor switches to produce a suitable DC output. It is a voltage regulator when its output voltage is fed back into a circuit, causing the voltage to remain constant. In this case, if the output voltage rises or falls, the feedback causes the output to remain the same.

The power converter can operate either as a switch-mode or a linear circuit. In a linear configuration, the controlling transistor always dissipates power. This can be minimized by use of low-dropout regulators (LDOs) even when there is a relatively low voltage difference between the input and output. LDO ICs have simpler circuits than their switch-mode cousins and produce less noise (no switching), but are limited by their current-handling and power dissipation capabilities. Some LDO ICs are specified for about 200 *mA* and others can handle up to about 1 *A* [1].

Voltage Regulator Fundamentals

As shown in Fig. 1, in general, a linear voltage regulator consists of an internal reference voltage, an error amplifier, a sensing network (normally, a feedback voltage divider), and a pass device (usually, a pass transistor). The output current is delivered via the pass element controlled by the error amplifier. Note that the design limit of the pass device defines the maximum load current the regulator can source and still maintain regulation.

The error amplifier compares both the reference and output feedback voltages. The control circuitry must monitor (sense) the output voltage, and adjust the current flowing through the pass element (as required by the load) to hold the output voltage at the desired value. If the output feedback voltage is lower than the reference, the error amplifier allows more current to flow through the pass transistor. As a consequence, the output voltage increases.

On the contrary, if the feedback voltage is higher than the reference voltage, the error amplifier allows less current to flow through the pass transistor, decreasing the output voltage.

As such, the output voltage is controlled using a feedback loop, which requires some form of compensation to assure loop stability. Most linear regulators have built-in compensation, and are completely stable without external components. Although recently external-capacitorless LDOs have being receiving attention, some linear regulators (especially low-dropout types) require some form of external capacitance connected from the output lead to ground to assure regulator stability [2]-[3].

Another characteristic of any linear regulator is that it requires a finite amount of time to "correct" the output voltage after a change in load current demand. This "time lag" defines the characteristic known as transient response, which is a measure of how fast the regulator returns to a steady-state condition after a load change.

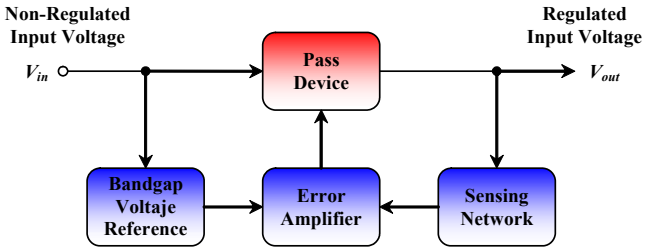

Figure 1. Block diagram of a series pass voltage regulator with feedback.

Different Types of Pass Element

NPN (quasi-LDO and Standard) Linear Regulators

Conventional linear regulators (Fig. 2) use NPN bipolar transistors as the pass element. Usually, the pass element is composed of a PNP base current driver transistor (Q_{1b}) and a single NPN power transistor or, even, a Darlington pair (Q_{1a}). In the first case, with a single NPN transistor, the regulator is usually called a ***quasi-LDO*** and, in the second case, a ***standard*** linear regulator.

Therefore, in the case of a single NPN power transistor, the drop voltage, i.e. the minimum voltage difference between input and output, is equal to:

$$V_{SAT,PNP} + V_{BE,NPN} , \tag{1}$$

which, in general, is about 1.2 *V*. Moreover, in the case of a Darlington pair, this drop voltage is given by:

$$V_{SAT,PNP} + 2V_{BE,NPN} , \tag{2}$$

which, in this case, is about 2.0 *V*.

In addition, in practical implementations, functionality and integrated protection are limited and additional protection circuitry is required.

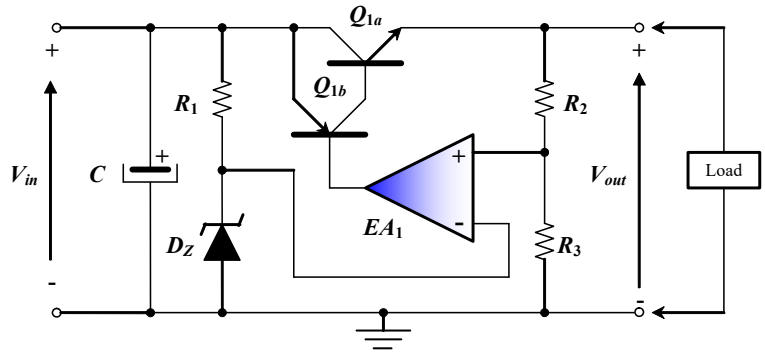

Figure 2. Series pass voltage regulator with feedback and NPN transistor as pass element.

PNP Linear Regulators

With only a single PNP bipolar transistor (Q_1 in Fig. 3) as the pass element, the drop voltage of a PNP regulator is about 0.5 *V*. For this reason, this type of regulator is called a ***low drop-out*** (LDO) regulator. This enables it to operate during a drop in battery voltage (e.g., with cranking). In addition, PNP regulators are protected against reverse polarity faults.

Standard regulators are usually the best for AC-powered applications, where their low cost and high load current make them an ideal choice. In AC-powered applications, the voltage across the regulator is usually at least 3 *V* or more. Therefore, in this kind of application, dropout voltage is not critical.

Curiously, in this type of application (where the voltage drop across the regulator is > 3 *V*) standard regulators are actually more efficient than LDO types (because the standard one has much less internal power dissipation due to ground pin current).

However, a LDO regulator is the most suitable for renewable (such as photovoltaic solar facilities) and battery-powered applications, because the lower dropout voltage translates directly into cost savings by reducing the number of battery cells required to provide a regulated output voltage. If the input-output voltage difference is low (like 1 *V* to 2 *V*), the LDO is more efficient than a standard regulator because of its reduced power dissipation resulting from the load current and the input-output voltage difference [4].

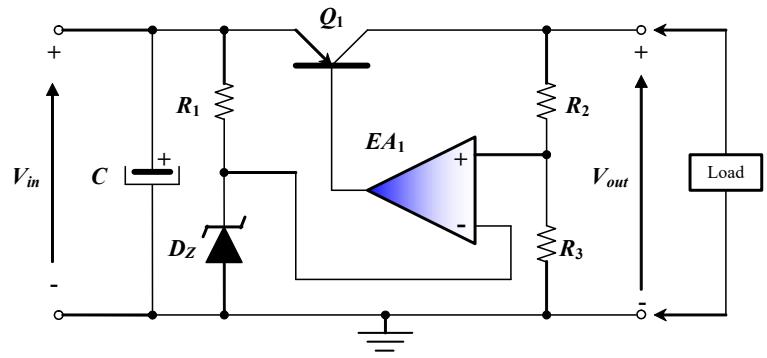

Figure 3. Series pass voltage regulator with feedback and PNP transistor as pass element.

NMOS Linear Regulators

NMOS pass transistors, as a pass element, provide very low drop-out voltage and minimal quiescent current. However, in this case, a charge pump is needed to achieve the low drop-out voltage, because the gate of the NMOS needs to be approximately 2 *V* higher than the voltage at source, to drive the pass element open. Taking into account this point, which is a disadvantage, the charge pump also introduces additional line noise.

PMOS Linear Regulators

Using PMOS linear regulators as the pass element provides a very low drop-out voltage and minimal quiescent current. In this case, an internal charge pump is not necessary for the PMOS pass element. In addition, new control loop concepts in PMOS linear regulators allow a faster regulation loop and better stability, requiring only a single output capacitor (in general, lower than 1 μF) for stable operation.

LDO Voltage Regulators Fundamentals

As discussed above, LDO voltage linear regulators [5]-[6]-[7]-[8] have gained significant importance due to the increased use of battery-powered devices and photovoltaic solar DC-DC voltage regulation. The main function of the LDO regulator is to provide a reliable, stable, and constant voltage. It has come to be considered an important component in the power management of cell phones, laptops, and wireless applications, etc., where dropout voltage is an important issue [9].

Fig. 4 shows the overall topology of the proposed LDO regulator. As can be seen, it consists of three main blocks: an error amplifier, a voltage reference, and a pass transistor with external load capacitance with a small value of internal resistance (ESR) for frequency compensation. The error amplifier of the LDO regulator, in the negative feedback condition, constantly compares the output voltage with the reference voltage and maintains a constant output voltage by varying the gate to source voltage of the pass transistor, according to the error signal. Since the output of the error amplifier is used to drive the gate of the pass transistor, which is naturally a capacitive load, the best option for the error amplifier is an operational transconductance amplifier (OTA) [10]-[11] with high output impedance (Fig. 5). In addition, it is very easy to model an OTA as a single pole system because of its high output impedance, which forms a low frequency pole with small load capacitance. Therefore, OTAs are the best components to drive these capacitive loads because their output signal is current controlled by a differential input signal.

The voltage reference is an important component of voltage regulators, since it decides the nominal output voltage. The main design issue will be its temperature coefficient, which ideally has to be zero, or very near to it. There are many approaches to obtain the reference voltage. However, one method is the use of a band gap voltage reference (BGR) with a very low temperature coefficient [12]. Finally, a PMOS pass transistor, which carries a major part of the current across the whole circuit, drives the load.

Its dimensions are determined such that it is able to withstand the maximum rated current and to achieve the rated low dropout voltage.

The chapter is organized as follows: in the next section, the design of the two-stage cascode OTA using CMOS technology is described. Next, the design of the LDO regulator is discussed, including the design of the error amplifier based on the proposed OTA, and the design of the pass transistor using CMOS technology. Finally, the simulation results obtained for both the proposed OTA and LDO regulator are presented.

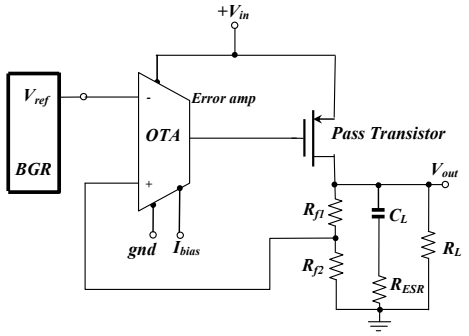

Figure 4. Topology of the proposed LDO linear voltage regulator.

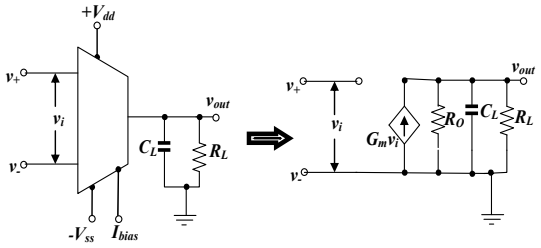

Figure 5. Small signal model of an OTA with C_L and R_L.

Design of the Operational Transconductance Amplifier (OTA)

Fig. 6 shows a classical two-stage OTA using CMOS technology [11], operated using a rail of $+V_{dd}$ and $-V_{ss}$ power supplies and with an external bias current I_{bias} and a single ended output. The first stage is the normal *n*-channel differential input pair (m_1 and m_2) with *p*-channel current mirror

as its active load (m_3 and m_4). The drain currents of m_1 and m_2 are mirrored by m_6 and m_5, respectively, which is the second (gain) stage in the classical current mirroring technique with the current ratio of 1:α. In Fig. 6, we get:

$$I_a = \left(I_{bias}/2\right) - g_{m(2)}\, v_i/2 \text{ , and } I_b = \left(I_{bias}/2\right) + g_{m(1)}\, v_i/2 \tag{3}$$

The single ended output is taken out from point $P1$, through which a current of:

$$I_o = g_{m(1,2)} \cdot \alpha \cdot v_i \tag{4}$$

flows, where $v_i = (v_+) - (v_-)$ is the differential input. Therefore, the voltage controlled current source is obtained and the transconductance of this OTA, G_m, is given by the expression:

$$G_m = \frac{I_O}{V_i} = \alpha \cdot g_{m(1,2)} \tag{5}$$

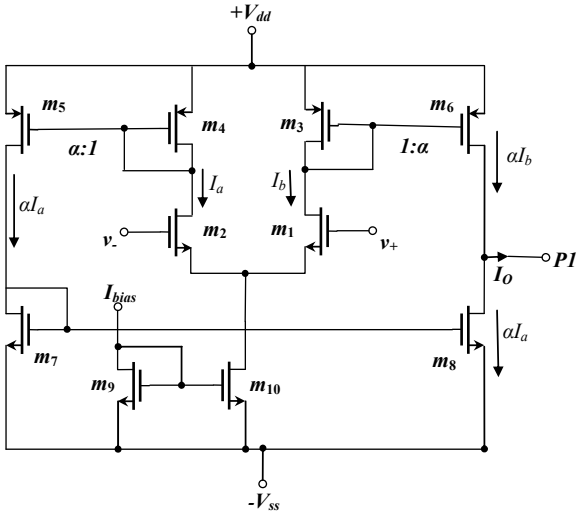

Figure 6. Classical two-stage OTA using CMOS technology.

It should be noted that according to equation (5), the transconductance of the OTA is dependent on the g_m of the MOS transistors of the input

differential pair, which is in-turn dependent on the DC current flowing through it, i.e., $\sqrt{I_{bias}/2}$. As such, it may be said to be a current-controlled gain OTA. The parameter α is called the gain factor and is modified by varying the ratio W/L of the second stage with respect to the input stage ($W/L_{(6,5)}$:$W/L_{(3,4)}$). The equivalent small signal model representation of the OTA is shown in Fig. 5. As seen in this figure, the voltage gain ($A_v(s)$) is given by the expression:

$$\frac{V_{out}(s)}{V_i(s)} = A_v(s) = \frac{A_v}{1+\frac{s}{\omega_o}} = G_m . Z_L(s) \quad , \tag{6}$$

where G_m is the transconductance of the OTA, given by equation (5), while the cut-off frequency ω_o is given by:

$$\omega_o = \frac{1}{(R_o \parallel R_L) C_L} \, , \tag{7}$$

Z_L(s) is the output impedance of the OTA, which is given by:

$$Z_L(s) = \frac{R_o \parallel R_L}{1+(R_o \parallel R_L)(C_L s)} \tag{8}$$

It should be noted that the OTA has a high output impedance thanks to the common source output configuration, which gives the high output impedance $r_o(m_8)\|r_o(m_6)$. The main advantage of the OTA is that, due to its high output impedance, frequency compensation is easier. The load capacitance (C_L) only creates the dominant pole. Hence, the unity gain bandwidth is varied by varying the load capacitance to obtain a suitable phase margin (PM) according to the application and ensuring the stability of the system.

Fig. 7 shows the improved two-stage OTA using CMOS technology, adopting the cascode technique to boost the output impedance and the DC voltage gain (no load) of the classical OTA, optimizing the proposed OTA.

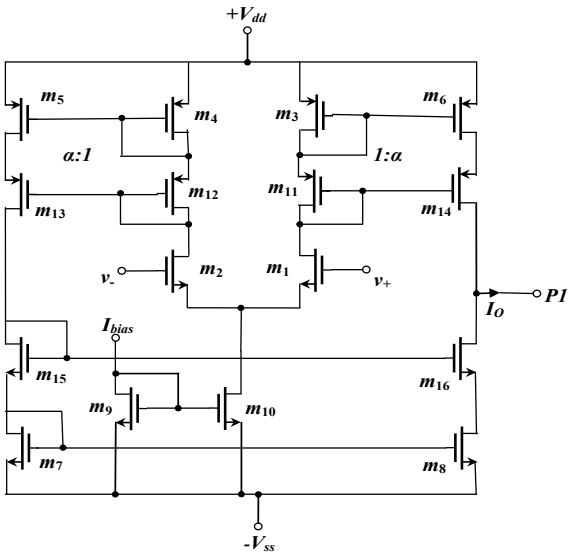

Figure 7. Proposed two-stage cascode OTA using CMOS technology.

In the proposed design ($m_{4,5}$) and ($m_{12,13}$); ($m_{3,6}$) and ($m_{11,14}$); and ($m_{15,16}$) and ($m_{7,8}$) form the cascode pairs with current mirroring. The main design criteria of the proposed OTA are the same as the classical OTA design, which depends on equations (5), (6), and (8). The output resistance is approximately equal to $g_{m(14)}r_o(m_{14})$. The main advantage is the boosting of output impedance by a factor of approximately $r_o(m_6)\|g_{m(16)}r_o(m_{16})r_o(m_8)$, which is quite significant. The output impedance, R_o, is varied by varying the ratios $W/L_{(6,14,16,8)}$ and in-turn varying g_m. Regarding the other important parameters, the input impedance $R_i \approx \infty$ (since the input is at the gate of the MOSFETs), the DC voltage gain of the OTA, from equations (6) and (8), is given by:

$$A_v = G_m \left(R_o \| R_L \right) \tag{9}$$

Equation (9) can be used to find $g_{m(1,2)}$ experimentally by obtaining the AC response of the proposed OTA for $R_L = \infty$, and obtaining its output impedance plot with respect to frequency. Therefore, the equation for DC gain reduces to:

$$A_v \approx G_m R_o \tag{10}$$

Later on, simulation results for a classical OTA are compared to the proposed OTA by considering certain parameters. In addition, different parameters of the proposed OTA, like AC response, DC gain, and output impedance, etc., are also presented.

Design of the Low Drop-out (LDO) Linear Voltage Regulator

Fig. 4 shows the classical topology of the proposed LDO regulator. It consists of three main blocks: the *error amplifier* block; the *voltage reference* block; and the *pass transistor*—it is biased by means of an external current I_{bias}. In standard voltage regulators, the main difference compared to an LDO is found in the pass transistor block. Normally, in a typical voltage regulator, the pass transistor element will be an *n*MOS (or *npn*) transistor in a source follower (or emitter follower) configuration, which has a typical dropout voltage of 2 *V*. However, in a LDO regulator, the pass transistor element is a *p*MOS (or *pnp*) transistor in a common source (or common emitter in bipolar counterpart) configuration, in which its dropout voltage is nothing, but its saturation voltage has a typical value of 0.3 ~ 0.5 *V*.

Since a *p*MOS transistor is used as the pass transistor in common source output configuration (Fig. 4), one of the handicaps in a LDO regulator is that it forms a high output impedance, creating a pole within the unity gain frequency. Because there is already a low frequency pole provided by the error amplifier (OTA), an extra phase is contributed by the pole formed by the high output impedance of the LDO and its overall response in decreasing the phase margin causes a stability issue in the system. Therefore, an output capacitance with a small R_{ESR} is needed to compensate the above-mentioned pole. R_{ESR} together with load capacitance (C_L) form a zero to compensate the effect of the pole created by the high output impedance of the LDO regulator.

The resistors R_{f1} and R_{f2} in Fig. 4 are used to set the output voltage (V_{out}). The error amplifier forms a negative feedback loop, which constantly compares the error signal at the output with the reference voltage to maintain a constant V_{out} by varying the gate voltage of the pass transistor, controlling the current flowing through it. As such, the output voltage is given by:

$$V_{out} = \left(1 + \frac{R_{f1}}{R_{f2}}\right) V_{ref} \tag{11}$$

By choosing the appropriate values for the resistors and reference voltage, the output voltage V_{out} is set.

The initial design specifications given for the proposed LDO regulator are shown in Table I. Fig. 8 gives the complete schematic of the CMOS LDO linear voltage regulator in order to perform in line with these design specifications. The dimensions of the circuit transistors in the proposed LDO linear voltage regulator in Fig. 8 are depicted in Table II.

As can be seen in Fig. 8, the proposed design has three main parts: (1) the error amplifier; (2) the voltage reference circuit; and (3) the pass transistor, as well as a suitable load capacitance C_L.

Design of the Error Amplifier in the Proposed LDO Regulator

The error amplifier in the proposed LDO regulator basically consists of the OTA previously discussed. It can be seen in Fig. 5 and its design criteria has already been discussed. The only difference is that here, it operates only at a positive voltage, i.e., without a negative voltage $-V_{ss}$, and instead that point is connected to ground. According to this design, the simulation for an open loop AC response is conducted several times with the OTA operating at $+V_{dd}$ and *GND* (Fig. 9). Since the OTA is operating at these two potentials, the input terminals must be provided with proper DC bias in order to get a good open loop AC response with high DC gain. As such, the proposed OTA is simulated with different values of offset voltage (V_{offset}) at the input points, while obtaining its open loop AC response.

For this particular design, after different simulations, it can be seen that to get a better response, $V_{offset} > 0.6$ *V*. When this OTA is working as an error amplifier in the proposed LDO, V_{offset} is set by the reference voltage (V_{ref}). Thus, the reference voltage has to be greater than 0.6 *V*. As a consequence, in the design specifications of the LDO regulator, $V_{ref} = 0.65$ *V*. The capacitor C_1 (Miller capacitor) is connected to two high impedance points in the circuit, which ensures a good phase margin in the proposed design; C_1 is set to 40 *pF*.

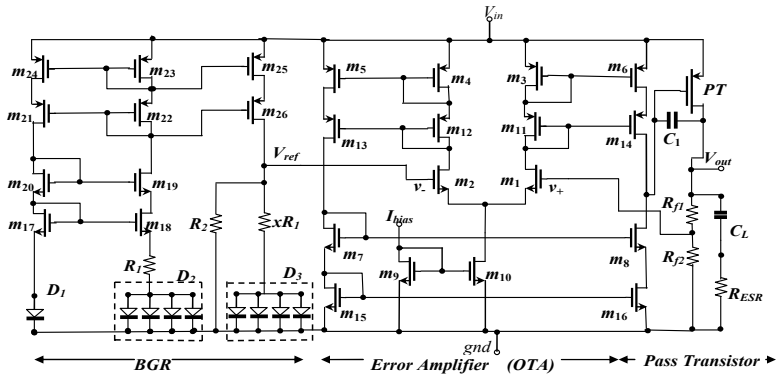

Figure 8. Proposed design of LDO linear voltage regulator.

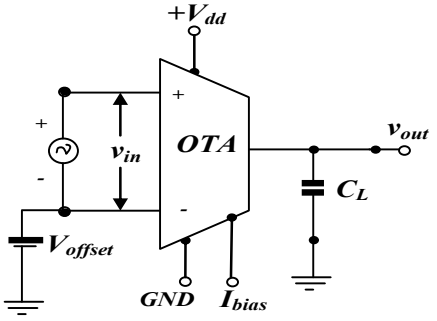

Figure 9. Proposed OTA operating in $+V_{dd}$ and GND with input offset.

Table I: Design specifications of the proposed LDO regulator

Design Specification	*Value*
Output voltage (V_{out})	4.5 *V* (1% allowance)
Max. output current ($I_{out,max}$)	450 *mA*
Reference voltage (V_{ref})	650 *mV*
Maximum drop-out voltage (V_{drop}) at I_{out} = 450 *mA*	500 *mV*

Table II: Dimensions of the transistors in the proposed LDO linear voltage regulator in Fig. 8

Transistor	*Width* (*W*) *in* μm	*Length* (*L*) *in* μm
m_1 , m_2	500	1
m_3 , m_4 , m_{11} , m_{12}	40	1
m_5 , m_6 , m_{14} , m_{13}	800	1
m_7 , m_8 , m_{15} , m_{16}	800	1
m_9 , m_{10}	100	1
m_{17} , m_{18} , m_{19} , m_{20}	100	1
m_{21} , m_{22} , m_{23} , m_{24}	100	1
m_{25} , m_{26}	100	1
PT (pass transistor)	8000	1

The error amplifier in the negative feedback condition decides the output voltage (V_{out}) by constantly comparing the error signal with V_{ref}, which is 0.65 *V*. According to equation (11), to get the desired value of $V_{out} = 4.5V$, $R_{f1} = 14.8\ k\Omega$ and $R_{f2} = 2.5\ k\Omega$ are chosen.

Simulation Results and Observations

The proposed circuit blocks were built in Cadence Hit-Kit V3.70, using CMOS technology. Simulation was done using the Spectre software package, with the BSIM-3.3 as the MOSFET model.

Operational Transconductance Amplifier

The proposed OTA, as shown in Fig. 7, was built and simulated with $+V_{dd} = 5\ V$, $-V_{ss} = 0\ V$, and with the bias current $I_{bias} = 50\ \mu A$. The circuit was simulated in order to obtain some parameters and then compared with the results from the classical OTA shown in Fig. 6. The open loop AC Response of the proposed OTA is plotted and shown in Fig. 10 for the load capacitance $C_L = 0.4\ nF$ under no-load conditions. The results showed DC gain of $A_V = 101.13\ dB$ and unity gain bandwidth of $UGB = 4.5\ MHz$ with a phase margin of $PM = 59.17^o$.

In addition, the proposed OTA circuit was simulated with $C_L = 1\ nF$. The DC gain was the same, but $UGB = 1.98\ MHz$ with $PM = 75.3^o$, whereas in the classical OTA, $UGB = 2.316\ MHz$ with $PM = 81.07^o$. This boosting of the DC gain in the proposed OTA when compared to the

classical OTA configuration under no load conditions is due to the increase in the output impedance thanks to the cascode current mirrors in the first configuration. The DC gain under no load condition matches equation (10).

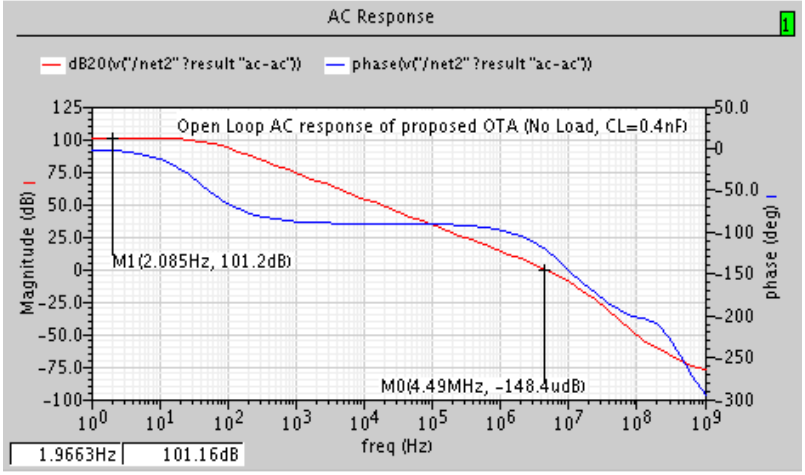

Figure 10. AC Response of the proposed OTA, with $C_L = 0.4\ nF$, $R_L = \infty$.

Another important parameter, the output impedance, was evaluated by simulating the circuit with differential inputs grounded and applying an AC voltage source at the output node, with $C_L = 1\ nF$, finding the current through that voltage source. Fig. 11 shows the output impedance $Z_L(s)$ with $R_L = \infty$, with respect to frequency change in the proposed OTA. It can be seen in this figure that the large signal output impedance (R_O) in the proposed OTA is 1.35 $M\Omega$, which is a high output impedance, thanks to the cascode current mirroring technique in the proposed OTA.

Another parameter that determines the gain is $g_{m(1,2)}$ of the input differential pair MOSFETs. This was found out experimentally, in Figs. 10 and 11, and using equations (5) and (10) under no load conditions. From these figures, the values of R_O and DC gain A_v can be obtained, with a gain factor α set to 20. Substituting appropriate values, it was found that $g_{m(1,2)} = 2.12\ mS$. This value fits well with the theoretical value found using the model file parameters (k_n, V_{tn}) and DC current $I_{bias}/2$, i.e., 2.204 mS.

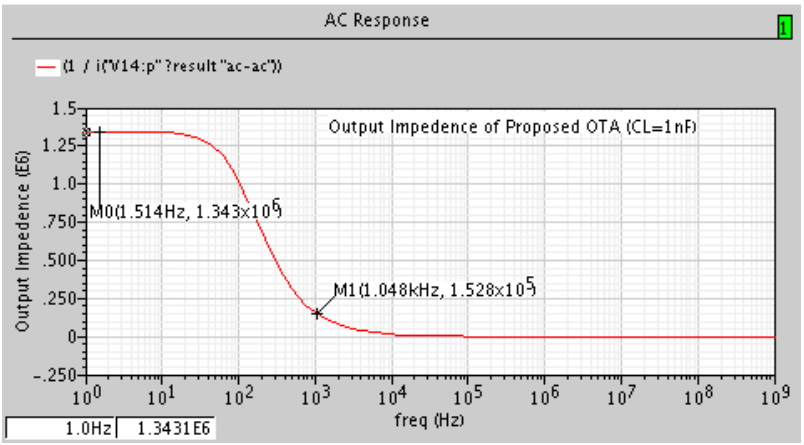

Figure 11. Output impedance vs. frequency of the proposed OTA.

LDO Voltage Regulator

Fig. 8 shows the proposed LDO regulator circuit with its three parts: the error amplifier (based on the previously proposed OTA); the band-gap reference circuit; and the pass transistor. This circuit was built and simulated with V_{in} ranging from 5 V to 20 V, $I_{bias} = 50\ \mu A$, and it was found that the designed circuit fits the specifications in Table I. Tables III and IV give a summary of the simulation results obtained for the band-gap reference voltage and LDO regulator circuits, respectively.

Table III: Simulation results of band-gap reference voltage circuit

Parameters	***Values***
V_{ref} at $T = 25\ ^oC$	653 mV
T_γ	0.025 $mV/^oC$
Line Regulation	0.44 mV/V
Power drawn, $V_{in} = 5\ V$	0.54 mW

Table IV: Simulation results obtained for the proposed LDO regulator

Parameter	***Value***		
	For R_L = ∞	***For R_L = 10 Ω***	***For R_L = 45 Ω***
V_{out} for V_{in} = 5 *V*	4.509 *V*	4.504 *V*	4.507 *V*
I_L for V_{in} = 5 *V*	0 *A*	450.4 *mA*	100.1 *mA*
V_{drop}	0.06 *V*	0.5 *V*	0.15 *V*
Line regulation	3.2 *mV/V*	3.4 m*V/V*	3.2 *mV/V*
Load regulation	0.012 *V/A*		
V_{out} settling time I_L = 0 – 450 *mA* in 1 μs	4.2 μ*s*		
V_{out} settling time I_L = 450 *mA* – 0 in 1 μs	40 μ*s*		
PSRR (full load)	@ 100 *Hz*	54.45 *dB*	
	@10 *kHz*	34.31 *dB*	
V_{out} settling time V_{in}=5 *V* – 20 *V* in 1 μ*s*	6 μ*s*		
V_{out} settling time V_{in}=20 *V* – 5 *V* in 1 μ*s*	4 μ*s*		

The proposed LDO regulator circuit (Fig. 8) was simulated to obtain its most important characteristics and parameters [13], like DC response, line regulation, load regulation, PSRR, open loop AC Response, response for load variations, settling time for load variations, and transient responses for input variations.

The DC response of the LDO circuit was obtained under different load conditions—R_L = 10 Ω, 45 Ω, and ∞. The typical response for R_L = 10 Ω and ∞ are shown in Fig. 12. This DC response was used to divine the drop-out voltage (V_{drop}) of the proposed LDO regulator by spotting the point at which the V_{out} reached a constant value. Thus, by knowing the corresponding value for V_{in}, the dropout voltage can be found. It can be seen in the figures that for R_L = ∞, V_{drop} = 0.06 *V*, and for full load conditions (R_L = 10 Ω), the dropout voltage was V_{drop} = 0.5 *V*. This shows that there is a trade-off between the maximum load and the drop-out voltage, hence the user has to use this proposed LDO regulator according to the application requirements. From the plots of the DC response (Fig.

12), the line regulation for the corresponding R_L can be discovered by considering V_{out} for $V_{in} = 5\ V \sim 20\ V$. Using equation (12):

$$LR = \frac{\frac{\Delta V_{out}}{V_{out}}}{\frac{\Delta V_{in}}{V_{in}}} \tag{12}$$

we can find that the line regulation (LR) for $R_L = \infty$ is 3.2 mV/V; for $R_L =$ 10 Ω it is 3.4 mV/V; and for $R_L = 45$ Ω it is 3.2 mV/V. Load regulation was obtained by sweeping I_L from 0 A to 450 mA with $V_{in} = 5\ V$. In Fig. 13, the load regulation is 0.012 V/A.

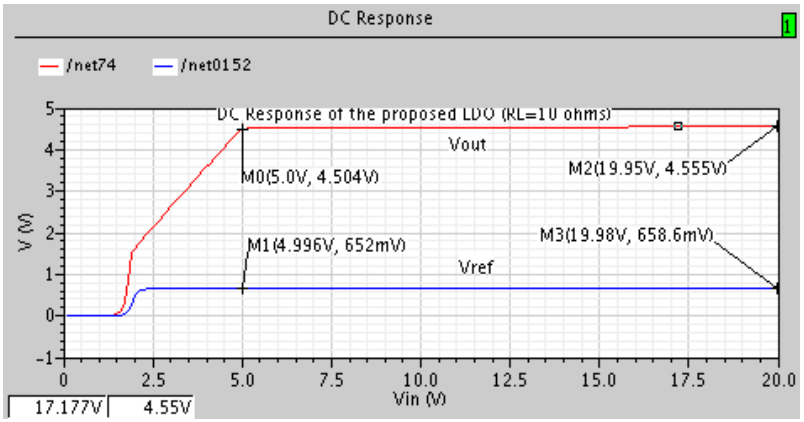

Figure 12. DC response of the proposed LDO and band-gap reference for full load condition.

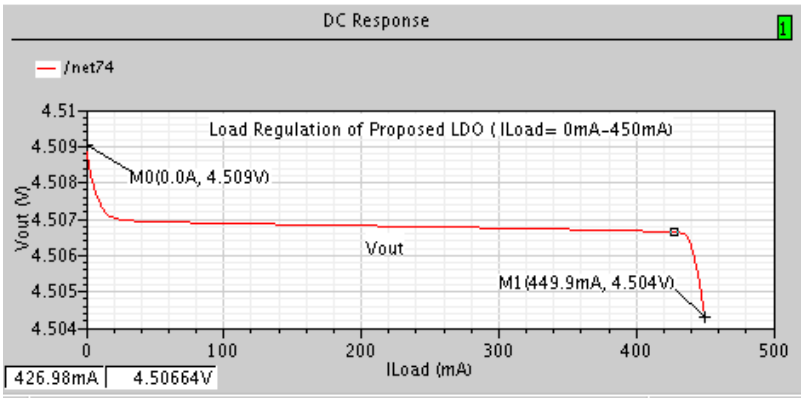

Figure 13. Load regulation of the LDO regulator, $I_L = 0\ A - 450\ mA$.

With $V_{in} = 5\ V$ and $R_L = \infty$, the current flowing through the supply had a value of 1.29 *mA*, which is usually referred to as the sum of the current needed to bias the whole circuit, with the leakage current through the feedback circuit in the error amplifier (quiescent current). This current is small compared to the maximum output rated current $I_{L(max)} = 450\ mA$, giving a power efficiency at a full load condition of 89.74%. On the other hand, $V_{out} = 4.509\ V$ for $R_L = \infty$ and $V_{out} = 4.504\ V$ for $R_L = 10\ \Omega$, while satisfying the initial design specifications in Table I.

Another important parameter to consider is the power supply rejection ratio (PSRR), which decides the ripple rejection capability of the circuit. The PSRR was found for two load conditions: no load and full load. It was found that under the no load condition at 100 *Hz*, PSRR = 56.26 *dB*; at 10 *kHz*, PSRR = 46.53 *dB*. For the full load condition at 100 *Hz*, PSRR = 54.45 *dB*; and at 10 *kHz*, PSRR = 34.31 *dB* (Fig. 14). The open loop AC Response of the LDO regulator is shown in Fig. 15. DC gain was found to be 32.56 *dB*, *UGB* = 18.68 *kHz* with a *PM* of 91.35º, ensuring the stability of the circuit.

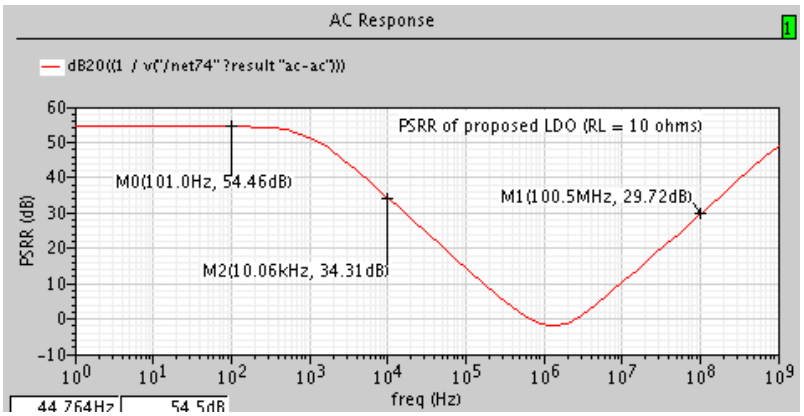

Figure 14. PSRR of the LDO regulator, $R_L = 10\ \Omega$.

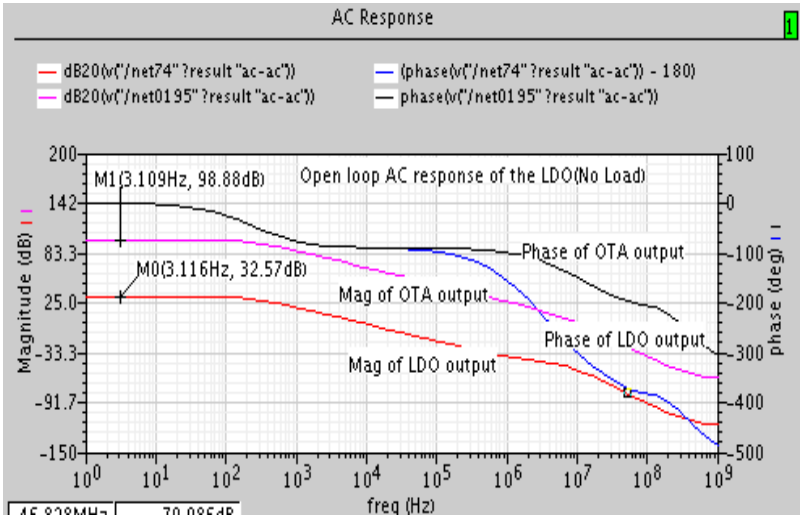

Figure 15. Open loop AC response at the LDO and error amplifier outputs.

Finally, the response for the load variations of the proposed LDO and the settling times for full load variations are depicted in Fig. 16; transient responses for input variations are given in Fig. 17.

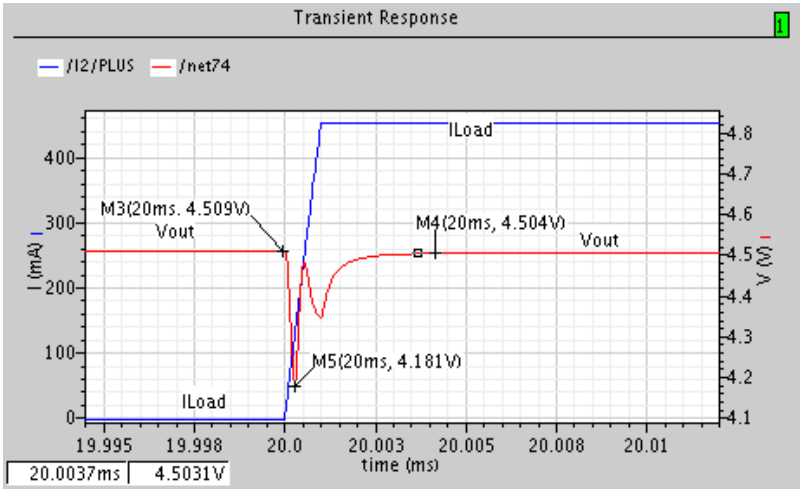

Figure 16. Settling time of V_{out} for a step $I_L = 0\ A - 450\ mA$ in 1 μs.

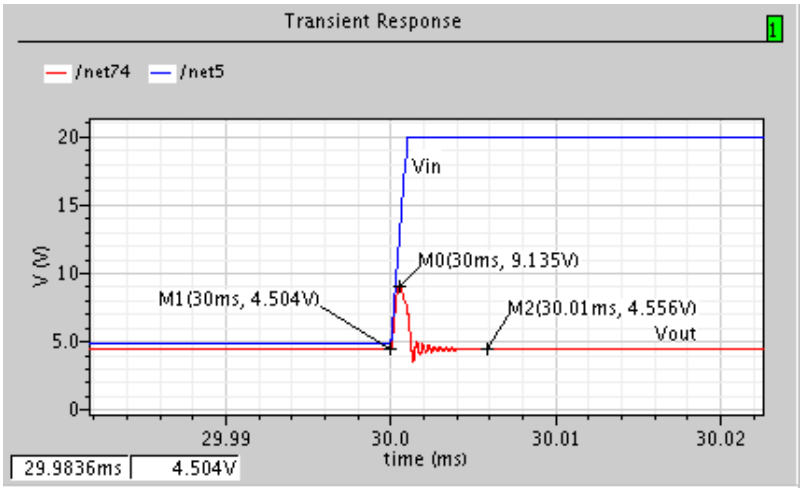

Figure 17. Response of V_{out} for $V_{in} = 5\ V - 20\ V$ in 1 μs for full load.

Conclusions and Further Research

This chapter has offered a proposal for a low drop-out voltage regulator based on a two-stage cascode operational transconductance

amplifier (OTA) as an error amplifier. It was designed in 0.35 μ*m* CMOS technology and simulated in Cadence Spectre software with the MOSFET model BSIM-3.3.

The current measured regulated output voltage was 4.5 *V* with a maximum current of 450 *mA*. The LDO regulator design has a dropout voltage of 0.5 *V* under full load conditions, with good line and load regulation of 3.2 *mV/V* and 0.012 *V/A*, respectively. The PSRR of the design was found to be 54.45 *dB* at 100 *Hz* and 34.31 *dB* at 10 *kHz* under full load conditions. The LDO linear voltage regulator includes a band gap reference circuit that provides a constant reference voltage of 0.653 *V* with a temperature co-efficient (T_γ) of 0.025 *mV/*ºC.

A majority of LDO voltage regulators operate with very large pass transistor as the power stage, to handle heavy-load currents, resulting in a large equivalent capacitance at the gate of the pass device, which, in turn, restricts the slew-rate at this node and thereby degrades the dynamic performance. Moreover, the stability of the LDO will degrade at no-load and light-load conditions, as the poles at the gate of the pass device and at the output node are very close together. Compelling evidence continues to show that operation in standby mode is expected for most of the time, suggesting that the large pass transistor should be eliminated for no-load conditions and its utilization for maximum load currents. When the power transistor is applied at its maximum, the greatest output voltage variations are due to the load transients that occur under no-load and light-load changes (usually less than 1 *mA*) [14]. Pass transistor segmentation into smaller sizes and adaptively controlling their action according to the load demands could be an alternative solution for increasing the slew-rate at the gate of the pass device and provide a wider closed-loop bandwidth. As a result, significant advancements in the stability and dynamic performance of the LDO voltage regulator will be made. This can be successfully accomplished by employing two pass transistors, the smaller one for no-load to light-load conditions, and the larger one for light-load to full-load conditions. This would offer a proper tradeoff between circuit complexity, power dissipation of the control circuitry, and overall dynamic performance.

In previous work [15], the authors carried out a stability and transient analysis on a LDO voltage regulator with two different size-segmented pass transistors in comparison to the conventional one, which has a single large size pass device and assuming the pass transistors are in the saturation region all the time for simplicity's sake. However, this is an approximation that may not be valid for all load conditions, especially for light and heavy loads. As such, there is a significant difference between

the theory and simulation results under certain load conditions. This issue needs to be reconsidered and reformulated to resolve these differences. Pass transistor operation in different regions depending on the load current, in the subthreshold region under no-load condition and the triode one by increasing the load current, is applied to derive the pole-zero equations.

Consequently, better relations for ensuring the stability and a wider bandwidth are achieved. In addition, a reliable and closed form output pole was calculated considering the feedback loop from the output of the LDO voltage regulator. These findings will inform the fabrication of the next generation of LDO voltage regulators meeting the characteristics of higher stability, lower power consumption, and improved dynamic performance at the expense of adding control circuitry.

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