A Closed-loop Capacitance-to-Frequency Converter for Single-Element and Differential Capacitive Sensors

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***Abstract*—A novel closed-loop switched-capacitor (SC) capacitance-to-frequency converter (CFC) is presented in this paper. The proposed CFC is capable of measuring from either a single-element or a differential capacitive sensor, providing ratio and ratio-metric outputs, respectively. Most of the existing auto-balancing schemes for capacitive sensors use the closed-loop approach but require precise sinusoidal AC excitation and provide an analog output that is sensitive to parasitic capacitances. Also, the use of voltage-controlled resistors (VCR) in many of these schemes limits the linearity and accuracy of their output. The SC-CFC presented in this paper, employs a simple DC reference for excitation, and gives a digital output that is insensitive to parasitic capacitances, by virtue of design. Additionally, the output is linear, irrespective of the sensor characteristic, and independent of the nominal value of the sensor. This feature, along with its compatibility with single-element and differential capacitive sensors, facilitates its ease of integration with a wide range of capacitive sensors. The CFC has a one-time correction mechanism that significantly reduces the impact of component mismatch. The prototype of the proposed scheme exhibits a maximum non-linearity error (NLE) of 0.24%, a resolution of 12.59 effective number of bits (ENOB), and a rise time of 6 ms. In addition, the proffered design is fit for integrated circuit (IC) fabrication as it employs a switched-capacitor approach.**

***Index Terms* — Capacitance-to-digital converter; Capacitance-to-frequency converter; Capacitive sensor; Closed-loop; Differential capacitive sensors; Single-element capacitive sensor; Interface circuit; Switched-capacitor.**

I. Introduction

CAPACITIVE sensors play a key role in myriad fields such as consumer electronics, automotive sensors, and industrial applications [1]. These sensors have an established record of providing sensor designers with an attractive option to realize non-contact measurement of various physical parameters. They exhibit high sensitivity, high resolution, broad bandwidth, low power dissipation, robustness, and are inexpensive [2].

Capacitive sensors with two electrodes as well as multiple electrodes have been reported, and are in use, for various applications. Two electrodes separated by a dielectric, or one electrode with the other being ground plane, are examples of single-element capacitive sensors. Single-element capacitive sensors with various electrode structures are used to sense touch [3], proximity [4], position [5], pressure [6], humidity [7], flow [8], and level [9]. Differential capacitive sensors (DCS) constitute another important category of capacitive sensors. They are used in a range of applications such as improved touch sensing [10], and determining position [11], displacement [12], acceleration [13], differential pressure [14], and permittivity distribution in the area of interest [15]. These sensors consist of two sensing capacitances, say, C_1 and C_2, with a common electrode. C_1 and C_2 vary with the parameter being sensed. $C_1 = C_2 = C_0$ when the measurand is zero. The change in C_1 due to the measurand is opposite to that in C_2, causing these sensors to be popularly known as push-pull type capacitive sensors. The change in capacitance with respect to the measurand, *x*, can be linear or non-linear (inverse) as given in (1) and (2), respectively, where k is the sensor constant, and C_0 is the nominal capacitance of the sensor [16]. The characteristic is linear, as in (1), in the case of the widely used parallel-plate arrangement of the electrodes which utilize the change in the area of overlap between the plates, or change in the dielectric constant, with respect to the measurand. It is an inverse characteristic, as in (2), if the change in capacitance is caused by the change in the distance between the plates. Similarly, the linear single-element sensors can be represented as C_1 in (1), while the inverse ones can be represented using C_2 given in (2).

$$C_1 = C_0(1 \pm kx) \text{ and } C_2 = C_0(1 \mp kx) \tag{1}$$

$$C_1 = \frac{C_0}{(1 \mp kx)} \text{ and } C_2 = \frac{C_0}{(1 \pm kx)} \tag{2}$$

The general approaches for output digitization in single-element capacitive sensors begin with the conversion of capacitance to an equivalent voltage signal [17], [18]. This signal is then given to an analog-to-digital converter. Other approaches include obtaining number of transitions [19], frequency [20] - [22] or time period [23] as a function of the capacitance, following which a corresponding digital value is derived. Similar approaches are employed to get a digital output from differential capacitive sensors. For instance, [24] is a commercially available Σ-Δ based converter for capacitive sensors. This does not provide ratio-metric output directly. Also, it has limited ranges for the sensor and acceptable

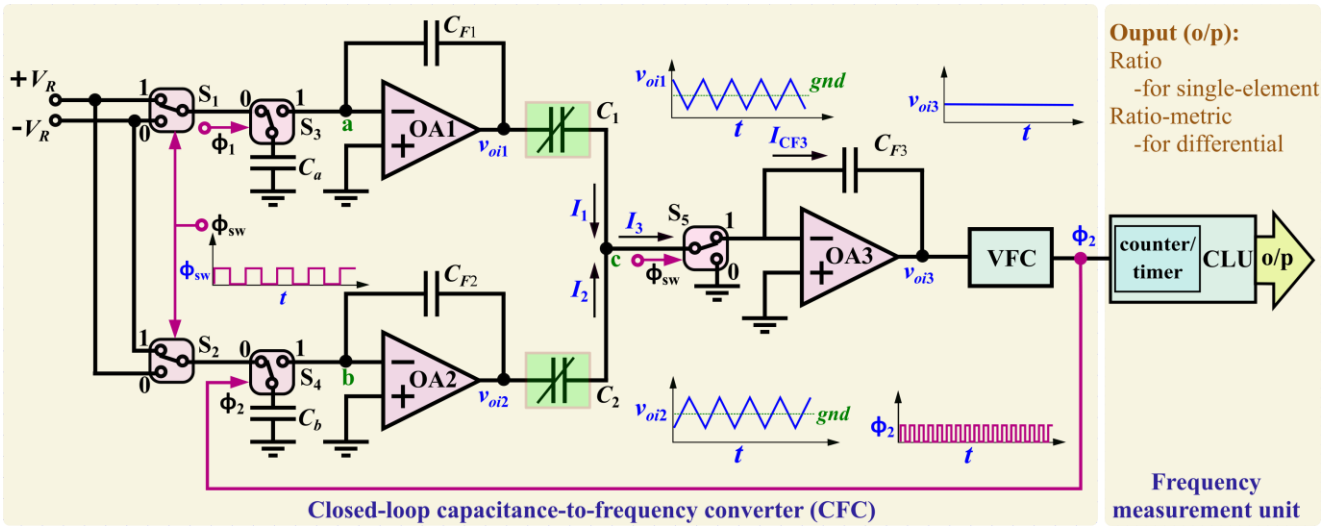

Fig. 1. Functional block diagram of the proposed SC-CFC. In the circuit, $C_{F1} = C_{F2} = C_F$ and $C_a = C_b = C$. VFC represents a voltage-to-frequency converter, and CLU is a control and logic unit.

magnitude of parasitic capacitance. The circuit in [25] uses capacitance-to-pulse-width conversion. Its output is parasitic-insensitive but requires two capacitance-to-voltage converters, followed by a voltage-to-pulse-width converter, and operates in an open-loop configuration. In [26], a switched-capacitor-based dual-slope capacitance-to-digital converter (CDC) is presented, but the update rate is relatively low. A low power CDC using successive approximation register (SAR)-based conversion is reported in [27]. A ratio-metric output [26] is preferred for DCS instead of a difference output [27]. A synchronous demodulator-based scheme is presented in [28]. It needs AC excitation, and provides an analog output. In [29] a switch-bridge-based circuit is presented for the DCS. This design avoids the limitations of its diode counterpart, but requires an AC source and the output voltage is not ratio-metric.

The measurement circuits given in [20], [30] and [31] adopt a closed-loop approach. The circuit in [20] is a closed-loop SC-CFC for a single-element capacitive sensor. Though it exhibits a high update rate, it is not suitable for interfacing differential capacitive sensors. The scheme proposed in [30] and [31] deals with differential capacitive sensors. It is an auto-balanced bridge circuit which requires a precise sinusoidal AC excitation and has a complex design involving a synchronous demodulator. It uses two multipliers in its feedback path, one of which is used to realize a voltage-controlled resistor (VCR). The worst-case error of the analog multiplier employed is typically high, e. g. 2% in the case of AD633, used in [30], [31]. The use of such components in the design limits its linearity and accuracy. In addition, this circuit provides an analog output (while digital is preferred) which is sensitive to parasitic capacitances.

The proffered measurement scheme, for single-element and differential capacitive sensors, is a closed-loop switched-capacitor capacitance-to-frequency converter (SC-CFC) circuit. It uses DC excitation, and achieves high accuracy and a relatively high update rate. In the case of differential capacitive sensors, the ratio-metric output from the scheme ensures a linear characteristic irrespective of the sensor characteristic being linear or inverse. Moreover, the final output does not depend on the nominal capacitance value of the sensor, enabling easy interfacing of the sensor to the measurement circuit. The same SC-CFC is suitable for single-element capacitive sensors, possessing either linear or inverse characteristic, and gives a linear ratio output directly, independent of the nominal capacitance. The proposed CFC is simple and relatively inexpensive to realize. Since a switched-capacitor approach has been employed in its implementation, this circuit is suitable for IC fabrication. The design and operation of this new closed-loop SC-CFC and its evaluation based on a hardware prototype are presented in the subsequent sections.

II. Capacitance-to-Frequency Converter

The circuit diagram of the proposed SC-CFC is shown in Fig. 1. The scheme is presented first for differential capacitive sensor, followed by single-element capacitive sensor.

A. Differential Capacitive Sensor

The variable capacitors C_1 and C_2 represent the differential capacitive sensor. V_R is a DC reference voltage, and it is connected to the single pole double throw (SPDT) switches S_1 and S_2. When clock ϕ_{sw} is high, the output of S_1 is at $+V_R$ and that of S_2 is at $-V_R$. The outputs of these SPDT switches will be flipped when ϕ_{sw} is low. The switch S_3 controlled by the clock signal ϕ_1, the operational amplifier OA1, and capacitors C_a, C_{F1} constitute an SC integrator. ϕ_1 is a fixed clock whose frequency f_1 is much higher than the frequency f_{sw} of ϕ_{sw}. When ϕ_{sw} is high, for every clock cycle of ϕ_1 the voltage v_{oi1} decreases by $V_R C_a / C_{F1}$. On the other hand, when ϕ_{sw} is low, v_{oi1} increases by the same amount for each clock cycle of ϕ_1. This process synthesizes a triangular voltage v_{oi1} as input to the capacitor C_1. This is illustrated in Fig. 2. Similarly, switch

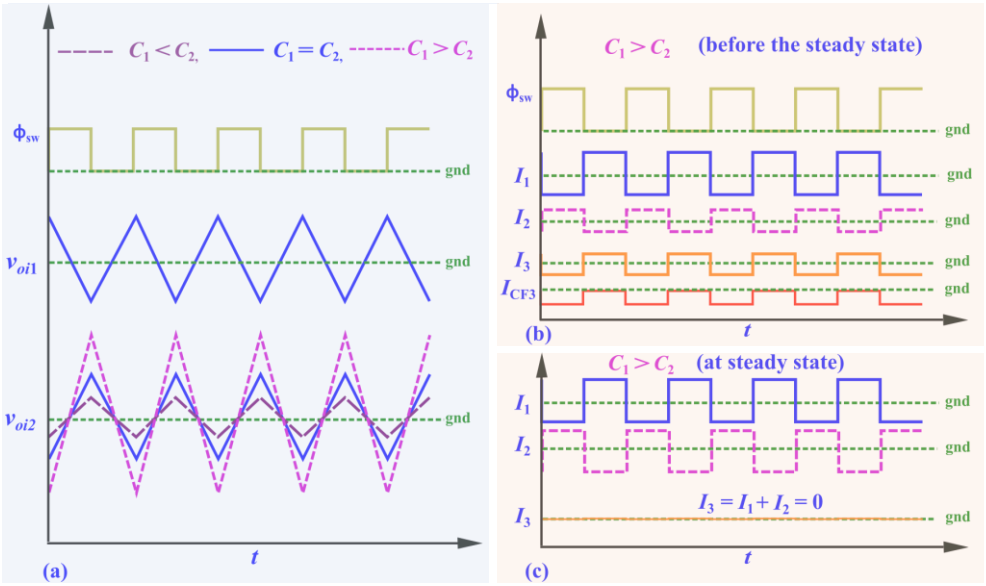

Fig. 2. (a) Important waveforms of the proposed CFC for different conditions of C_1 and C_2. ϕ_1 and ϕ_2 are at a much higher frequency compared to ϕ_{sw}. v_{oi1} and v_{oi2} increment and decrement, in steps, as they are outputs of SC integrators. The individual steps become less visible as they get smaller. (b) Pictorial representation of the waveforms of the currents for $C_1 > C_2$, before reaching the steady state of the circuit. The currents, once the circuit is in steady state, are given in (c). I_{CF3} is not shown in (c) as it is zero.

S_4, capacitors C_b, C_{F2}, and opamp OA2 forms another SC integrator with output v_{oi2}. The polarity of the slope of the triangular wave v_{oi2} will be opposite to that of v_{oi1} as, at any instant of time, the outputs of S_1 and S_2 have opposing signs. S_4 is operated using ϕ_2, which is the output of the voltage to frequency converter (VFC). ϕ_2, with a frequency f_2 corresponding to the voltage fed into the VFC, is used together with switched-capacitor integrator to realize the auto-balancing mechanism which forms the core of the proposed closed-loop circuit.

The currents I_1 and I_2, indicated in Fig. 1, combine at node c, and the resultant current I_3 flows into the SPDT switch S_5. S_5 is controlled by ϕ_{sw}, which is the same signal that controls S_1 and S_2. In the absence of S_5, the output v_{oi3} of the integrator, consisting of feedback capacitor C_{F3}, and opamp OA3, would always tend to zero since I_3 is a bipolar signal when $C_1 \neq C_2$, before the circuit reaches steady state, as shown in Fig. 2b. The presence of S_5 ensures that the current I_{CF3} through C_{F3} is unidirectional (refer Fig. 2b), and hence v_{oi3} monotonously accumulates, and achieves auto-balancing at a different voltage for each set of values of C_1 and C_2.

Let $C_{F1} = C_{F2} = C_F$, and $C_a = C_b = C$. In this case, the slopes of v_{oi1} and v_{oi2}, namely $\frac{\partial v_{oi1}}{\partial t}$ and $\frac{\partial v_{oi2}}{\partial t}$, have the same magnitude but opposite polarity, as shown in Fig. 2. When ϕ_{sw} is high the slope of v_{oi1} is negative, whereas that of v_{oi2} is positive. Thus, I_1, I_2 and I_3 can be expressed by (3), (4) and (5) respectively. If $C_1 = C_2$, I_1 and I_2 will be of equal magnitude and opposite polarity. Thus, I_3 and I_{CF3} (= $I_3/2$) are zero, producing an output $v_{oi3} = 0$. The expression for v_{oi3} is given in (6). The VFC is configured such that when v_{oi3} is zero, the frequency output, f_2 will be the same as the fixed frequency f_1.

$$I_1 = -C_1 \frac{\partial v_{oi1}}{\partial t} = -C_1 \frac{V_R C}{C_F} f_1 \quad (3)$$

$$I_2 = C_2 \frac{\partial v_{oi2}}{\partial t} = C_2 \frac{V_R C}{C_F} f_2 \quad (4)$$

$$I_3 = I_1 + I_2 = [\, C_2 f_2 - C_1 f_1] \frac{V_R C}{C_F} \quad (5)$$

$$v_{oi3} = -\frac{1}{C_{F3}} \int I_{CF3}\, dt = [C_1 f_1 - C_2 f_2] \frac{V_R C}{2 C_F C_{F3}} t \quad (6)$$

Now, when $f_1 = f_2$, let C_1 and C_2 be changed such that $C_1 > C_2$. Then, $C_1 f_1 > C_2 f_2$. This causes a non-zero I_3 (actually, $I_3 < 0$ since I_1 is a negative quantity) to flow through C_{F3} increasing v_{oi3} as per (6). Thus, the VFC delivers an increased output frequency f_2, leading to an increase in $\frac{\partial v_{oi2}}{\partial t}$, as shown in Fig. 2. As f_1, and hence $\frac{\partial v_{oi1}}{\partial t}$, remain constant, the increase in $\frac{\partial v_{oi2}}{\partial t}$ reduces $|I_3|$. This goes on until $|I_1| = |I_2|$ following which v_{oi3} ceases to vary. In this condition, (7) can be obtained from (6).

$$C_1 f_1 = C_2 f_2 \quad (7)$$

$$\text{or} \quad C_1 / C_2 = f_2 / f_1 \quad (8)$$

If instead $C_1 < C_2$, when $f_1 = f_2$, then $|I_1| < |I_2|$, and v_{oi3} decreases until f_2 is sufficiently decreased such that $|I_1| = |I_2|$. The decrease in $\frac{\partial v_{oi2}}{\partial t}$ due to the decreased f_2 is also shown in Fig. 2.

The ratio of the capacitances C_1 and C_2 can be estimated using (8). However, if a ratio-metric computation of f_1 and f_2,

as in (9), is performed, the ratio-metric output due to C_1 and C_2 is obtained. In (9), the output follows a linear relation with the measurand x, where k is the sensor constant. Thus, the measurand can be linearly estimated for sensors possessing either linear or inverse characteristic. Polarity of x is taken as positive if $f_1 < f_2$, and negative for $f_1 > f_2$.

$$\frac{(f_2 - f_1)}{(f_2 + f_1)} = \frac{(C_1 - C_2)}{(C_1 + C_2)} = \pm kx \tag{9}$$

B. Single-Element Capacitive Sensor

To interface a single-element capacitive sensor, either C_1 or C_2 (refer to Fig. 1) is set as the sensor capacitance, keeping the other as the reference capacitor. If the sensor C_x possesses a linear characteristic as $C_x = C_0(1 \pm kx)$, it is connected in place of C_1. Then, C_2 is set as C_0. In this case, from (8), (10) is obtained.

$$\frac{(f_2 - f_1)}{f_1} = \frac{C_0(1 \pm kx)}{C_0} - 1 = \pm kx \tag{10}$$

To interface single-element sensor C_x that follows inverse characteristic, i.e., $C_x = C_0/(1 \pm kx)$, it should be connected in place of C_2 and C_1 set as C_0 in Fig. 1. In such case, a linear final output is obtained, i.e., (10) holds true for both types of single-element sensors.

C. Measurement of f_2

Since f_1 is known and f_2 can be measured using a frequency counter, the output estimated using (9) or (10) is available in digital domain. The frequency counter is part of the Control and Logic Unit (CLU) in Fig. 1. To measure f_2, it counts the number pulses n_t of ϕ_2 within a gate time T_G. The counter is set such that its output increments by one for every cycle of ϕ_2. Then, f_2 is computed as $f_2 = (n_t/T_G)$. For an update rate higher than the one achieved using the frequency counter, the measurement unit could be modified to measure the time period T_2 of ϕ_2. Then f_1 can be replaced by $1/T_1$, where T_1 is the time period of ϕ_1, and f_2 by $1/T_2$ in (9) or (10), to obtain the ratio-metric or ratio outputs in terms of the respective time periods. However, due to limitations in the highest achievable frequency of the reference clock signal of the CLU, this approach has lower resolution and SNR than the frequency counter method. To improve these parameters the time-domain values can be averaged, for a given window size. Thus, the choice of output in the time-domain or frequency counter methods is essentially based on a tradeoff between update rate and resolution. In the prototype developed, the frequency counter has been used to perform the measurement.

D. Effect of Mismatch and a Correction Method

In the derivation of (8), it is assumed that $C_{F1} = C_{F2} = C_F$ and $C_a = C_b = C$. However, in practice there can be mismatch in the values of these components, which can impact the final output as explained below. Let,

$$C_{F1} = C_{F2}(1 + \epsilon_1) \text{ and } C_a = C_b(1 + \epsilon_2), \tag{11}$$

where $\epsilon_1 = \Delta C_{F2}/C_{F2}$ and $\epsilon_2 = \Delta C_b/C_b$. Substituting (11) in (3) gives (12), while $I_2 = C_2 \frac{V_R C_b}{C_{F2}} f_2$. Under this condition, (8) will get modified as in (13).

$$I_1 = -C_1 \frac{V_R C_b (1+\epsilon_2)}{C_{F2}(1+\epsilon_1)} f_1 \tag{12}$$

$$f_2/f_1 = (C_1(1 + \epsilon_2))/(C_2(1 + \epsilon_1)) \tag{13}$$

Defining the ratio $(1 + \epsilon_2)/(1 + \epsilon_1) = k_\epsilon$, (13) can be re-written as in (14). This shows that the mismatch introduces a gain error in f_2.

$$f_2/f_1 = k_\epsilon (C_1/C_2) \tag{14}$$

From (14), it is evident that (C_1/C_2) can be obtained by measuring k_ϵ, and taking the ratio of (f_2/k_ϵ) and f_1 as in (15).

$$(f_2/k_\epsilon)/f_1 = (C_1/C_2) \tag{15}$$

The factor k_ϵ can be obtained by noting down f_2 for $x = 0$, i.e., by setting $C_1 = C_2$. Under this condition, $k_\epsilon = f_2/f_1$. This is a one-time measurement. From then onwards, for any new measurement, a corrected output frequency $f_{2\text{cal}} = (f_2/k_\epsilon)$ can be computed from the measured frequency f_2. Now, if f_2 is replaced by $f_{2\text{cal}}$ in (9), the ratio-metric output given by (16) will remain unaffected due to the mismatch, which is a major advantage. The same correction can be incorporated in (10), when a single-element sensor is interfaced. These computations can be realized using the CLU shown in Fig. 1.

$$\frac{(f_{2cal} - f_1)}{(f_{2cal} + f_1)} = \frac{(C_1 - C_2)}{(C_1 + C_2)} = kx \tag{16}$$

E. Range of the Sensor Capacitance

The ranges of C_1 and C_2 for which (8) is applicable is limited by the operating ranges of the opamps and VFC used to realize the circuit given in Fig. 1. The maximum output current, I_{O1max}, of OA1 will limit the maximum acceptable value, C_{1max}, of C_1, for a given C_a $(= C_b = C)$, $C_{F1}(= C_{F2} = C)$ and f_1, such that $C_{1max} < I_{o1max} \frac{C_F}{V_R C f_1}$. Similarly, $C_{2max} < I_{o2max} \frac{C_F}{V_R C f_2}$, where C_{2max} is the maximum value of C_2 and I_{o2max} is the maximum output current of OA2. The maximum output frequency, f_{2max}, possible for the VFC corresponding to the maximum (less than saturation) output voltage v_{oi3max} of OA3 will introduce another limiting factor for the maximum change ΔC_{max} possible for C_1 and C_2, i. e., $\Delta C_{max} = 2C_0(f_{2max} - f_1)/(f_{2max} + f_1)$. Considering the above factors, for sensors following (1),

$$C_{imax} < \min\left[I_{oimax} \frac{C_F}{V_R C f_i},\ C_0\left(1 + \frac{f_{2max} - f_1}{f_{2max} + f_1}\right)\right],$$

and for those satisfying (2),

$$C_{imax} < \min\left[I_{oimax} \frac{C_F}{V_R C f_i},\ C_0/\left(1 - \frac{f_{2max} - f_1}{f_{2max} + f_1}\right)\right],$$

where i = 1or 2. For the prototype developed, for sensors with linear characteristic, the C_{imax} works out to be 1.66 C_0 when f_{2max} = 500 kHz and f_1= 100 kHz. In case of sensors

satisfying (2), $C_{imax} = 3C_0$. For both cases, the resulting maximum kx is 0.66, which is sufficient for many applications of differential capacitive sensors [10], [15], [32]. To achieve a larger kx range, f_1 can be reduced keeping the same $f_{2\max}$ or a more suitable VFC can be selected.

F. Sensitivity of the Interface

In the case of the differential capacitive sensor, when $C_1 = C_2$, $f_2 = f_1$. When $C_1 = C_0 + \Delta C$ and $C_2 = C_0 - \Delta C$, (8) becomes

$$\frac{C_0+\Delta C}{C_0-\Delta C} = \frac{f_1+\Delta f}{f_1}. \quad (17)$$

or

$$\frac{1+\frac{\Delta c}{c_0}}{1-\frac{\Delta c}{c_0}} = 1+\frac{\Delta f}{f_1} \quad (18)$$

For $\frac{\Delta C}{C_0} \ll 1$, (18) can be approximated as $1 + 2\frac{\Delta C}{C_0} \approx 1+\frac{\Delta f}{f_1}$, or

$$\frac{\Delta f}{\Delta C} \approx \frac{2f_1}{C_0}, \quad (19)$$

which gives the sensitivity of the proposed CFC. For the single-element, the right-hand side of (19) reduces to $\frac{f_1}{C_0}$.

III. Error Analysis

The effect of important non-idealities in the output of the proposed SC-CFC is analyzed below. Here, let $C_{F1} = C_{F2} = C_F$, and $C_a = C_b = C$.

A. Input Offset Voltage

Let V_{OS1}, V_{OS2}, and V_{OS3} be the input offset voltages at the non-inverting terminals of OA1, OA2, and OA3, respectively. Since S_5 is used only to connect and disconnect node c to the input of OA_3, v_{oi3}, due to V_{OS3}, will be V_{OS3} alone, with no other integrating components. Hence the effect of V_{OS3} at the output of OA3 can be compensated by appropriately designing the VFC. This is required to maintain $f_1 = f_2$, when $C_1 = C_2$.

V_{OS1} and V_{OS2} contribute an additional voltage step in v_{oi1} and v_{oi2}, respectively. The impact of V_{OS1} in v_{oi1} and that of V_{OS2} in v_{oi2}, at any instant n, are given by (20) and (21), respectively, where $m = 1$ if ϕ_{sw} is high and $m = -1$, otherwise. Also, $v_{oi1}(n) = V_{OS1}$, and $v_{oi2}(n) = V_{OS2}$, when $n = 0$.

$$v_{oi1}(n+1) = v_{oi1}(n) + V_{OS1}C/C_F - m\,V_R C/C_F \quad (20)$$

$$v_{oi2}(n+1) = v_{oi2}(n) + V_{OS2}C/C_F + m\,V_R C/C_F \quad (21)$$

Thus, for ϕ_{sw} = high, when $I_1 = -I_2$,

$$(C_1\,(V_{OS1}-V_R)\;C/C_F)\,f_1 = (C_2(V_{OS2}+V_R)\;C/C_F)\,f_2. \quad (22)$$

Rearranging (22), gives

$$(C_1/C_2) = \left|\frac{(V_{OS2}+V_R)}{(V_{OS1}-V_R)}\right| (f_2/f_1) \quad (23)$$

Assuming V_{OS1}, V_{OS2}, V_R to be not time varying, (23) can be re-written as

$$(C_1/C_2) = k_{OS}(f_2/f_1). \quad (24)$$

In the case of the prototype of the proffered circuit, the maximum values of V_{OS1} and V_{OS2} is 75 μV. Substituting these in (23) shows that V_{OS1}, $V_{OS2} \ll V_R$ (= 2.5 V) and so, in the developed prototype, input offset voltage has a negligible impact. Thus, as long as the opamps used in the proposed circuit are chosen such that V_{OS1} and $V_{OS2} \ll V_R$, and the VFC designed to compensate for V_{OS3}, the impact of the input offset voltages in the final output is negligible.

B. Input Bias Current

Let I_{B1}, I_{B2}, and I_{B3} be the input bias currents at the inverting terminals of OA1, OA2, and OA3 respectively. The presence of I_{B1} will change v_{oi1} by $I_{B1}T_1/C_F$ in each cycle of ϕ_1. However, in practice, $\frac{I_{B1}T_1}{C_F} \ll V_R C/C_F$. Hence the effect of I_{B1} in I_1 is negligible. Similarly, the effect of I_{B2} in I_2 is not significant. However, since the bias current is flowing continuously in the same direction, v_{oi1} and v_{oi2} will go into saturation. To prevent this, resistors of appropriate values (20 MΩ) are connected in parallel to C_{F1} and C_{F2}, respectively. Since this resistor is in the feedback-path of OA1 and OA2, it can be implemented using relatively low-value resistors, say the largest being in 100 kΩ range, connected in a T- network. It has been reported that the leakage resistance of on-chip capacitors is in the range of few mega ohms [33]. In such a case, the additional resistor in parallel, as in the prototype, may not be necessary. In case the above options are not feasible, keeping these resistors external to the IC can be considered, to save the chip area, when an IC is designed.

In the ideal condition, at steady state, $I_3/2 = I_{CF3} = 0$. Due to the presence of I_{B3}, at the input of OA3, at steady state

$$(I_3)/2 = I_{CF3} = -I_{B3}. \quad (25)$$

Substituting (3) and (5) in (25) with f_2 replaced with f_2', to indicate the new condition $I_{CF3} = -I_{B3}$, and rearranging, (26) is obtained.

$$f_2' = \frac{(-I_{B3}C_F/V_R C)}{C_2} + \left(\frac{C_1}{C_2}\right) f_1 \quad (26)$$

Substituting the values from the prototype of the proposed circuit (I_{B3} = 30 pA, C_F = 2 nF, C = 20 pF, V_R = 2.5 V, f_1 = 100 kHz, along with the smallest value of C_2 used, 100 pF, and the corresponding C_1= 400 pF) in (26), the relative error in f_2', with respect to f_2, obtained is –0.003%. Thus, as long as OA1, OA2, and OA3 are chosen such that $\frac{I_{B1}T_1}{C_F}$, $\frac{I_{B2}T_1}{C_F} \ll V_R C/C_F$ and $\frac{(-I_{B3}C_F/V_R C)}{C_2} \ll \left(\frac{C_1}{C_2}\right) f_1$, in the proffered circuit, the impact of bias current in the final output is negligible.

C. Mismatch between $+V_R$ and $-V_R$

Let the positive DC excitation be $+V_R$, whereas the negative be $-V_R(1+\epsilon_V)$, where ϵ_V is the relative mismatch between the magnitudes of the V_R and $-V_R$. ϵ_V = 0, in an ideal case. This voltage mismatch contributes to I_{CF3} when ϕ_{sw} = 1. In this condition, I_2 and I_3 given in (4) and (5) will get modified as (27) and (28), respectively.

$$I_2 = +C_2 \frac{\partial v_{oi2}}{\partial t} = +C_2 \frac{V_R(1+\epsilon_V)C}{C_F} f_2 \quad (27)$$

$$I_3 = I_1 + I_2 = \frac{V_R C}{C_F}(C_2 f_2 - C_1 f_1) + C_2 \epsilon_V \frac{V_R C}{C_F} f_2 \quad (28)$$

In a balanced condition, $I_{CF3} = I_3 = 0$. Then, the condition (29) can be obtained from (28).

$$\frac{C_1}{C_2} = k_V \frac{f_2}{f_1} \quad (29)$$

Comparing (29) with (8), it can be seen that the mismatch in reference voltages results in a multiplication factor $k_V = (1 + \epsilon_V)$. The value of k_V can be calculated, to correct the measurement, by setting $C_1 = C_2$ and comparing the f_{2meas} measured to the expected f_2 (= f_1), i.e. $k_V = \frac{f_1}{f_{2meas}}$. If there is a drift in ϵ_V, a periodic calibration/correction will be required.

D. Variations in the Switch Control Signals ϕ_{sw} and ϕ_1

A change in the frequency f_{sw} of ϕ_{sw}, will change the duration for which ϕ_{sw} is high. During the operation, the step change in v_{oi2} is $V_R C/C_F$. The maximum number of such steps, expected, when ϕ_{sw} is high is $(f_{2max})/(2f_{sw})$. Let us say that the maximum output voltage swing of OA2 is $2(V_{SAT} - 1)$, where V_{SAT} is the saturation voltage of opamp. This means $[(f_{2max})/(2f_{sw})] < [2(V_{SAT} - 1)/(V_R C/C_F)]$, or the design should satisfy the condition

$$\frac{(f_{2max} V_R C)}{4(V_{SAT}-1)C_F} < f_{sw(min)},$$

where $f_{sw(min)}$ in the minimum value of f_{sw} expected.

Any change in the frequency of ϕ_1 will impact the accuracy of the measurement. In the proposed CFC, the value of f_1 was found to be stable and accurate during the measurement time. However, it is advisable to measure f_1 periodically, using the same counter/timer, and use in (9) or (10), to ensure that the accuracy of the measurement of kx is not affected.

E. Non-idealities of the Switches

The effects of charge injection and ON resistance of the switches on the final output of the CFC are discussed below.

1. Charge Injection

To analyze the effect of charge injection, each SPDT switch in Fig. 1 can be replaced by the charge injection model given in [34]. The charge injected at the output of each switch is a combination of charges generated during breaking of a contact, say position '1', and making of the next, say position '0'. S_3, S_4, and S_5 inject charges into C_{F1}, C_{F2}, and C_{F3}, respectively, changing v_{oi1}, v_{oi2}, and v_{oi3}, respectively, thereby affecting the final output of the proposed CFC. To realize the switches, IC MAX4709 from Maxim Integrated has been used. This IC is so designed that the switches inject zero charges during the making and breaking of the input-output connections. The functional diagram can be found in [34], [35]. The implementation of these ICs on the silicon substrate is done using the CMOS process [34]. As this is a zero-charge injection switch, the associated error will be negligible.

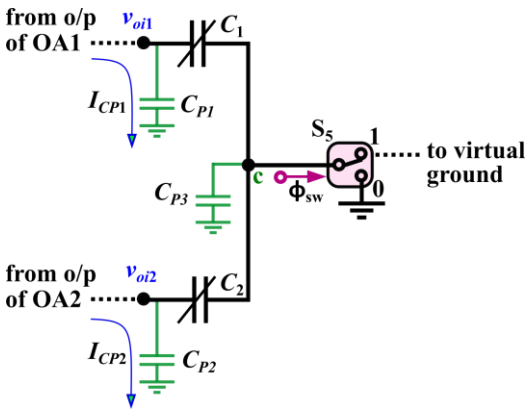

Fig. 3. The parasitic capacitances C_{P1}, C_{P2} and C_{P3}, associated with the differential capacitive sensor consisting of C_1 and C_2, are indicated.

2. ON Resistance

The impact of the switch ON-resistances can be analyzed by replacing the switches S_1-S_4 by the corresponding resistances R_{ON1}, R_{ON2}, R_{ON3}, and R_{ON4}, respectively. Consider first that ϕ_{sw} = high. If for $\phi_1 = 0$, $\phi_2 = 0$, as long as $(R_{ON1} + R_{ON3})C_a << (1/f_1)$ and $(R_{ON2} + R_{ON4})C_b << (1/f_2)$, C_a and C_b get fully charged to $+V_R$ and $-V_R$, respectively, and vice-versa for ϕ_{sw} = low. For $\phi_1 = 1$, $\phi_2 = 1$, the outputs of OA1 and OA2 will be negligibly affected by the ON-resistances while $R_{ON3}C_a << (1/f_1)$ and $R_{ON4}C_b << (1/f_2)$ holds true.

F. Parasitic Capacitances

Parasitic capacitance to ground will be present when shielded cables, with shield connected to ground, are used to connect the capacitive sensor to the interface circuit. Similarly, there will be parasitic capacitance between the ground plane and traces of the printed circuit board or lines of the bread-board. The equivalent lumped model of the parasitic capacitances is shown as C_{P1}, C_{P2}, and C_{P3} in Fig. 3. C_{P1} and C_{P2} do not impact the performance of the proposed circuit as long as the outputs of the opamps OA1 and OA2 are not overloaded by them. C_{P3} is inactive as one end of it is connected to the virtual ground or ground while the other is always at ground. Hence, it has no impact on the final output.

IV. Experimental Setup and Results

A. Prototype

The hardware prototype of the proposed closed-loop SC-CFC, given in Fig. 1, was realized using the components and ICs listed in Table I. In the prototype, the clock signals ϕ_{sw} and ϕ_1 were set using a function generator to f_{sw} = 1 kHz and f_1 = 100 kHz, respectively. Since these are generated from the same dual-channel function generator, they are in synchronization. Alternatively, the synchronization can be maintained by generating ϕ_{SW} and ϕ_1 using the timer/counter

TABLE I

COMPONENTS AND ICS USED IN THE PROTOTYPE

Component	Part/Value	Component	Part/Value
V_R	Using LM385-2.5	C_a, C_b	20 pF
S_1 - S_5	MAX4709	C_{F1}, C_{F2}	2 nF
VFC	ADVFC32	C_{F3}	2 nF
OA1, OA2	OPA227	ΔC	±150 pF
OA3	LF357	f_{sw}	1 kHz
CLU	ATSAM3X8E	f_1	100 kHz

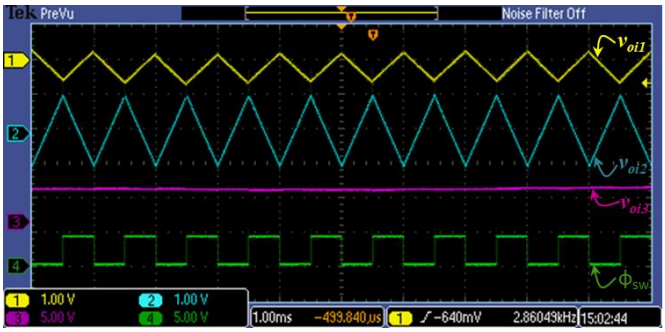

Fig. 4. A snapshot of the integrator waveforms, from the prototype, for $C_1 > C_2$.

unit of a microcontroller, with appropriate pre-scaler.

The linearity of the VFC limits the linearity of the overall system. In the protype, ADVFC32 was employed. It has high linearity, e.g., 0.05% in the 100 kHz range and 0.2% in the 500 kHz range. The VFC was set to output $f_2 = f_1$, for $x = 0$, by selecting the values of the resistors and capacitors in accordance with the design calculations given in [36]. Also, the VFC was configured to handle both positive and negative values of v_{oi3}.

Frequency f_2 corresponding to $C_1 = C_2$, was used to determine the mismatch correction factor, k_ϵ as in (14). The prototype was then tested using two identical standard variable capacitance boxes, with high leakage resistances, representing C_1 and C_2, set to the nominal capacitance value, C_0 = 250 pF. The final ratio-metric output, as per (16), was obtained after applying the corrections for mismatch discussed in section-II.A. The counter in the CLU was programmed to measure f_2 for a gate time of 10 ms. This was used in the CLU to compute the final output applying (15). The important waveforms from the prototype were observed using MSO 2014, Mixed Signal Oscilloscope, during the test. A snapshot of the waveforms, from the oscilloscope, for $C_1 > C_2$ is given in Fig. 4.

B. Power Consumption

As a proof-of-concept, the prototype was implemented with discrete components and ICs and, hence, it was not optimised for low power consumption. In this prototype, the power consumption of the opamps, VFC, switches and V_R were, P_{OA} = 110 mW, P_{VFC} = 80 mW, P_{SW} = 6 mW and P_{VR} = 50 µW, respectively. The clock is generated in the prototype by a function generator, but in practice it can be generated by the microcontroller. When the microcontroller is used to generate ϕ_{SW} and ϕ_1, in addition to measuring f_2, the power $P_{\mu C}$ taken was about $P_{\mu C} \cong$ 3 mW. Thus the total power = $P_{OA} + P_{VFC} + P_{SW} + P_{VR} + P_{\mu C} \cong$ 200 mW. If the entire unit is designed and fabricated as a single chip, the overall power consumption could be reduced to as low as that of a dual-slope ADC (≅ 10 mW [37]).

C. Testing the Effectiveness of the Mismatch Correction

To test the effectiveness of the correction mechanism against component mismatch, discussed in section-II.A, a test was conducted by intentionally introducing a mismatch between C_a and C_b by setting $C_b = C_a/2$. The error percentage in the VFC output before and after correction for different values of ΔC (deviation of C_1 from the nominal capacitance) is given in Table II. As can be seen, the correction mechanism almost completely removes the effect of the mismatch. The same test was conducted by similarly introducing a mismatch between the C_{F1} and C_{F2}, and the correction was also found to be effective.

TABLE II

EFFECTIVENESS OF THE MISMATCH CORRECTION

ΔC (pF)	-10	-5	0	+5	+10
% Error before correction	48.39	48.32	48.40	48.00	48.48
% Error after correction	0.01	0.15	0.00	0.17	0.15

D. Linearity and Sensitivity

In this test, the values of C_1 and C_2 were first set to nominal capacitance C_0 = 250 pF. Then they were varied in steps of 10 pF in opposing directions, for 15 steps in either direction. This process emulates a differential capacitive sensor with a linear characteristic as in (1), with a full-scale change kx^{FS} = 0.6. The CLU provided the output as per (15), for each step. In this manner, the output was recorded for a range of capacitance, ΔC = ±150 pF, from nominal value. The results are presented in Fig. 5. This corresponds to a full-scale $kx = \pm 0.6$. This tested range covers the range of measurement in several applications, e.g., 0.35 [10], 0.536 [15] and 0.6 [32]. This is within the possible range discussed in section-II.D.

To obtain the maximum non-linearity error (NLE), the recorded output-data was first plotted. A trend-line of the same was then obtained using the Least Squares Algorithm. Subsequently, the values of the y-axis were determined by substituting the corresponding x-axis data in the trend-line equation. These values are taken as the expected output values, had the system been linear. Each measured value was subtracted from the corresponding expected value, for the full measurement range. This gives the NLE in each measurement. The % with respect to the full-scale (kx^{FS} = 0.6) gave the % NLE. The maximum NLE observed was 0.24%.

In addition, the linearity was tested for the single-element capacitive sensor. For this test the same value of C_0 was used and the value of C_1 alone varied in steps of 10 pF from 100 pF

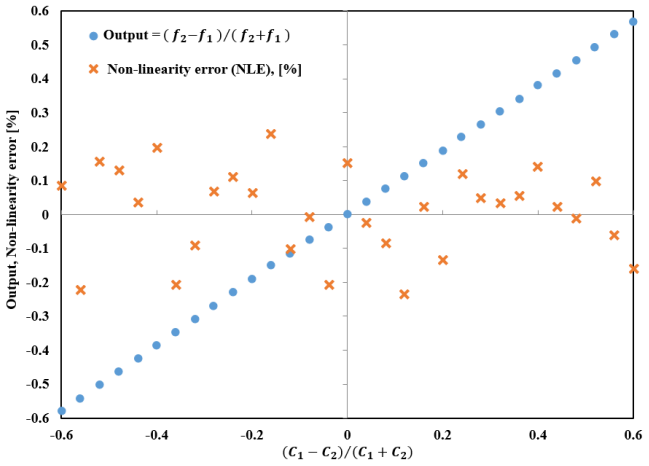

Fig. 5. Results from the prototype by varying C_1 and C_2. The output and the percentage non-linearity error obtained are shown.

to 400 pF. The worst-case %NLE found in this test was 0.19 %. The linearity of the prototype circuit has also been verified for single-element and differential capacitive sensors that follow inverse characteristic as in (2).

The sensitivity of the frequency output f_2 with respect to ΔC was computed using (19). For the prototype developed f_1= 100 kHz and C_0= 250 pF. The resulting sensitivity is $\frac{\Delta f}{\Delta C} \approx 0.8$ kHz/pF. The same has been verified practically from the prototype. For the single-element capacitive sensor, this was found to be ≈ 0.4 kHz/pF.

E. Resolution, Signal-to-Noise Ratio (SNR) and Repeatability

To determine the resolution and repeatability, the prototype CFC was operated for ΔC = 5 pF, and the ratio-metric output, $(f_2 - f_1)/(f_2 + f_1)$, was recorded 30 times and tabulated. The formulae given in Table III, based on the approach given in [38], were used to determine the resolution and repeatability parameters, given in the same table. The proffered circuit shows a resolution of 12.59 bits (ENOB), signal-to-noise ratio (SNR) of 77.56 dB and repeatability error of 0.01%.

F. Rise Time

To ascertain the rise time of the proffered CFC, initially, the sensor capacitance was set to its mid-scale and then a sudden change in capacitance was introduced, in parallel, using a switching arrangement controlled by the signal v_{step}. When v_{step}= 0, an additional capacitance of 10 pF was introduced in parallel to C_1, using a capacitance box, with negligible leakage conductance, from Rohde and Schwarz. The rise time was 6 ms for f_{sw} = 1 kHz and f_1 = 100 kHz. A snapshot of the waveforms, in this case, is given in Fig. 6. As mentioned in section-II. B, f_2 is measured using a counter. In the prototype, a change in the measurand will be correctly reflected in the output, at steady state, after about 16 ms, considering the rise time of 6 ms, and the gate time of 10 ms.

To verify the impact of the values of the operating frequencies in the rise time of the prototype SC-CFC, both f_{sw} and f_1 were decreased to 100 Hz and 10 kHz, respectively.

TABLE III

REPEATABILITY STUDY

Parameter	Formula	Value
Signal-to-noise ratio (SNR)	$SNR = 10\ log\ \frac{\sum_{i=1}^{M} X(i)^2}{\sum_{i=1}^{M}[X(i)-\bar{X}]^2}$	77.56 dB
Standard Deviation, σ	$\sigma = \sqrt{\frac{\sum_{i=1}^{M}[X(i)-\bar{X}]^2}{M-1}}$	4.33×10^{-5}
Resolution (ENOB), n bits	$n = \frac{(SNR-1.76)}{6.02}$	12.59 bits
Repeatability, d	$d = \frac{\Delta_{rmax}}{X_u - X_l} \times 100\%$	0.01%

$X(i)$ = i^{th} measurement; $\bar{X}$ = average value of the measured data

M = total number of measurements

X_u, X_l = upper and lower limits of CFC

Δ_{rmax} = maximum difference between repeated measurements

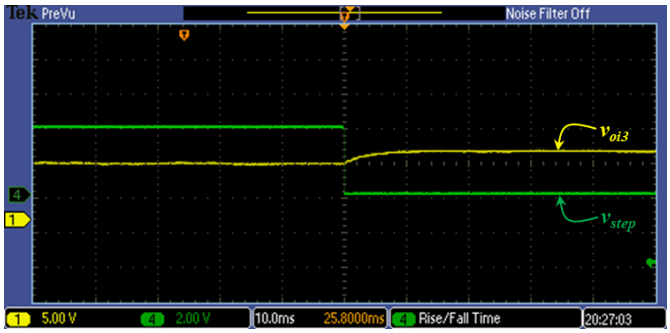

Fig. 6. Rise time of the CFC for f_{sw} = 1 kHz, f_1 = 100 kHz.

Then, the rise time was 65 ms. The results in both cases show that the rise time improved by approximately ten times when the operating frequencies f_{sw} and f_1 were increased tenfold.

V. DISCUSSION

The main features of the new scheme have been analyzed in comparison with the best ten of the existing schemes, and presented in Table IV. The proposed scheme is suitable for single-element and differential capacitive sensors (DCS), which is a main difference as can be seen in Table IV. The CFCs [20] - [22] presented in Table IV are suitable only for single-element capacitive sensor. The presented approach provides a linear output, without any additional computation or correction, even for single-element sensor that follows an inverse characteristic which is another specialty.

Other important factors of the proposed approach are: (a) It uses a closed-loop approach. Differential capacitance-to-frequency converter with this feature has not been sufficiently explored before. Closed-loop approach has been used to realize self-balancing bridges in [30], [31]. However, the outputs of these bridge schemes are sensitive to parasitic capacitance. In addition, they need a precise sinusoidal AC excitation. These designs have limited linearity and accuracy due to the use of analog multipliers, with high error (as large

TABLE IV

COMPARISON STUDY

	Methods	Capacitance-to-digital/time			Current-mode interface [39]	Auto-balancing bridge [28]-[31]	µC-based [16]	Capacitance-to-frequency			
		SAR [27]	Σ-Δ [24]	Time [25]				[20]	[21]	[22]	This work
Parameters	Suitable for differential capacitive sensor (DCS)	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	Yes
	Suitable for single-element and DCS	No	Yes[a]	No	No	No	No	No	No	No	Yes
	OL / CL	CL	OL	OL	OL	CL	OL	CL	OL	OL	CL
	Excitation (AC/DC)	DC	AC	DC	DC	AC	DC	DC	AC	DC	DC
	Ease of IC fabrication	High	High	High	Yes	Low	---	High	Low	High	High
	Resolution	150 aF	20 aF	160 aF	800 aF[b]	NS	7 bits	17.5 fF	20 zF[c]	NS	12.5 ENOB[d]
	%NLE	---	0.01	---	1.5	---	1	0.1	0.1	0.13	0.24
	Sensitivity	---	---	127 ns/fF	5 nA/fF	---	---	---	12 kHz/pF	---	0.8 kHz/pF
	Insensitivity to parasitic capacitance	Yes	Limited	Yes	Limited	No	No	Yes	No	Yes	Yes
	Insensitivity to component mismatch	NS	---	No	NS	No	Yes	---	No	---	Yes[e]
	Digital/quasi-digital output	Yes	Yes	Yes[f]	No	No	Yes	Yes	Yes	Yes	Yes
	Ratio-metric output (Ease of integration[g])	No	No	Yes	Yes	No	Yes	No	No	No	Yes
	Power consumption (mW)	1.59×10^{-3}	3.94	0.720	0.22	---	---	3645[h]	---	---	200[h]
	Conversion time (ms)	0.81	124	0.5	----	---	---	0.45	---	---	16

OL - open-loop, CL - closed-loop, NS - not studied, NLE - non-linearity error, --- not available or not applicable. [a] Unlike the proposed scheme, this converter in [24] is not designed to provide ratio-metric output, for differential capacitive sensors. In addition, it will not automatically give a linear output for single-element sensor with inverse characteristic. [b] Simulated, not measured. [c] theoretical. [d] Resolution of the ratio-metric output in Effective Number of Bits. 12.59 corresponds to 80 fF in terms of absolute capacitance. [e] Needs one-time correction. [f] changes the pulse-width. [g]Easy to interface to new sensor as the output is not sensitive to C_0. [h] Will be much less once designed as a single IC.

as 2%), in them. (b) Excitation is derived from a simple DC reference source. (c) Since it uses switched-capacitor circuit, it is relatively easy to design and fabricate its IC. (d) Insensitive to parasitic capacitance and mismatch in values of components used. (e) Ratio-metric output for DCS and ratio output for single-element capacitive sensor. Hence a linear output is obtained independent of the sensor characteristic, and nominal capacitance. Some of the existing schemes have only some of the features of the proposed scheme as can be seen in Table IV.

The proposed design does not rely on voltage-controlled resistors to realize auto-balancing [30], [31]. Instead, a VFC, together with a switched-capacitor mechanism, effectively realizes the auto-balancing. It is important to select a VFC with sufficient linearity. VFCs with very high linearity, as the one used in the prototype, are available [36].

VI. CONCLUSION

The design, development, and realization of a new closed-loop switched-capacitor capacitance-to-frequency converter (CFC) have been presented in this paper. The developed CFC is suitable for single-element and differential capacitive sensors. The scheme provides a linear output, irrespective of the sensor characteristic being linear or inverse. The output is independent of the value of the nominal capacitance, and insensitive to the parasitic capacitances, which enhance the ease of interfacing. Thus, the presented circuit is compatible for integration with a wide variety of single and differential capacitive sensors. It uses a simple DC excitation source, as opposed to complex AC sinusoidal excitation which needs precise amplitude stabilization and very low total harmonic distortion. As the scheme is realized using switched-capacitor circuit, the presented CFC is suitable for IC fabrication. The prototype of the proposed CFC possesses desirable features such as a low maximum non-linearity error (NLE) of 0.24%, a resolution of 12.59 bits (ENOB), signal-to-noise ratio (SNR) of 77.56 dB, and rise time of 6 ms. The range of the prototype CFC developed is ±60% of the nominal capacitance of the sensor. The range and measurement time can be modified by suitably selecting the frequency of clock signals, components, and ICs. The design presented specifies criteria to minimize the impact of circuit non-idealities such as input offset voltage and input bias current of opamp, and mismatch between the magnitudes of the DC reference voltages.

ACKNOWLEDGMENT

The authors would like to thank the Department of Science and Technology (DST), Govt. of India, for its financial assistance (Grant Number SERB/F/4573/2016-17) in carrying out the research activities presented in this paper.

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