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Design of a low-power VLSI temperature sensor

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Dedication

I would like dedicate this work to my family (Micaela, Paola, Estefania, Samael, Adrian), especially my mom Lourdes and my niece Valentina.

I also want to thank my girlfriend Sabine for all her help, particularly with grammar corrections made during the editing of my thesis. (♡ $\rightarrow \infty$)

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Abstract

A low power CMOS temperature sensor with digital output is presented in this work. The sensor is current based, the combination of dependent and independent current that control the frequency of 2 ring oscillators. The difference in frequency of this two ring oscillator is converted into a digital temperature code by asynchronous counters. The reference current and the PTAT current is generated by applying a temperature dependent voltage across two resistors with different temperature coefficients. To achieve a low power consumption, the temperature voltage reference operates under 200 mV and resistors in the Mega Ohms range are utilized. In order to save area, an additional current mirror is used to reduce the current without increasing the resistor's value.

This sensor was implemented in TSMC 180nm technology and occupies an area of $0.085mm^2$. After post layout simulations, the sensor shows a current consumption of $1.7\mu A$, a resolution of 0.17ºC in the 0-60ºC temperature range with a conversion time of $1.8ms$ and 3.2 nJ of energy per conversion.

1 Introduction

Low-power operation has become a popular trend in the design of very large-scale integration (VLSI) circuits, particularly in technologies like wireless sensors networks (WSN), which require extremely low power circuits. A WSN consists of a distributed network of sensors with wireless communication. In base of the functionality and power consumption a WSN is organized in three node levels (figure 1): The sensor node (TAG), the clustering node (HUB), and final processing node (BASE STATION).

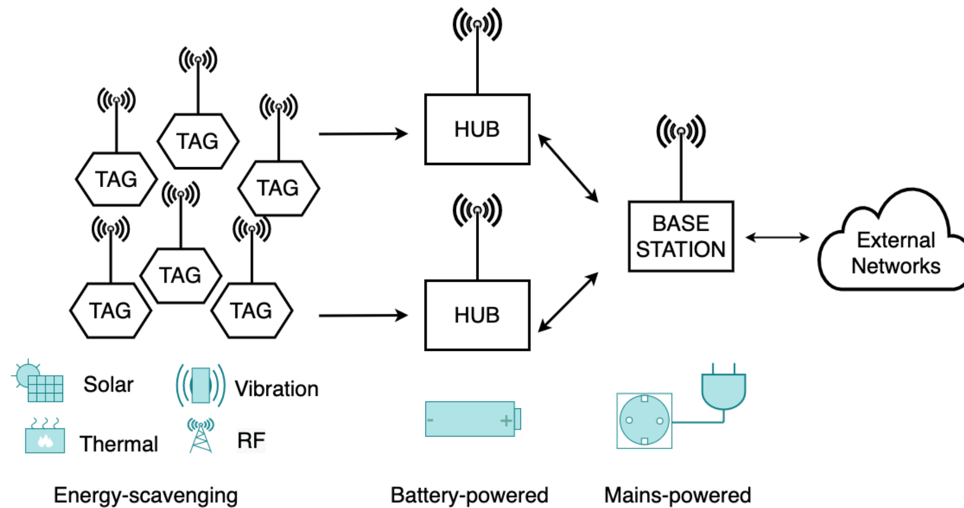


Figure 1: A typical WSN system organization [1] .

The base station is main-powered and performs more of the functionalities since has not powered constrains. The battery-powered HUB node collects the data from the sensors, it performs some limited calculations to send the recollected data towards the base station. The TAG node doted with energy harvesting or scavenging incorporates a physical or environmental sensor. The TAG node digitizes and sends the sensor measurement to the HUB node [1].

The WSN can be used in a wide range of applications, including medical, environmental monitoring, and radio frequency identification (RFID) tracking systems. Among the different sensor types, the temperature is one of the most commonly used sensors and therefore become an important element in WSN systems.

1.1 Motivation

The Integrated Smart Sensor and Health Technologies (ISSET) Research Group of the Universitat Politècnica de Catalunya (UPC) works in the development of integrated solutions to distributed sensing networks and Internet of Things (IoT) applications through the evaluation, design and experimental testing of multiples sensors in CMOS technology for environmental monitoring with emphasis in low-power consumption.

Beyond environmental applications, there are some physical, biological, chemical, mechanical, and electronic systems that exhibit a temperature dependence. For this reason, the temperature

measurement is a critical task in many of these systems. Traditionally temperature sensors were implemented with external components like thermistors or thermocouples. Nowadays most of the temperature sensors are based in CMOS and incorporate read-out circuitry with digital output in the same chip, resulting in a simple, compact and low power temperature sensor.

1.2 Objectives

The objective of this thesis is to develop a VLSI temperature sensor, using standard CMOS technologies. The sensor is based in dependent/independent current sources used to control an oscillator and counter that generate the digital temperature code. All the signals are generated in the on-chip to avoid using external circuits for autonomous operation. The design includes a schematic and physical layout with special focus in low-power operation.

1.3 Project scope

The following scope was set to achieve the main objective. First, a new sensing element based in 2 NMOS transistors and resistors, available in the process library, were thermally characterized for its posterior implementation into a voltage to current converter that generates a reference and proportional to absolute temperature (PTAT) currents. These currents were converted into two frequencies with the same characteristics. The relationship between these two currents was translated into a digital temperature code by a frequency to digital converter. After this, the physical implementation and verification was performed using Calibre DRC, LVS, and PEX tools. Finally, the sensor performance was obtained after resistive-capacitive (R C) parasitic extraction.

1.4 Work structure

This thesis is organized in 5 sections:

- State of the art: CMOS Temperature Sensors

  In this section the full compatible CMOS sensing elements are introduced, the operating principle is presented with an emphasis on how the thermal variations are converted into an electrical parameter for use as a temperature sensor. Also, some aspects of current consumption and the benefit and drawbacks of the sensing elements are briefly discussed.

- Methodology

  In this section the temperature sensor is analyzed in detail. First, the CMOS sensing element is analyzed and the generation of sensitive/insensitive to temperature currents is explained. Second, the analysis of current-frequency conversion is explained and two types of ring oscillator are introduced. After that, the frequency to digital conversion is analyzed. Finally, in the last part of this section the component's values and transistor sizing of the temperature sensor are explained.

- Results

  The final implementation of the sensor is presented in this section. Schematic and post-layout simulations were realized to determine the performance of the sensor.

- Conclusion and future work

  The last section presents the conclusion, as well as gives suggestions for future works.

2 State of the art: CMOS Temperature Sensors

A CMOS smart temperature sensor combines in the same chip all the functions and circuits needed to provide a temperature measurement in a digital format. At the system level, a smart temperature sensor has three basic parts: the sensing element, the reference, and the analog to digital block A/D.

To obtain a digital representation of the temperature, the sensor requires two signals: one well-behaved and thermal dependent signal, and another insensitive to temperature used as a reference. When a reference signal increases with the temperature, it is denominated as proportional to absolute temperature PTAT. On the contrary, if its value decreases in respect to the temperature, then it is known as complementary to absolute temperature or CTAT. By combining PTAT and CTAT references, it is possible to obtain a voltage reference insensitive to the temperature.

In a bandgap reference voltage (BGR), a PN junction is forward-biased with a constant current, the voltage drop across the junction exhibits a CTAT behavior. This CTAT characteristic of the diode is compensated by the intrinsic PTAT characteristic of the thermal voltage to achieve an insensitive to temperature voltage reference. The PN junction can be implemented with a diode or be replaced by a diode configuration in BJT or MOSFET transistor.

CMOS technology has some microelectronic devices that are very sensitive to temperature that can be used as sensors. The right choice of the sensing element depends on the application area and requirements: cost, accuracy power, resolution, speed, etc. One of the advantages of the CMOS-based temperature sensor is the cost since it allows integration of all the components in the same substrate without the use of external sensing elements.

Compared with external referenced sensors like the Pt-100 based, the CMOS based sensor is limited to a lower temperature range around -50º and 150ºC and the accuracy is between 0.5 and 2 ºC [2].

Some electronic devices with thermal characteristics suitable for temperature sensing, which are available in most of the CMOS technologies, are presented below. The analysis is mostly focused on how the conversion from temperature to electrical domain is performed.

2.1 Bipolar Junction Transistor (BJT)

In CMOS technology it is possible to design lateral and vertical BJTs transistors. Regardless of the transistor type, both are based on the thermal dependency of the base-emitter voltage V_{BE} [3].

$$V_{BE} = V_T ln\left(\frac{I_C}{I_S}\right) \tag{1}$$

Where V_T is the thermal voltage, I_C is the collector current, and I_S is the saturation current, a parameter process dependent. In a BJT temperature sensor, a proportional to absolute temperature (PTAT) voltage is generated by combining two BJTs biased with different I_C currents. If the collector current in one of the two transistors is dimensioned ρ-times greater than the other, then the difference between these two V_{BE} voltages has a PTAT behavior that depends on the thermal voltage and the current ratio between both transistors [3].

$$\Delta_{V_{BE}} = V_T ln(\rho) \tag{2}$$

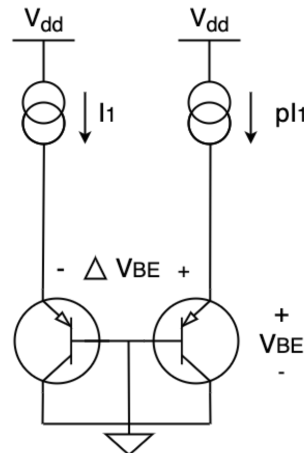


Figure 2: BJT based sensing element.

The thermal characteristic of the V_{BE} and $\Delta_{V_{BE}}$ makes BJTs transistors especially useful for bandgap voltage references (BGR) and temperature sensors applications. In these sensors, the reference and the PTAT voltages are generated simultaneously by the same circuit, so its implementation is simpler.

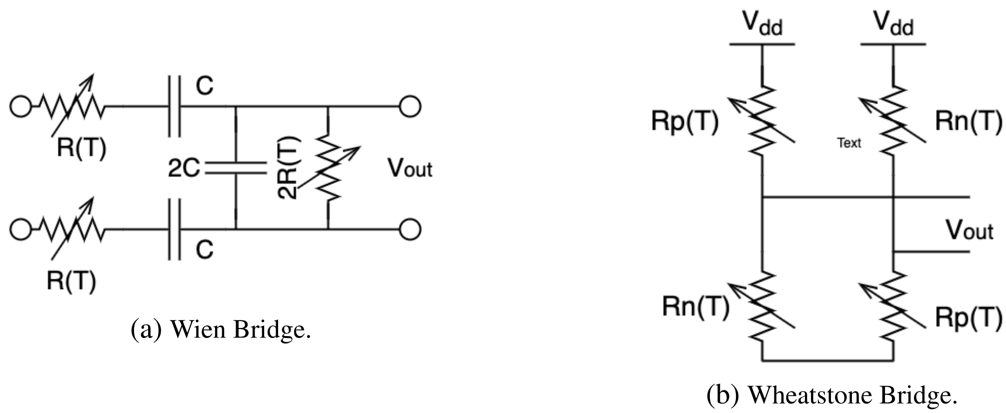
To provide a digital output for this type of sensor, the PTAT voltage is fed into an analog to digital converter (ADC). The sensor resolution depends on the type of ADC used, for example with a sigma-delta analog to digital converter, (ΣΔ-ADC), a resolution in the 0.02ºC range is reported [4] [5]. An important aspect of these sensors is that they require a current in the *uA* or even in the *mA* range to operate properly [6].

2.2 Resistor based

Most CMOS processes offer different resistors types, some of them exhibit an important temperature dependence suitable to be used as a temperature sensor. The resistivity varies in a complex way; depending on the accuracy required it can be approximated by a first-order model.

$$R(T) = R_0(1 + TC1(T - T_0)) \tag{3}$$

Where $R(T)$ is the resistance as a function of the temperature T, R_0 is the resistance at a given T_0 temperature (typically 25ºC) and $TC1$ is the first-order temperature coefficient expressed in parts per million. Depending on the type, the resistance has a PTAT or CTAT behavior. The resistor has first-order temperature coefficients in the range of -1000 to 6000 ppm/ºC [25]. For instance, a resistor with a $TC1 \approx 6000 ppm/°C$ that operates in a temperature range between -50ºC to 125ºC would imply an increase in resistivity around 90%, that is considerably temperature sensitive.



(a) Wien Bridge.

(b) Wheatstone Bridge.

Figure 3: Resistor based sensing elements.

The resistor based temperature sensor [7] employs a Wien bridge filter (figure 3a) with a phase domain sigma delta modulator $PD\Sigma\Delta M$ to achieve a resolution $\approx 6m$ºC in a temperature range between -40ºC to 85ºC. Another example of a resistor based sensor uses a Wheatstone bridge (figure 3b) combined with a time domain sigma delta modulator $TD\Sigma\Delta M$ and reports a resolution around 16mºC in the same temperature range [8].

Some drawbacks of resistor based temperature sensors are their higher variations across the process, minimum supply voltage requirements, thermal noise, and area constraints that impose multiple temperature calibrations in order to achieve good accuracy.

2.3 Electro-thermal filters ETF

The operation principle of ETF temperature sensors is the thermal diffusivity of the silicon D, defined as the rate at which heat transfers from a hot end to a cold end. The thermal diffusivity of the silicon D is a well-defined parameter, in the temperature military range it is approximated by a power-law [9].

$$D \propto T^{-n} \tag{4}$$

Where T is the absolute temperature and $n \approx 1.8$ (recommended value for high purity undoped silicon in the military temperature range). The thermal dependence of D is the principle used to develop temperature sensors.

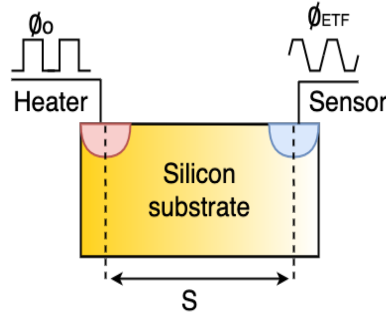


Figure 4: ETF based sensing element.

Temperature sensors based in ETF integrate a heating element and a temperature sensor (thermopile) located in the same substrate at a distance S respect to each other. The temperature variations induced by the thermal element are converted into a small voltage signal, then due to the thermal substrate dependency, this structure acts as a low-pass filter. If the hot end of the thermal filter is excited by a signal with a known reference frequency f_{ref}, then the phase shift of the reference signal at the cold end of the thermal path Φ_{ETF} is modeled by the equation 5.

$$\Phi_{ETF} = (-S\sqrt{f_{ref}})T^{\frac{n}{2}} \tag{5}$$

Where f_{ref} is the frequency of the reference signal, S is the distance between the heather and the sensor, and T is the absolute temperature. Additionally in order to provide a digital output, a phase domain analog to digital converter is used. Also, given that Φ_{ETF} is not a linear function, an extra linearization step is performed in the digital domain.

The use of ETF technique reports a resolution of 0.03ºC [10]. The accuracy of the sensor depends principally on the lithography that establishes the distance S because the thermal diffusivity is not a process-dependent parameter [11]. Compared with the other sensing techniques, it dissipates more power at mW range (without heaters) [9], and tolerates a high-temperature range($\approx$ 160ºC) [12].

2.4 MOSFET based temperature sensor

The MOSFET based temperature sensors depend on the exponential characteristics of the drain current I_D when they operate in the sub-threshold region. In a similar way to the BJT transistor, the sub-threshold current is modeled as follows [13]:

$$I_D = I_o \times e^{\left(\frac{V_G - T_{th}}{mV_T}\right)} \tag{6}$$

Where I_0 is the leakage current (process dependent parameter), m is the subthreshold slope and V_{th} is the threshold voltage. The similarity between equation 2 and 6 makes it possible for the MOSFET transistor to replace BJTs as a temperature sensing element. For low-power applications, time to digital or frequency to digital converters are used instead of the conventional ADCs. In this configuration a PTAT current is generated, this current feeds a current controlled

oscillator and generates a PTAT frequency [14]. Finally, the temperature is measured by comparing the PTAT frequency with an insensitive to temperature reference [13]. The performance of the sensor is related to the reference clock. Compared with Band-gap temperature sensors that are self-referenced, the reference in a time-domain digital converter (TDC) is commonly provided by an external clock.

In contrast to the BJT temperature sensors, the MOSFET based sensor has lower power consumption at the expense of range and resolution. However, a more recent temperature sensor based in a dynamic threshold MOSFET (DTMOS) reports higher accuracy compared to the conventional MOSFET based sensor [16]. In a similar way, the BJT sensor (figure 2) in a DTMOS temperature sensor 2 diodes configuration DTMOS produces a PTAT $\Delta_{V_{GS}} = V_T ln(\rho)$ that is digitized through ADC and it reports a very high resolution 63m°C with a sub μW of power consumption [15].

2.5 State of art comparison

Table 1 shows some state of the art temperature sensors that employ different types of sensing elements. The sensor [6] employs a BJT sensing element to improve resolution and variation tolerance. The sensor employs multiple BJT transistor pairs distributed around the hots spots in the chip. The current ratio between BJT pairs is controlled by a programmable current source and for the digital conversion a 2nd order $\Sigma\Delta ADC$ is used.

The temperature sensor [18] combines two different resistors with a new 2 NMOS sensing element to generate a PTAT and reference current. In the analog to digital conversion it employs a time-domain digital converter. Also, by avoiding the use of a bandgap reference, an ultra low power operation is achieved.

The work in [17] presents a resistor-based CMOS temperature sensor. The reference and the PTAT voltages are derived directly from the resistor without using bandgap references. The PTAT voltage is digitized through 9-bit BGR-free successive approximation ADC.

The sensor [12] uses n^+-diffusion resistors like heather and a stack of 20 p^+-diffusion /aluminium thermocouples. The temperature-dependent phase shift is digitized by a $PD\Sigma\Delta M$. Since the temperature information is in the time domain, leakage currents do not introduce significant errors. Also as a result of this, the temperature range is the widest possible in a full CMOS temperature sensor.

Temperature sensor in CMOS				
Parameters	[6]	[18]	[17]	[12]
Technology	0.32μm	0.18μm	0.18μm	0.7μm
Type	BJT	MOSFET	RESISTOR	ETF
Area	0.02mm^2	0.09mm^2	0.18mm^2	0.5mm^2
Supply Voltage	1.05V	1.2 V	1.2-2V	5V
Range	-10-110ºC	0-100ºC	0-100ºC	-55-160ºC
Resolution	0.45ºC	0.3ºC	0.1ºC	0.03ºC
Inaccuracy	5ºC	3-1.6ºC	0.5ºC	1ºC
Conversion time	1ms	30ms	12.5 μ s	3030 ms
Power	1.6mW	71nW	40μW	5mW
Energy/conversion	1.6μJ	2.2nJ	0.5nJ	1.5mJ
Application	Microprocessor thermal management	Wireless sensor nodes	General purpose	High temperatures sensor

Table 1: Temperature sensors with different sensing elements

After analyzing different types of CMOS temperature sensors, MOSFET based temperature sensors report the lowest power consumption. Low power operation sensors use time-domain analog to digital converters (ADC). In this configuration, the temperature sensor tracks the changes in a delay line generated by thermal effects. The temperature is obtained after comparing it with an insensitive to temperature clock reference. For the reference an external clock signal can be used [19] or it can be implemented on-chip [30].

3 Methodology

In this work the temperature sensor is based on the low power temperature sensor topology proposed by [18] and implemented using the TSMC 180 nm process. To reduce current consumption this topology uses a new sensing element instead of the conventional band-gap references. Additionally, the PTAT and the reference signal are generated by the same circuit without external references.

The proposed topology of figure 5 is composed of three main blocks: the temperature sensing block, a current to frequency converter, and a frequency to digital converter.

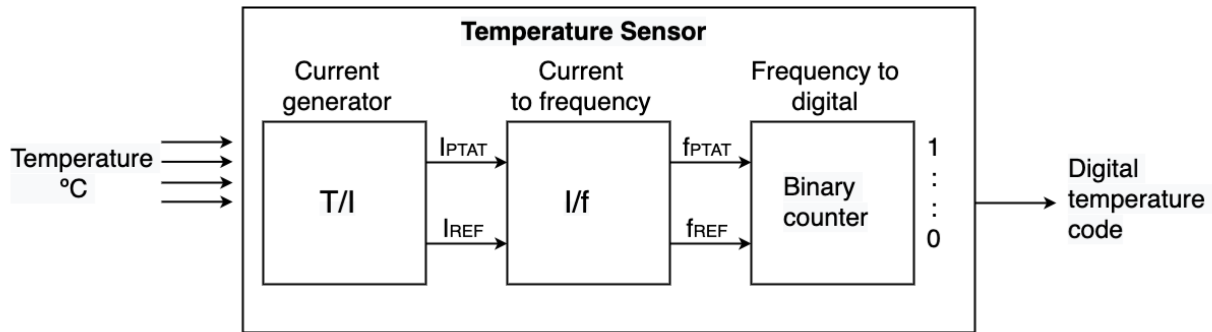


Figure 5: Temperature sensor block diagram [18].

The sensing block converts temperature into current variations, here a reference and PTAT currents are generated. These two currents feed a current controlled ring oscillator, where dependent/independent to temperature frequencies are generated. The last block consists of a couple of asynchronous counters that converts these two frequencies into a digital output temperature code.

3.1 Temperature sensing block

The temperature sensing block is based on a conventional voltage to current converter, shown in figure 6. In this configuration the voltage output of the sensor V_{sense} is applied to the resistor terminals, generating a current I_R that is modeled by the Ohm's law.

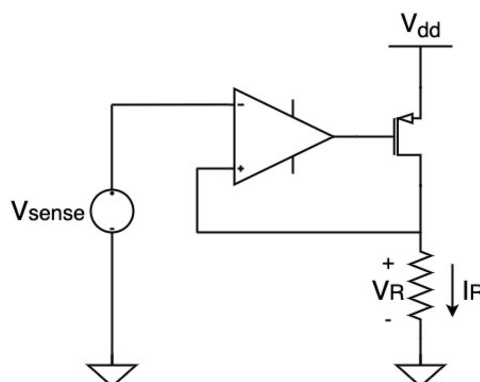


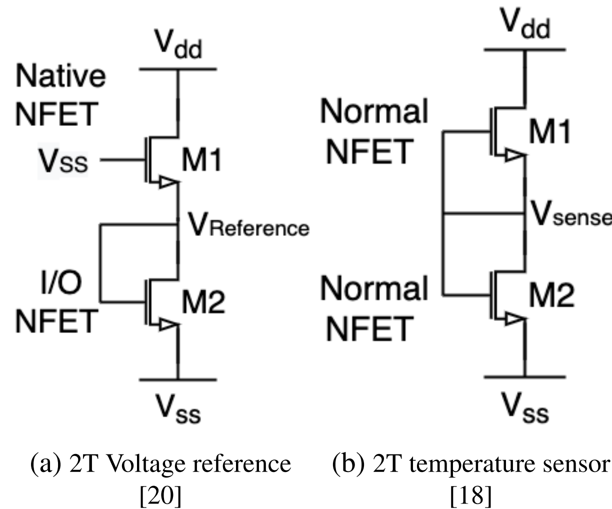
Figure 6: Voltage to current Converter.

According to equation 7, in order to obtain a current in the nA range, a low voltage $Vsense$ or a high resistance R is required. For example in the BJT temperature sensor, a BGR voltage reference produces approximately 1 V. If a current lower than $100nA$ is needed, then a very big resistor ($R \geq 10M\Omega$) would be required, which would be impractical in regards to the silicon area.

$$I_R = \frac{V_{sense}}{R} \tag{7}$$

3.1.1 Temperature sensing element

To achieve a lower current consumption without incurring area penalties, the new sensing element based on MOSFET leakage current, in figure 7b is used [20]. This new sensor provides a PTAT voltage in the $100mV$ range with only a few pW of current consumption. This new sensing element is based in the 2T voltage reference, as in figure 7a [20]. The 2T voltage reference combines two types of transistors with very different threshold voltages ($V_{th2} \gg V_{th1}$) to generate a voltage reference insensitive to temperature.



(a) 2T Voltage reference [20] (b) 2T temperature sensor [18]

Figure 7: 2T voltage reference and temperature sensor

In figure 7a, the analytical solution of $V_{Reference}$ is obtained by equating the sub threshold current (equation 8) at M1 and M2 transistors [20].

$$I_{Sub} = \mu C_{ox}\frac{W}{L}(m-1)V_T^2 e^{(\frac{V_{gs}-V_{th}}{mV_T})}(1-e^{\frac{-V_{ds}}{V_T}}) \tag{8}$$

$$V_{Reference} = \frac{m_1 m_2 (V_{th2}-V_{th1})}{m_1+m_2} + \frac{m_1 m_2}{m_1+m_2} V_T \ln\left(\frac{\mu_1 C_{ox1} W_1 L_2}{\mu_2 C_{ox2} W_2 L_1}\right) \tag{9}$$

Where μ is the mobility, C_{ox} is the oxide capacitance, W and L are the transistor width and length respectively, m is the subthreshold slope factor, V_T is the thermal voltage, V_{gs} is the gate-source voltage, V_{th} is the threshold voltage and V_{ds} is the drain-source voltage.

The equation 9 has two main components: the threshold voltage with CTAT behavior [21], and the thermal voltage V_T with PTAT characteristic. With appropriate M1 and M2 transistor sizes, the thermal effects of these two terms of the equation 9 can cancel each other out or else be maximized to increase the temperature dependence in order to obtain a temperature sensor, as in this work.

From a practical point of view, the use of transistors with different threshold voltages implies that the output voltage is too susceptible to process variations, which would result in linearity degradation and sensing errors. To avoid this problem, two transistors of the same type were used to implement the 2T temperature sensor, as shown in figure 7b.

The output voltage of the temperature sensor V_{sense} in figure 7b is modeled by the subthreshold current equation with body and drain-induced barrier lowering (DIBL) effect (equation 10) [22].

$$I = \mu_0 C_{ox}\left(\frac{W}{L}\right)V_T^2 e^{1.8} e^{\frac{-\Delta V_{th}}{\eta V_T}} \times e^{\frac{1}{mV_T}(V_{gs}-V_{th0}-\gamma' V_{sb}+\eta V_{ds})} \times \left(1-e^{\frac{-V_{ds}}{V_T}}\right) \tag{10}$$

Where V_{th0} is the threshold voltage at zero bias, $V_T = kT/q$ is the thermal voltage, γ' is the linearized body effect coefficient, η is the drain induced barrier lowering (DIBL) coefficient, C_{ox} is the gate oxide capacitance, μ_0 is the zero bias mobility, m is the sub-threshold slope coefficient and ΔV_{TH} is a term introduced to account for the transistor to transistor leakage variations. Considering $V_{sense} \gg V_T$ and the negligible DIBL effect due to the use of long devices ($\eta V_{ds} \approx 0$), the current at M1 and M2 result as follows:

$$I_1 = \mu_1 C_{ox1}\left(\frac{W_1}{L_1}\right)V_T^2 e^{1.8} e^{\frac{-\Delta V_{th1}}{\eta V_T}} \times e^{\frac{1}{m_1 V_T}(0-V_{th1}-\gamma_1' V_{sense})} \tag{11}$$

$$I_2 = \mu_2 C_{ox2}\left(\frac{W_2}{L_2}\right)V_T^2 e^{1.8} e^{\frac{-\Delta V_{th2}}{\eta V_T}} \times e^{\frac{1}{m_2 V_T}(V_{sense}-V_{th2}-\gamma_2' 0)} \tag{12}$$

Equating I_1 and I_2 currents and given that M1 and M2 are the same type of transistor, $V_{th1} \approx V_{th2}$, $m_1 \approx m_2$ and assuming $V_{ds} \gg 3V_T$, $e^{\frac{-V_{ds}}{V_T}} \approx 0$, the output voltage of the sensing element can be approximated by the equation 13 [18].

$$V_{sense} = \frac{m_1 m_2}{m_1 + \gamma_1' m_2} V_T \ln\left(\frac{\mu_1 C_{ox1} W_1 L_2}{\mu_2 C_{ox2} W_2 L_1}\right) \tag{13}$$

By comparing equations 9 and 13 it is possible to appreciate how the threshold voltage dependency is canceled out and by connecting the gate of the M1 transistor to the output V_{sense}, a higher sensitivity is achieved.

A 2T sensor was implemented using a standard threshold voltage NMOS transistor. Although the V_{sense} equation has a first-order temperature dependency, the results obtained after simulations (figure 8) suggest a second-order temperature dependence. Nevertheless, the second-order trend is canceled out if the sensor is designed in such a way that $W_1 L_2 \gg W_2 L_1$. After fulfilling this condition, the sensor response can be approximated by a linear model.

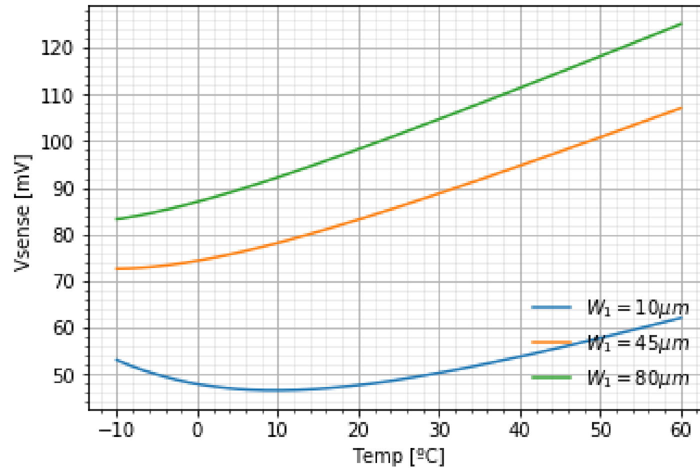
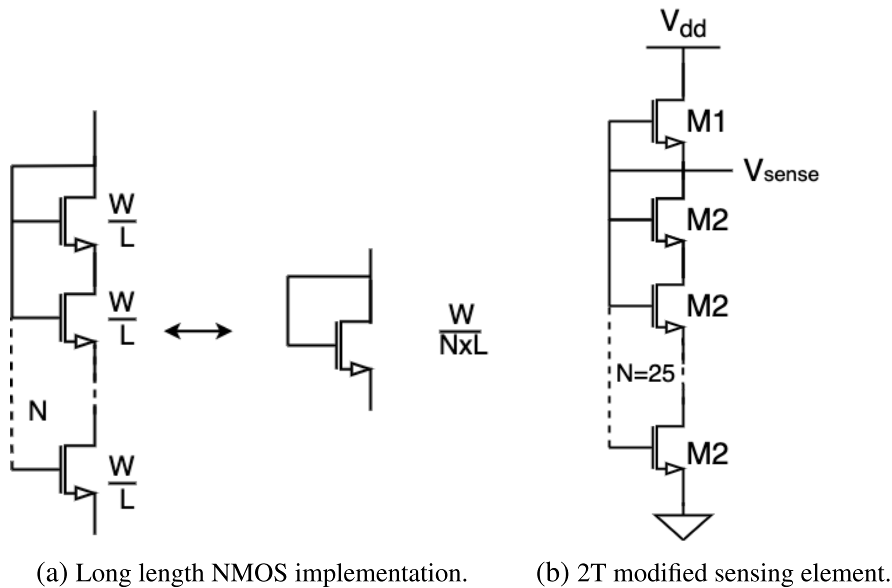


Figure 8: Transistor sizes impact in linearity.

There are some physical aspects in respect to the condition $W_1L_2 \gg W_2L_1$. For example, in the original implementation, the sensor used to generate the reference current required transistors with a very asymmetrical aspect ratio ($(W/L)_{M1} = 200/0.5$ and $(W/L)_{M2} = 0.5/19$), which resulted in a very area-inefficient and poor matching design. Then instead of using a wider M1 transistor and a long transistor M2, N-equal M2 devices were used to implement a long L MOSFET transistor [23].



(a) Long length NMOS implementation. (b) 2T modified sensing element.

Figure 9: 2T sensor long length implementation

By using N-equal $M2$ transistors, the equation 13 is rewritten as follows:

$$V_{sense} = \frac{m_1 m_2}{m_1 + \gamma_1' m_2} V_T \ln\left(\frac{\mu_1 C_{ox1} W_1 \times N L_2}{\mu_2 C_{ox2} W_2 L_1}\right) \quad (14)$$

3.1.2 Current generation

The current generation is based on the voltage to current converter in figure 6 and consists of a negative feedback loop formed by an operational amplifier, a PMOS transistor, and a resistor. The circuit copies the output voltage of the sensing element and applies it across the resistor. The 60dB open-loop gain of the amplifier ensures that the output voltage of the sensing element is copied through the resistor with low error.

To reduce the current consumption the operational amplifier works in the sub-threshold region and reports a current consumption around 45 nA at room temperature (simulated results). Additionally, two current mirrors are required to obtain the control voltages VH and VL used to control the ring oscillator in the current to frequency converter stage.

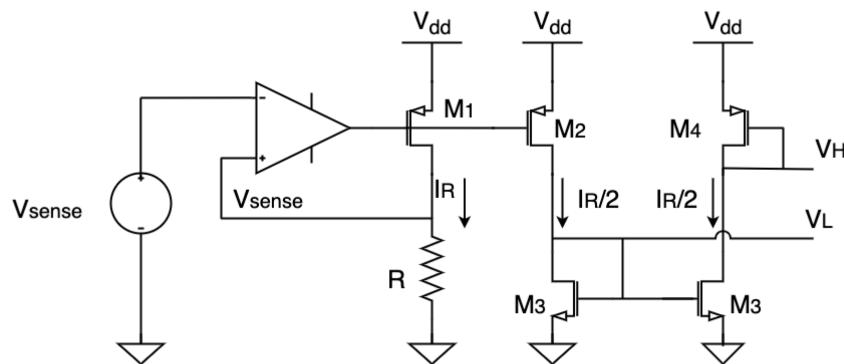


Figure 10: Current generation circuit.

The first current mirror M1-M2 divides I_R current in half in order to reduce the frequency at the oscillators by the same factor without increasing the resistor value. As a result, dynamic power consumption in the binary counters is reduced. The second current mirror allows the inclusion of the diode-connected transistors M3 and M4, this structure ensures that transistors M3 and M4 are saturated. The control voltages VH and VL are generated by M3 and M4 transistors rather than M1 and M3 transistors in order to avoid large loading in the OpAmp output. This enhances the phase margin and the bandwidth, and also relaxes the output voltage swing by biasing the OpAmp output away from the power supply levels [18].

3.1.3 Reference and PTAT current generation

A temperature insensitive reference current I_{REF} and a PTAT current I_{PTAT} are generated by two sets of the current generation circuit of figure 10. Each circuit uses two different types of resistors combined with two different 2T temperature sensing elements. The temperature sensing element is sized after the thermal characterization of the resistor.

To simplify the current analysis, once the linearity condition is fulfilled the sensor response is approximated by a first-order temperature model. The resistor model provided by the process documentation considers thermal and voltage effects $R(T,V) = R_0(1+\alpha_{R1}T+\alpha_{R2}T^2)(1+\alpha_{V1}V+\alpha_{V2}V^2)$[24]. However, since the sensor voltage is in the range of 100mV, the voltage contribution is not taking in to account $(1+\alpha_{V1}V+\alpha_{V2}V^2 \approx 1)$. After this simplification, the

V_{sense} and $R(T)$ is modeled as follows:

$$V_{sense} = V_0(1+\alpha_{V1}T) \tag{15}$$

$$R(T) = R_0(1+\alpha_{R1}T+\alpha_{R2}T^2) \tag{16}$$

Where V_0 is the voltage at 0ºC, α_{V1} is the first-order temperature coefficient of the sensing element given by the slope of the equation 13, R_0 is the resistor value at 0ºC, α_{R1} and α_{R2} are the first and second-order temperature coefficients of the resistor and T is the temperature.

Combining equations 15 and 16 according to the Ohms law, the current through the resistor I_R results in:

$$\begin{aligned} I_R = \frac{V_{sense}}{R} &= \frac{V_0(1+\alpha_{V1}T)}{R_0(1+\alpha_{R1}T+\alpha_{R2}T^2)} \\ &= \frac{V_0}{R_0}\Big(\frac{1+\alpha_{V1}T}{1+\alpha_{R1}T+\alpha_{R2}T^2}\Big) \\ &= I_0\Big(\frac{1+\alpha_{V1}T}{1+\alpha_{R1}T+\alpha_{R2}T^2}\Big) \end{aligned} \tag{17}$$

After second-order Taylor's series approximation, I_R results:

$$\begin{aligned} I_R &= I_0\Big(1+(\alpha_{V1}-\alpha_{R1})T+(\alpha_{R1}^2-\alpha_{R1}\alpha_{V1}-\alpha_{R2})T^2\Big) \\ I_R &= I_0(1+\alpha_{I1}T+\alpha_{I2}T^2) \end{aligned} \tag{18}$$

With first order α_{I1} and second order α_{I2} coefficients:

$$\alpha_{I1} = \alpha_{V1} - \alpha_{R1} \tag{19}$$

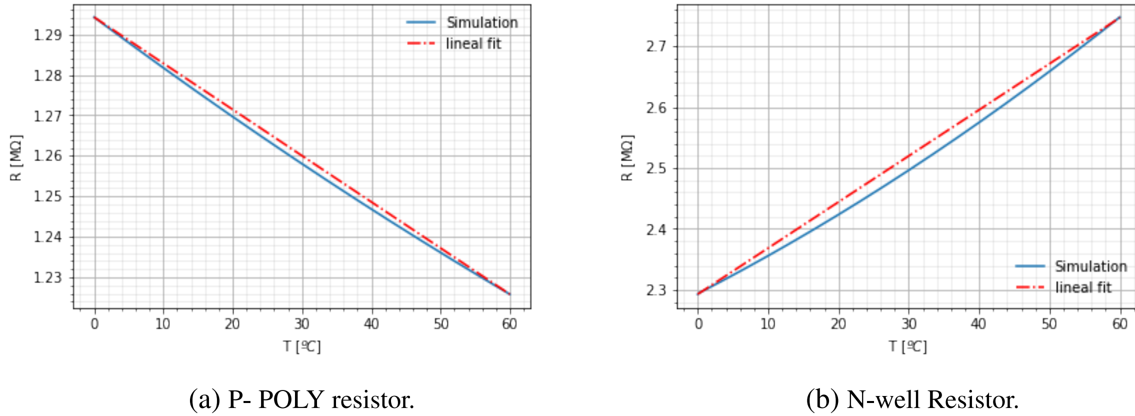
$$\alpha_{I2} = \alpha_{R1}^2 - \alpha_{R1}\alpha_{V1} - \alpha_{R2} \tag{20}$$

Due to the intrinsic PTAT characteristic of the sensing element, α_{V1} is positive. Then to increase the temperature dependence of I_R, according to the equation 17, a resistor with CTAT characteristic $(-\alpha_{R1})$ is required to increase the thermal dependence in the I_{PTAT} current. For example when the temperature increases, V_{sense} also increases, while R decreases $\big(\frac{V_{sense}\uparrow}{R\downarrow} \implies I_R\uparrow\big)$. Thus the quotient between these two values increases.

To generate an insensitive to temperature reference current, a resistor with a positive α_{R1} is used. The sensing element is sized to match with the temperature coefficient of the resistor. As a consequence, if ($\alpha_{V1} = \alpha_{R1} \implies \alpha_{I1} = 0$), then an insensitive to temperature current I_R is achieved.

The CMOS process used in this work has some resistor models with the characteristics mentioned above. For the I_{REF} and I_{PTAT} current generation, a N-well and high-resistance implant (HRI) P-POLY resistors were used respectively. Although there are more resistors with PTAT and CTAT characteristics, these resistors were chosen due to their high sheet resistance, ($R_{sh} \approx 1K\Omega$), which allows implementation of large resistors without excessive use of silicon area. The resistor used in the PTAT current circuit was implemented with 40 series-connected resistors, with a total resistance of $R = 1.29M\Omega$. The resistor used in the reference current

circuit was implemented with 25 series-connected resistors and report a total resistance of $R = 2.29M\Omega$.



(a) P- POLY resistor.

(b) N-well Resistor.

Figure 11: Resistor Thermal response.

The thermal characterization of the resistors was performed by applying a constant voltage to its terminals with a DC sweep using temperature as a variable. The parameters R_0 and α_{R1} were obtained after a simulation, according to equation 21.

$$\alpha_{R1} \approx \frac{\Delta R}{R(0) \times \Delta T} \tag{21}$$

Where $R(0)$ is the resistor value at 0ºC, ΔR is the resistor increment in the temperature range ΔT. Since the current behavior is linear, the second-order temperature coefficient α_{R2} was obtained after simulation analysis by polynomial curve fitting using python. The parameters of the resistor model are summarized in table 2.

Resistor type	$R_0[M\Omega]$	α_{R1}	α_{R2}
P- POLY resistor	$1.294M\Omega$	-9.3×10^{-4}	1.707×10^{-6}
N-well	$2.293M\Omega$	3.31×10^{-3}	1.177×10^{-5}

Table 2: Resistor model parameters

Comparing the values obtained in table 2 with values provided by the process documentation [24], the coefficient α_{R1} reports an increment around 10%. These variations are due to the simplified model of the resistor (equation 16), which does not take into account the voltage modulation and other non-linear effects like self-heating, high-field velocity saturation, and depletion region encroachment [25].

Although both resistors have linear behavior, the linearity error in the N-well resistor (figure 11b) is bigger than the linearity error in the P-POLY resistor (figure 11a). This is because the

α_{R2} coefficient in the N-well resistor is approximately 10-times bigger than P-POLY resistor. This produces a second-order effect on the thermal response of the N-well resistor.

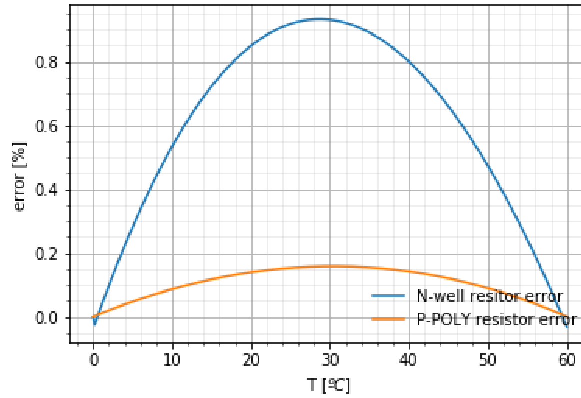
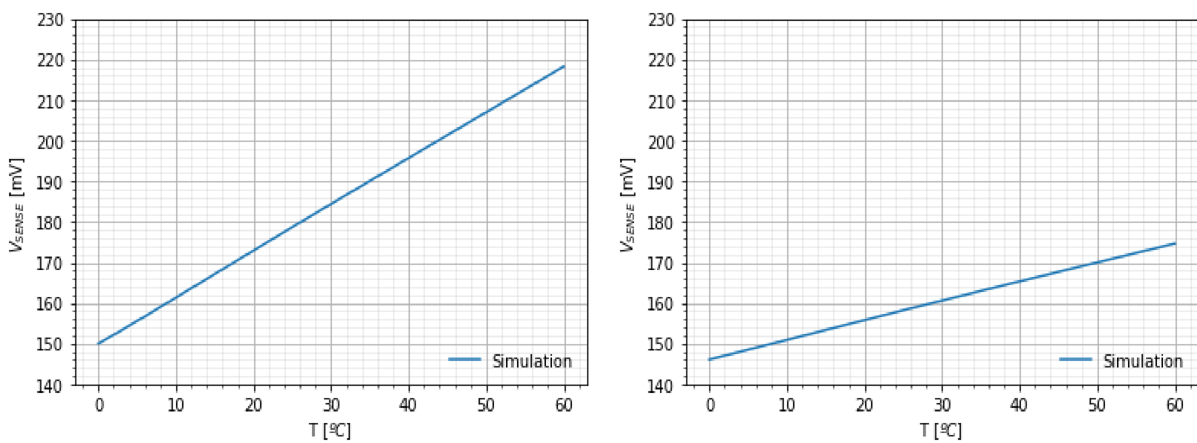


Figure 12: Resistor relative linearity error.

Figure 12 depicts the relative error due to the non-linear response of the resistors. The maximum error is in $T \approx 30ºC$ and corresponds to an approximate value of $\approx 0.9\%$. The R^2 correlation coefficient in N-well and P-POLY resistor are 0.998467 and -0.999547 respectively. As expected, a lower correlation coefficient value in the N-well resistor reflects the lower linearity of this resistance.

The two 2T sensors in figure 13 have a PTAT behavior with a different slope. The linearity error in figure 14 is minimum compared with the resistor's errors (figure 12). This is reflected in the correlation coefficient R^2 of the 2T-sensor used in the PTAT and reference current circuits that are 0.999983 and 0.999951 respectively.



(a) Thermal response of the 2T-sensor used in the PTAT current circuit

(b) Thermal response of the 2T-sensor used in the reference current circuit

Figure 13: Sensing element thermal response

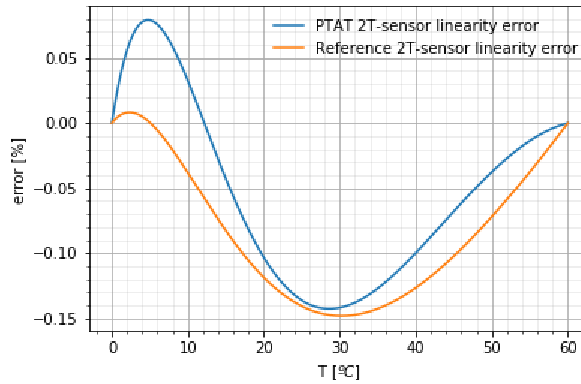


Figure 14: 2T-sensor relative linearity error.

The sensing element used in reference current generation circuit was specially sized to fit with the α_{R1} coefficient of the N-well resistor in order to eliminate the first-order temperature dependence in equation 18. While on the contrary, the sensing element in the PTAT current generation circuit was sized to increase the first order α_{I1} coefficient in equation 18.

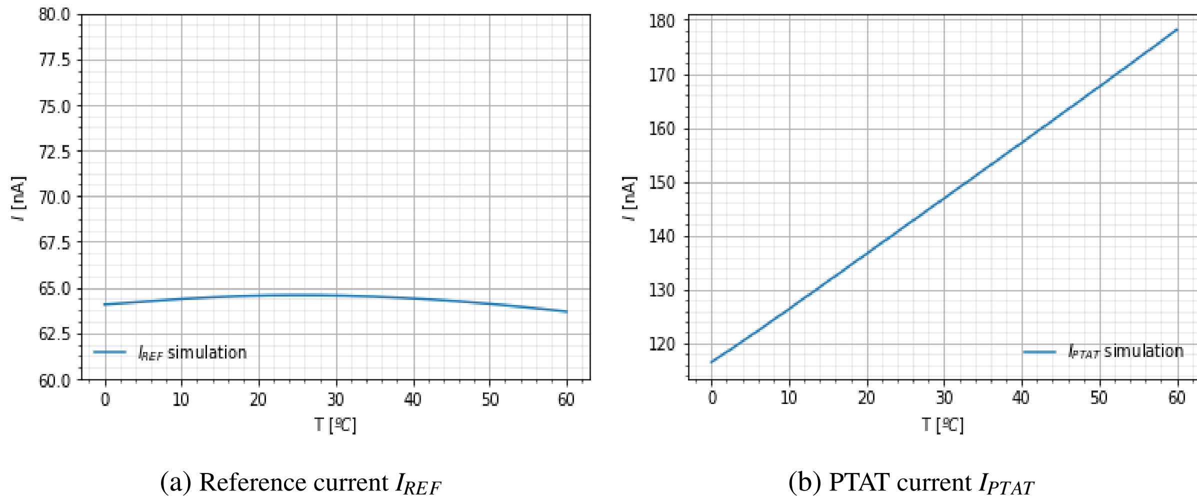
Figure 13a depicts the sensor output (V_{sense}) of one of the 2T temperature sensor used in the PTAT current circuit. Figure 13b corresponds to the sensor output of the second 2T temperature sensor used in the reference current circuit. The temperature parameters of both 2T temperature sensors are presented in table 3, and was obtained in the same way as the resistors (equation 21).

Sensing Element	$V_0[mV]$	α_{V1}
2T sensing element I_{PTAT}	$150mV$	7.57×10^{-3}
2T sensing element I_{REF}	$146mV$	3.308×10^{-3}

Table 3: Sensing element model parameters

After combining the parameters from tables 2 and 3 in equation 18, the resulting parameters model of the reference current I_{REF} are $I_0 = 63.7nA$, $\alpha_{I1} = 2 \times 10^{-6}/°C$ and $\alpha_{I2} = -11.7 \times 10^{-6}/°C^2$. Whereas the I_{PTAT} current parameters model are $I_0 = 115.9nA$, $\alpha_{I1} = 8.5 \times 10^{-3}/°C$ and $\alpha_{I2} = 6.19 \times 10^{-6}/°C^2$.

As can be seen in figure 15a, I_{REF} current is not constant and has second-order behavior, this is because the coefficients α_{I1} and α_{I2} are very similar to each other. According to equation 20, the linearity in the current I_{REF} can be improved if another resistor type with a lower coefficient α_{I2} is used. (for example rnwod or rpodwo resistor). However, if it is compared with the I_{PTAT} current (figure 16) does not have a significant variation and can be considered as constant.



(a) Reference current I_{REF}

(b) PTAT current I_{PTAT}

Figure 15: Sensing element thermal response

Additionally, I_{REF} and I_{PTAT} were reduced through the current mirror in figure 10 for two main reasons. The first is to reduce the frequency in the ring oscillator stage in order to save dynamic power consumption in the digital part. The second reason is to create the VH and VL signals that control the current controlled ring oscillator.

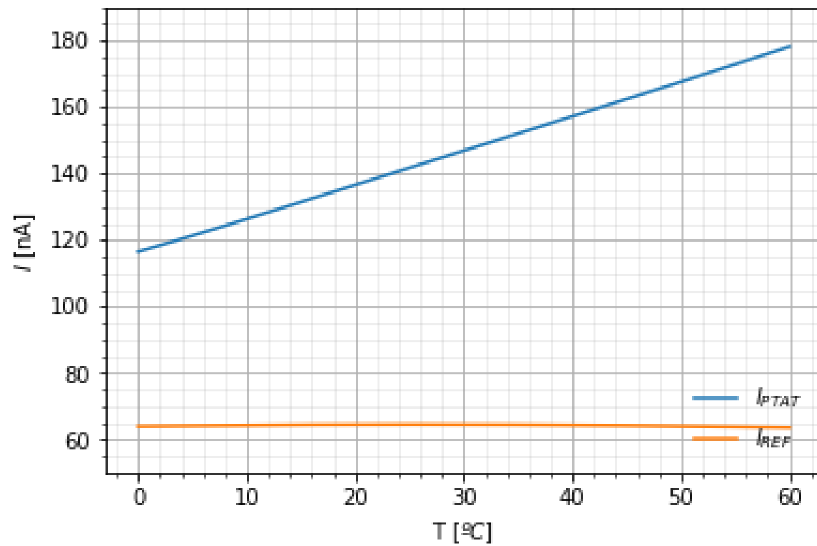
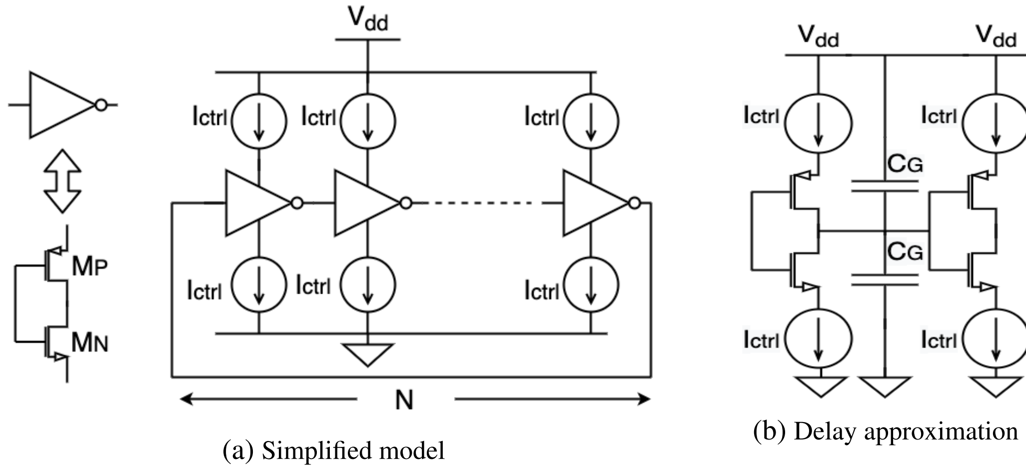


Figure 16: I_{PTAT} and I_{REF} Currents.

3.2 Frequency generation

The I_{PTAT} and I_{REF} currents are converted into frequencies by the current to frequency conversion stage through the current starved voltage controlled oscillator (VCO). A current starved

VCO consists of a string of N-inverters (N is odd number) where the oscillation frequency is controlled by the current through each inverter.



(a) Simplified model

(b) Delay approximation

Figure 17: Voltage controlled ring oscillator

In a VCO ring oscillator the oscillation frequency is given by [28].

$$f_{osc} = \frac{1}{2N\tau} \tag{22}$$

Where τ is the delay of each inverter stage, N is the number of stages. From the equivalent circuit of the figure 17b the delay and voltage in a single stage is given by:

$$V_{osc} = \int \frac{I_{ctrl}}{C_G} dt \tag{23}$$

$$\tau = \frac{V_{osc} C_G}{I_{ctrl}} \tag{24}$$

Where V_{osc} is the oscillation amplitude and C_G is the total parasitic capacitance that takes into account the input and output parasitic contribution of the inverters, then after combining equations 24 and 22, the oscillation frequency results as follows:

$$f_{osc} = \frac{I_{ctrl}}{2NV_{osc}C_G} \tag{25}$$

In equation 25 the oscillation frequency is determined by I_{ctrl}, the number of stages N, the amplitude of oscillation V_{osc} and the total parasitic capacitance C_G. Once the number of stages is fixed and the inverters are sized, the oscillation frequency can be controlled by the I_{ctrl} current.

By implementing a current reference I_{CTRL} and M_C transistor, the current starved VCO becomes current-controlled VCO. Transistors M_P and M_N operate as inverters, transistors M_1 and M_2 work like a sink and source current respectively [26]. In this configuration, a wide oscillation frequency range can be tuned by the control current. Nevertheless, its main drawback is that for

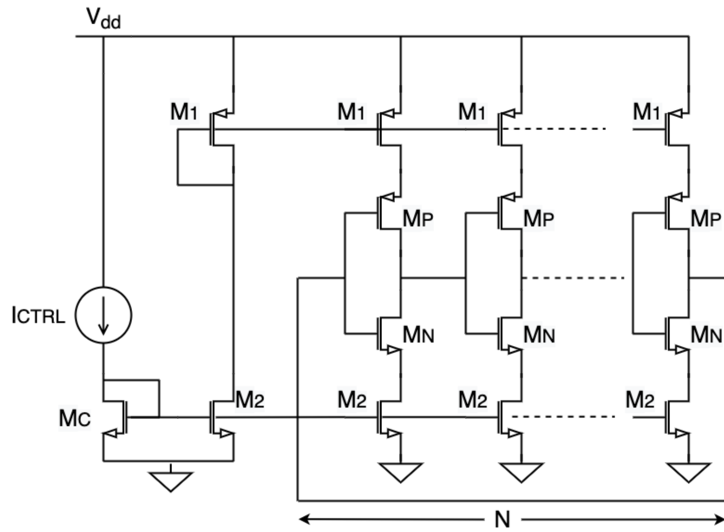


Figure 18: Current starved VCO [27]

low I_{CTRL}, the voltage swing of the oscillator is also small. This condition makes it unsuitable for low power applications [28].

To avoid the use of a large I_{CTRL} current, the transmission gate based (TG) ring VCO in figure 20 is used instead of the current starved VCO. In this TG-based VCO, a variable resistor implemented with transmission gates transistors is used to control the delay of each inverter stage. The delay of each stage is estimated by the equivalent RC circuit in figure 19. The CMOS inverter is modeled by a $1/G_M$ resistance, the transmission gate resistor is R_V, and the total parasitic capacitance like C_G, with these simplifications the delay τ_2, is obtained as follows:

$$\tau_2 = \frac{C_G(1+G_M R_V)}{G_M} \tag{26}$$

After combining equation 26 with equation 22, the oscillation frequency of the transmission gate VCO results in:

$$f_{osc} = \frac{G_M}{2NC_G(1+G_M R_V)} \tag{27}$$

The equivalent resistance of the transmission gate R_V is the average between V_{DS}/I_{DS} during a switching event and is approximated by equation 28 [29].

$$R_V = \frac{ln2}{\frac{V_{DD}}{2}} \int_{\frac{V_{DD}}{2}}^{V_{DD}} \frac{V}{I_{DS}} dV \approx \frac{V_{DD}}{2I_{DS}} \tag{28}$$

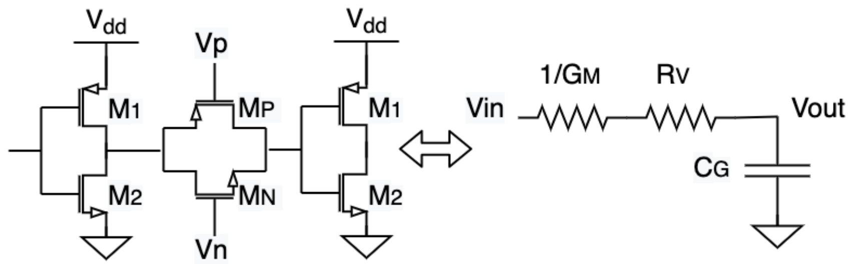


Figure 19: Delay approx single delay stage [28].

Finally, after replacing equation 28 and assuming $G_M R_V \gg 1$, the oscillation frequency results in the next expression [18].

$$f_{osc} \approx \frac{I_{DS}}{NC_G V_{DD}} \tag{29}$$

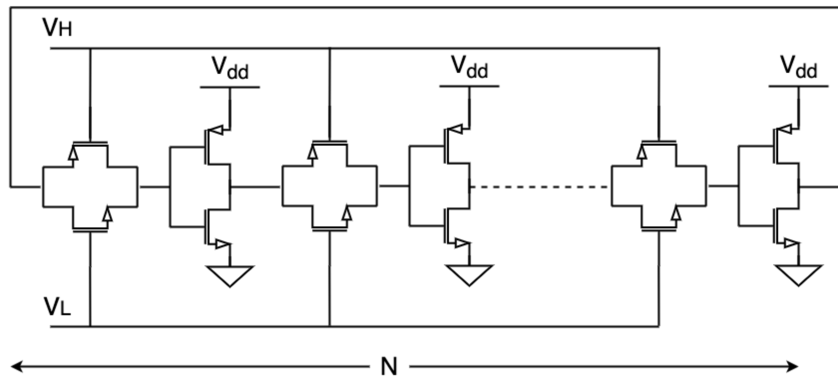


Figure 20: Transmission gate based voltage controlled ring oscillator [28].

The transmission gate are connected to VH and VL voltages, as a consequence the current I_{DS} tracks the I_{REF} and I_{PTAT} currents from the previous stage. As a result, the two-oscillator generates a reference frequency (f_{REF}) and PTAT frequency (f_{PTAT}).

Finally, a three-stage ring oscillator was implemented. NAND gate is used in the first stage in order to prevent unnecessary oscillation. The control voltages VH and VL come from the generation current stage and are connected to the transmission gates. Since the delay path introduces large rise and fall times, an output buffer is added to avoid an unnecessary short-circuit current in the frequency to digital converter stage.

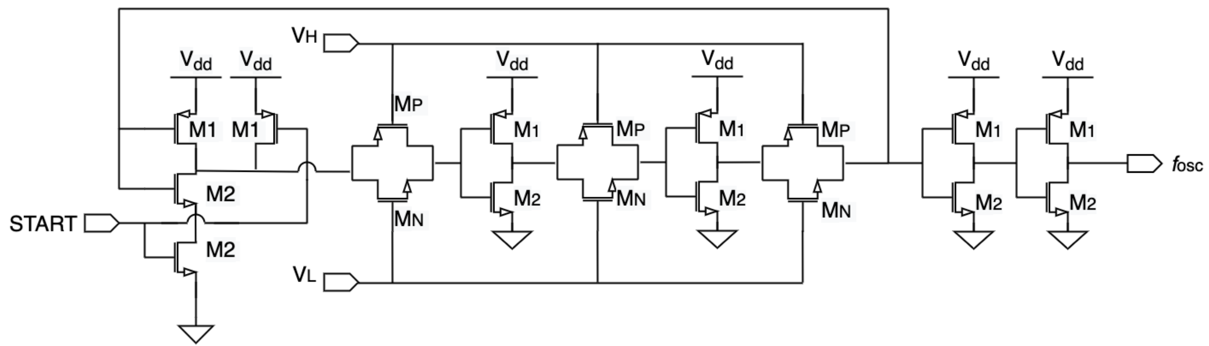


Figure 21: Current to frequency converter.

The current generation circuit (figure 10) is integrated with the current to frequency converter (figure 21), then two different signals f_{REF} and f_{PTAT} are generated. The simulation results in figure 22 show the temperature response frequency. The PTAT frequency, f_{PTAT} has a value between $f_{PTAT}(0°C) = 478KHz$ and $f_{PTAT}(0°C) = 719KHz$ while the reference frequency, f_{REF} has a more or less constant value between $f_{REF}(0°C) = 81.3KHz$ and $f_{REF}(0°C) = 83.5KHz$.

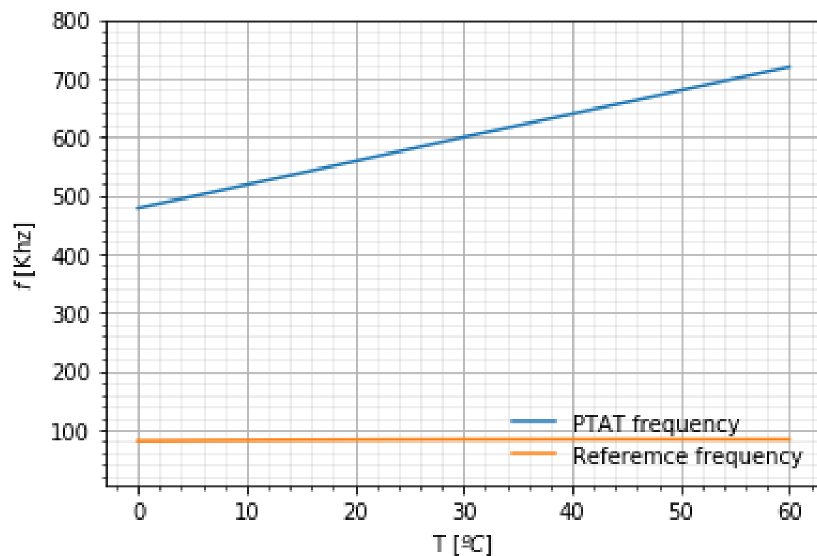


Figure 22: f_{REF} and f_{PTAT} temperature response.

3.3 Frequency to digital conversion

The f_{PTAT} and f_{REF} frequencies are converted into a digital code through a frequency to digital converter, shown in figure 23. The two asynchronous counters translate the f_{PTAT} and f_{REF} frequencies into a digital code. The REF counter is a frequency divider and provides a constant time interval over all the temperature range T_{DONE}. Meanwhile the PTAT counter is fed with the thermal dependent f_{PTAT} frequency. Then the final count of the PTAT counter over T_{DONE} time will also depend on the temperature.

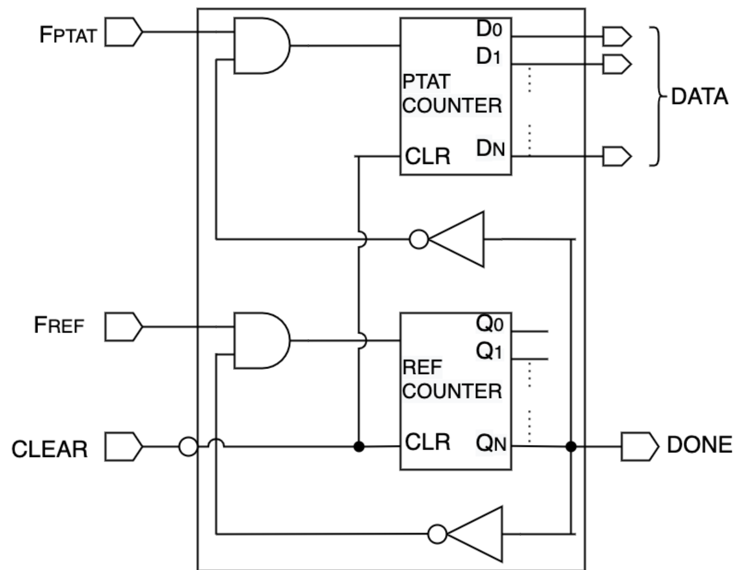


Figure 23: Frequency to digital converter block diagram [18].

When the start signal is activated, the PTAT and reference counters start to count upward simultaneously until Q_7 bit of the reference counter switches to 1, when this happens the count stops and then the output data is ready to be read or saved.

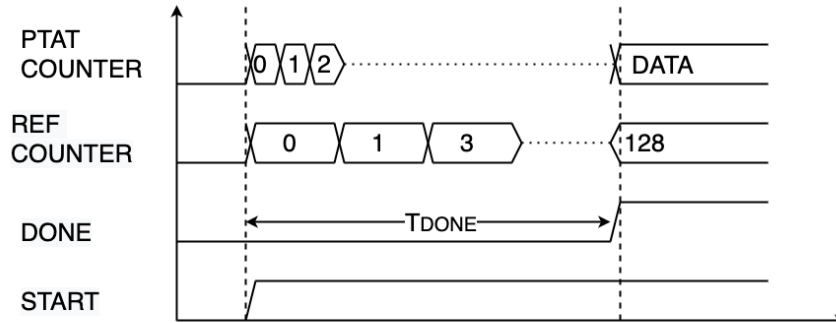


Figure 24: Sensor timing diagram

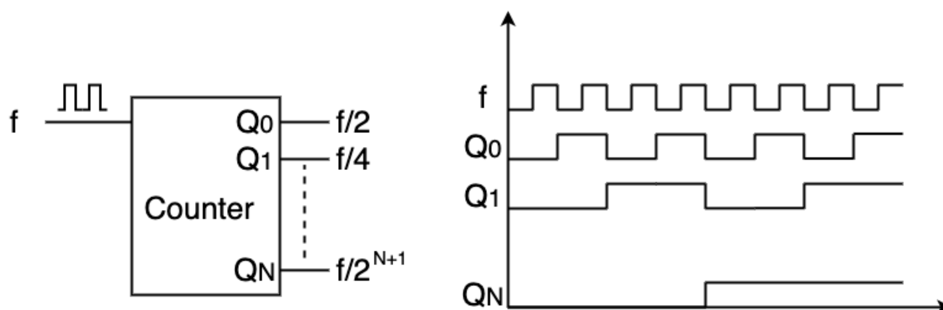


Figure 25: Frequency divider.

As both counters are triggered simultaneously the DATA count obtained after T_{DONE} period is given by the quotient of the T_{DONE} and the period of f_{PTAT}. According to the frequency divider in the figure 25, the output frequency at the Q_N bit of the REF counter is as follows:

$$T_{QN} = \left(\frac{f_{REF}}{2^{N+1}}\right)^{-1} \tag{30}$$

Where N is the Nth-bit output of REF counter, f_{REF} is the reference frequency of the previous stage. Given that T_{DONE} is half of the period of T_{QN}, then T_{DONE} results in the next expression:

$$T_{DONE} = \frac{T_{QN}}{2} = (T_{QN})2^{-1} = \left(\frac{2^{N+1}}{f_{REF}}\right)2^{-1} = \frac{2^N}{f_{REF}} \tag{31}$$

Sensor resolution, T_{res}, is determined by the quotient between the temperature range and the difference of the DATA count obtained in the same temperature range.

$$T_{res} = \frac{\Delta_T}{\Delta_{DATA}} \tag{32}$$

Where $\Delta_T = T_f - T_i$ is the difference between two temperatures and Δ_{DATA} is the difference between the count obtained at temperature T_f and temperature T_i.

$$\Delta_{DATA} = DATA(T_f) - DATA(T_i) \tag{33}$$

The DATA count for a given temperature T is obtained by dividing T_{DONE} (equation 31) by the period of f_{PTAT} as follows:

$$DATA(T) = \frac{T_{DONE}}{T_{PTAT}} = \frac{2^N f_{PTAT}(T)}{f_{REF}(T)} \tag{34}$$

Where T is the temperature, N is the Nth output bit of the REF counter, f_{REF} and f_{PTAT} are the reference and PTAT frequencies respectively. After combining equation 34 and equation 33, the Δ_{DATA} becomes:

$$\Delta_{DATA} = \frac{2^N(f_{PTAT}(T_f) - f_{PTAT}(T_i))}{f_{REF}} \tag{35}$$

The PTAT frequency $f_{PTAT}(T)$ is approximated by a first-order model.

$$f_{PTAT}(T_f) = f_{PTAT}(T_i) + \alpha f_p(T_f - T_i) \tag{36}$$

Where $\alpha f_p = (f_{PTAT}(T_f) - f_{PTAT}(T_i))/(T_f - T_i)$ is the frequency gain of f_{PTAT} oscillator. After replacing in the equation 35, Δ_{DATA} results.

$$\Delta_{DATA} = \frac{2^N(\alpha f_p(T_f - T_i))}{f_{REF}} \tag{37}$$

Finally replacing equation 37 in the equation 32, the sensor resolution, T_{res} is given by the next expression.

$$Tres = \frac{\Delta T}{\Delta_{DATA}} = \frac{f_{REF}}{2^N \alpha f_P} \tag{38}$$

According to equation 38, a higher resolution can be achieved by increasing the frequency gain of the PTAT oscillator αf_P, or the number of bits of the REF counter or by decreasing the reference frequency f_{REF}.

In practice the f_{REF} frequency is not constant and has thermal dependence that affects the resolution of the sensor, which mus be taken into consideration. Then a better approximation of the resolution that includes non-idealities of the reference frequency is given by the equation 39 [30]:

$$Tres = \frac{\Delta T}{\Delta_{DATA}} = \frac{f_{REF}}{2^N(\alpha f_P - \alpha f_R)} \tag{39}$$

Where αf_R is the frequency gain of the reference frequency f_{REF}.

From simulations results in figure 22, the frequency values at the beginning and end of the temperature range are $f_{PTAT}(60ºC) = 719.3KHz$, $f_{PTAT}(0ºC) = 478KHz$, $f_{REF}(0ºC) = 81.3KHz$ with the DONE signal connected at the Q_7 output of the REF counter and ignoring the thermal dependence of f_{REF}, $\alpha f_R \approx 0$, the sensor has a resolution of $\approx 0.158ºC$. But in fact this is the most optimistic approximation because the phase and thermal noise, frequency offset and process mismatch will affect the sensor resolution.

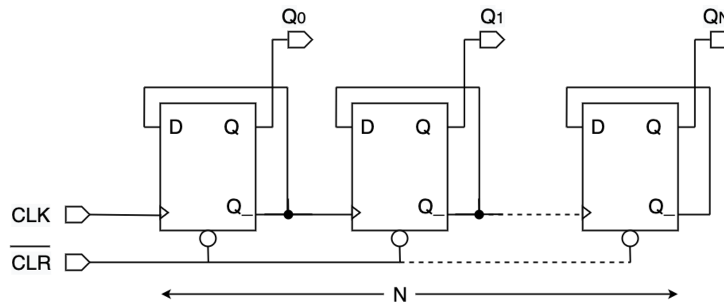


Figure 26: Asynchronous counter

In a synchronous counter, all the flip-flops are connected to the same clock signal that implies dynamic power consumption in every clock cycle. To reduce power consumption PTAT and REF counters are designed asynchronous. According to figure 26, the next bit is triggered by the preceding flip-flop stage. Then the switching activity decreases by a 2^N factor in each posterior stage of the counter, by this way unnecessary switching activity is reduced. For an asynchronous counter with a size larger than 4 bits, the power consumption is reduced by more than 50% compared with an equivalent synchronous counter [31].

The frequency to digital converter was designed with an 8 bit (reference) and 11 bits (PTAT) asynchronous counter in figure 26. Higher resolution can be achieved if the number of bits in the reference counter is increased. The PTAT counter was designed in order to avoid overflow at high temperatures.

Each flip-flop of the counters was implemented using D flip-flops similar to figure 27. Additionally D-FF incorporates asynchronous set and clear inputs to synchronize the data acquisition.

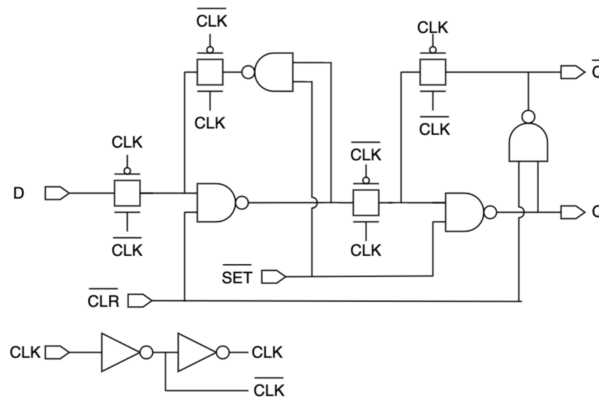


Figure 27: Transmission gate based D-FF

3.4 Component values and transistor sizing

3.4.1 Current generator design

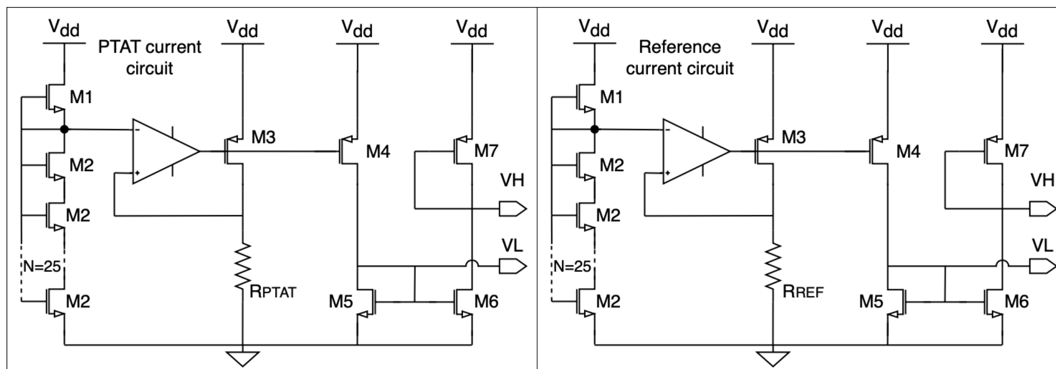


Figure 28: PTAT and reference current circuits.

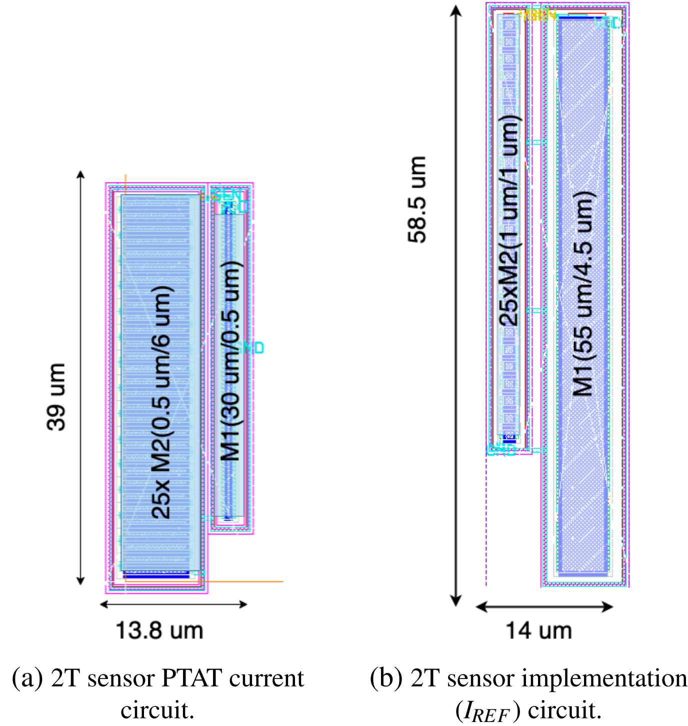
The PTAT and reference current generation circuits in figure 28 were implemented combining two different 2T-sensing elements with R_{PTAT} and R_{REF} resistors. The 2T-sensing element of the PTAT and reference current circuit were sized to match with the first-order temperature coefficient α_{R1}, of the high-resistance implant (HRI) POLY-resistor and N-well resistors respectively.

Although the transistor of the 2T-sensing element can be sized according to equation 14, the subthreshold slope (m) and the body coefficient (γ_1') are not directly provided by the process documentation [24] and require extra simulation steps to obtain them. Instead, the first-order temperature coefficient of the 2T-sensing element was measured in the same way as the resistors (equation 21).

$$\alpha_{V1} \approx \frac{\Delta V}{V_{sense}(0°C) \times \Delta T}$$

To simplify the design, the parameters of the equation 14, N, W_2, L_2 and W_1 were fixed. The last parameter L_1 was obtained by parametric analysis simulation until the first-order temperature

coefficient α_{V1} matched with α_{R1} coefficient of the HRI POLY-resistor and the N-well resistor in table2.



(a) 2T sensor PTAT current circuit.

(b) 2T sensor implementation (I_{REF}) circuit.

Figure 29: 2T sensor Reference current circuit.

Transistors $M3$ and $M4$ were sized to allow the replication of a current 5 times smaller than them. To improve the current matching, multiple fingered transistors were used. The number of fingers of M3 transistor was set to 10, and the aspect ratio $(W/L)_3 = 10 \times (4/2)$. The aspect ratio of the M4 transistor was sized according to the MOSFET current mirror equation [32].

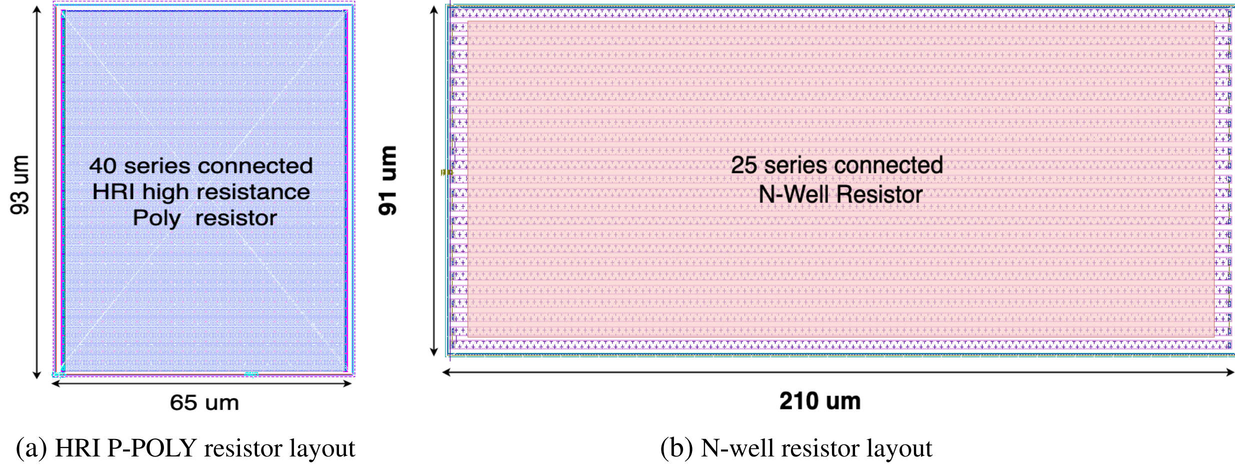
$$I_{copy} = \frac{(W/L)_4}{(W/L)_3} I_{REF} \tag{40}$$

With $I_{copy} = I_{REF}/5$ and $(W/L)_3 = 10 \times (4/2)$ in the equation 40, results in an aspect ratio of $(W/L)_4 = 2 \times (4/2)$. Transistor M5 was sized $L_5 > W_5$ to provide a voltage $VL \approx 300mV$. Transistor M6 has the same aspect ratio as M5 in order to have the same current in both branches. Transistor M7 was sized $L_7 > W_7$ to obtain a voltage $VH \approx 700mV$. The resistor was implemented with 25 series N-well resistors under STI with a total resistance $R_{REF} \approx 2.45M\Omega$.

The PTAT current circuit was sized in the same way as the reference circuit. The main difference in respect to the previous circuit, is that the number of fingers in the transistor M4 was set to 6. The $R_{PTAT} \approx 1.26M\Omega$ implemented with an HRI high resistance poly resistor, and M6 and M7 transistors were sized to obtain a $VL \approx 400mV$ and $VH \approx 600mV$ respectively.

The left side of figures 29a and 29b correspond to the layout of 25 M2 transistors. The right side of the figures correspond to the M1 transistor. Figure 30a and 30b correspond to the physical

implementation of 40 series-connected high-resistance implant (HRI) P-POLY resistors and 25 N-well under shallow trench isolation (STI) resistors. The final values are summarized in table 4.



(a) HRI P-POLY resistor layout

(b) N-well resistor layout

Figure 30: Resistor used in I_{PTAT} and I_{REF} current generation circuits

Reference current	$\frac{W}{L}$	PTAT current	$\frac{W}{L}$
M1	$55\mu m/4.5\mu m$	M1	$30\mu m/0.5\mu m$
M2	$1\mu m/1\mu m$	M2	$0.5\mu m/6\mu m$
M3	$10\times(4\mu m/2\mu m)=40\mu m/2\mu m$	M3	$10\times(4\mu m/2\mu m)=40\mu m/2\mu m$
M4	$2\times(4\mu m/2\mu m)=8\mu m/2\mu m$	M4	$6\times(4\mu m/2\mu m)=8\mu m/2\mu m$
M5	$2\times(1\mu m/4\mu m)=2\mu m/4\mu m$	M5	$2\times(1\mu m/4\mu m)=2\mu m/4\mu m$
M6	$2\times(1\mu m/4\mu m)=2\mu m/4\mu m$	M6	$2\times(1\mu m/4\mu m)=2\mu m/4\mu m$
M7	$4\times(1.5\mu m/2\mu m)=6\mu m/2\mu m$	M7	$5.5\mu m/2\mu m$
R_{REF}	$2.45887M\Omega$	R_{PTAT}	$1.26383M\Omega$

Table 4: PTAT and reference current circuit sizes

3.4.2 Operational amplifier design

The Operational amplifier (OpAmp) was designed to provide high DC-gain and low-power consumption, taking into account that the amplifier will deal with a DC signal from the sensing element, so the OpAmp does not require high bandwidth or slew rate. To reduce current consumption the operational amplifier operates in the subthreshold region, using a 2 stages miller compensated topology [34].

The two stages OpAmp architecture was chosen by their simplicity with respect to other architectures. For instance single-ended telescopic cascode or folded cascode OpAmp requires multiple bias voltages and also employs more transistors than the 2 stages topology [36]. Regarding

compensation technique, the miller compensation was chosen for two main reasons: first, save silicon area by void the use of large resistors (or MOSFET in triode region) ($R_Z \approx 1/gm_6$) required by the zero nulling techniques [34], and second because this method has a practical issue that is the wasted power dissipated by the additional circuitry [23].

In the subthreshold operation the DC-gain is given by [35]:

$$A_{DC} = gm_1(rds_1||rds_3)gm_6(rds_6||rds_7) \tag{41}$$

Where gm is the transconductance

$$gm = \frac{I_d}{mV_T} \tag{42}$$

and rds the small signal output resistance.

$$rds = \frac{mVT}{\lambda_D I_d} = \frac{V_A}{I_d} \tag{43}$$

Where V_T is the thermal voltage, $m \approx 1.5$ is the sub threshold slope [35], λ_D is the DIBL coefficient and V_A is the Early-voltage. Given that V_A is more or less constant for a fixed transistor length [37], rds is obtained by the second equivalent expression $rds = \frac{V_A}{I_d}$.

According to equation 41, DC-gain does not depend on the transistor size, in fact, once the current I_d is fixed, the intrinsic MOSFET gain ($gm \times rds$) only depends on the λ_D parameter, that is related with the distance between drain and source regions. As a consequence the DC-gain is mostly determined by the transistor length [34].

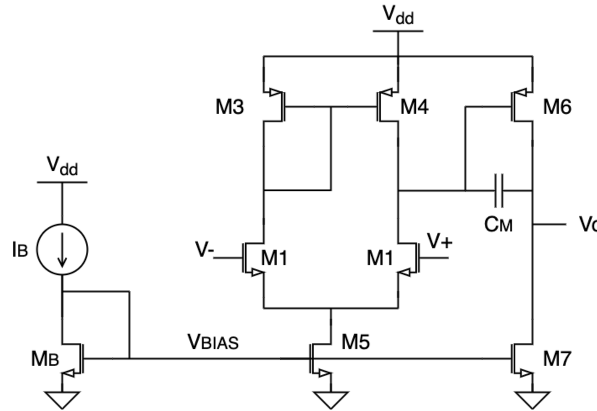


Figure 31: Two stages operational amplifier.

The current and aspect ratio in the reference was fixed to $I_B = 50nA$ and $(W/L)_{MB} = 40/1$. The M5 and M7 transistors were sized to provide a current of 20nA and 40nA respectively, according to equation 40.

$$(W/L)_5 = \frac{I_{M5} \times (W/L)_{MB}}{I_B} = \frac{20nA \times 40}{50nA} = 16$$

$$(W/L)_7 = \frac{I_{M7} \times (W/L)_{MB}}{I_B} = \frac{40nA \times 40}{50nA} = 32$$

Due to the current relationship between M5 and the differential pair M1-M2, both transistors were sized a half of M5 aspect ratio, but in order to increase the DC-gain in the first stage the aspect ratio was finally set to $(W/L)_1 = 8/2$. With this aspect ratio transistor M1 has $m_1 \approx 1.5$, $V_A \approx 13.1$ (simulation results) and $V_T \approx 26mV$ (room temperature) that according to the equations 42 and 43 results in a $gm1 \approx 266nS$ and $rds_1 = 1.31G\Omega$. Transistor M3 and M4 were sized with an aspect ratio 6 times bigger than the aspect ratio of the differential pair M1-M2, resulting in a $rds_3 \approx rds_1 \approx 1.12G\Omega$.

The 4/1 current relationship between M3 and M6 transistor set the aspect ratio between both transistors $(W/L)_6 = 4(W/L)_3$. Nevertheless in order to enhance the DC-gain some adjustments were performed and the final aspect ratio results in $(W/L)_6 = 80$. With this transistor size a $gm_6 \approx 1.06uS$ and $V_{A6} = 13.21$ is measured, and according to the equation 43 gives an $rds_6 = 330.25M\Omega$. The measured rds value in M7 transistor was $rds_7 = 9.41M\Omega$.

By replacing all these values in equation 41 the DC gain of the operational amplifier is :

$$A_{DC} \approx 266n(1.31G||1.12G)1.06u(387M||9.41M) \approx 1563 \approx 63dB$$

Once the transistor were sized the compensation capacitor C_M is set to 3.2pF to achieve a minimum phase margin of 60º ($C_M > 0.2C_L$) [36]. Once the Miller capacitor was set the gain-bandwidth product GBW is obtained as follows:

$$GBW = \frac{gm_1}{2\pi C_M} = \frac{266nS}{2\pi 3.2pF} = 13.2KHz$$

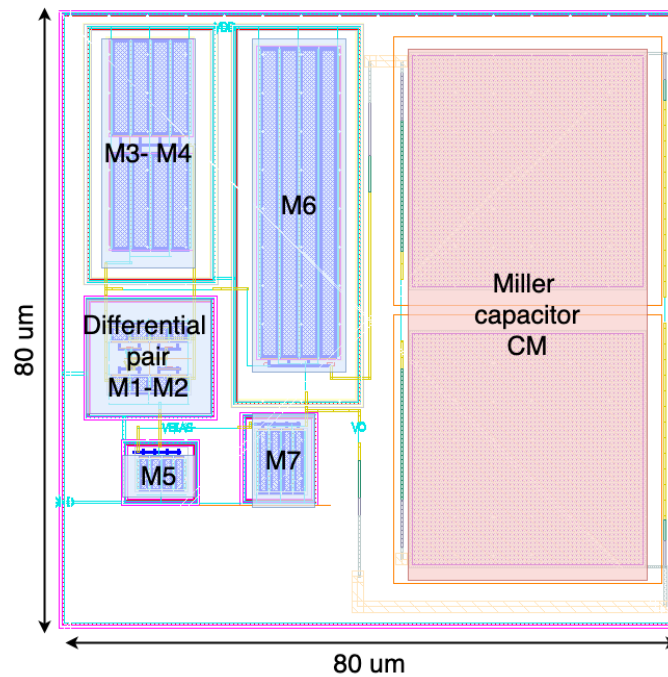


Figure 32: OpAmp Layout.

All the transistors in the OpAmp were sized using 4 multiple fingers.Tthe differential pair M1-M2 was implemented with a common-centroid layout to improve its matching. Table 5 summarizes the sizes of the transistors used in the OpAmp.

Device	$\frac{W}{L}$
M_1, M_2	$4 \times 2\mu m/2\mu m$
M_3, M_4	$4 \times 12\mu m/2\mu m$
M_5	$4 \times 4\mu m/1\mu m$
M_6	$4 \times 40\mu m/2\mu m$
M_7	$4 \times 8\mu m/1\mu m$
I_B	$50nA$
M_B	$10 \times 4\mu m/1\mu m$
C_M	$2 \times 1.6pF$

Table 5: Operational amplifier design.

Figures 33 and 34 show the transient and the frequency response of the operational amplifier. The plot shows the DC-gain is $A_{DC} = 63.9dB$, the bandwidth $BW = 8.6Hz$, and the gain-bandwidth product $GBW = 11.59KHz$.

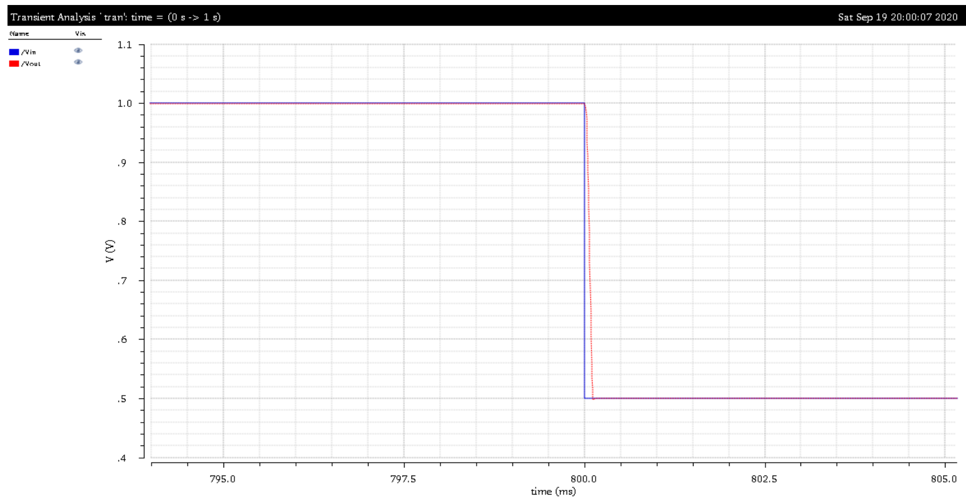


Figure 33: Transient response of the operational amplifier.

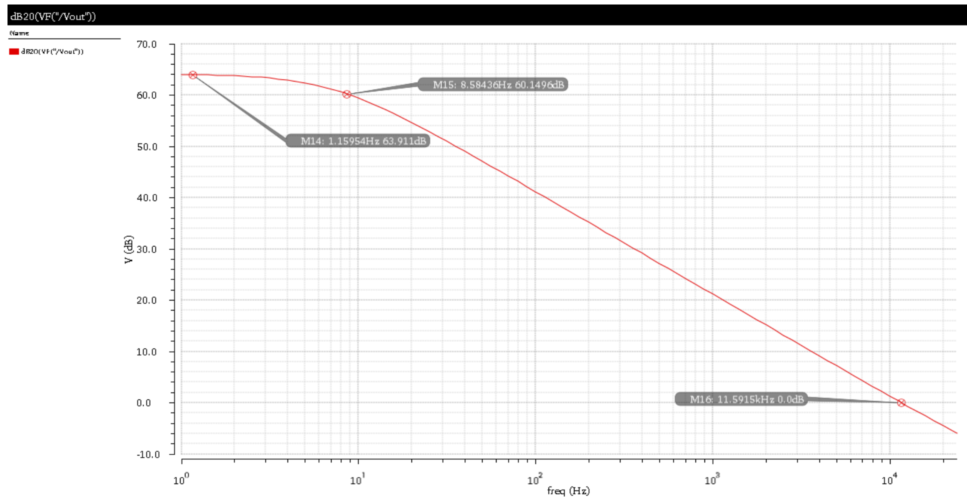


Figure 34: Frequency response of the operational amplifier.

3.4.3 Current to frequency converter design

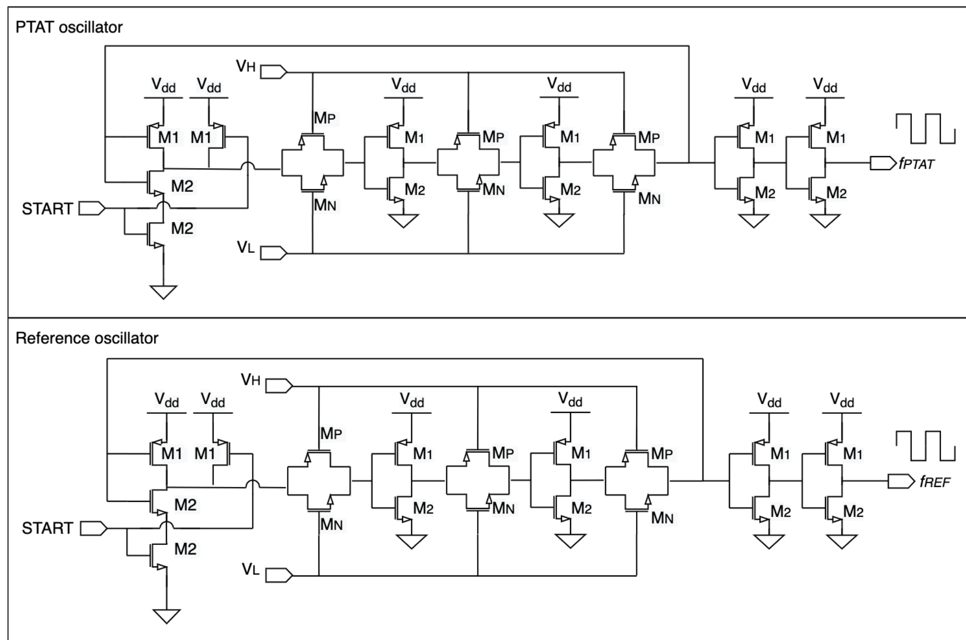


Figure 35: PTAT and reference oscillator.

The reference and PTAT oscillator of figure 21 were sized according to equation 27, with this approximation transistor M1 and M2 must comply with two main condition: first they must have similar parasitic capacitances $C_{GS1} \approx C_{GS2}$ and second have the same transconductance $G_{M1} \approx G_{M2}$. In order to fulfill these conditions PMOS and NMOS transistors have to be sized according to equation 44:

$$\frac{(W/L)_1}{(W/L)_2} = \frac{\mu_N}{\mu_P} \approx 2 \tag{44}$$

Where μ_N is the NMOS mobility, μ_P is the PMOS mobility and W, L are the transistor width and length respectively [33].To have similar parasitic capacitance $C_G \approx C_{ox}WL$ [32], transistor must be sized to have the same area.

$$W_1L_1 = W_2L_2 \tag{45}$$

To fulfill the conditions imposed by equation 44 and 45, M1 and M2 are sized with an aspect ratio $(W/L)_{M1} = 2$ and $(W/L)_{M2} = 1$. To simplify the design transistor M1 is set to $W_1 = 2\mu m$, $L_1 = 1\mu m$ and $W_2 = L_2$. According to equation 45, M2 transistor results in the following dimensions $W_2 = L_2 = \sqrt{2} \approx 1.41\mu m$.

The transmission gates M_P and M_N were sized in the same way as M_1 and M_2, in order to have similar parasitic capacitance and effective resistance. Since the effective resistance does not depend on the transistor size (equation 28), the dimension of the transmission gates were tuned until they had a more symmetric fall and rise time in the generated signal. The dimension of the transistors is summarized in table 6.

Device	$\frac{W}{L}$
M_1	$2\mu m/1\mu m$
M_2	$1.41\mu m/1.41\mu m$
M_P	$5.5\mu m/2\mu m$
M_N	$1.25\mu m/2\mu m$

Table 6: Ring oscillator current circuit dimension.

Figure 36 shows the layout implementation of the current to frequency converter circuit that occupies an area of $59\mu m \times 21\mu m$.

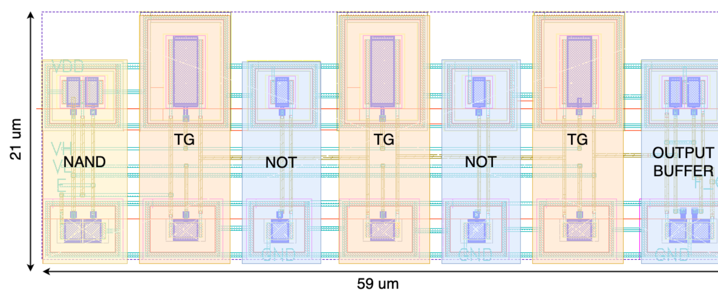


Figure 36: Current to frequency converter layout.

Once the current generation circuit is combined with the current to frequency converter, the analog part is finished. Figure 37 shows the physical layout implementation of the analog part of the circuit.

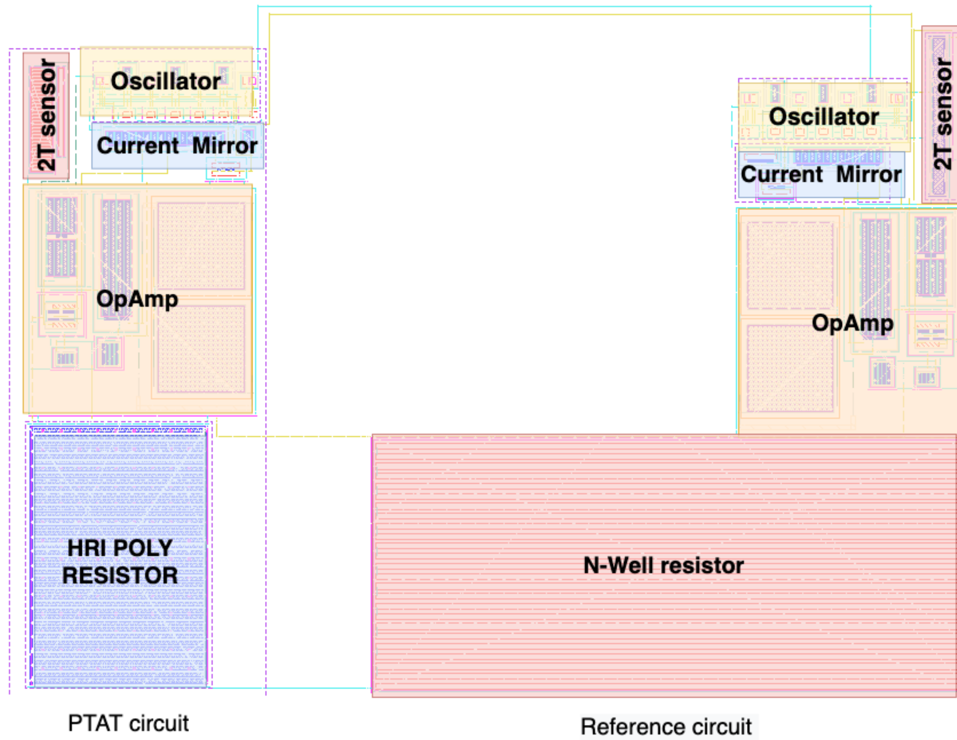


Figure 37: Analog block layout.

3.4.4 Frequency to digital converter design

All the counters used in the frequency to digital converter were implemented with the basic logical blocks in figure 39. First, a D-FF was implemented with the logic components provided by the process library $(W/L)_P = (W/L)_N = 2\mu m/0.18\mu m$ [24]. After the D-FF implementation, the PMOS transistor was resized two times the NMOS aspect ratio to achieve a switching threshold voltage $V_M \approx 0.5V_{DD}$ in the CMOS inverter (Figure 40). Table 7 summarizes the transistor dimensions of the CMOS logical blocks.

Device	$\frac{W}{L}$
M_P	$4\mu m/0.18\mu m$
M_N	$2\mu m/0.18\mu m$

Table 7: Transistor sizes used in the frequency to digital converter.

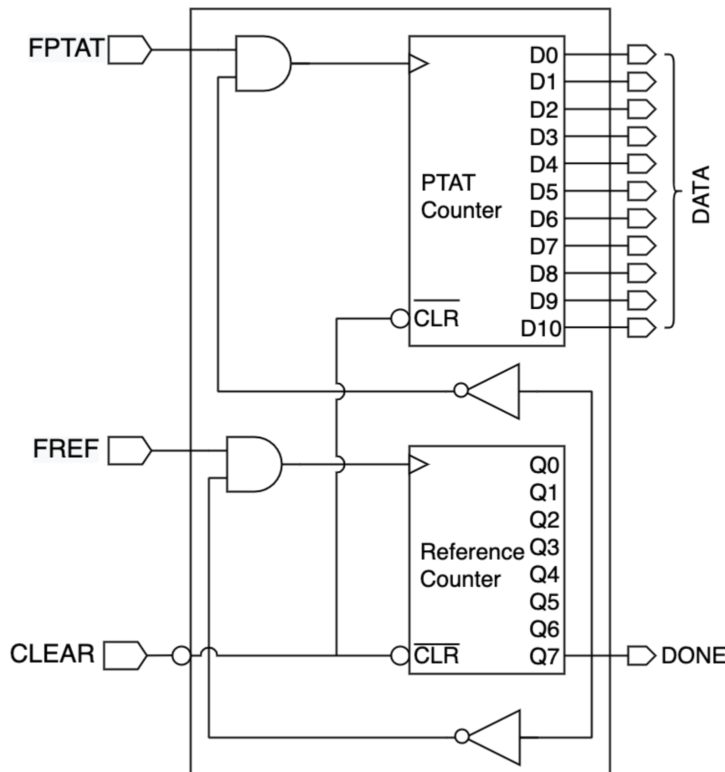


Figure 38: Frequency to digital converter.

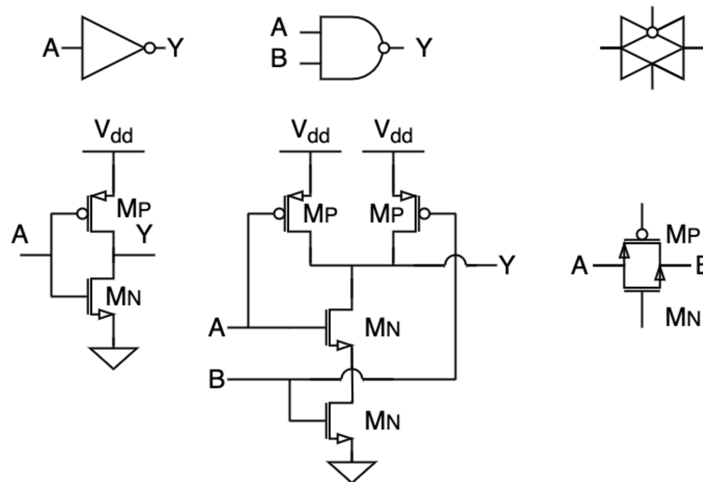


Figure 39: CMOS logical blocks.

Figures 41 and 42 show the physical implementation of the D-FF and the frequency to digital converter respectively. Each flip-flop has a size of $17\mu m \times 30\mu m$, the final layout of the frequency to digital converter was designed to fit between the empty space in the analog block (figure 37) and has a size of $144\mu m \times 102\mu m$.

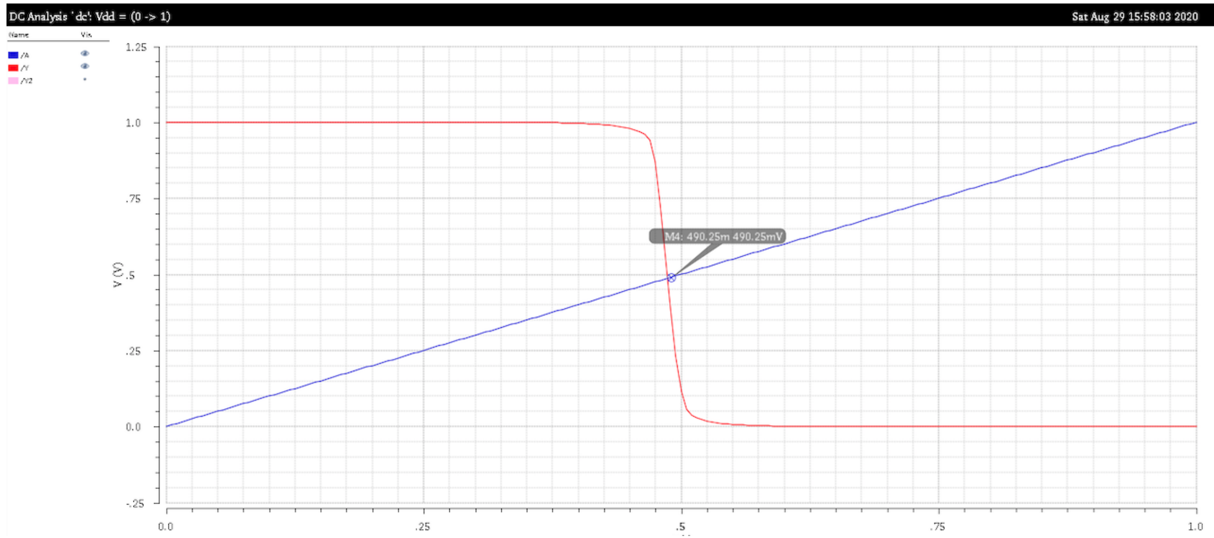


Figure 40: DC voltage characteristic of the CMOS inverter.

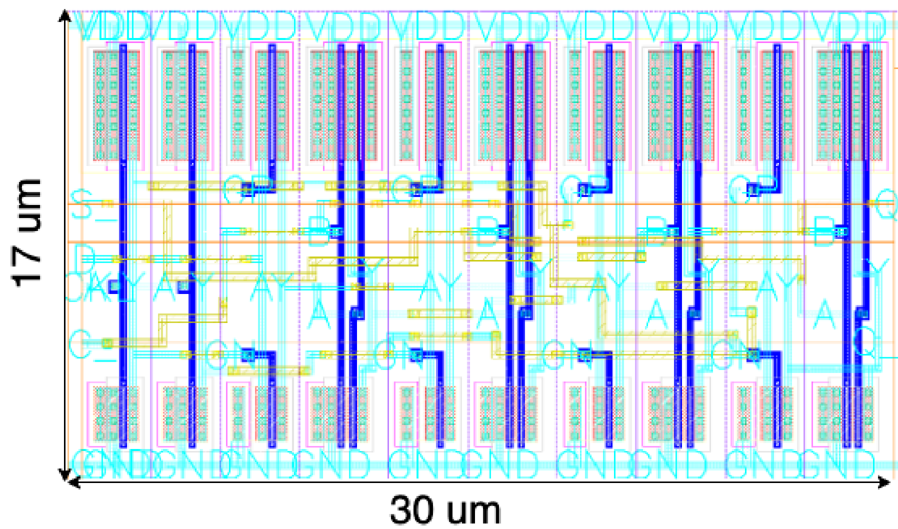


Figure 41: D-FF layout.

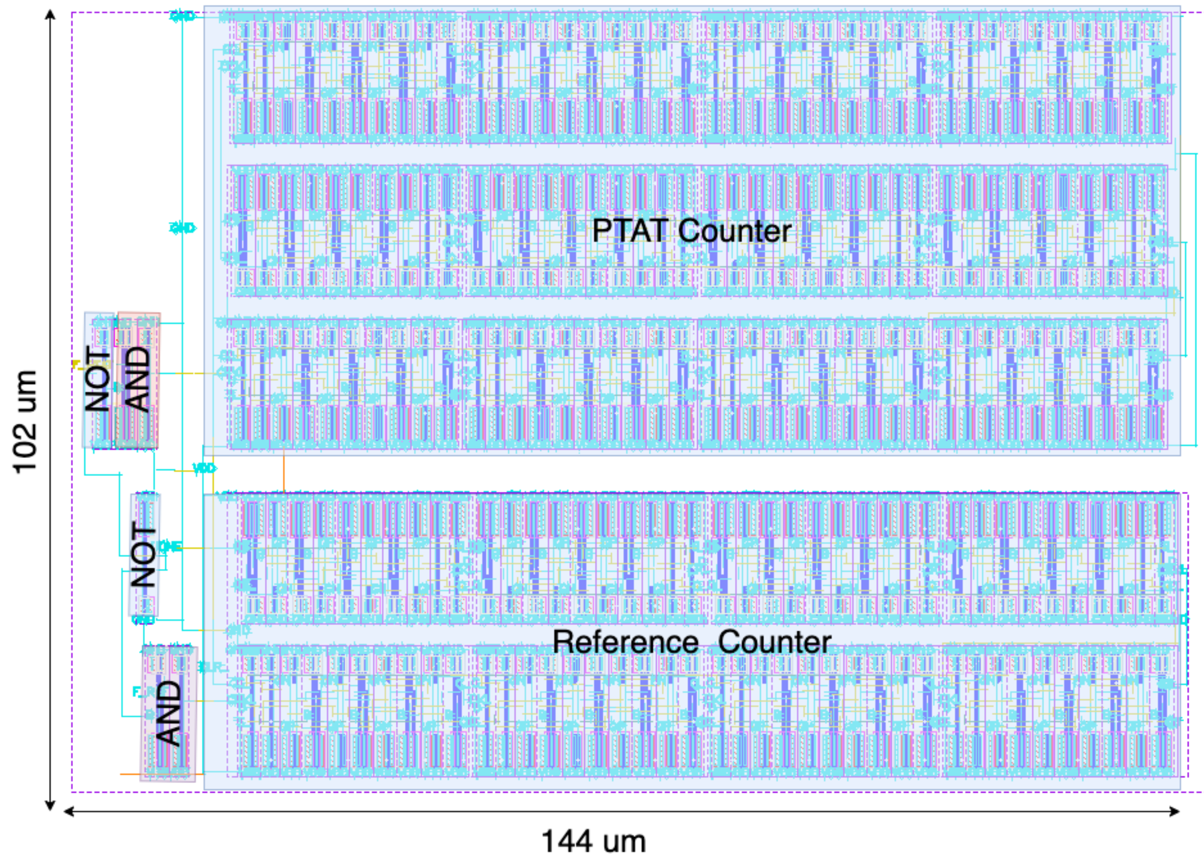


Figure 42: Frequency ti digital converter layout.

4 Results

4.1 Top level temperature sensor

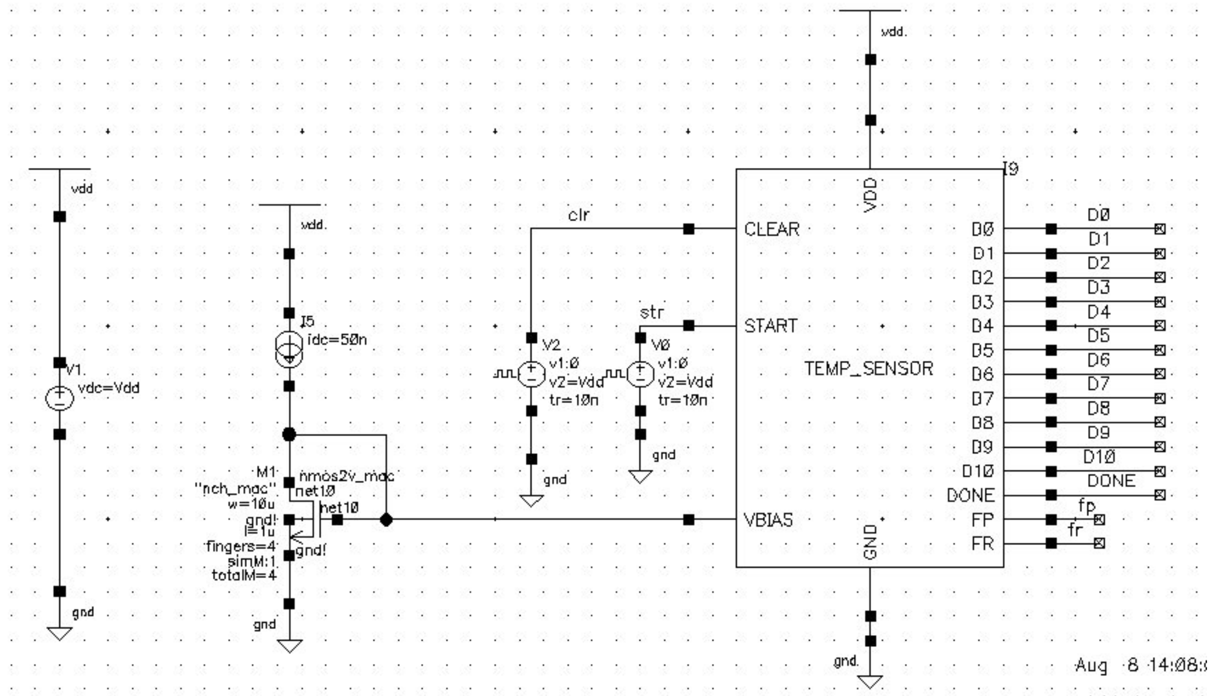


Figure 43: Top level temperature sensor.

The figure 43 corresponds to the top-level temperature sensor designed in this work. The sensor was provided with CLEAR and STAR input signals and D0-D10 output signals, the VBIAS input used to bias the OpAmp. The CLEAR input corresponds to the asynchronous reset of the counters. The START input is used to set the beginning of the conversion. The output ports D0 to D10 correspond to the 11-bits output of the PTAT counter. The output ports FP and FR correspond to the f_{REF} and f_{PTAT} signals generated by the current to frequency converters, this pins was added to obtain the post layout behavior of the sensor and can be removed from the sensor. The ports VDD and GND correspond to the power supply terminals.

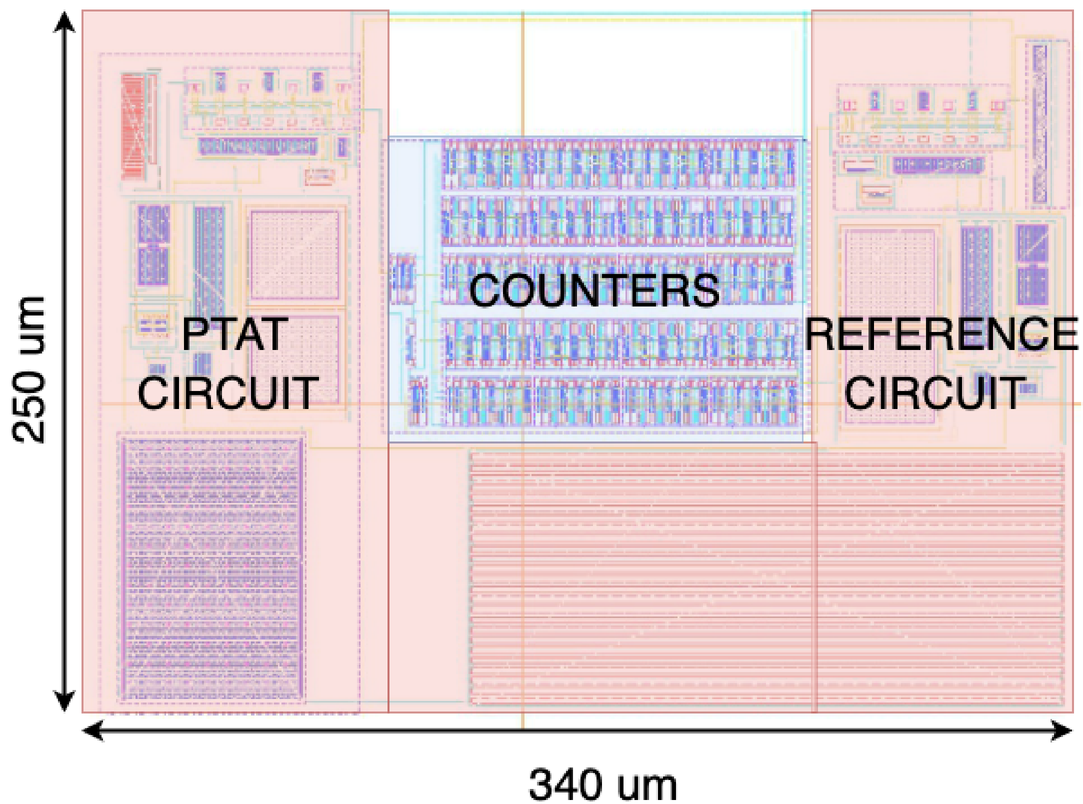


Figure 44: Temperature sensor layout.

Figure 44 shows the layout physical implementation of the temperature sensor. The layout of this work was developed using Calibre DRC, LVS, and PEX tool and occupy an area of $250\mu m \times 340\mu m$.

4.2 Simulations

Obtaining the data output of the sensor requires a transient analysis of 1.8 ms. Each transient analysis takes a couple hours of computer simulations, so the characterization of the sensor was performed by the f_{REF} and f_{PTAT} response. First a parametric analysis in the 0ºC to 60ºC temperature range with temperature increments close to theoretical resolution 0.2ºC was performed. After that, the data output was computed by substituting the f_{REF} and f_{PTAT} values into the equation 34. To corroborate the accuracy of this approximation, some full transient simulations were performed at 0ºC, 15ºC, 30ºC, 45ºC, and 60 ºC.

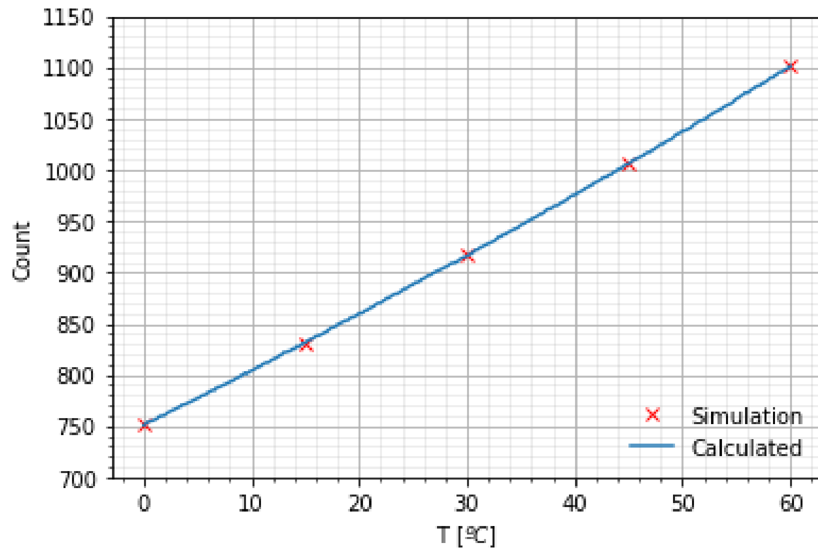


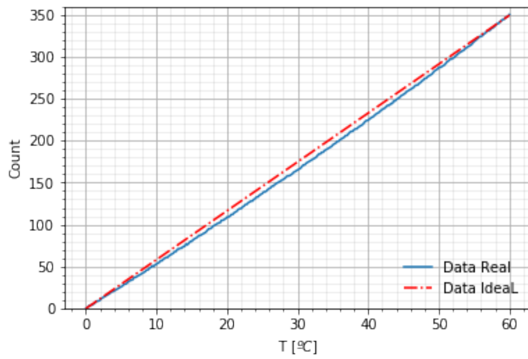
Figure 45: Temperature sensor output.

The blue line in figure 45 shows the data output obtained by the fast approximation. And the red x mark shows the obtained data after a full transient simulation. According to the graph, both results match.

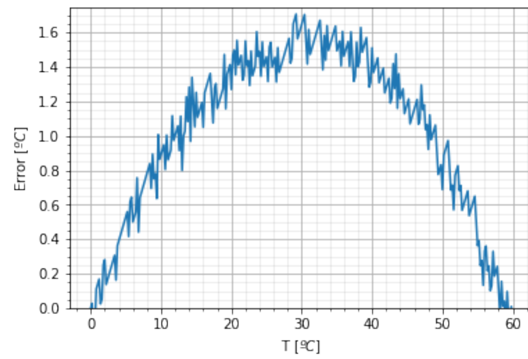
Sensor Output			
Temperature [ºC]	Digital Output	Decimal Output	Δ_{DATA}
0	0101110111	751	-
15	01100111111	831	80
30	01110010101	917	86
45	01111101110	1006	89
60	10001001101	1101	–

Table 8: Temperature sensor simulation results.

Table 8 shows in binary and decimal format the data obtained after conversion at different temperatures. Figure 45 shows a linear tendency in the values obtained after conversion and also a more or less constant increment between the different measures realized $\Delta_{DATA} \approx 85$. That results in a resolution similar to the theoretical value ($15/85 \approx 0.17ºC$).



(a) Ideal vs simulated data output.



(b) Error in ºC.

Figure 46: Conversion error at schematic simulation.

The conversion error was obtained after offset cancellation and the ideal transfer function of the digital conversion was based on the end-point fit line over the 0-60ºC [38][39]. According to figure 46b, the maximum error observed is 1.7ºC in the middle of the sensor range.

4.2.1 Power consumption

Table 9 displays the current consumption by circuit component. The most current demanding circuits are the ring oscillator with 46.38%, followed by the current generation circuits that represent the 39.57%, and finally, the counters and OpAmp represent 21.41% of the total. The 2T sensing element with 0.0021% does not have a representative current consumption.

Current consumption				
Component	REF	PTAT	TOTAL	Contribution
Sensing element	14.9 pA	11.04 pA	25.94 pA	0.0021%
OpAmp	45.6 nA	47.09 nA	92.69 nA	7.36%
Reference current	65.03 nA	143.7 nA	208.73 nA	16.58%
Current mirrors	26.2 nA	170.58 nA	196.78 nA	15.63%
Ring Oscillator	246.9 nA	336.97 nA	583.87 nA	46.38%
Counter	18.2 nA	158.64 nA	176.84 nA	14.05%
TOTAL			**1.2589μA**	

Table 9: Temperature sensor current consumption.

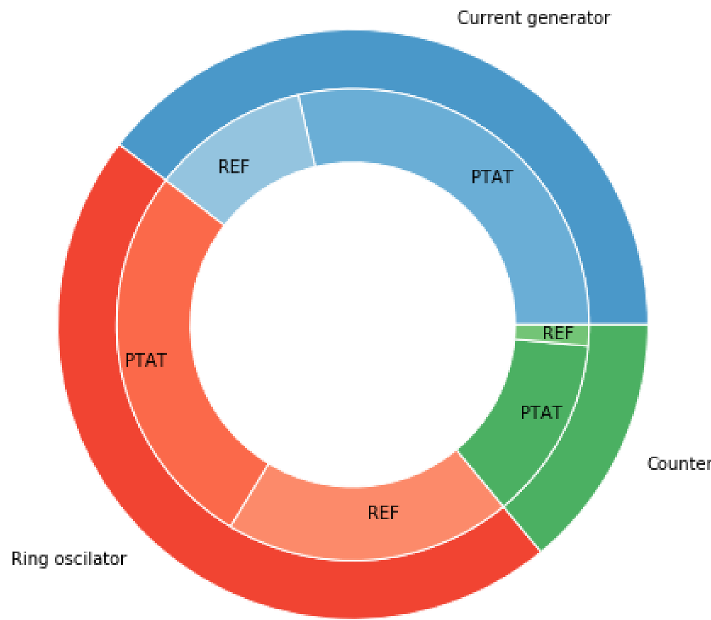


Figure 47: Sensor current consumption by blocks.

Figure 47 outlines the current consumption by functional component, and compares the reference with PTAT subcircuits. The current consumption in the current generation, oscillator, and counter PTAT subcircuits are always bigger because the resolution of the sensor depends on the ratio between f_{REF} and f_{PTAT} that is determined by I_{REF} and I_{PTAT} currents relationships. The PTAT counters have a current consumption higher than the reference counters because the frequency and the size of the counters increase the dynamic current consumption in the PTAT counter.

4.2.2 Sensor Performance

There is not one single way to measure the performance of a smart temperature sensor given the wide variety of sensors that can be implemented in standard CMOS technologies. However, most of the CMOS temperature sensors employ two indicators to quantify the sensor performance; the $E_{conversion}$ that represents the amount of energy dissipated during conversion, and the resolution figure-of-merit (FoM) that relates the energy/conversion and the square of the resolution [16].

$E_{conversion}$, and FoM according to the definition are given by :

$$E_{conversion} = V \times I \times T_{DONE} \tag{46}$$

$$FoM = E_{conversion} \times (T_{res})^2 \tag{47}$$

Where V is the supply voltage, I is the sensor current consumption, T_{DONE} is the conversion time and T_{res} is the resolution of the sensor.

With $V = 1V$, $I = 1.26\mu A$, $T_{res} = 0.17°C$ and according to the data used in figure 22 the $E_{conversion}$ and FoM results.

$$T_{DONE} = \frac{2^7}{82.4KHz} = 1.55ms$$
$$E_{conversion} = 1V \times 1.26\mu A \times 1.55ms = 1.95nJ$$
$$FoM = 1.95nJ \times (0.17ºC)^2 = 0.056nJ(ºC)^2$$

4.3 Post layout simulation

After R C extraction, transient simulations require a lot of computing. Although the complete characterization of the sensor (figure 45), can be done through f_{REF} and f_{PTAT}, due to the time limitations a simple characterization at 5ºC temperature steps was performed.

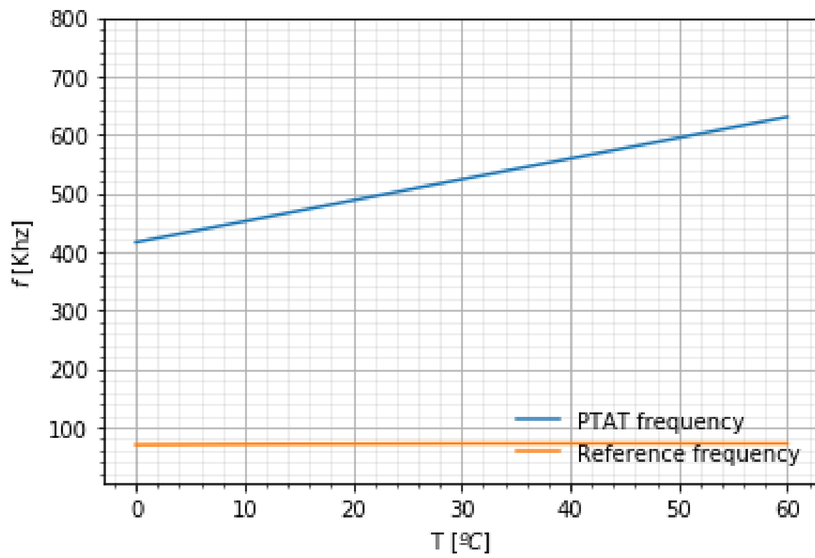


Figure 48: Post layout reference and PTAT frequency .

From the values obtained to plot figure 48,the post layout resolution of the sensor is obtained by the equation 39 that considers the non ideal behaviour of reference frequency. With $f_{REF}(0) = 70.45KHZ$ and $f_{REF}(60) = 72.6KHZ$ the frequency gain $\alpha f_R = 0.35KHz/ºC$ and with the PTAT frequency $f_{PTAT}(0) = 416.45KHZ$ and $f_{PTAT}(60) = 630.2KHZ$ the frequency gain of the PTAT oscillator is $\alpha f_P = 3.56KHz/ºC$ gives a resolution:

$$Tres = \frac{70.45KHz}{2^7(3.56KHz/ºC - 0.35KHz/ºC)} \approx 0.17ºC$$

Table 10 summarizes the data output obtained at different temperatures. Although after parasitic extraction, f_{REF} and f_{PTAT} suffer a frequency reduction the resolution is preserved. Also figure 50 shows an increase in the DATA values obtained in comparison with the schematic simulation.

Sensor Output			
Temperature [ºC]	Digital Output	Decimal Output	Δ_{DATA}
0	01011110100	756	-
15	01101000101	837	81
30	01110011100	924	87
45	01111110110	1014	90
60	10001010111	1111	–

Table 10: Sensing element post layout simulation results

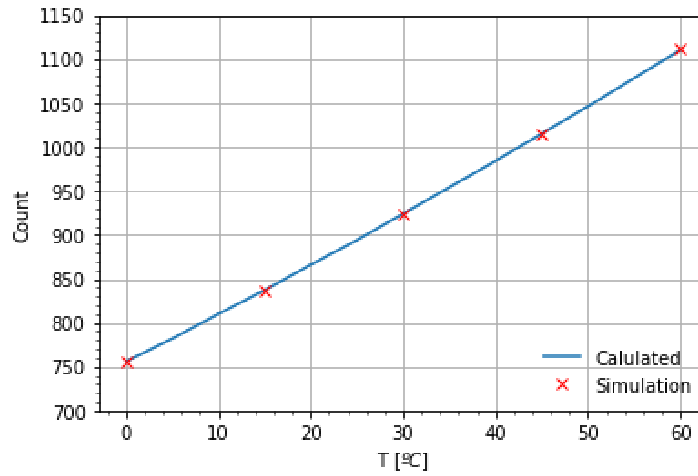


Figure 49: Data output after extraction.

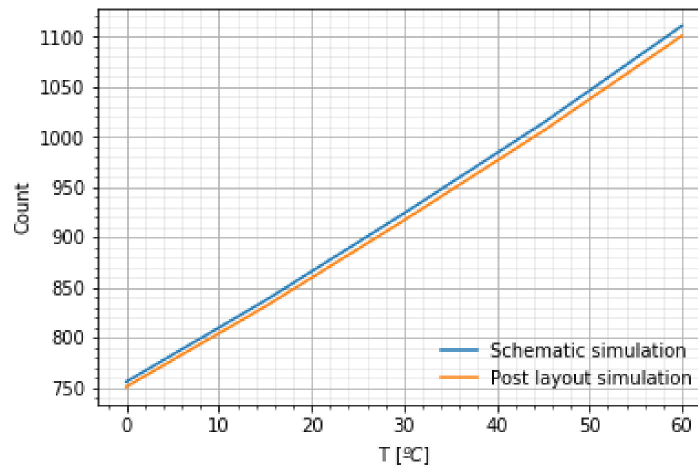
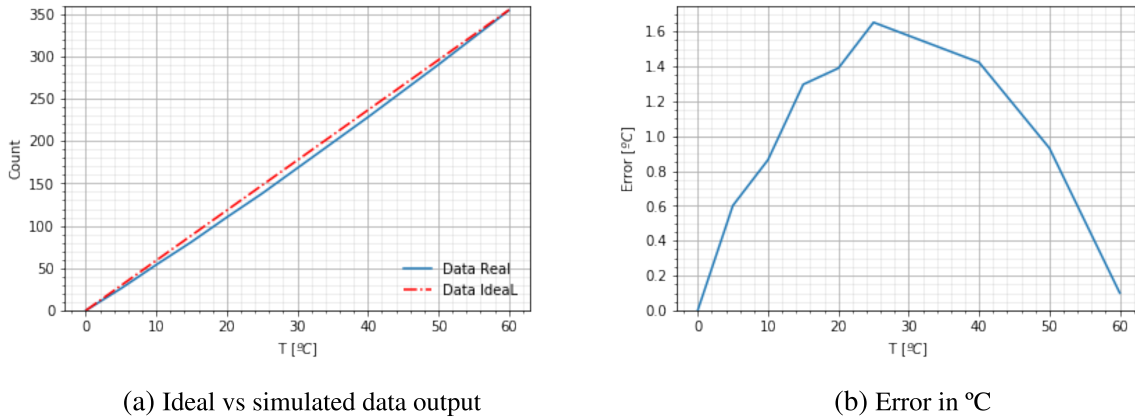


Figure 50: Schematic and post layout simulation data output.

In a similar way to the schematic simulations, the data output is shown in figure 49. The error in the post-layout simulation (figure 51b) has a maximum value of 1.65ºC in the middle of the

scale, this error is similar to the one obtained in the schematic simulation.



(a) Ideal vs simulated data output

(b) Error in ºC

Figure 51: Conversion error after post layout simulation

Figure 52 shows the supply sensitivity of the sensor. The supply sensitivity obtained is -2.8ºC to 2.17ºC from a supply voltage variation of 0.8 to 1.4V.

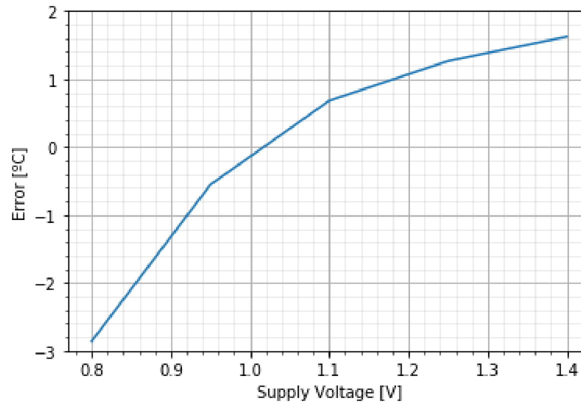


Figure 52: Simulated Voltage sensitivity of the sensor at 30ºC.

With a post layout current consumption of $I = 1.79\mu A$, a conversion time $T_{Done} = 1.81ms$ and a $T_{res} = 0.17ºC$ the energy per conversion and FoM are calculated by equation 46 and equation 47.

$$E_{conversion} = 1V \times 1.79\mu A \times 1.81ms = 3.2nJ$$

$$FoM = 3.2nJ \times (0.17ºC)^2 = 0.092nJºC^2$$

4.3.1 Sensor performance

Finally, the sensor performance is summarized and compared with other low power CMOS temperature sensors (table 11). The values of the sensor performance correspond to the post-layout simulation. In fact, the other sensors were tested after their full implementation. Some

variations in respect to the post layout simulation will be expected when the sensor is fabricated.

Performance and comparison with other low power CMOS sensor				
Parameters	This Work	[18]	[40]	[15]
Technology	$0.18\mu m$	$0.18\mu m$	$0.16\mu m$	$0.16\mu m$
Type	MOSFET	MOSFET	BJT	DTMOS
Area	$0.085mm^2$	$0.09mm^2$	$0.09mm^2$	$0.085mm^2$
Supply Voltage	1V	1.2 V	1.2-2 V	0.85-1.2 V
Temperature range	0-60ºC	0-100ºC	-55-125ºC	-40-125ºC
Resolution	0.17ºC	0.3ºC	0.02C	0.063ºC
Inaccuracy	1.7ºC	3-1.6ºC	0.015ºC	0.4ºC
Conversion time	1.8ms	30ms	5.3ms	6ms
Power	$1.78\mu W$	$71nW$	$5.1\mu W$	$595\mu W$
Energy/conversion	$3.2nJ$	$2.2nJ$	$27nJ$	$3.57\mu J$
FoM	$0.092nJ(ºC)^2$	$0.198nJ(ºC)^2$	$0.0108nJ(ºC)^2$	$14.16nJ(ºC)^2$

Table 11: Performance and comparison of the sensor

According to table 11, the Energy/conversion in this work and sensors designed by [18] and [40] have values quite similar to each others, even with very different power consumptions. This is because the power consumption is compensated for by the conversion time. For example, [18] has power consumption 25 times lower than that obtained in this work. But if the conversion time is compared this work is 17 times faster than [18]. Then according to equation 46, the energy/conversion results in a similar value for both sensors.

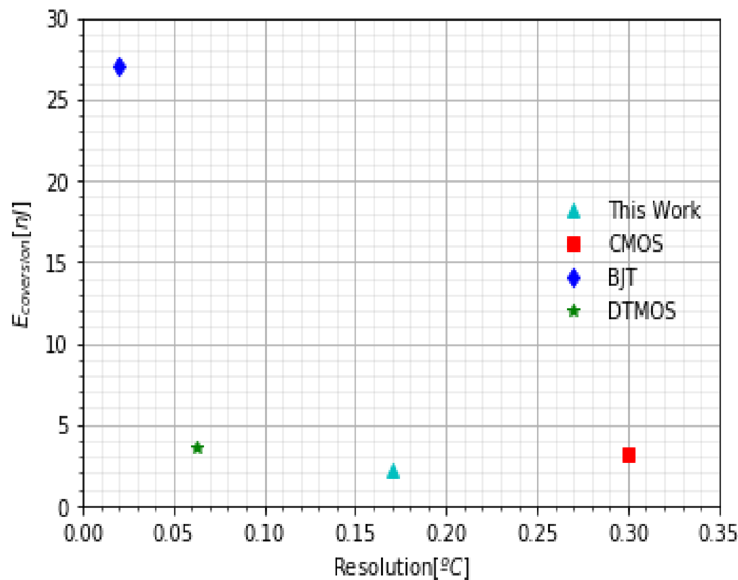


Figure 53: Energy per conversion versus resolution.

Figure 53 shows the energy per conversion versus the resolution of the smart temperature sensor. The Resistor and ETF based sensors were not considered in this analysis due to their higher power consumption. The BJT temperature sensor has a higher resolution at expense of energy/-conversion. This work has an Energy/conversion value similar to other CMOS-based temperature sensors with the same resolution.

4.4 Post layout transient simulation

The following plots (figures 54, 55, 56, 57 and 58) correspond to the post-layout transient simulation of the sensor at different temperatures along a 0-60ºC temperature range. The DATA signals D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, and D10 correspond to 11 bits that represent the temperature digital code. The temperature conversion stops when the signal DONE switches to 1 and the PTAT counter stops. After this, the values at the output of the sensor are ready to be read or saved.

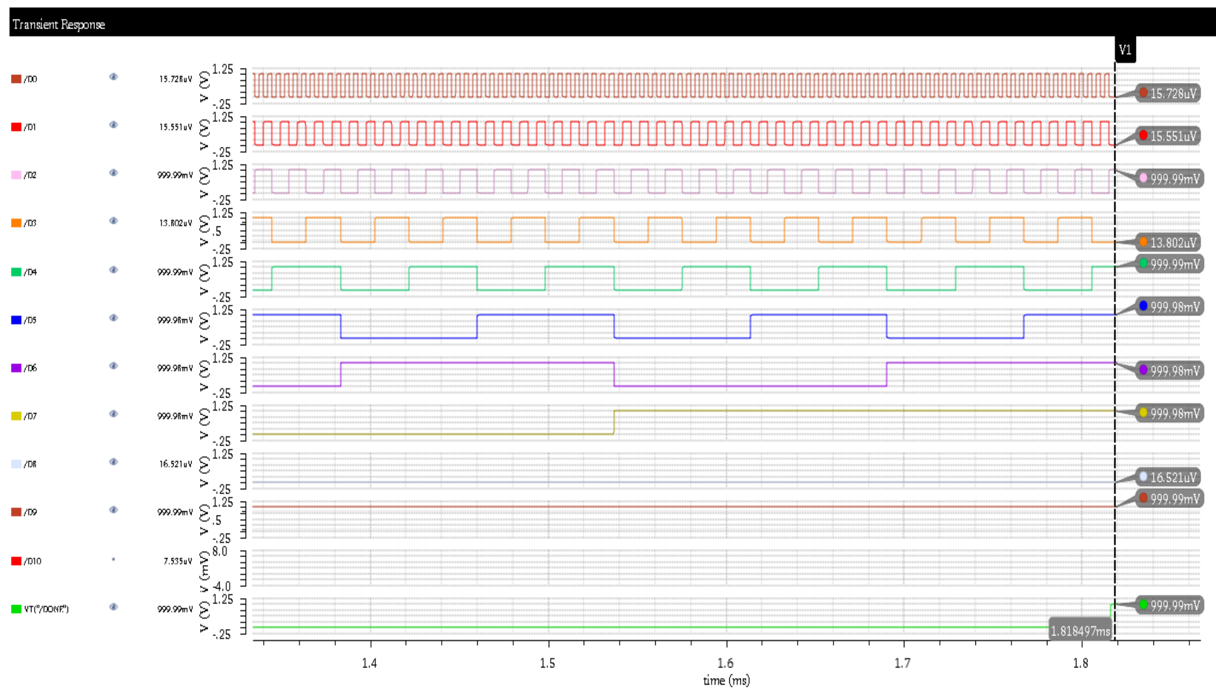


Figure 54: Digital temperature output at 0ºC, 01011110100.

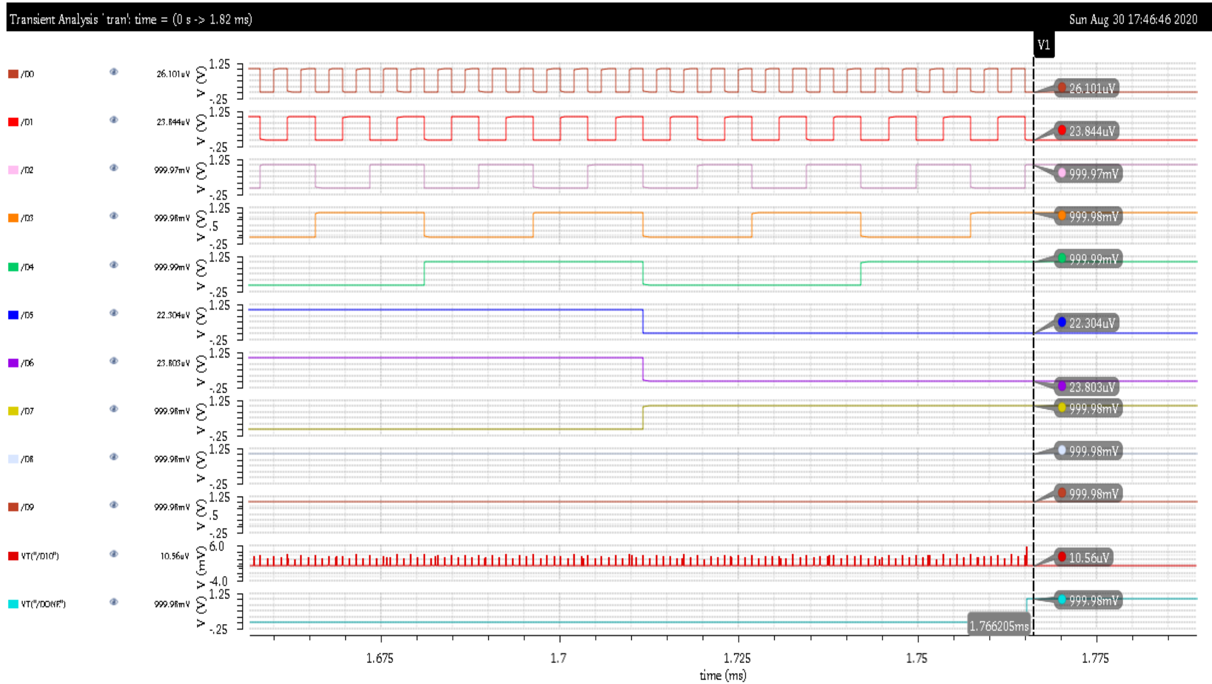


Figure 56: Digital temperature output at 30ºC, 01110011100.

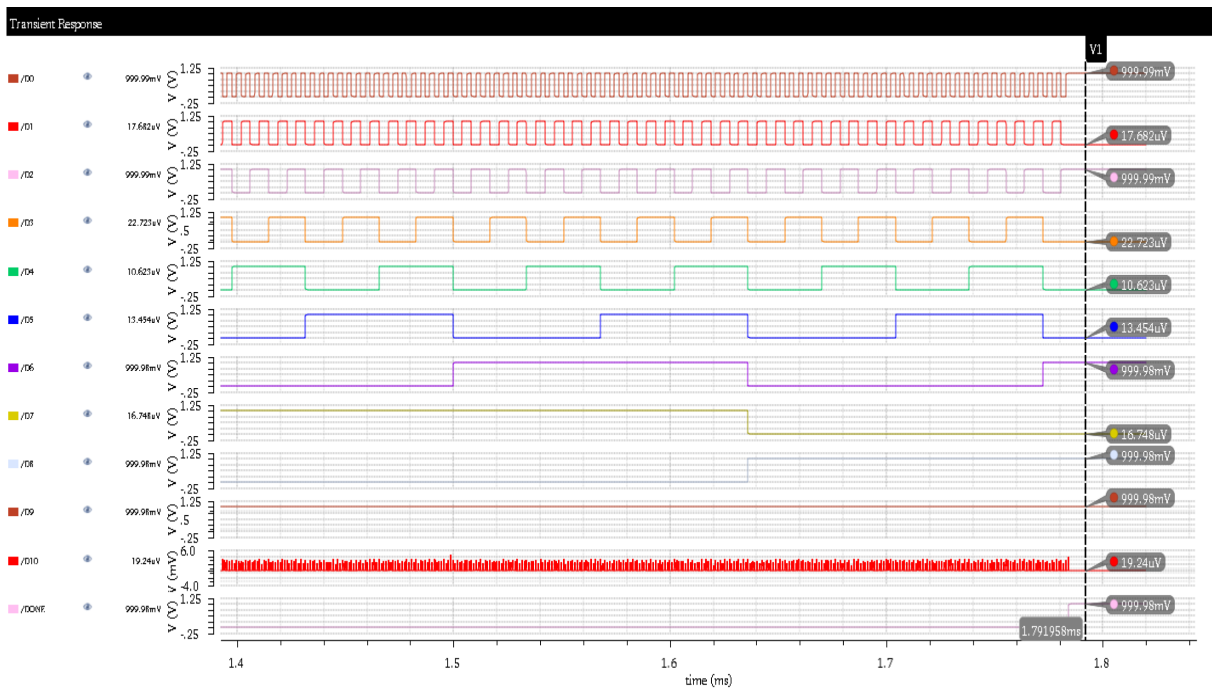


Figure 55: Digital temperature output at 15ºC, 01101000101.

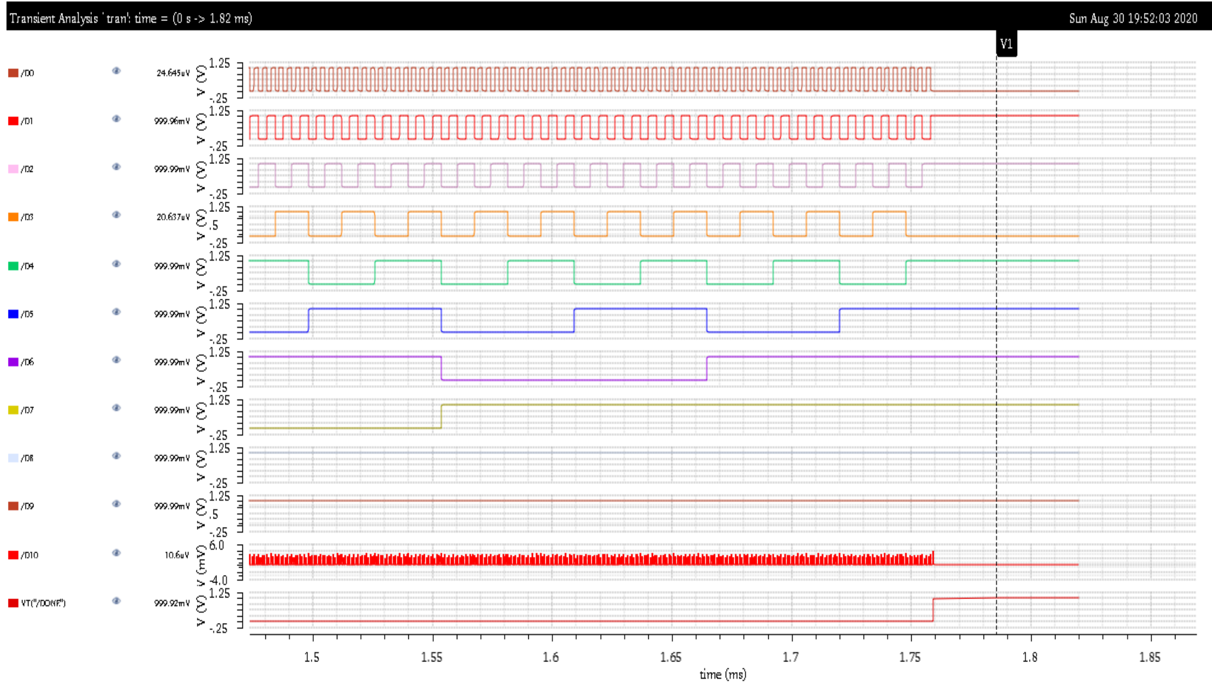


Figure 57: Digital temperature output at 45ºC, 01111110110

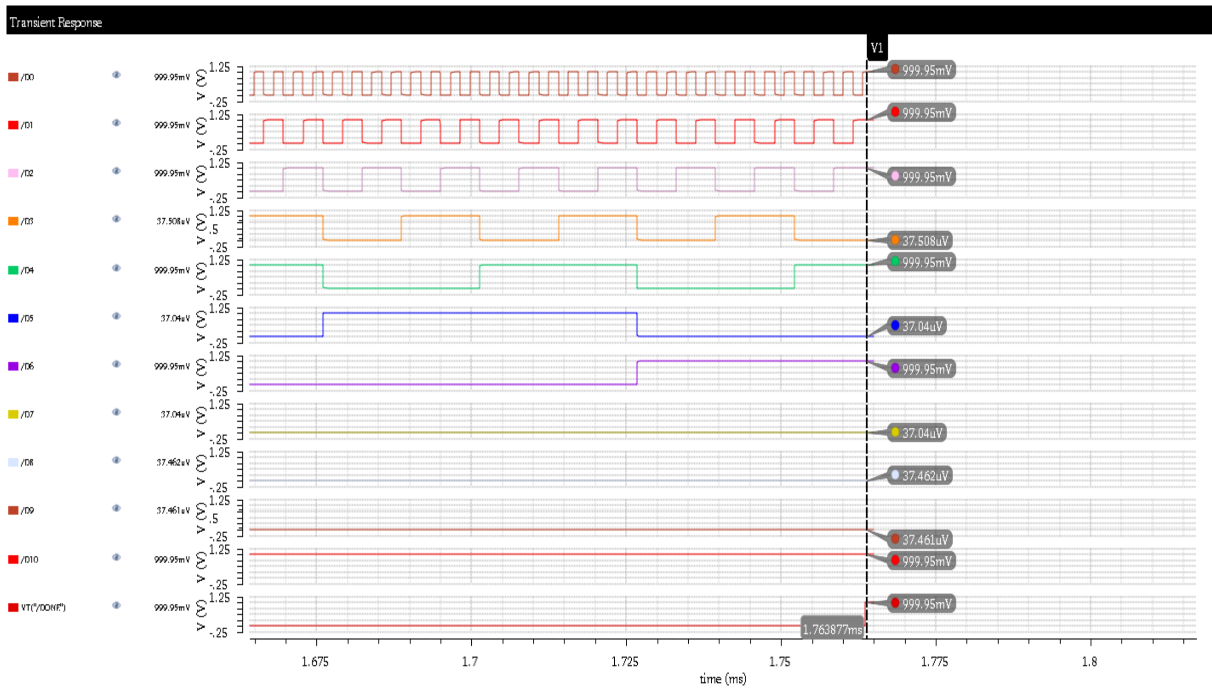


Figure 58: Digital temperature output at 60ºC, 10001010111.

5 Conclusions and future development:

5.1 Conclusions and future development:

In this work, a low power VLSI temperature sensor was developed in a TSMC 180 nm CMOS process. The proposed temperature sensor combines the PTAT characteristics of a 2-T sensing unit with a CTAT and PTAT resistor to generate two currents: ideal and PTAT. An insensitive to temperature reference and PTAT frequencies are generated by a current controlled ring oscillator. An 11-bit digital output temperature code is generated by two asynchronous counters. The digital output is produced by the relationship between the PTAT frequency and a reference frequency. The reference frequency is generated internally by a similar circuit used to provide the PTAT signal and to enhance the resolution the reference frequency is divided by an 8 bits counter.

After the post-layout simulation, the temperature sensor consumes $1.78\mu W$ and occupies an area of $0.085mm^2$. The sensor achieves a resolution of 0.17ºC for an uncalibrated accuracy of $< 2ºC$ in the 0ºC to 60ºC temperature range.

The sensor achieves low power consumption by the use of the 2T sensing element instead of a conventional bandgap temperature sensor. The current consumption in the analog part can be reduced by increasing the resistors at the expense of the silicon area. The most power demanding block of the circuit is the ring oscillator due to the delay introduced by the transmission gates, which generates a large rise and fall time.

Although the sensor was tested in a temperature range of 0-60ºC, the f_{REF} and f_{PTAT} frequencies preserve its behavior in a wide range. Given that the maximum error is located around 30ºC , the temperature range of the sensor can be extended from -10ºC to 100ºC with a similar accuracy.

5.2 Future development:

The first step is to reduce the current consumption in the current generation and oscillators circuits. Next, the sensor requires the implementation of the readout and control circuit. Additionally the current reference used to bias the operational amplifier needs to be added.

As the performance of the sensor is mainly determined by the characteristics of the reference current and therefore the type of resistance used to obtain it. Another important future work is to analyze the impact of the resistor type in the sensor performance, particularly the resistor type used in the I_{REF} current circuit. For these, two new versions of the sensor will be implemented using resistors with a lower α_{R2} coefficient available in the TSMC 180 nm process (table 12).

Resistor type	R_{sh} $[\Omega/sq]$	α_{R1}	α_{R2}
P+ diffusion resistor	140.6	1.383×10^{-3}	8.632×10^{-7}
N-well under OD resistor	440	3.68×10^{-3}	9.54×10^{-6}

Table 12: TSMC 180nm resistor types

The digital control block should clear the counter output, synchronize the START and CLEAR signals and save the conversion DATA in an output register for the posterior processing.

Another future improvement is the design of the digital back end of the sensor, similar to the smart temperature sensor in figure 59 [41]. In this block an extra error and offset correction will be realized. Nevertheless, this can be implemented on-chip or through a programmable logic implementation.

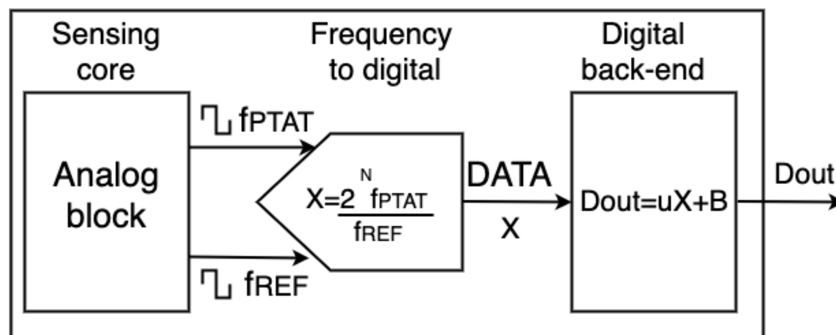


Figure 59: Digital back-end.

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