Digital Control Strategy for an LLC converter

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Abstract

Since the beginning of power electronics studies, the key objective has been to reduce the size of the transformation equipment. The invention of controlled semiconductor devices set up a step forward to this objective, by increasing the switching frequency and hence reducing the volume of reactive elements. However, this new operation strategy came also with an increment of the converter switching losses and setting a constrain due heat dissipation. A new thread in the pursuit of size reduction is set on resonant or quasi-resonant converters which use reactive networks to obtain soft switching topologies. This commutation strategy achieves a drastic reduction of the switching losses (on the switching devices) so the heat constrain is only attached to the conduction losses.

In this thesis, a deep analysis of one particular resonant converter has been performed, the LLC topology. LLC structure’s main particularity relies on handling the power flow, by using frequency modulation instead of Pulse Width Modulation (PWM) like traditional converters. This intrinsic characteristic eases the control strategy but hinders the model linearization since State Space Averaging Method (SSAM) can no longer be applied. There are two main reasons: The first one is that the method relays on averaging the state variables over a switching period where this period is time invariant. In this particular case the switching period is time dependent, it is our control tool. The second reason is that due converter operation, part of the state variables are sinusoidal zero-centered waveforms. In order to avoid this inconvenience, we will relay on a cycle-by-cycle analysis to define a linear model of the converter state equations so that linear control can be applied.

Finally, the designed controllers are discretized with different methods and tested in a 3.3 kW converter through an M4 ARM platform developed by Monolithic Power Systems (MPS).
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Chapter 1

Introduction

1.1 Motivation

I personally find electronics a fascinating branch of science. Firstly, because of the great number of problems that can be solved, and secondly due to the ease with which an idea can be transformed from a prototype to industrial production. Although this process is often full of frustration and despair, the fact that we do not give up on finding the right solutions gives us great satisfaction. Particularly, power electronics leads you to understand not only the different variants of electronics such as analog and digital but also other branches of science. Amongst them, the physics of ferromagnetic materials, thermal dissipation, electromagnetic compatibility and most importantly: patience.

In addition to personal motivation, there is also an environmental awareness because the consumption of electricity is increasing every year, as well as the number of switched-mode converters connected to the power grid. Therefore, there is a clear trend to constantly improve the efficiency of these devices, both in terms of improved component properties and switching structures.

Previously, before enrolling in the master’s degree, I had been working designing converters, but as it is common in the industrial world, priority is given to obtaining a finished product that can be sold rather than having absolute knowledge of the device. That is the reason why I decided to investigate through the different subjects of the master the path that links the study of a problem with the conception and analysis of the necessary structure to finally implement the proper design of a prototype.

1.2 Project Framework

This thesis development is part of a design process aimed to define new switching structures for smart grids. The main drawback faced by the power grid is to integrate micro generation power plants from renewable sources without compromising the overall operation. The solution to this problem can be solved through smart grids and the control over the different elements involved in the distribution of energy.

The option shown in the figure 1.1 consists on a design of 4 converters, two of them bi-directional, so as to guarantee the supply in the different possible scenarios. As it can be observed, the use of an analogical control complicates quite a lot the implementation of a system like this one,
since the converter in charge of regulating the DC bus voltage will depend on the structure and the energy flow. Furthermore, it is possible to connect converters in parallel in order to have a more stable efficiency with the load and a better maintenance. Using digitally controlled equipment in parallel allows interleaving configurations to reduce the current ripple in the DC bus and therefore their size and cost.

![Smart grid structure for Electric Vehicle (EV) recharge station or power server.](image)

In figure 1.1 the following acronyms have been used:

- **AC/DC bidirectional**: The Totem Pole structure [14] allows a bi-directional energy flow with high efficiency. In the case of obtaining energy from the network, with the appropriate control, a high power factor is achieved. In addition, using three converters in parallel it is possible to raise from a three-phase input to 800 V DC bus.

- **DC/DC**: In this position the LLC resonant converter will be located to deliver isolated power to the load (EV or server) with high efficiency.

- **MPPT**: To obtain solar energy, a Maximum Power Point Tracker (MPPT) converter will be used to maximize the conversion of radiation. The most common structure for this type of device is the Boost or quasi-resonant Boost converter to further increase efficiency.

- **DC/DC bidirectional**: In this case a soft switching structure like Phase Shift can provide also bidirectional power [2]. This converter topology is similar to the LLC one but instead of frequency modulation the power flow is regulated by the overlapping of the switching signals between both half bridges.

### 1.3 Objectives

The objective of this thesis is to understand the LLC topology as well as its strengths and weaknesses. It also aimed to analyze the converter through its state equations in order to design a voltage control loop. At the end, it will be validated through simulations with PSIM® and with a platform (EVF32020) developed by Monolithic Power Systems.

The work has been distributed in the following chapters:

- **2 Resonant Converter Topology**: Description of the different parts of the used topology as well as the principles of operation of the resonant converter. It also details the most interesting feature of the LLC converter which is the soft switching and how it influences the efficiency.
• 3 LLC Resonant Converter Modeling: Presentation of the non-linear model of the converter and analysis of the linearized small signal model. The transfer functions frequency-current, current-voltage and frequency-voltage are obtained to configure the different control loops.

• 4 Control Design: Definition of the different loops to control the voltage. Single voltage loop and double voltage-current loop. Evaluation of the constants for the different compensators on Octave® to ensure stability.

• 5 Simulation: Verification of the different control loops designed on an ideal circuit model. Obtain steady state waveforms as well as load change and input voltage responses for both loops.

• 6 Discretization of the Designed Controller: Comparison between the different methods of discretization and development of the different equations in differences for each type of compensator.

• 7 Prototype Validation: Verification of the double loop behavior on a 3.3 kW LLC prototype with an MPS control card. Analysis in steady state and with disturbances in both load and input voltage.
Chapter 2

Resonant Converter Topology

Resonant converters are based on the resonance effect which is the exchange of energy between reactive elements or to be more precisely between an inductance and a capacitance. Ideally once the system is excited with electrical energy, it will remain oscillating at the resonance frequency. In practice, passive parasitic elements will dissipate the energy in form of heat. The resonance frequency is determined by the reactive elements.

2.1 Resonant Tank

There are two different types of resonant networks (series and parallel) depending on the position of the reactive elements [6, Chapter 19].

2.1.1 Series Network

In this type of circuit the inductor and the capacitor are connected in series (figure 2.1) and the transfer function can be expressed as:

\[
H(s) = \frac{v_o(s)}{V_s(s)} = \frac{R_C}{R_C + sL + \frac{1}{sC}} = \frac{s}{Q_w w_r} \left( \frac{s}{w_r} \right)^2 + \frac{s}{Q_w w_r} + 1
\]

were:
\[w_r = \frac{1}{\sqrt{LC}} = 2\pi f_r; \quad Q_w = \frac{\sqrt{LC}}{R_C};\]

Figure 2.2 shows the bode diagram of a series network \((R_C = 10\Omega; L = 100\mu H; C = 100nF)\). There is a clear dominance of the capacitor before the resonance where the low frequency components are attenuated and a dominance of the inductor after the resonance where the high frequency components are also attenuated.
The LLC topology is a type of series resonant network in where the inductance is replaced by a transformer as isolation is required. This transformer adds two parasitic inductances to the circuit: The leakage ($L_r$) that is proportional to the coupling primary-secondary and the magnetizing ($L_m$) one that is related to winding over a ferromagnetic material.

### 2.1.2 Parallel Network

In this type of circuit the inductor and the capacitor are connected in parallel (figure 2.3) and the transfer function can be expressed as:

$$H(s) = \frac{v_o(s)}{V_s(s)} = \frac{Z(s)}{sL} = \frac{sL}{sL} \| \frac{1}{\pi f_r} R_e \frac{1}{R_e} \left( \frac{s}{w_r} \right)^2 + \frac{s}{w_r Q} + 1$$

where:

$$w_r = \frac{1}{\sqrt{LC}} = 2\pi f_r; \ Q_e = R_e \sqrt{\frac{C}{L}}$$

Figure 2.4 shows the bode diagram of a parallel network ($R_e = 100\Omega; L = 100\mu H; C = 100nF$). The system response is the same of a second order low pass filter, low frequencies remain intact but above the resonance all high frequencies are attenuated. This topology is widely used in quasi-resonant structures.
2.2 Switching Network

A Switching Network (SN) is the association of semiconductor devices that create the input signal of a power converter. In general terms there are three types of SN: Half Bridge (HB), Full Bridge (FB) and Push Pull (PP). Since HB and FB are the ones used in this work and the most used in LLC only these will be explained. Nevertheless, if the reader have interest in push pull resonant structures can refer to [13] for an unregulated converter with 93 % reported efficiency.

2.2.1 Half Bridge

Buck, boost and buck-boost converters use it due its simplicity and cost effective solution to generate a square wave signal from the DC power source. In the case of an LLC converter (figure 2.5a) driving the resonant tank with this structure have its pros and cons: On the one hand, it simplifies the driving and is more cost effective, also the RMS voltage applied to the resonant tank is lower than with a FB. This will lead to a lower voltage rating for the resonant capacitor. On the other hand the turn ratio needs to be doubled. This structure is adopted for low-medium power applications, typically $\leq 1$kW.

![Figure 2.4: Parallel resonant network bode diagram.](image)

![Figure 2.5: Half bridge switching network.](image)
Figure 2.5b shows the signals applied to top and bottom switches of the HB structure. Also, it shows the generated voltage in the switch node (the input signal of the resonant tank).

### 2.2.2 Full Bridge

The full bridge switching structure works by joining two half bridge stages operating in counter phase (figure 2.6a). This structure drain power from the input source in both switch node stages, something highly recommended when working with high power or high density converters. Moreover, the virtual input voltage is doubled so the required turn ratio is reduced to the half. This will save space and cooper in the transformer and also reduce the power loss. The cons of FB is that more switching elements are used so there is a higher economical impact.

![Diagram](image)

**Figure 2.6: Full bridge switching network.**

Figure 2.6b shows the signals applied to top and bottom switches in the first branch of FB structure, the second branch uses the same signals but reversed so it is not possible to short-circuit the input voltage. Also, the generated voltage in the switch node (the input signal of the resonant tank).

### 2.2.3 Soft Switching

Soft switching is the phenomenon that contributes to drastically reduce the commutation losses on a power switch. There are two types of soft switching: ZVS (Zero Voltage Switching) and ZCS (Zero Current Switching) depending on the parameter that is decreasing through the commutation device (voltage or current).

The losses in a power switch are distributed between commutation and conduction.

- **Commutation losses**: They depend on how fast the transition between ON and OFF states is. The elements in charge of determining this magnitude involve the reverse recovery of the parasitic diode and the parasitic capacitances (output and gate-source). Basically, this energy dissipation is related to the dynamic behaviour of the switching devices.

- **Conduction losses**: They depend on the switch series resistance \( R_{DS_{ON}} \) and the current through the device. They occur during the ON state.

It can be noticed that the commutation losses are related to the switching frequency, which means that the higher the switching frequency is the higher the commutation losses are. This
becomes a problematic when trying to develop compact solutions because the only way to reduce the size of the reactive components is by increasing the frequency.

The solution to this problem is achieved through soft switching, where the parasitic components of the switching devices and a resonant network operate in a precise way to reduce the commutation losses. In the case of ZVS there will be a small current flowing through the reverse polarity diode (the one that is in the OFF state) that will reduce the drain-source voltage ($V_{DS}$), using a MosFET device, to the anode-cathode direct one ($V_{AK} \approx 0.7V$). In figure 2.7b a graphical comparison between soft and hard switching is shown. The losses in the device are computed with the product between voltage and current.

![Graphical Comparison between Soft and Hard Switching](image)

Figure 2.7: Comparison between traditional hard switching behaviour and soft one.

For further information regarding soft switching operation the reader can refer to [9] where the author explains the reactive elements involved in each part of a switching period and a proper way to dimension them for an optimal operation.

## 2.3 Rectification Stage

The rectification stage is an association of switching devices that converts the transformer’s AC output signal to a non negative pulsating signal that will be filtered by the output stage. There are two different types of rectification stages: Center taped and Full bridge. The design criteria to select one type or the other rely on each design specifications but typically the full bridge structure is used $\geq 1$kW.

### 2.3.1 Center Tapped

The center-tapped structure is similar to a push pull where the transformer has a common point in the middle of the secondary winding. This point delivers the positive line for the rectified output and the negative one returns through the semiconductor depending on the polarisation of the primary side (figure 2.8). The use of this rectification structure is cost effective since only two power switch are used. From the other side, transformer’s secondary winding need to be doubled wasting part of the window area. This solutions is widely adopted for low power and non high density converters. Also, it can help to boost efficiency in low output voltage - high current solutions since conduction losses are halved.

### 2.3.2 Full bridge

Full bridge rectification stage is the same switch configuration that the one explained in 2.2.2 but instead of generating a pulsating signal from a DC source operates the other way around. This
CHAPTER 2. RESONANT CONVERTER TOPOLOGY

2.3. RECTIFICATION STAGE

Figure 2.8: Center-tapped structure states.

type of structure is more expensive than center-tapped but from the other side allow smaller transformers designs up to 41% [10, Chapter 7]. This is because center-tapped produces a discontinuous current in the transformer that increase 1.41 times the apparent power handled.
Chapter 3

LLC Resonant Converter Modeling

Model high order non linear systems usually can lead to complex mathematical analysis, that is the reason why modelling systems by its dominant behaviour and neglect the less important dynamics is a common practice. This will reduce the order of the system and ease the stability analysis. The case of LLC fits on this description since it is a four state variables converter. In this chapter the non linear state equations of the full bridge LLC converter will be presented, followed by a cycle-by-cycle analysis to linearize the converter. Finally, the state equations of the model are extracted and its principal transfer functions announced.

3.1 Non Linear Model

In figure 3.1 the full bridge LLC power converter used in this work is depicted. This converter is based in four reactive elements. $L_r, C_r$ and $L_m$ build up the series resonant tank and in the secondary side $C_o$ will filter the generated AC signal into a constant DC voltage. $S_1$ to $S_4$ work in soft switching operation as explained in 2.2.3 but, since the current flowing through the transformer in resonant operation is sinusoidal, the commutation losses in the rectification devices is also reduced.

![Figure 3.1: Full bridge LLC resonant converter.](image)

From the control point of view, two structures are derived from this converter. On the one hand, when $S1$ and $S4$ are ON then input voltage ($V_s$) is applied to the resonant tank. On the other hand, when $S2$ and $S3$ are ON minus input voltage is applied to the resonant tank. In real operation between each structure commutation there is a death time to ensure soft switching and prevent shoot through events.

Structure $I$, from figure 3.2a applying Kirchhoff, low can be described by the following equations:

$$V_s = v_{L_r} + v_{C_r} + nv_o$$

(3.1)
CHAPTER 3  LLC RESONANT CONVERTER MODELING

3.1  NON LINEAR MODEL

Figure 3.2: Operating modes for LLC full bridge converter: 3.2a) Structure I with positive input voltage. 3.2b) Structure II with negative input voltage.

\[ i_{C_r} = i_{L_r} \]  
\[ v_{L_m} = nv_o \]  
\[ n(i_{L_r} - i_{L_m}) = i_{C_o} + \frac{v_o}{R_L} \]

Rearranging the equations in state variables format:

\[
\begin{align*}
L_r \dot{i}_{L_r} &= V_s - v_{C_r} - nv_o \\
C_r \dot{v}_{C_r} &= i_{L_r} \\
L_m \dot{i}_{L_m} &= nv_o \\
C_o \dot{v}_o &= n(i_{L_r} - i_{L_m}) - \frac{v_o}{R_L}
\end{align*}
\]

Structure II from figure 3.2b applying Kirchhoff low can be described by the following equations:

\[ 0 = V_s + v_{L_r} + v_{C_r} + nv_o \]  
\[ i_{C_r} = i_{L_r} \]  
\[ v_{L_m} = nv_o \]  
\[ n(i_{L_r} - i_{L_m}) = i_{C_o} + \frac{v_o}{R_L} \]

Rearranging the equations in state variables format:

\[
\begin{align*}
L_r \dot{i}_{L_r} &= -V_s - v_{C_r} - nv_o \\
C_r \dot{v}_{C_r} &= i_{L_r} \\
L_m \dot{i}_{L_m} &= nv_o \\
C_o \dot{v}_o &= n(i_{L_r} - i_{L_m}) - \frac{v_o}{R_L}
\end{align*}
\]

At this point, with traditional fixed frequency converters we use State-Space Average Modelling (SSAM) [8] theory to combine both set of equations 3.5 and 3.10 into an averaged model. After this operation, the system can be linearized with the small signal analysis to properly obtain the converter transfer functions. In this case, this theory can not be applied by the following reasons:

- The average operator behaves as a low pass filter, in this converter structure \( i_{L_r}, i_{L_m} \) and \( v_{C_r} \) only have high frequency components under steady state and resonance switching frequency. So all the information regarding these state variables is lost.
The averaging process requires a fixed averaging period, usually the converters switching period. In this case, the converter operates at different switching frequencies (control variable) under a 50% duty cycle.

- The ripple of $i_{Lr}$, $i_{Lm}$ and $v_{Cr}$ state variables cannot be neglected in front of their DC component.

Taking into consideration this comments, other methods need to be studied to obtain a linear model of the system.

### 3.2 Averaged Large Signal Model

One viable solution is explained in [4], where the converter dynamics are analysed in a cycle-by-cycle manner. This procedure is based on rearranging the differential equations into a discrete time dependent expressions under resonant switching frequency operation.

The converter remains in structure I the first half of the switching period and the second half in structure II. Since the system will operate at resonance frequency, taking into account 2.1 the discrete time framework is defined by:

$$
k_k = k \frac{t_r}{2} = k \frac{1}{2f_r} = k \pi \sqrt{L_rC_r}$$

(3.11)

where $k$ is a positive monotonically increasing integer set.

![Discrete time framework.](image)

The thesis [4] present a time dependent expressions for each state variables by solving 3.5 and 3.10 differential equations by Extended Describing Function (EDF) method. These expressions describe the behaviour of the converter for all $t$ under certain initial conditions ($X(t_k)$, $X(t_{k+1})$) for each structure. The equations for the structure $I$ are the following:

$$i_{Lm}(t) = i_{Lm}(t_k) + \frac{nv_o(t_k)}{L_m}t$$

(3.12)

$$i_{Lr}(t) = i_{Lr}(t_k) + \left(\frac{C_o}{C_o + n^2C_r}\right)(V_{in} - nv_o(t_k) - v_{Cr}(t_k)) \sin(w_r t) + \frac{nv_o(t_k)}{L_m}t$$

(3.13)

$$v_{Cr}(t) = v_{Cr}(t_k) + \left(\frac{C_o}{C_o + n^2C_r}\right)(V_{in} - nv_o(t_k) - v_{Cr}(t_k))(1 - \cos(w_r t)) + \frac{nv_o(t_k)}{2L_m}t^2$$

(3.14)
\[ v_o(t) = v_o(t_k) + \left( \frac{n C_r}{C_o + n^2 C_r} \right)(V_{in} - n v_o(t_k) - v_{Cr}(t_k))(1 - \cos(w_r t)) \] (3.15)

The equations for the structure II are the following:

\[ i_{Lm}(t) = i_{Lm}(t_{k+1}) - \frac{n v_o(t_{k+1})}{L_m} t \] (3.16)

\[ i_{Lr}(t) = i_{Lr}(t_{k+1}) + \left( \frac{C_o}{C_o + n^2 C_r} \right) \left( -V_{in} + n v_o(t_k) - v_{Cr}(t_{k+1}) \right) \sin(w_r t) + \frac{n v_o(t_{k+1})}{L_m} t \] (3.17)

\[ v_{Cr}(t) = v_{Cr}(t_{k+1}) + \left( \frac{C_o}{C_o + n^2 C_r} \right) \left( -V_{in} + n v_o(t_k) - v_{Cr}(t_{k+1}) \right) (1 - \cos(w_r t)) + \frac{n v_o(t_{k+1})}{2 L_m} t^2 \] (3.18)

\[ v_o(t) = v_o(t_{k+1}) + \left( \frac{n C_r}{C_o + n^2 C_r} \right) \left( -V_{in} + n v_o(t_k) - v_{Cr}(t_{k+1}) \right) (1 - \cos(w_r t)) \] (3.19)

The author evaluates the system for a step response in a cycle-by-cycle analysis. Taking the transition values in \( t_k \) from one set of equations to another. The conclusion is that the output voltage response is similar to a second order LC circuit. In figure 3.4 the output voltage behaviour is illustrated.

![Figure 3.4: Step response of the non linear system.](image)

One can see that the fundamental frequency of the system can be expressed by:

\[ f_{eq} = \frac{1}{T_{eq}} = \frac{n}{2 \pi \sqrt{L_{eq} C_o}} \] (3.20)

where:

\[ L_{eq} = \frac{n^2 C_r}{C_o} \cos^{-1}\left[ \frac{\pi^2 L_r}{L_{eq} C_o \left( 1 - \frac{n^2 C_r}{C_o} \right)} \right] \approx \frac{\pi^4}{4 L_r} \] (3.21)

At this point, the average large signal equivalent model is defined by its dominant frequency behaviour.

### 3.3 Small Signal Linear Model Analysis

In order to design a proper control loop and ensure the stability of the plant, a small signal model is required. At this point, after the system order reduction the SSAM theory can be applied for the following reasons:
3.3 SMALL SIGNAL LINEAR MODEL ANALYSIS

Figure 3.5: Average large signal equivalent circuit.

- The low pass filter approach from the average operator will not compromise the model as \(i_{Leq}\) and \(v_o\) have a lower frequency dynamics than the averaging frequency.
- The system model is assumed to be working under resonant operation so the fundamental frequency that will be the averaging frequency is fix.
- The ripple on \(i_{Leq}\) and \(v_o\) state variables can be neglected in front of its DC component.

Figure 3.6 illustrates the small signal equivalent circuit obtained from the large signal model explained in 3.2. \(k_f\) is known as dynamic small signal gain assuming resonant operation (eq. 3.22). From this circuit, we can obtain the small signal equations of the system and develop the required transfer functions.

![Small Signal Circuit](image)

\[
k_f = \frac{\partial v_o}{\partial f_s} = -\frac{8V_m L_m}{\pi n L_f f_f} \tag{3.22}
\]

Applying Kirchhoff laws the following equations can be obtained:

\[
\frac{\hat{f}_s k_f}{n} - \hat{v}_{Leq} - \hat{v}_{Co} = 0 \tag{3.23}
\]

\[
\hat{v}_{Leq} = \frac{\hat{v}_{Co}}{R_L} + i_{Co} \tag{3.24}
\]

Rearranging the equations in state variables format:

\[
\begin{cases}
\frac{\dot{i}_{Leq}}{L_{eq}} = n\frac{\hat{f}_s k_f}{n} - n^2 \hat{v}_{Co} \\
C_o \dot{v}_{Co} = \hat{i}_{Leq} - \frac{1}{R_L} \hat{v}_{Co} 
\end{cases} \tag{3.25}
\]

where:
- \(f_s\) is our control variable
- \(\begin{bmatrix} i_{Leq} \\ v_{Co} \end{bmatrix}\) the new state variables vector. For simplicity the small signal components (\(\hat{i}_{Leq}\)) will be expressed without hat (\(i_{Leq}\)).
3.3.1 Transfer Functions

The required transfer functions depend on the control structure. There are two possible options in order to properly regulate the output voltage. Firstly, is a simple voltage loop where the control variable is directly dependent on the output voltage \(v_{Co}\). Secondly, there is the double loop control approach where an outer stage is in charge of regulating the voltage and an inner one controls the current \((i_{Leq})\). Then, a control to current transfer function is required for the inner loop and a current to voltage to the outer one. The features of each control strategy and how to decide between on or the other will be developed in chapter 4.

Regarding control to voltage transfer function, replacing \(i_{Leq}\) into the output voltage expression of 3.25 we obtain:

\[
sC_o v_{Co} = \frac{1}{sL_{eq}}(n_f s k_f - n^2 v_{Co}) - \frac{1}{R_L} v_{Co} \tag{3.26}
\]

Rearranging the terms the control to voltage transfer function can be expressed as:

\[
G_{vf}(s) = \frac{v_{Co}(s)}{f_s(s)} = \frac{k_f}{\frac{n}{\pi}} \frac{C_o L_{eq}}{n^2 s^2 + \frac{L_{eq}}{n^2 R_L} s + 1} \tag{3.27}
\]

where:

\[
w_o = \frac{n}{\sqrt{C_o L_{eq}}}; Q = n R_L \sqrt{\frac{C_o}{L_{eq}}}
\]

Regarding current to voltage transfer function rearranging the voltage expression in 3.25 we obtain:

\[
G_{vi}(s) = \frac{v_{Co}(s)}{i_{Leq}(s)} = \frac{R_L}{R_L C_o s + 1} \tag{3.28}
\]

Finally, 3.28 is replaced in the current expression of 3.25:

\[
L_{eq} s i_{Leq} = n_f s k_f - n^2 (i_{Leq} \frac{R_L}{R_L C_o s + 1}) \tag{3.29}
\]

Rearranging the terms, the control to current transfer function can be expressed as:

\[
G_{if}(s) = \frac{i_{Leq}(s)}{f_s(s)} = \frac{k_f}{\frac{n R_L}{\pi}} \frac{(C_o R_L s + 1)}{\frac{C_o L_{eq}}{n^2 s^2 + \frac{L_{eq}}{n^2 R_L} s + 1}} \tag{3.30}
\]

where:

\[
w_z = \frac{1}{\frac{1}{C_o R_L}}
\]
Chapter 4

Control Design

A control loop is always recommended in a system that operates under certain perturbations. In the case of power converters, these perturbations depend on the application but generally appear in form of input voltage changes and load variations. In most power converters, the desired parameter to control is the output voltage. To do so, feedback networks and compensators are designed to match the system specifications (table 4.1).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>$V_{in}$</td>
<td>390 V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>$V_{out}$</td>
<td>52 V</td>
</tr>
<tr>
<td>Output Current</td>
<td>$I_{out}$</td>
<td>63.5 A</td>
</tr>
<tr>
<td>Output Resistance</td>
<td>$R_L$</td>
<td>0.819 Ω</td>
</tr>
<tr>
<td>Output Power</td>
<td>$P_{out}$</td>
<td>3.3 kW</td>
</tr>
<tr>
<td>Resonant Capacitor</td>
<td>$C_r$</td>
<td>132 nF</td>
</tr>
<tr>
<td>Resonant Inductor</td>
<td>$L_r$</td>
<td>41.5 uH</td>
</tr>
<tr>
<td>Resonance Frequency</td>
<td>$f_r$</td>
<td>68 kHz</td>
</tr>
<tr>
<td>Magnetizing Inductor</td>
<td>$L_m$</td>
<td>311.2 uH</td>
</tr>
<tr>
<td>Equivalent Inductor</td>
<td>$L_{eq}$</td>
<td>102.4 uH</td>
</tr>
<tr>
<td>Output Capacitance</td>
<td>$C_o$</td>
<td>300 uF</td>
</tr>
<tr>
<td>Equivalent Frequency</td>
<td>$f_{eq}$</td>
<td>908 Hz</td>
</tr>
<tr>
<td>Turn Ratio</td>
<td>$n$</td>
<td>7.5</td>
</tr>
</tbody>
</table>

Table 4.1: System component specification.

Regarding the system control performance, the specifications are:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Steady-State Error</td>
<td>$e_{ss}$</td>
<td>zero</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>$f_{BW}$</td>
<td>$\geq \frac{1}{10}f_r$</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>$PM$</td>
<td>$\geq 50^\circ$</td>
</tr>
<tr>
<td>Percentage Overshoot</td>
<td>$PO$</td>
<td>$\leq 5%$</td>
</tr>
<tr>
<td>Settle Time</td>
<td>$T_{ST}$</td>
<td>10ms</td>
</tr>
</tbody>
</table>

Table 4.2: Steady-state and dynamic control specifications.
4.1 Single Loop Structure

A single loop structure (figure 4.1) is the simplest one to control the output voltage. There is no need to sense the output current from the control point of view. This confirm that a single loop controller leads to a more economical solution.

![Figure 4.1: Single voltage loop control diagram.](image)

Analysing the frequency response (figure 4.2) of the frequency to voltage transfer function (eq. 3.27) enables us to observe a second order behaviour with poor low frequency gain. To assure static and dynamic system performances, the controller \( G_v \) need to be properly tuned [3].

![Figure 4.2: Frequency to voltage transfer function.](image)

Low frequency asymptote:

\[
\lim_{w \to 0} |G_{vf}(jw)|_{dB} = 20\log\left(\frac{|k_f|}{n}\right) = -54.21 dB
\]  \hspace{1cm} (4.1)
4.1 SINGLE LOOP STRUCTURE

CHAPTER 4. CONTROL DESIGN

High frequency asymptote:

\[
\lim_{w \to \infty} |G_{vf}(jw)|_{db} = 20 \log \left( \frac{|k_f|}{n} \right) - 40 \log \left( \frac{w}{w_o} \right) = -\infty \quad (4.2)
\]

Value at \(w_o\):

\[
|G_{vf}(jw_o)|_{db} = 20 \log \left( \frac{|k_f|}{n} \right) + 20 \log(Q) = -33.77 \text{dB} \quad (4.3)
\]

where:

\[w_o = \frac{n}{\sqrt{L_{eq}C_o}}\]

Controller design statements:

- The system response is very similar to a voltage mode buck converter with a phase shift of 180° due the negative sign in the \(k_f\) coefficient (eq. 3.22).
- The un-compensated frequency response ensure enough phase (\(\geq 50^\circ\)) to guaranty stability for the system.
- This system can be controlled with a simple Proportional Integrator (PI) that will provide enough bandwidth, phase margin and zero steady state error.

In a frequency control design the equations to be fulfilled are:

\[
G_{vOL}(s) = G_c(s) \cdot G_{vf}(s) \quad (4.4)
\]

\[
\left\{ \begin{array}{l}
|G_{vOL}(jw_c)|_{db} = |G_c(jw_c)|_{db} + |G_{vf}(jw_c)|_{db} = 0 \text{dB} \\
\angle G_{vOL}(jw_c) = \angle G_c(jw_c) + \angle G_{vf}(jw_c) = -180^\circ + \text{PM}
\end{array} \right. \quad (4.5)
\]

where \(w_c\) is the cross over frequency for the open loop compensated system \(G_{vOL}(s)\).

Tuning a PI compensator to ensure the open loop frequency response meet the specifications:

\[
G_c(s) = K_p + \frac{K_i}{s} = \frac{w_p}{s} \left( \frac{s}{w_z} + 1 \right) \quad (4.6)
\]

where:

\[w_z = \frac{K_i}{K_p}; \quad w_p = K_i\]

With the following calculations one can adjust the cross over frequency of the compensated system.

\[
\lim_{w \to 0} |G_c(jw)|_{db} = 20 \log \left( \frac{K_i}{w} \right); \quad \angle G_c(jw) = -90^\circ \quad (4.7)
\]

\[
\lim_{w \to \infty} |G_c(jw)|_{db} = 20 \log(K_p); \quad \angle G_c(jw) = 0^\circ \quad (4.8)
\]

\[
|G_c(jw_c)|_{db} = 20 \log(K_p) \geq 33.77 \text{dB} \Rightarrow K_p = 55 \quad (4.9)
\]

\[
w_z = \frac{w_o}{10} = \frac{n}{10 \sqrt{C_oL_{eq}}} = \frac{K_i}{K_p} \Rightarrow K_i = 235349.5 \quad (4.10)
\]

The figure 4.3 illustrates the open loop system response. With the configured PI compensator (eq. 4.11) the cross over frequency is 6965.21 Hz and the phase margin is 60°.
From the control point of view, a double loop structure can provide a better dynamic response. The reason is that it has information of two systems state variables. In applications, like server power supplies, poor control response means that load changes could have an impact on the output voltage causing over or undershoots unacceptable behaviour for this type of solutions. In

$$G_c(s) = \frac{235349.5}{s} \left( \frac{s}{4279.1} + 1 \right)$$ (4.11)

From the closed loop system depicted in figure 4.1 in front of a unitary step function ($R(s) = \frac{1}{s}$), one can deduce:

$$E(s) = R(s) - E(s)G_c(s)G_{vf}(s)H_v(s) = R(s) \frac{1}{1 + G_c(s)G_{vf}(s)H_v(s)}$$ (4.12)

$$e_{ss} = \lim_{t \to \infty} e(t) = \lim_{s \to 0} s \cdot E(s) = \lim_{s \to 0} s \cdot \frac{1}{s} \cdot \frac{1}{1 + G_c(s)G_{vf}(s)H_v(s)} = \frac{1}{\infty} = 0$$ (4.13)

Therefore, the steady state error is zero and consequently indicating the good performance of the compensated system.

### 4.2 Double Loop Structure

From the control point of view, a double loop structure can provide a better dynamic response. The reason is that it has information of two systems state variables. In applications, like server power supplies, poor control response means that load changes could have an impact on the output voltage causing over or undershoots unacceptable behaviour for this type of solutions. In
those situations, the double loop control is able to achieve a better voltage regulation cancelling these undesired effects.

![Figure 4.4: Double loop voltage-current diagram.](image)

### 4.2.1 Design of the Inner Current Loop Compensator

In a double loop structure the design procedure consist in tuning first the inner loop (current); assuming the reference coming out from the outer loop is constant. This approximation can be done because the dynamics of the loops are different; the bandwidth of the outer one is set at least one decade below the inner one.

![Figure 4.5: Inner current loop control diagram.](image)

Analysing the frequency response (figure 4.6) of the frequency to current transfer function (eq. 3.30), we observe a second order behaviour with poor low frequency gain. To guarantee static and dynamic system performances, the controller \( G_i \) needs to be properly tuned.

**Low frequency asymptote:**

\[
\lim_{w \to 0} |G_{vf}(jw)|_{db} = 20 \log \left( \frac{|k_f|}{nR_L} \right) = -52.49 dB
\] (4.14)

**High frequency asymptote:**

\[
\lim_{w \to \infty} |G_{vf}(jw)|_{db} = 20 \log \left( \frac{|k_f|}{nR_L} \right) - 40 \log \left( \frac{w}{w_o} \right) = -\infty
\] (4.15)

Value at \( w_o \):

\[
|G_{vf}(jw_o)|_{db} = 20 \log \left( \frac{|k_f|}{nR_L} \right) + 20 \log(Q) + 20 \log \left( \frac{w_o}{w_z} \right) = -11.63 dB
\] (4.16)

where:

\[
w_o = \frac{n}{\sqrt{L_{eq}C_o}}
\]

Controller design statements:

- The frequency response is very similar to the control to voltage transfer function but in this case there is a zero below the natural frequency \( w_o \) that increases the magnitude.
• The un-compensated frequency response ensures enough phase ($\geq 50^\circ$) to guarantee stability for the system.

• For the inner loop a PI compensator is used providing zero steady state error and the maximum bandwidth allowed by the plant.

$$G_{iOL}(s) = G_i(s) \cdot G_{if}(s)$$  \hspace{1cm} (4.17)

$$\left\{ \begin{array}{l} |G_{iOL}(jw_c)|_{db} = |G_i(jw_c)|_{db} + |G_{if}(jw_c)|_{db} = 0dB \\ \angle G_{iOL}(jw_c) = \angle G_i(jw_c) + \angle G_{if}(jw_c) = -180^\circ + PM \end{array} \right.$$  \hspace{1cm} (4.18)

where $w_c$ is the cross over frequency for the inner open loop compensated system.

The same procedure used in section 4.1 to tune the PI is developed to tune the inner current loop.

$$G_i(s) = K_p + \frac{K_i}{s} = \frac{w_p}{s} \left( \frac{s}{w_z} + 1 \right)$$  \hspace{1cm} (4.19)

With the following calculations one can adjust the cross over frequency of the compensated system.

$$|G_i(jw_c)|_{db} = 20\log(k_p) \geq 11.63dB \rightarrow K_p = 5$$  \hspace{1cm} (4.20)
4.2. DOUBLE LOOP STRUCTURE

\[ w_z = \frac{w_o}{10} = \frac{n}{10 \sqrt{C_o L_{eq}}} = \frac{K_i}{K_p} \rightarrow K_i = 21395.4 \tag{4.21} \]

The figure 4.7 illustrates the open loop system response. With the configured PI compensator (4.22) the cross over frequency is 6533.59 Hz and the phase margin is 150°.

The final expression for the inner current control loop can be expressed as:

\[ G_i(s) = \frac{21395.4}{s} \left( \frac{s}{4297.1} + 1 \right) \tag{4.22} \]

4.2.2 Design of the Outer Voltage Loop Compensator

After having the inner current loop properly compensated, we can start to design the outer one. To reduce the interaction between one loop and the other, the cut off frequency of the outer one is set one decade below (650Hz). This reduces the bandwidth of the overall system but ensures the effectiveness of the designed compensators.

By analysing the frequency response (figure 4.9) of the current to voltage transfer function (eq. 3.28), it is found a second order behaviour with poor low frequency gain. To guaranty static and dynamic system performances, the controller \((G_v)\) need to be properly tuned. As the bandwidth of the loops is far enough, the inner close loop transfer function \((G_{iCL}(s))\) can be neglected to
design the controller.

![Bode Diagram](image)

Figure 4.8: Outer voltage loop control diagram.

Figure 4.9: Current to voltage transfer function.

Low frequency asymptote:

\[
\lim_{w \to 0} |G_{vi}(jw)|_{db} = 20 \log(R_L) = -1.73 dB
\]  
(4.23)

High frequency asymptote:

\[
\lim_{w \to \infty} |G_{vi}(jw)|_{db} = 20 \log(R_L) - 20 \log \left( \frac{w}{w_o} \right) = -\infty
\]  
(4.24)

Value at \( w_o \):

\[
|G_{vi}(jw_o)|_{db} = 20 \log(R_L) - 3 dB = -4.73 dB
\]  
(4.25)
Controller design statements:

- The transfer function presents a first order response.
- There is enough bandwidth in the uncompensated response to guaranty the stability of the system ($\geq 50^\circ$).
- The goal for the design of this compensator is obtain zero steady state error and a bandwidth of 650Hz. This will be achieved with a PI + pole (TYPE $II$). The PI will guaranty a zero steady state error since it have a low frequency pole and the high frequency one will help to reduce the system bandwidth.

\[
G_{vOL}(s) = G_v(s) \cdot (G_{iCL}(s)) \cdot G_{vi}(s)
\]

(4.26)

\[
\begin{align*}
|G_{vOL}(jw_c)|_{db} = |G_v(jw_c)|_{db} + |G_{vi}(jw_c)|_{db} &= 0dB \\
\angle G_{vOL}(jw_c) &= \angle G_v(jw_c) + \angle G_{vi}(jw_c) = -180^\circ + PM
\end{align*}
\]

(4.27)

where $w_c$ is the cross over frequency for the outer open loop compensated system.

To adjust the type $II$ compensator, both poles ($w_{p0}$ and $w_{p1}$) are placed one decade below the natural frequency of the transfer function ($w_o$). Then, the cut off frequency is adjusted with the proportional gain ($K_p$).

\[
G_v(s) = (K_p + \frac{K_i}{s}) \cdot (\frac{1}{\frac{s}{w_{p1}} + 1}) = \frac{w_{p0}}{s} (\frac{s}{w_z} + 1)(\frac{1}{\frac{s}{w_{p1}} + 1})
\]

(4.28)

\[
w_{p0} = w_{p1} = \frac{1}{10} w_o = 407 \frac{rad}{s}
\]

(4.29)

\[
|G_i(jw_c)|_{db} = 20\log(R_L) + 20\log(\frac{w_c}{w_o}) + 20\log(k_p) + 20\log(\frac{w_c}{w_{p0}}) + 20\log(\frac{w_c}{w_{p0}}) = 0 \rightarrow K_p = 17
\]

(4.30)

The figure 4.10 shows the open loop system response. With the configured type $II$ compensator (4.31) the cross over frequency is 638.8 Hz and the phase margin is 50.8°.
The final expression for the outer voltage control loop can be expressed as:

\[
G_v(s) = \frac{407}{s} \left( \frac{s}{24} + 1 \right) \left( \frac{1}{\frac{s}{407} + 1} \right)
\]  
(4.31)

From the closed loop system depicted in figure 4.8 in front of a unitary step function \((R(s) = \frac{1}{s})\), one can deduce:

\[
E(s) = R(s) - E(s)G_v(s)G_{iCL}(s)G_{vi}(s)H_v(s) = R(s)\frac{1}{1 + G_v(s)G_{iCL}(s)G_{vi}(s)H_v(s)}
\]  
(4.32)

\[
e_{ss} = \lim_{t \to \infty} e(t) = \lim_{s \to 0} s \cdot E(s) = \lim_{s \to 0} s \cdot \frac{1}{1 + G_v(s)G_{iCL}(s)G_{vi}(s)H_v(s)} = \frac{1}{\infty} = 0
\]  
(4.33)

Therefore, the steady state error is zero, thus indicating the good performance of the compensated system.
Chapter 5

Simulation

In this chapter, an ideal circuit model - with no losses - is used to analyse the converter waveforms in steady state and also to test the designed compensators. In power electronics, it is highly recommended to simulate the circuit behaviour before to test the prototypes, especially if high voltage and power levels are handled. This operation can help the design engineer to properly design key components, such as: switching devices, inductor wire gauge and resonant capacitor RMS voltage. To do so, we use PSIM® simulation software, which is available in a LITE student version for free. The LLC converter is a hot topic topology in many applications, so there is plenty of information on how to model the control diagram to generate the gate signals with the PSIM software blocks. Periodically, the company behind this software (Powersim Inc.) offers public seminars like [11] to help the users.

5.1 Open Loop

The open loop simulation gives a first approach of the model to ensure that, under nominal conditions, the system works properly. Figure 5.1 shows the circuit schematic of the converter used. In this case the mosfet transistors are driven by a gating block with a square signal of 50% duty cycle and a frequency of 68kHz.

![Figure 5.1: Open loop schematic of the LLC full bridge topology.](image)

In figure 5.2 the open loop and full load start-up of the converter can be seen. There is an important overshoot ($\geq 90\%$) for two main reasons. The first one is that there is no control loop...
and the second, from the very beginning, the converter is switching at the resonance frequency. Power systems regularly include a soft start control, where the voltage is gently driven to its nominal operation point. In LLC resonant converters, this is done by setting the start-up switching frequency two or three times higher than the resonance one, and then proportionally reduce it.

In figure 5.3 the resonant current ($I_r$) and the magnetizing one ($I_m$) are shown. The almost pure sinusoidal shape indicates that the converter is switching at the natural resonance frequency, so the components are well suited for this design.
5.2 Closed Loop

In this section, the control diagrams presented in chapter 4 are simulated in order to determine and improve its dynamic response. To generate the gate signals, we have used the blocks depicted in figure 5.4. They transform the output frequency reference (Hz) into $\frac{rad}{s}$ to feed an internal resetable integrator. The integrator generates a saw-tooth signal with the same frequency requested from the compensator. Then, the sinusoidal block transforms the signal into a sinusoidal one with the same frequency. Finally, a comparator generates the square wave signals for the transistor gates. For more information regarding PSIM blocks the reader can consult [12].

LLC resonant converter, as mentioned earlier, manages the energy flux by means of the switching frequency. The relation between frequency and voltage gain is inversely proportional (increase frequency - reduce voltage). This interdependence is taken into account during the control design since the $K_f$ (eq. 3.22) presented in chapter 3 has a negative sign. In the simulation model, it is also contemplated by means of subtracting the control output signal from a maximum operating frequency ($75kHz$). See left part of figure 5.4.

![Figure 5.4: Gate signal generation sub-circuit.](image)

5.2.1 Single Loop (Voltage)

In figure 5.5 one can see the circuit diagram with the single loop voltage control. The compensator designed for the single voltage loop (eq. 4.11) is implemented splitting the proportional and the integrator part. In this way the response can be analysed independently and adjusted more precisely. Values in black are adjusted to meet the desired dynamic response (table 4.2).

![Figure 5.5: Single loop control LLC converter PSIM schematic.](image)
Figure 5.6: Single loop response under a 15 to 45A load step and an input voltage perturbation.
As shown in figure 5.6 that the control loop is regulating the output voltage to 52V under different load and input conditions. The analytically calculated values set a starting point that worked well but can be improved.

The first thing we notice is the slow response of the integrator \((37457 \text{ Hz} / 235349.5 \text{ rad/s})\) in-front of perturbations. This lead to a relaxed tendency to cancel the error but, in the framework of operation (10ms), appears as a small error \((\geq 0.5V)\) so a bad load and line regulation.

Secondly, the fact that with a high proportional gain important overshoots and non steady operation appear in the output voltage. This is due the fast dynamics of this element, even the contribution to the output signal is low in comparison with the integrator, and it can modify the output frequency enough to observe the perturbations. Low pass filtering the output voltage sensed signal could also reduce this inconvenience.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Analytical</th>
<th>Adjusted</th>
</tr>
</thead>
<tbody>
<tr>
<td>Steady-State Error</td>
<td>(e_{ss})</td>
<td>0.13 V</td>
<td>0.04 V</td>
</tr>
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<td>Load Regulation</td>
<td>(Load_{Reg.})</td>
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<td>0.25 %</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>(Line_{Reg.})</td>
<td>1.21 %</td>
<td>0.52 %</td>
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<tr>
<td>Percentage Overshoot</td>
<td>(PO)</td>
<td>5.15 %</td>
<td>5.15 %</td>
</tr>
<tr>
<td>Settle Time</td>
<td>(T_{ST})</td>
<td>(\geq20\text{ms})</td>
<td>14.6 ms</td>
</tr>
</tbody>
</table>

Table 5.1: Dynamic response results with single loop.

5.2.2 Double Loop (Current - Voltage)

In figure 5.7 the circuit simulation model for the double loop control is depicted. The compensators designed (voltage eq. 4.31 and current eq.4.22) are implemented in the same way that in the single loop structure (5.2.1). Values in black are adjusted to meet the desired dynamic response (table 4.2).

![Double loop control LLC converter PSIM schematic](image)
Figure 5.8: Double loop response under a 15 to 45A load step and an input voltage perturbation.
The analytically designed control seems to have a faster response than the single loop, but there is the same problem with the integrative constants. The natural response of the system would be driving the voltage towards the reference value due to the integrator (65 Hz / 408.4 rad/s) but analyzing the system in this time framework (10ms) it results in a small error.

Another problem was that a too slow response on the outer loop cause a wrong reference for the current ($I_{ref}$) loop. This behaviour also forces the system to a non zero steady state as the inner loop is not working properly.

By increasing the pole and integrator constants the system have a faster response and less steady state error. Regarding the proportional gain for the outer loop, increase it, also help to reduce the settle time but higher values than 45-50 will destabilize the system causing oscillations in the output voltage.

The simulation results, figure 5.8, shows how the adjusted compensators can regulate the output voltage to 52V applying different perturbations. Table 5.2 summarize the values obtained from both the analytical and the adjusted analyses.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Analytical</th>
<th>Adjusted</th>
</tr>
</thead>
<tbody>
<tr>
<td>Steady-State Error</td>
<td>$e_{ss}$</td>
<td>1.57 V</td>
<td>0.02 V</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>$Load_{Reg.}$</td>
<td>1.98 %</td>
<td>0.23 %</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>$Line_{Reg.}$</td>
<td>3.27 %</td>
<td>0.27 %</td>
</tr>
<tr>
<td>Percentage Overshoot</td>
<td>$PO$</td>
<td>1.35 %</td>
<td>4.4 %</td>
</tr>
<tr>
<td>Settle Time</td>
<td>$T_{ST}$</td>
<td>$\geq$20ms</td>
<td>9.8 ms</td>
</tr>
</tbody>
</table>

Table 5.2: Dynamic response results with double loop.

The table 5.3 compare the steady state and dynamic response figures of each solution. It is obvious that with a voltage loop the system can perfectly operate, but including the inner one the dynamic and static performance are improved.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Single Loop</th>
<th>Double Loop</th>
</tr>
</thead>
<tbody>
<tr>
<td>Steady-State Error</td>
<td>$e_{ss}$</td>
<td>0.04 V</td>
<td>0.02 V</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>$Load_{Reg.}$</td>
<td>0.25 %</td>
<td>0.23 %</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>$Line_{Reg.}$</td>
<td>0.52 %</td>
<td>0.27 %</td>
</tr>
<tr>
<td>Percentage Overshoot</td>
<td>$PO$</td>
<td>5.15 %</td>
<td>4.4 %</td>
</tr>
<tr>
<td>Settle Time</td>
<td>$T_{ST}$</td>
<td>14.6 ms</td>
<td>9.8 ms</td>
</tr>
</tbody>
</table>

Table 5.3: Double and single loop dynamic response comparison.

Finally figure 5.9 shows the bode diagrams for the analytical and the adjusted type II compensators. The open loop with the adjusted compensator have less phase margin but more bandwidth. Also, the low frequency gain is doubled. This features lead to a system with faster response and better low frequency error rejection, but less stable.
Figure 5.9: Open loop frequency response (blue) for the compensated current to voltage transfer function (orange) and the adjusted (purple). Type $II$ analytical compensator response (yellow) and adjusted (green).
Chapter 6

Discretization of the Designed Controller

Analog control has been traditionally used in power electronics to regulate the state variables of the energy converters. The reason for it is that it offers a low cost and simple solution with more than enough bandwidth for most applications. With the development of higher power converters and more complex topologies (power factor corrector and inverter), the use of digital control systems became a necessity. The main problem at the beginning of digital control was that low resolution and processing power could lead to unstable solutions. This set a restriction, in terms of switching frequency, that limited the size of power converters.

With the information era, a new digital systems state of art offers power electronics the possibility of using high resolution Analog to Digital Converters (ADC) and Pulse Width Modulation (PWM) signals combined with a high computation power in relatively small devices. This framework made that digital control systems became more and more common in high end solutions. Also, qualities like flexibility, build-in protections and the possibility to implement higher order controllers are leading to that direction.

From the mathematical point of view, certain operations need to be performed before the implementation of the control law. Figure 6.1 illustrates the double loop control diagram highlighting the parts that will be implemented in the digital system (Micro Controller Unit - MCU). Notice that voltage and current compensators no longer depend on $s$ but on $z$. The reason is that the digital system operates under discrete time domain instead of a continuous one. The goal of this chapter is to present the different conversion methodologies for the compensator transfer functions and decide the best for the current design.

![Figure 6.1: Digital double loop control diagram.](image-url)
The compensators used in chapter 4 are the Proportional Integral (PI) and the Type II, which is essentially a PI plus a high frequency pole. In order to simplify the mathematical expressions the compensators designed will be analyzed in separate blocks \((A[z], B[z], Z[z] \text{ and } W[z])\).

\[
F'(s) = \frac{K_i}{s} \cdot E(s) \rightarrow F'[z] = A[z] \cdot E[z] + B[z] \cdot F'[z] \quad (6.1)
\]

\[
I(s) = \frac{w_p}{s + w_p} \cdot F(s) \rightarrow I[z] = Z[z] \cdot F[z] + W[z] \cdot I[z] \quad (6.2)
\]

In this application an M4 ARM platform with the following characteristics will be used.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control Processing Unit</td>
<td>(CPU_b)</td>
<td>32 bit</td>
</tr>
<tr>
<td>Maximum Clock Frequency</td>
<td>(f_{CLK})</td>
<td>120 MHz</td>
</tr>
<tr>
<td>Analog interface</td>
<td>(ADC_b)</td>
<td>12 bit</td>
</tr>
<tr>
<td>Sampling Time</td>
<td>(T)</td>
<td>14.5 (\mu s)</td>
</tr>
<tr>
<td>Timer</td>
<td>(PWM_b)</td>
<td>16 bit</td>
</tr>
</tbody>
</table>

Table 6.1: Digital platform specifications.

### 6.1 Forward Euler Method

The forward Euler method approximates the Continuous Time (CT) system in to a Discrete Time (DT) as \(kT \leq t \leq (k + 1)T\) by the derivative in \(kT\). This means that in the difference equation the value of the output depends on the error of the previous sample.
One can define the mapping of a CT into a DT system by replacing its zeros and poles with eq. 6.3.

\[ z = e^{Ts} \]  

(6.3)

Taking into account that a function \( y = f(x) = e^{Tx} \) evaluated around \( x = 0 \) can be approximated as:

\[
\begin{align*}
    y &= f(0) + \frac{df(x)}{dx}|_{x=0} \cdot x + \frac{d^2f(x)}{dx^2}|_{x=0} \cdot x^2 + \ldots + \frac{d^n f(x)}{dx^n}|_{x=0} \cdot x^n \\
    \quad &\quad \text{Truncating at first term: } y \simeq 1 + Tx
\end{align*}
\]  

(6.4)

Replacing \( s \) in eq.6.1 and eq.6.2 with the mapping equation 6.5 one can develop the following expressions.

- **Integrator:**

  \[
  \frac{F'(s)}{E(s)} = \frac{K_i}{s} \rightarrow \frac{F'[z]}{E[z]} = \frac{K_i T z^{-1}}{1 - z^{-1}}
  \]

  (6.6)

  \[
  K_i T z^{-1} E[z] = F'[z] - F'[z] z^{-1}
  \]

  (6.7)

  \[
  \begin{cases}
    A[z] = K_i T z^{-1} \\
    B[z] = z^{-1}
  \end{cases}
  \]

  (6.8)

- **Pole:**

  \[
  \frac{I(s)}{F(s)} = \frac{w_p}{s + w_p} \rightarrow \frac{I[z]}{F[z]} = \frac{w_p}{\frac{1}{T z^{-1}} + w_p}
  \]

  (6.9)

  \[
  Tw_p z^{-1} F[z] = I[z] - z^{-1} I[z] + Tw_p z^{-1} I[z]
  \]

  (6.10)

  \[
  \begin{cases}
    Z[z] = Tw_p z^{-1} \\
    W[z] = (1 - Tw_p) z^{-1}
  \end{cases}
  \]

  (6.11)

### 6.2 Backward Euler Method

The backward Euler method approximates the CT system at \((k-1)T \leq t \leq kT\) by the derivative in \(kT\). This means that in the difference equation the value of the output will depend on the error of the actual sample.

![Figure 6.4: Backward approximation of a CT system. Execution and evaluation time.](image-url)
Another option to evaluate the approximation of equation truncated at the first term is:

\[ z = e^{Ts} \rightarrow z^{-1} = e^{-Ts} \approx 1 - Ts \rightarrow s = \frac{1 - z^{-1}}{T} \quad (6.12) \]

Replacing \( s \) in eq. 6.1 and eq. 6.2 with the mapping equation 6.12, one can develop the following expressions.

- **Integrator:**

\[
\frac{F'(s)}{E(s)} = \frac{K_i}{s} \rightarrow \frac{F'[z]}{E[z]} = \frac{K_i T}{1 - z^{-1}} \quad (6.13)
\]

\[
K_i T E[z] = F'[z] - F'[z] z^{-1} \quad (6.14)
\]

\[
\begin{cases}
A[z] = K_i T \\
B[z] = z^{-1}
\end{cases} \quad (6.15)
\]

- **Pole:**

\[
\frac{I(s)}{F(s)} = \frac{w_p}{s + w_p} \rightarrow \frac{I[z]}{F[z]} = \frac{w_p}{\frac{1 - z^{-1}}{T} + w_p} \quad (6.16)
\]

\[
Tw_p F[z] = I[z] - z^{-1} I[z] + Tw_p I[z] \quad (6.17)
\]

\[
\begin{cases}
Z[z] = Tw_p \\
W[z] = z^{-1} - Tw_p
\end{cases} \quad (6.18)
\]

### 6.3 Bilinear Method

The bilinear transform (also known as Tustin’s or trapezoidal transform) [7, Discrete Approximation of Continuous-Time Systems] approximates the CT system by means of the derivatives between samples of the Discrete Time (DT) system. The execution and evaluation times occur in different frames; this introduces a delay between the error and the action.

\[
y_{CT}(t) \quad y_{DT}(k)
\]

\[
y_{DT}(k-\frac{1}{2}T) \quad y_{CT}(k-\frac{1}{2}T)
\]

\[
y_{CT}((k - \frac{1}{2})T) = \frac{y_{DT}[k] + y_{DT}[k - 1]}{2} \quad (6.19)
\]

Figure 6.5: Bi-linear approximation of a CT system. Execution and evaluation time.
\[ \dot{y}_{CT}(k - \frac{1}{2}T) = \frac{yDT[k] - yDT[k - 1]}{T} \]  

(6.20)

Another variant of the eq.6.3 is developed to obtain the mapping equation for the bilinear method.

\[ z = e^{sT} = \frac{e^{\frac{T}{2}s}}{e^{\frac{T}{2}s}} \simeq \frac{1 + \frac{T}{2}s}{1 - \frac{T}{2}s} \rightarrow s = \frac{2}{T} \frac{1 - z^{-1}}{1 + z^{-1}} \]  

(6.21)

Replacing \( s \) in eq.6.1 and eq.6.2 with the mapping equation 6.21 one can develop the following expressions.

- **Integrator:**

\[
\frac{F'(s)}{E(s)} = \frac{K_i}{s} \rightarrow \frac{F'[z]}{E[z]} = \frac{K_i T}{2} \frac{1 + z^{-1}}{1 - z^{-1}}
\]

(6.22)

\[
F'[z] = \frac{K_i T}{2} E[z] + \frac{K_i T}{2} z^{-1} E[z] + z^{-1} F'[z]
\]

(6.23)

\[
\begin{align*}
A[z] &= \frac{K_i T}{2} (1 + z^{-1}) \\
B[z] &= z^{-1}
\end{align*}
\]

(6.24)

- **Pole:**

\[
\frac{I(s)}{F(s)} = \frac{w_p}{s + w_p} \rightarrow \frac{I[z]}{F[z]} = \frac{w_p}{2 \frac{1 - z^{-1}}{1 + z^{-1}}} + w_p
\]

(6.25)

\[
(2 + Tw_p)I[z] = Tw_p (1 + z^{-1}) F[z] + (2 - Tw_p) z^{-1} I[z]
\]

(6.26)

\[
\begin{align*}
Z[z] &= \frac{Tw_p}{2 + Tw_p} (1 + z^{-1}) \\
W[z] &= \frac{2 - Tw_p}{2 + Tw_p} z^{-1}
\end{align*}
\]

(6.27)

### 6.4 Implemented Method

To choose the method that best suits our needs some considerations have to be taken into consideration:

- Firstly, regarding the computation time, the control algorithm needs to be evaluated each switching cycle \((1/68000Hz = 14.5\mu s)\). If the main clock frequency is \(120 \text{ MHz}\) there are 1740 cycles to process the difference equations but also, other peripherals like ADC sensing plus signal conditioning, timer configuration, alarm evaluation and external communications. So the complexity of the control expressions cannot be too high.

- Second, in order to have a fast transient response its interesting that the evaluation of the control law is done with the values captured during the execution time.

- Finally, regarding memory space, since we will work with an MCU, is required to use just the necessary variables. If the control law implies the evaluation of one or two steps before the processing time, this information needs to be properly stored. Since the control is evaluated with different expressions, this can lead to few extra stored variables.
The method that fulfils all the requirements is the Backward Euler. In equation 6.15 the integrator simply requires an anterior sample of the output state but not from the error. Besides, the number of operations that are needed to be performed to evaluate the constants are few. The same consideration applies to equation 6.18 with the pole discretization.

The following equations represent each compensator of the double loop configuration. These expressions can be implemented directly on the digital platform.

- **Proportional Integrator:**
  \[
  F[k] = K_p \cdot E[k] + K_i T \cdot E[k] + F[k-1]
  \] (6.28)

- **Type II:**
  \[
  I[k] = T w_p \cdot (K_p \cdot E[k] + K_i T \cdot E[k] + F[k-1]) + I[k-1] - T w_p \cdot I[k-1]
  \] (6.29)

where:
\[
F[k] = F[z]; \quad F[k-1] = F[z] \cdot z^{-1}
\]
Chapter 7

Prototype Validation

In power electronics, due to the great amount of parasitic elements involved that often are not taken into account in the design process, it is imperative to verify the viability of the proposed solutions in a functional prototype.

7.1 Prototype Description

The prototype is part of a set of evaluation boards that MPS makes available to the public for developing solutions with digital control from a range of powers between 2 and 5 kW. The power electronics market has grown very fast in the last years with the expansion of the server clusters and all kind of electric mobility solutions. This is why more and more customers are interested in compact and efficient solutions.

7.1.1 Hardware Framework

The EVF32020 is an evaluation board designed specifically for low profile (1U) solutions with a high efficiency requirements. It is presented as a front end of a product and requires a pre-regulation stage to raise the bus voltage from the power grid. To meet specifications, the inductive components ($L_r$ and $L_m$) distributed in four elements and are connected series in the primary side and parallel in the secondary side, so as to distribute the high output current. Then the output current and voltage are sensed for the control loops and the primary side current for over load protections.

![EVF32020 schematic diagram.](image)
Otherwise, the control board has a microcontroller based on an ARM M4 core to sense the mentioned signals and later evaluate the control algorithm. The control signals are then generated at the relevant frequency. The use of this type of solution instead of a Digital Signal Processor (DSP) or a Field-Programmable Gate Array (FPGA) significantly reduces the final cost without compromising the performance of the equipment.

![Prototype power stage.](image1)

![Prototype control card.](image2)

### 7.1.2 Firmware Framework

The c-based firmware, through an RS485 protocol, allows the parameters needed to run the control loop. It is also possible to configure the constants to adjust the output voltage, as well as over/under voltage, current and temperature protections.

<table>
<thead>
<tr>
<th>Description</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal Output Voltage</td>
<td>$V_{out}$</td>
<td>52 V</td>
</tr>
<tr>
<td>Maximum Output Current</td>
<td>$I_{max}$</td>
<td>63.5 A</td>
</tr>
<tr>
<td>Under Voltage Lockout</td>
<td>$V_{UV}$</td>
<td>350 V</td>
</tr>
<tr>
<td>Over Voltage Lockout</td>
<td>$V_{OV}$</td>
<td>420 V</td>
</tr>
<tr>
<td>Over Current Lockout</td>
<td>$I_{OC}$</td>
<td>20 A</td>
</tr>
<tr>
<td>Maximum temperature</td>
<td>$T_{max}$</td>
<td>80 ºC</td>
</tr>
<tr>
<td><strong>Voltage Control Loop (TYPE II)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Proportional Gain</td>
<td>$K_p$</td>
<td>40</td>
</tr>
<tr>
<td>Integral Gain</td>
<td>$K_i$</td>
<td>10000</td>
</tr>
<tr>
<td>High Frequency Pole</td>
<td>$w_p$</td>
<td>500</td>
</tr>
</tbody>
</table>

### Current Control Loop (PI)

<table>
<thead>
<tr>
<th>Description</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proportional Gain</td>
<td>$K_p$</td>
<td>5</td>
</tr>
<tr>
<td>Integral Gain</td>
<td>$K_i$</td>
<td>3405</td>
</tr>
</tbody>
</table>

Table 7.1: General User Interface (GUI) programmable parameters.
7.2 Test Set-up

The set-up to verify the prototype will have the usual laboratory equipment, that is, an oscilloscope, power supply and electronic load. Besides, in this type of devices it is necessary to use the correct instruments for the sensing of certain signals, since it is not possible to join primary and secondary with the same reference of the oscilloscope. For current sensing, a transducer type probe is used in the case of pulsed signals and a shunt resistor in the case of continuous signals.
Figure 7.5: Test set-up with power source, load and thermal monitoring.

Figure 7.6 illustrates the connection diagram between the laboratory equipment and the power stage. Once the system is powered, high voltage signals are present so in order to avoid injuries all must be properly wired before turning on the power supply.

Figure 7.6: Connection diagram.

### 7.2.1 Instrumentation

The following table lists the model and main characteristics of the laboratory equipment used.

<table>
<thead>
<tr>
<th>Description</th>
<th>Model</th>
<th>Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electronic Load</td>
<td>EA-ELR 9500-90</td>
<td>500 V 90 A 10.5 kW</td>
</tr>
<tr>
<td>Power Supply</td>
<td>EA-PSI 9500-90</td>
<td>500 V 90 A 15 kW</td>
</tr>
<tr>
<td>Oscilloscope</td>
<td>R&amp;S RTM3004</td>
<td>4 ch. 5 Gsa/s 10 bit ADC</td>
</tr>
<tr>
<td>High Voltage Probe</td>
<td>R&amp;S RT-ZH10</td>
<td>100:1 400 MHz</td>
</tr>
<tr>
<td>Isolated Voltage Probe</td>
<td>R&amp;S RT-ZD01</td>
<td>100:1/1000:1 100 MHz</td>
</tr>
<tr>
<td>Current Probe</td>
<td>PEM Rogowski CWT</td>
<td>300 A 20.0 mV/A</td>
</tr>
<tr>
<td>Multi-meter</td>
<td>FLUKE 179</td>
<td>True RMS 1000 V 10 A</td>
</tr>
<tr>
<td>Thermal Camera</td>
<td>FLIR E6</td>
<td>±2ºC</td>
</tr>
</tbody>
</table>

Table 7.2: Laboratory equipment used during the prototype tests.
7.2.2 Static Performance

Once the system is connected, the most representative waveforms under nominal conditions of the open-loop system can be captured (fig. 7.7 primary and fig. 7.8 secondary). In this way, as in the simulation section, the correct operation of all components is verified in open loop operation.

Figure 7.7: C2: Switch Node Primary side ($SW_p$), C3: Resonant inductor current ($I_{Lr}$), C4: Output voltage ($v_o$)

Figure 7.8: C2: Switch Node Secondary side ($SW_s$), C3: Secondary current current ($I_{sec}$), C4: Input voltage ($V_s$)
7.2.3 Dynamic Performance

Once the open-loop system properly generates the signals, the closed-loop converter with the designed compensators can be analyzed.

Figures 7.9 and 7.10 show the system performance in front of input voltage perturbations. The power supply is configured to generate a square waveform from 385 to 395 V and the load is kept constant at 50 A.

Figure 7.9: C1: Output current ($I_{out}$), C2: Output voltage ($v_o$), C4: Input voltage ($V_s$)

Figure 7.10: C1: Output current ($I_{out}$), C2_AC: Output voltage ($v_o$), C4_AC: Input voltage ($V_s$)
Figures 7.9 and 7.10 show the system performance in face of load perturbations. The electronic load is configured to generate an square waveform from 15 to 45 A and the input voltage is kept constant at 390 V. This represents a load step of 20 to 70%.

Finally, table 7.3 summarizes a comparison between the simulation results and the experimental ones. It can be observed that, although they are not the same, are quite similar. The greatest difference is the high frequency oscillation present in the simulations but not int the prototype. The more viable explanation for this effect is that, in the simulation model, the output capacitor
do not have any series parasitic resistance. This could lead to a resonance effect between it and the transformer component.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Simulation</th>
<th>Prototype</th>
</tr>
</thead>
<tbody>
<tr>
<td>Steady-State Error</td>
<td>$e_{ss}$</td>
<td>0.02 V</td>
<td>0.05 V</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>$Load_{Reg.}$</td>
<td>0.23 %</td>
<td>0.10 %</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>$Line_{Reg.}$</td>
<td>0.27 %</td>
<td>0.86 %</td>
</tr>
<tr>
<td>Percentage Overshoot</td>
<td>$PO$</td>
<td>4.4 %</td>
<td>4.8 %</td>
</tr>
<tr>
<td>Settle Time</td>
<td>$T_{ST}$</td>
<td>9.8 ms</td>
<td>15 ms</td>
</tr>
</tbody>
</table>

Table 7.3: Simulation and prototype dynamic response comparison.
Chapter 8

Conclusions and Future Works

8.1 Conclusions

In this work we have presented a resonant structure full bridge LLC with which you can design compact converters with powers greater than 1 kW. Through the phenomenon of soft switching, reducing the switching losses of the device, is possible to obtain very high efficiencies for an isolated converter.

After obtaining the non-linear model of the converter, the problem in using the standard techniques to linearize the state equations is observed and it is decided to develop a small signal linearized model presented in [4]. From this model one can obtain and analyze the transfer functions of the system. A behavior similar to the Buck converter topology is observed due to the reduction of four to two state equations. This simplifies the control design as only low frequency dynamics are taken into account.

Once the control has been designed, simulations on a lossless model show that the approach is realistic and does not impede the control to regulate the output voltage in the face of disturbances. Even though the control designed in chapter 4 is fully functional, the compensators’ constants are adjusted to obtain a better response (lower settle time and lower overshoot).

The backward approximation method allows us to discretize the control algorithm and present the difference equations to be implemented in the digital platform. This method offers a good balance between computation time and a quick response in front of an error. This is finally demonstrated in the tests on the MPS EVF32020 platform reporting an efficiency higher than 96% for all load conditions. Comparing with the state of the art in reference designs ([1],[5]) the prototype presents a good dynamic and static behavior.

On a personal level, this work has allowed me not only to learn from the field of digital control for medium power converters but also to know deeper and better one of the most used topologies for high end solutions as it is the LLC converter. Both the results obtained and the opportunity to share experiences with the academic team and co-workers encourage me to continue growing in the world of power electronics.
8.2 Future Works

Once the project is finished and having a global vision of it, certain improvements are determined to optimize the behavior of both the analysis and the prototype.

- To include in the model presented in figure 3.6 the perturbations for the input voltage and output current. In this way, it would be possible to analyze the transfer functions of these new variables with respect to the state variables.

- To evaluate the compensators on the bode diagram for different load conditions, input voltage and component tolerances. This would allow to predict possible instabilities and would give the possibility to make a worst case analysis to determine the constants.

- To evaluate the bode diagram of the discrete compensators and observe the response for the different methods. This would give another argument when selecting the approach to be implemented.

- For a better concordance between the simulation and the behavior of the prototype, the control blocks could be replaced by a Dynamic-link Library (DLL). By this, the only thing that would differ between simulation and design would be the unmodelled parasitic components.

- In terms of the prototype, it has been observed a good performance but can be improved in some aspects such as thermal dissipation especially in the secondary, where there are more conduction losses. On the other hand, when making high load changes the control reduces the working frequency to the minimum configured. In this situation some element of the resonant tank (probably the inductance) enters almost saturation by triggering the current and rapidly increasing the output voltage. A possible solution is to modify the control constants to avoid a sudden response, this would make the stabilization time longer. Another possibility would be to design the component for a lower operating frequency to ensure that it works in its linear area.
Bibliography


Appendix A

Control Design Files

- **SingleVoltageLoop.m**: Evaluation file to tune the PI for the single loop voltage control.

```matlab
clear all
close all
cle

% Load packages
pkg load control
s = tf('s');

% INPUT PARAMETERS
% OUTPUT
Vout_min = 42;
Vout_max = 70;
Vout = 52;
Iout = 63.5;
Pout = Vout*Iout;

% INPUT
Vin_min = 370;
Vin = 390;
Vin_max = 410;

% COMPONENTS
Lr = 41.5E-6;
Lm = 311.2E-6;
Cr = 132E-9;
n = 7.5;
Ln = Lr / Lm;
fr = 1/(2*pi*sqrt(Lr*Cr));
Co = 300E-6;
RL = Vout/Iout;

kf = -(8*Vin*Lm)/(pi*n*Lr*fr);
Leq = (pi^2/4)*Lr;
```
% VOLTAGE COMPENSATOR \(\text{[PI (1p1z)]}\)

\[ \begin{align*}
Ki & = 235349.5; \\
Kp & = 55; \\
Wp & = Ki; \\
Wz & = Ki / Kp; \\
Ge & = Kp + Ki / s;
\end{align*} \]

% PSIM CONSTANTS \([K, T]\)

% printf("PSIM constants\n");
% printf("K is : %d \n", Ki);
% printf("T is : %d \n", Kp/Ki);

% EVALUATION

\[ G_{vf} = \frac{k f}{n} \ast \frac{1}{((Co \ast Leq) / n^2) \ast s^2 + (Leq / (n^2 \ast RL)) \ast s + 1)}; \]
figure (1);
bode (Gvf);

Gvol = Ge \ast Gvf ;
figure (2);
bode (Gvol, Gvf, Ge);

\([\text{GAMMA, PHI, W GAMMA, W PHI}] = \text{margin} (\text{Gvol}); \% \text{Gain Margin, Phase Margin} \]

printf(" \%d V/V " , GAMMA);
printf(" \%d Deg " , PHI);
printf(" \%d Rad " , W PHI);
printf(" \%d Hz " , W PHI/(2*pi));

- **DoubleVoltage.m**: Evaluation file to tune the Type II for voltage in the double loop control.

\begin{verbatim}
clear all
close all
clc

pkg load control
s = tf('s');

% INPUT PARAMETERS
% OUTPUT
Vout_min = 42;
Vout_max = 70;
Vout = 52;
Iout = 63.5;
Pout = Vout*Iout;
\end{verbatim}
APPENDIX A. CONTROL DESIGN FILES

% INPUT
Vin_min = 370;
Vin = 390;
Vin_max = 410;

% COMPONENTS
Lr = 41.5E-6;
Lm = 311.2E-6;
Cr = 132E-9;
n = 7.5;
Ln = Lr / Lm;
fr = 1/(2*pi*sqrt(Lr*Cr));
Co = 300E-6;
RL = Vout/Iout;

kf = -(8*Vin*Lm)/((pi*n*Lr*fr));
Leq = (pi^2/4)*Lr;

% VOLTAGE COMPENSATOR [TYPE II (2p1z)]
Kp = 17;
Ki = 407;
Wp0 = Ki;
Wz = Ki/Kp;
Wp1 = 407;
Gc = (Wp0/s)*(s/Wz + 1)/(s/Wp1 + 1);

% PSIM CONSTANTS [K, T]
##printf("PSIM constants\n");
##printf("K is: %d \n", Ki);
##printf("T is: %d \n", Kp/Ki);

% EVALUATION
Gvi = RL/(1 + s*Co*RL);
figure(1);
bode(Gvi);

Gvol = Gc * Gvi;

Gv = Gc;
figure(2);
bode(Gvol,Gvi,Gv);

[GAMMA, PHI, WGAMMA, W_PHI] = margin(Gvol); %Gain Margin, Phase Margin
printf("Gain Margin: %d V/V \n",GAMMA);
printf("Phase Margin: %d Deg \n",PHI);
printf("Cross Over Freq.: %d Rad \n",W_PHI);
printf("Cross Over Freq.: %d Hz \n",W_PHI/(2*pi));
• **DoubleCurrent.m**: Evaluation file to tune the PI for current in the double loop control.

```matlab
clear all
close all
clc

% Load packages
pkg load control
s = tf('s');

% INPUT PARAMETERS
% OUTPUT
Vout_min = 42;
Vout_max = 70;
Vout = 52;
Iout = 63.5;
Pout = Vout*Iout;

% INPUT
Vin_min = 370;
Vin = 390;
Vin_max = 410;

% COMPONENTS
Lr = 41.5E-6;
Lm = 311.2E-6;
Cr = 132E-9;
n = 7.5;
Ln = Lr / Lm;
fr = 1/(2*pi*sqrt(Lr*Cr));
Co = 300E-6;
RL = Vout/Iout;

kf = -(8*Vin*Lm)/(pi*n*Lr*fr);
Leq = (pi^2/4)*Lr;

% CURRENT COMPENSATOR [PI (1p1z)]
Kp = 5;
Ki = 21395.4;
Wp = Ki;
Wz = Ki/Kp;
Gc = Kp + Ki/s;

% PSIM CONSTANTS [K, T]
###printf("PSIM constants\n");
###printf("K is: %d \n", Ki);
###printf("T is: %d \n", Kp/Ki);

% EVALUATION
```
Gif = ((kf/(n*RL))*(1 + s*RL*Co))/((Leq*Co/n^2)*s^2 + (Leq/(RL*n^2))*s + 1);

figure(1);
bode(Gif);

Giol = Gc* Gif;
Gi = Gc;

figure (2)
bode(Giol,Gif,Gi);

[GAMMA, PHI, WGAMMA, W_PHI] = margin (Giol); %Gain Margin, Phase Margin
printf("Gain Margin: %d V/V \n",GAMMA);
printf("Phase Margin: %d Deg \n",PHI);
printf("Cross Over Freq.: %d Rad \n",W_PHI);
printf("Cross Over Freq.: %d Hz \n",W_PHI/(2*pi));
Appendix B
Simulation Files

- SingleLoop.cct: Net list simulation file to tune the PI for the single loop voltage control.

```
1 .TIME 1E−007 0.05 0 2 0 0 0 0 0
2 BDIODE1 BD11 1 2 3 0 0 0 0 0 0 0 0 0 0 0
3 MOSFET MOS1 4 5 6 0 0 0 0 0
4 MOSFET MOS2 5 7 8 0 0 0 0 0
5 MOSFET MOS4 4 9 10 0 0 0 0 0
6 C C1 5 11 132n 0 0
7 L L1 9 12 41.5u 0 0
8 C C2 3 0 300u 52 0
9 IP Iout 3 13
10 VP2 Vsw 9 5
11 VSEN VSEN1 14 0 15 0.1
12 P P1 16 17 2*3.1415926
13 RESET1_I RESET1_I 17 18 1 0 0 2*3.1415926
14 SIN_R SIN_R 17 18 1 19
15 COMP COMP1 19 0 20
16 NOTGATE NOT1 20 21
17 ONCTRL ON1 21 10
18 ONCTRL ON2 20 22
19 ONCTRL ON3 20 6
20 ONCTRL ON4 21 8
21 TF_IDEAL TI1 23 11 1 2 7.5 1
22 L L3 24 25 311.2u 0 0
23 IP Ir 12 24
24 IP Iprim 24 23
25 IP Im 25 11
26 ISEN ISEN1 13 14 26 1
27 R R1 14 0 3.46 0
28 VSTEP VSTEP1 27 0 1 0.005
29 VDC VDC2 28 0 5.2
30 R R2 14 29 1.74 0
31 SSWI SS1 29 0 30 0 0
32 VSTEP VSTEP5 27 31 1 0.02
33 ONCTRL ON5 31 30
34 VP Vout 14
```
APPENDIX B. SIMULATION FILES

• **DoubleLoop.cct**: Net list simulation file to tune the Type II and the PI for the double loop voltage-current control.

```
. TIME 1E−007 0.05 0 2 0 0 0 0 0
BDIODE1 BD11 1 2 3 0 0 0 0 0 0 0 0 0 0 0 0 0
MOSFET MOS1 4 5 6 0 0 0 0 0
MOSFET MOS2 5 7 8 0 0 0 0 0
MOSFET MOS4 4 9 10 0 0 0 0 0
C C1 5 11 132n 0 0
L L1 9 12 41.5u 0 0
C C2 3 0 300u 52 0
IP Iout 3 13
VP Vsw 9 5
VSEN VSEN1 14 0 15 0.1
P P1 16 17 2*3.1415926
RESETI1 RESETI11 17 18 1 0 0 2*3.1415926
SIN R SIN_R1 18 19
COMP COMPl 19 0 20
NOTGATE NOT1 20 21
ONCTRL ON1 21 10
ONCTRL ON2 20 22
ONCTRL ON3 20 6
ONCTRL ON4 21 8
TF_IDEAL TI1 23 11 1 2 7.5 1
L L3 24 25 311.2u 0 0
IP Ir 12 24
IP Iprim 24 23
```
APPENDIX B. SIMULATION FILES

25  IP Im 25 11
26  ISEN ISEN1 13 14 26 0.1
27  R R1 14 0 3.46 0
28  VSTEP VSTEP1 27 0 1 0.005
29  VDC VDC2 28 0 5.2
30  R R2 14 29 1.74 0
31  SSWI SS1 29 0 30 0 0
32  VP Vout 14
33  VP Rads 17
34  MOSFET MOS3 9 7 22 0 0 0 0 0
35  SUM2 SUM1 28 15 31 1 -1
36  VDC VDC4 32 0 750
37  SUM2 SUM7 32 33 34 1 -1
38  VP Pi 35
39  VDC VDC1 4 36 385
40  VP2 Vin 4 7
41  VP C 33
42  VP E 31
43  SUM2 SUMS 37 26 38 1 -1
44  VP Ii 39
45  I B1 40 39 1 0
46  P P2 38 40 3405
47  P P3 38 35 5
48  SUM2P SUMP6 39 35 41 1 1
49  VP Iv 42
50  I B2 43 42 1 0
51  P P4 31 43 10000
52  P P5 31 44 40
53  SUM2P SUMP7 42 44 45 1 1
54  VP Ei 38
55  VP Iref 37
56  VP Pp 44
57  VSTEP VSTEP8 46 36 5 0.03
58  VSTEP VSTEP7 46 7 10 0.015
59  VSTEP VSTEP5 27 47 1 0.02
60  ONCTRL ON5 47 30
61  VSTEP VSTEP9 48 0 1 0.035
62  R R3 14 49 1.74 0
63  SSWI SS2 49 0 50 0 0
64  VSTEP VSTEP10 48 51 1 0.04
65  ONCTRL ON6 51 50
66  P P6 34 16 100
67  LIM LIM3 41 33 0 120
68  VP Fsw 16
69  TFCTN TFNC2 45 37 1 1 0. 1. 0.002 1.