A simple switching frequency regulated sliding mode controller for a VSI with a full digital implementation

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***Abstract*—This paper describes the design of a first order sliding mode controller for a VSI operating at fixed switching frequency. The proposal is simple, as it does not include any integral or resonant action in the switching function, and good results are obtained in terms of robustness, steady-state tracking error, fast transient response, and low THD. The implementation methodology using a micro controller preserves all the benefits of a continuous time implementation. Moreover, the paper analyses the sliding motion dynamics, and stability conditions are derived. Experimental results obtained with a 2.2 kW inverter show that fixed switching frequency operation and robust output voltage regulation with good performance indexes are achieved.**

***Index Terms*—Sliding mode control, voltage source inverter, fixed switching frequency, nonlinear load**

I. Introduction

Nowadays, voltage source inverters (VSI) are widely used in stand-alone industrial applications as uninterrupted power systems (UPS), or AC grid emulators in small power generation systems (as renewable), suitable for domestic appliances. As a consequence, VSI shall meet good levels of power quality, total harmonic distortion (THD) and transient response. Different PWM-based controllers have been proposed for such systems, as repetitive control [1], [2], predictive control [3], or finite-state machines [4], among others, usually leading to complex control architectures.

Theoretically, sliding mode control is able to provide AC signal with low THD, presenting good transient responses and robust operation with controllers based on a sign function. The drawback is that it assumes infinite switching frequency. In practice, it is feasible to achieve quasi-sliding motion with hysteresis comparators instead of sign functions, operating at finite switching frequency. These type of implementations can be found in [5]–[10], showing very good dynamics and robustness. Unfortunately the application of both hysteretic or SMC control with fixed hysteresis band to VSI results in a variable switching frequency, which produces electromagnetic noise and complicates the filter design. Some approaches have been proposed to overcome this problem [11]–[15]. Among them there is the work of Holmes et al. [11], which adapts the hysteresis of the comparator by using an expression, obtained under some assumptions, that depends on the input voltage and on an estimation of the voltage drop across the load series resistance, or the work of Ho et al. [12], where the fixed switching frequency is achieved by appropriately calculating the on and off intervals of the power transistors. The approaches show good performances keeping the SMC properties, but the algorithms designed to set the switching frequency are, in general, VSI parameter-dependent and require the measure of one or more VSI variables, so the control simplicity is seriously affected.

SMC operation at fixed switching frequency can also be achieved by using a zero averaged dynamics (ZAD) approach. The ZAD implementation determines the value of the control signal that ensures a null average value of the switching surface in a switching period. An application of this control to VSI is found in [14]. Results show good dynamics with low THD and robustness of the controlled system with respect to load variations. However, the high computation requirements of the controller constitutes the main drawback of the proposal.

Several authors have proposed the use of a PWM, operating at fixed switching frequency and performing the so-called PWM-based SMC [16]–[22]. For instance, Abrishamifar et al. [16] smooth the control signal replacing the discontinuous control law $u = \operatorname{sign}(S(X))$ by $\frac{S(X)}{\Phi}$, where $S(X)$ and Φ are the switching surface and the boundary layer parameter, respectively. This technique has an easy control implementation but both tracking error and robustness are highly compromised. Another approach is based on the use of the equivalent control as duty cycle of a PWM. Recalling that the equivalent control is the ideal control that induces the sliding mode dynamics, the design procedure generates the duty cycle as a linear combination of several terms, namely $d = d_{eq} + d_L + d_N$, d_{eq}, d_L and d_N being the equivalent control, the linear term and the nonlinear term, respectively. The added terms are required to ensure convergence to the sliding surface. Among the works that follow this idea we find: Hao et al. [17], where a multiresonant SMC in a grid-connected VSI with an LCL filter is designed; Zheng et al. [18], where a repetitive control is embedded into a discrete-time SMC to enhance the steady-state performance of a VSI; Vieira et al. [19], which presents a combination of proportional plus resonant control and an SMC for a three-phase VSI with LCL output filter connected to the grid, and the interesting work of Pichan et al. [20], where the term $K \operatorname{sign}(S(X))$ is added to the equivalent control to obtain the duty cycle. All these papers achieve good performance indexes (low steady-state errors, low THD, etc.) working at fixed switching frequency, but in general the control designs requiere a trade-off between simplicity and robustness. The

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robustness of the SMC stems from the fact that the control law is independent of the system parameters. Therefore, when the hysteresis-based SMC is replaced by a PWM-based SMC, the control becomes parameter sensitive and the SMC robustness has to be recovered by adding new terms to compensate the parameter dependence of the equivalent control, which in turn leads to more complex control architectures.

An alternative to set the switching frequency in an SMC was proposed in [23], where direct regulation of the switching period is achieved by using an additional loop to adjust the bandwith of a hysteresis comparator. Following the procedures detailed in that work, the switching frequency controller (SFC) is designed here to be applied to SMC VSI guaranteeing convergence of the switching period to its reference value. Differently from [23], where the SMC was implemented with analogue hardware in a low power converter, a much more versatile full digital controller applied to a 2.2kW power inverter is presented in this work. The novelties of the proposal in this paper are:

1) The control scheme is simpler than the ones cited in the above paragraphs. Only the SMC and the switching frequency regulation loops are required to obtain performance indexes close to those inherent to the ideal sliding motion, such as very low THD or fast transient response.
2) The continous time behaviour of a comparator with hysteresis has been emulated in a microcontroller, enforcing the switching function to be constrained in a symmetric hysteresis bandwidth under sliding motion. In this scenario, the average of the switching function is null in steady-state [24]. Therefore, the average value of the steady-state error becomes null as well without using integral or resonant terms in the switching surface.

The article is structured as follows. The VSI model is described in Section II. The sliding mode control is designed in Section III, which also includes the corresponding stability and tracking performance analyses for different loads. Some implementation issues are discussed in Section IV. The experimental results are shown in Section V, and a comparative analysis with different control techniques available in the literature is provided in Section VI. Finally, conclusions are drawn in Section VII.

II. Voltage source inverter model

Figure 1 shows the block diagram of a VSI with the proposed SMC and SFC. The VSI dynamics is described by the following state space equations:

$$C\frac{dv_c}{dt} = i_l - i_o, \tag{1}$$

$$L\frac{di_l}{dt} = -v_c + E\,u, \tag{2}$$

where i_l is the inductor current, v_c is the output voltage, i_o is the load current, L is the inductance, C is the capacitance, and E is the input voltage. The load current depends on the output voltage, namely $i_o = f(v_c)$, f being a function encompassing any reactive linear load, as shown in Figure 1. The power switches are represented by M_1, M_2, M_3, and M_4. Switches M_1 and M_4 are short circuited when $u = 1$ and remain in open state when $u = -1$, whereas M_2 and M_3 work in a complementary way. Therefore, the discontinuous control input u takes values in the discrete set $\{-1, 1\}$.

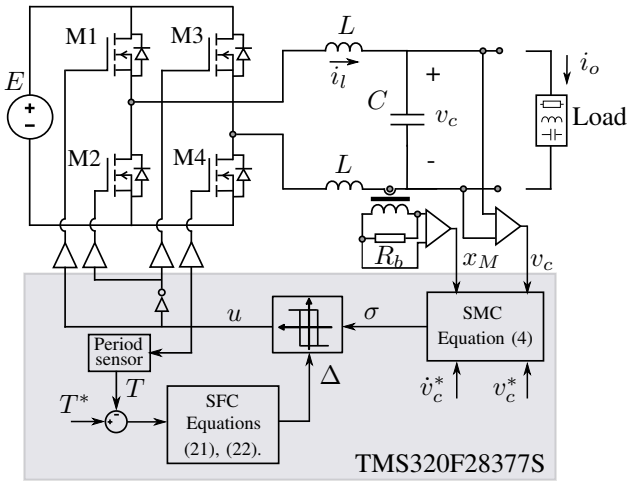

Fig. 1. Block diagram of a VSI circuit scheme with a generic linear load connected at the output, including the SMC and SFC control loops.

III. Sliding mode control design

A. Switching surface

The control goal is to track a sinusoidal reference voltage, v_c^*, at the VSI output. Specifically,

$$v_c^* = A\sin\omega t. \tag{3}$$

The proposed switching function is:

$$\sigma\left(v_c, x_M\right) := \psi_1(v_c^* - v_c) + \psi_2 C\frac{dv_c^*}{dt} - \psi_2\frac{L_x}{MR_b}x_M, \tag{4}$$

where x_M is the signal coming from a current transformer (CT) measuring the high frequency components of the inductor current, and $\psi_1, \psi_2 > 0$ are the switching function parameters.

Notice that the switching function does not include any integral or repetitive term and the inductor current is measured using the CT. The CT is a ferrite core-based current transformer with insertion losses lower than other sensing solutions, such as shunt resistors. Moreover, it is designed to work with high frequencies, thus achieving a bandwidth larger than Hall effect sensors do. Therefore, the CT provides the fast dynamics of the switching function around $\sigma = 0$, this yielding the desired relative degree. Taking into account the magnetic coupling of the CT and considering that the secondary winding of the transformer is loaded with a resistor R_b, the equation that relates the voltage through R_b, x_M, and the current flowing through the transformer primary winding, i_l, is

$$L_x\frac{dx_M}{dt} = -R_b x_M + R_b M\frac{di_l}{dt}, \tag{5}$$

where M and L_x are the mutual and secondary inductances, respectively.

B. Ideal sliding motion

The ideal sliding dynamics is found using the equivalent control method [25]. The equivalent control, u_{eq}, is the control value that guarantees invariance of the sliding manifold, i.e. $\sigma = \dot{\sigma} = 0$. On the one hand, once the surface is reached, i.e. $\sigma = 0$, it stems from (4) that

$$x_M = M\beta \left[g\left(v_c^*\right) - \alpha v_c \right], \tag{6}$$

where $\alpha = \psi_1/\psi_2$, $\beta = R_b/L_x$, and

$$g\left(v_c^*\right) = \alpha v_c^* + C\frac{dv_c^*}{dt}.$$

On the other hand, it follows from (4), (5) that:

$$\dot{\sigma} = \psi_2 \left[\dot{g}\left(v_c^*\right) - \alpha\frac{dv_c}{dt} + \frac{1}{M}x_M - \frac{1}{L}\left(E\ u - v_c\right) \right]. \tag{7}$$

Hence, demanding $\dot{\sigma} = 0$ and using (6) one gets that

$$u_{eq} = \frac{L}{E}\left[\left(\frac{1}{L} - \alpha\beta \right) v_c - \alpha\frac{dv_c}{dt} + \beta g\left(v_c^*\right) + \dot{g}\left(v_c^*\right) \right]. \tag{8}$$

Finally, the ideal sliding dynamics follows taking (8) to (1), (2):

$$\frac{dv_c}{dt} = \frac{1}{C}\left(i_l - i_o\right) \tag{9}$$

$$\frac{di_l}{dt} = -\alpha\beta v_c - \frac{\alpha}{C}\left(i_l - i_o\right) + \beta g\left(v_c^*\right) + \dot{g}\left(v_c^*\right), \tag{10}$$

this yielding

$$C\frac{d^2v_c}{dt^2} + \alpha\frac{dv_c}{dt} + \alpha\beta v_c = C\frac{d^2v_c^*}{dt^2} + (\alpha + \beta C)\frac{dv_c^*}{dt} + \alpha\beta v_c^* - \frac{di_o}{dt}. \tag{11}$$

As expected, the dynamics depends on the output current, i_o. Therefore, the stability of (11) should be analysed for the different (linear or nonlinear) output loads. In particular, when the converter works with a linear load, the output current in the s domain can be expressed as $I_o(s) = V_c(s)Z^{-1}(s)$, $Z(s)$ being the load impedance. Notice that for resistive loads it is $Z(s) = R$, while in the general case it answers to a rational function of s.

Then, the closed-loop transfer function, $T(s)$, stemming from the Input-Output (I/O) system (11) reads as

$$T(s) = \frac{V_c(s)}{V_c^*(s)} = \frac{Cs^2 + (\alpha + \beta C)\, s + \alpha\beta}{Cs^2 + (\alpha + Z^{-1}(s))\, s + \alpha\beta}, \tag{12}$$

where $V_c(s), V_c^*(s)$ denote, respectively, the Laplace transforms of the output voltage, v_c, and its reference, v_c^*, defined in (3). Hence, the poles of $T(s)$ are given by the solutions of

$$1 + G(s)Z^{-1}(s) = 0, \quad \text{with } G(s) = \frac{s}{Cs^2 + \alpha s + \alpha\beta}. \tag{13}$$

Proposition 1. *The I/O linear system with transfer function* (12) *shows a unique $\frac{2\pi}{\omega}$-periodic solution, which is asymptotically stable.*

Proof. Notice that, as $C, \alpha, \beta > 0$, the poles of $G(s)$ in (13) are in the left complex plane; moreover,

$$\mathrm{Re}\left(G(j\omega)\right) = \frac{\omega^2\alpha}{\left(\alpha\beta - \omega^2 C\right)^2 + \omega^2\alpha^2} > 0, \quad \forall\omega.$$

Then, $G(s)$ is a Positive Real (PR) transfer function, and $|\arg\left(G(j\omega)\right)| \leq \frac{\pi}{2}$ [26]. In turn, non-ideal linear loads can be considered as networks that combine resistors, lossy capacitors and lossy inductors, so the impedance $Z(s)$ is dissipative and, consequently, Strictly Positive Real (SPR) [27]. Hence, its inverse, $Z^{-1}(s)$, is also an SPR function [28], and $\left|\arg\left(Z^{-1}(j\omega)\right|\right. < \frac{\pi}{2}$. Therefore, $\left|\arg\left(G(j\omega)Z^{-1}(j\omega)\right)\right| < \pi$, which means that the Nyquist plot of $G(s)Z^{-1}(s)$ neither crosses nor encircles -1. Consequently, by the Nyquist criterion, $1 + G(s)Z^{-1}(s)$ has all its roots in the left complex plane, so $T(s)$ is a stable transfer function, this entailing that the solutions of the corresponding I/O linear system are asymptotically stable.

Finally, (i) the fact that all the poles of $T(s)$ be in the left complex plane guarantees that the unforced I/O linear system with transfer function $T(s)$, i.e. that with $v_c^* = 0$, has no other periodic solutions but $v_c = 0$, and (ii) according to (12), the input of the I/O linear system with transfer function $T(s)$ depends on v_c^* and a number of its derivatives, so it is $\frac{2\pi}{\omega}$-periodic as well. The result is therefore guaranteed by standard theory of linear periodic systems (see [29], for example). □

C. Switching function parameters design

The design of the parameters α and β should guarantee a good behaviour in the sliding mode response and an accurate steady-state tracking performance. On the one hand, assuming that the converter operates with linear load, a proper design of β ensures perfect tracking of the reference for a nominal resistive load. This statement is established in the following proposition.

Proposition 2. *Assume that a resistive load with impedance $Z(s) = R$ is connected to the converter output. If $R = R_n$, with*

$$R_n = \frac{1}{\beta C},$$

then perfect tracking is achieved, i.e. v_c tends asymptotically to the periodic signal $v_c^*(t)$ as t tends to infinity.

Proof. In this case (12) boils down to

$$T(s) = \frac{Cs^2 + \left(\alpha + R_n^{-1}\right) s + \alpha\beta}{Cs^2 + \left(\alpha + R^{-1}\right) s + \alpha\beta}. \tag{14}$$

When $R = R_n$ one has that $T(s) = 1$, so $v_c^*(t)$ is a periodic solution of the ideal sliding dynamics (11). Uniqueness and asymptotic stability stem immediately from the fact that $Cs^2 + \left(\alpha + R^{-1}\right) s + \alpha\beta$ has its two roots in the left complex plane. □

For $R \neq R_n$, Proposition 2 indicates that a steady-state error between v_c and v_c^* occurs, as v_c tends asymptotically to a $\frac{2\pi}{\omega}$-periodic solution different from v_c^*. However, it is possible to keep such a tracking error small enough for values of R belonging to a wide vicinity of the nominal R_n through a proper design of the control parameter α. Replacing $\beta = \frac{1}{R_n C}$ in (14) and defining $\gamma = \frac{1}{RC}$, one gets

$$T(s) = \frac{Cs^2 + (\alpha + \beta C)\, s + \alpha\,\beta}{Cs^2 + (\alpha + \gamma C)\, s + \alpha\,\beta}. \tag{15}$$

The transfer function $T(s)$ has two zeros and two poles with the same natural frequency, $\omega_n = \sqrt{\frac{\alpha\beta}{C}}$, but with different damping factor:

$$\xi_z = \frac{1}{2}\left(\mu + \frac{1}{\mu}\right)$$

for the zeros, and

$$\xi_p = \frac{1}{2}\left(\mu + \frac{R_n}{R}\cdot\frac{1}{\mu}\right)$$

for the poles, with $\mu = \sqrt{\frac{\alpha}{\beta C}}$. The magnitude and phase of $T(s)$ at the reference frequency measure the accuracy of the tracking behaviour, and ideally (when $R = R_n$) they take the values of 1 and 0, respectively, indicating a perfect tracking of the reference. It is clear that to ensure a good tracking performance ω_n should be as high as possible and

$$|\xi_z - \xi_p| = \frac{1}{2\mu}|1 - \frac{R_n}{R}|$$

should take a low value. Both specifications are fulfilled when α takes a high value.

The parameter α is designed to ensure a good dynamics in sliding motion. From (14), the characteristic polynomial of $T(s)$ is:

$$Cs^2 + (\alpha + \gamma C)\, s + \alpha\beta = 0. \tag{16}$$

In order to plot the root locus of (16), the equation is re-written as:

$$1 + \frac{\alpha}{C}\cdot\frac{s+\beta}{s^2+\gamma s} = 0. \tag{17}$$

Figure 2 depicts the root locus when a load satisfying $\gamma = 0.5\,\beta$ is used. The values of the breakaway and break-in points, s_1, s_2, and the corresponding values of α for those points, are also shown.

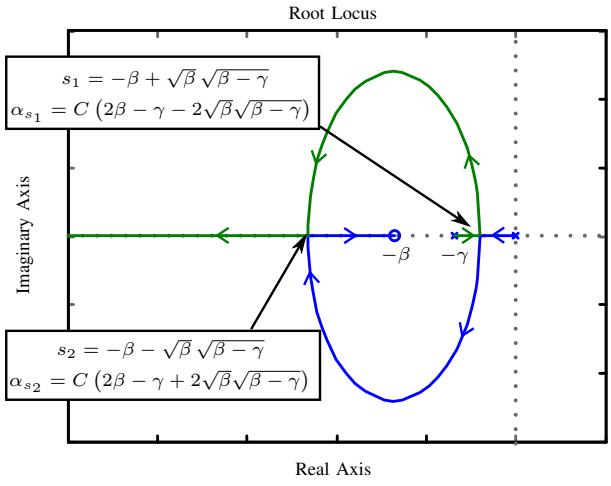

Fig. 2. Root locus of (17) for $\gamma = 0.5\,\beta$.

From the plot, one can infer that the roots of (16) providing a fast overdamped response are obtained when $\alpha > \alpha_{s_2}$. Therefore, in order to ensure an overdamped response whatever the value of the load is, s_2 and α_{s_2} should be evaluated for the expected range of R. Choosing R_n as the minimum resistive load, the working range for γ is $0 < \gamma \leq \beta$. As

$$s_2(\gamma) = -\beta - \sqrt{\beta}\sqrt{\beta-\gamma}$$
$$\alpha_{s_2}(\gamma) = C\left(2\beta - \gamma + 2\sqrt{\beta}\sqrt{\beta-\gamma}\right)$$

are, respectively, increasing and decreasing functions within the working range, it is immediate that, for all $\gamma \in (0, \beta]$,

$$s_2 \in \left(\lim_{\gamma\to 0} s_2(\gamma), \lim_{\gamma\to\beta} s_2(\gamma)\right] = (-2\beta, -\beta]$$
$$\alpha_{s_2} \in \left[\lim_{\gamma\to\beta} \alpha_{s_2}(\gamma), \lim_{\gamma\to 0} \alpha_{s_2}(\gamma)\right) = [\beta C, 4\beta C).$$

Therefore, if α fulfils

$$\alpha > 4\beta C = \frac{4}{R_n},$$

the roots of (16) are overdamped for all $R \in [R_n, +\infty)$. Additionally, according to Figure 2, it is clear that (16) will have a root in the range $(s_2, -\beta)$, thus entailing a transient response with a time constant, τ, at least equal or higher than $(2\beta)^{-1}$ and always smaller than β^{-1}.

As a conclusion, the control parameters design guidelines can be summarized in the following steps:

1) Take the minimum value of the load, R_n.
2) Determine $\beta = \dfrac{1}{R_n C}$.
3) Select $\alpha > \dfrac{4}{R_n}$ to guarantee an overdamped response in the output voltage dynamics for all the expected load conditions.
4) Set the transformer ratio $\left(\dfrac{N_1}{N_2}\right)$ and the secondary inductance L_x of the CT, and the value of ψ_2. Finally, calculate the rest of parameters as $\psi_1 = \alpha\psi_2$, $R_b = \beta L_x$ and $M = L_x\dfrac{N_1}{N_2}$.

Table I shows the converter parameters of the assembled prototype. The sliding mode controller has been designed for a peak power of 3.3 kW, and hence $R_n = 14.7\ \Omega$. Therefore, β has been calculated as $\beta = 680$, and α has been set to $\alpha = 1$. With this design the magnitude and phase of (14) for different load levels between 15 Ω and 200 Ω are plotted in Figure 3. As expected, the amplitude and phase tracking errors are below 1% and 1.5°, respectively, at 50 Hz.

Remark 1. *The switching function parameters depend on the output capacitor value (recall* (4)*). An analysis of the effect of the capacitor variations shows that the maximum values of the amplitude and phase tracking errors at 50 Hz are of 1.4% and 1.52°, respectively, when the capacitance undergoes a 20% variation with respect its nominal value, and the response of the output voltage is still overdamped for variations up to 100%.*

D. Control law and sliding domain

Sliding motion [25] is enforced on $\sigma = 0$ using the discontinuous control law

$$u = \text{sign}(\sigma). \tag{18}$$

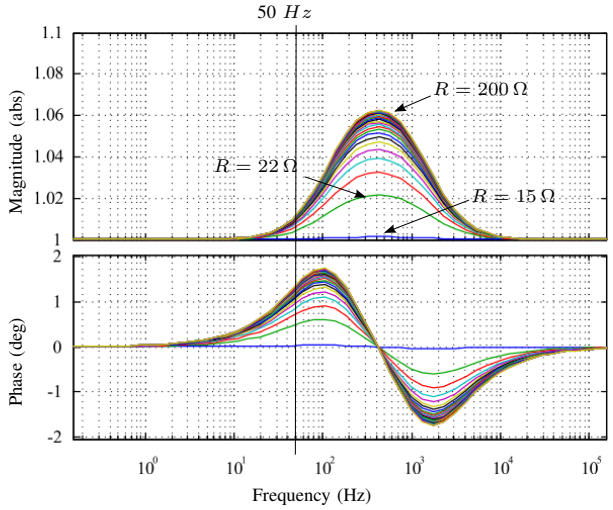

Fig. 3. Frequency response of $T(s)$ in (15) for different resistive loads between 15Ω and 200Ω; $\alpha = 1, \beta = 680$.

Proposition 3. *The control law* (18) *induces sliding motion on the switching surface* $\sigma = 0$ *within the sliding domain given by*

$$-1 < u_{eq} < 1, \tag{19}$$

with u_{eq} *defined in* (8)*.*

Proof. Using (7), (5), (8), and the fact that $E, L, \psi_2 > 0$, it results that

$$\sigma\dot{\sigma} = -\frac{E\psi_2}{L}\sigma\left(\text{sign}(\sigma) - u_{eq}\right) < 0, \forall\sigma \neq 0,$$

whenever (19) is verified. □

E. Switching frequency regulation

SMC is usually implemented by means of hysteresis comparators and therefore the control law in (18) is replaced by:

$$u = \begin{cases} -1 \text{ if } & \sigma < -\Delta_k \quad \text{or } (|\sigma| < \Delta_k \ \& \ \dot{\sigma} > 0) \\ 1 \text{ if } & \sigma > \Delta_k \quad \text{or } (|\sigma| < \Delta_k \ \& \ \dot{\sigma} < 0) \end{cases}, \tag{20}$$

where $\Delta_k > 0$ is a hysteresis added to bound the switching frequency [5]. It is well known that hysteresis comparators with fixed bandwidth lead to a variable switching frequency when used in VSI. In order to get a fixed switching frequency operation this work uses the SFC scheme proposed in [23]. That paper details the design procedure of the SFC for a general SMC controlled affine system and determines the set of hypotheses to be fulfilled in order to guarantee the desired switching frequency regulation. Following those steps the SFC parameter can be set to ensure asymptotic stability of the switching frequency regulation loop. Moreover, note that with the proposed switching function, defined in (4), the switching function derivatives, given by (7), do not depend on the VSI load current. Therefore, the design of the SFC parameter guaranties stability whatever the load connected to the VSI is.

IV. Implementation Details

The SMC and the SFC are implemented using the TMS320F28377S microcontroller (μC) from Texas Instrument, see Figure 1. The control law accelerator (CLA) executes the SMC with a frequency of 1 MHz. In order to keep the expected behaviour of a hysteresis comparator in a discrete time implementation, the emulation strategy proposed in [30] is applied. This methodology assumes piecewise behaviour of σ within the hysteresis region, which is a reasonable assumption under a proper control design (see [23] for details). The technique predicts the incoming value of the switching function, detects if this value is within the hysteresis band or not, and generates a PWM signal in a 1 μs period to ensure the commutation of the switching function at the proper value.

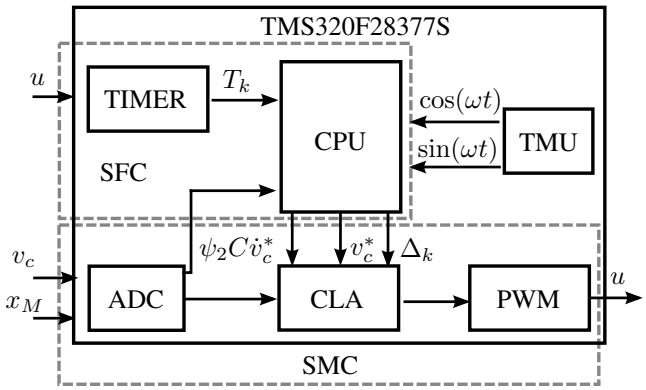

Fig. 4. Block diagram of the peripheral used for the implementation of the SMC and the SFC in the TMS320F28377S μC.

A sketch of the implementation is displayed in Figure 4. The main CPU executes the SFC once per rising edge of u. The algorithm output is the hysteresis value, $\Delta_k = \Psi_k + \Omega_k$, composed by an integral action, Ψ, and a feedforward action, Ω_k. The discrete-time integrator is given by:

$$\Psi_k = \Psi_{k-1} + \gamma e_{k-1}, \tag{21}$$

where the error at the kth switching period is defined as the difference between the actual switching period, T_k, and the reference period, T^*. A general purpose timer of the μC (200 MHz, 32 bit) measures the on time, T_k^+, the off time, T_k^-, and the switching period, T_k, of the control action u when the kth switching interval ends (rising edge of u). Regarding the feedforward control, it is defined as:

$$\Omega_k = \frac{\hat{\rho}_{k-1} - \rho_k^+}{\hat{\rho}_k}\Omega_{k-1} + \frac{\rho_{k-1}^+}{\hat{\rho}_k}\Omega_{k-2} + \frac{\tilde{\rho}_{k-1} - \tilde{\rho}_k}{\hat{\rho}_k}\Psi_{k-1}, \tag{22}$$

where $\hat{\rho}_k := \rho_k^+ - 2\rho_k^-$ and $\tilde{\rho}_k := 2\left(\rho_k^+ - \rho_k^-\right)$, with

$$\rho_k^+ := \left[\dot{\sigma}_k(v_c, x_M)_{u=-1}\right]^{-1}, \ \rho_k^- := \left[\dot{\sigma}_k(v_c, x_M)_{u=+1}\right]^{-1},$$

being the inverses of the samples of the switching function derivatives (given by (7)) in the kth switching interval (see [23] for details). Notice that there exists a delay of one period in the measurement of the switching period. This issue is addressed

by approximating Ω_k by its preceding sample, i.e, $\Omega_k \approx \Omega_{k-1}$, and the values of $\rho^{\pm}_{k-1}$ are estimated as:

$$\rho^{+}_{k-1} = \frac{T^{+}_{k-1}}{\Delta_{k-1} + \Delta_{k-2}}, \quad \rho^{-}_{k-1} = \frac{T^{-}_{k-1}}{2\Delta_{k-1}}. \tag{23}$$

It should be noticed that (23) provides $\rho^{\pm}_{k-1}$ directly, avoiding the well-known problems related to the amplification of the switching noise produced by standard time derivation.

V. Experimental results

The parameter values of the VSI prototype, the SMC and the SFC are shown in Table I.

TABLE I
VOLTAGE SOURCE INVERTER PARAMETERS.

Parameter	Symbol	Value
Input voltage	E	420 V
Desired output voltage amplitude	A	$220\sqrt{2}$ V
Output voltage frequency	f	50 Hz
Inductor	L	440 μH
Capacitor	C	100 μF
Output power (Linear Load)	P	2.2 kW
Switching period reference	T^*	50 μs
Current transformer parameters	L_x, M, R_b	10 mH, 33 μH, 6.8 Ω
Sliding mode control parameters	ψ_1, ψ_2	100, 100
SFC control parameter	γ	$[10^4, 10^7]$

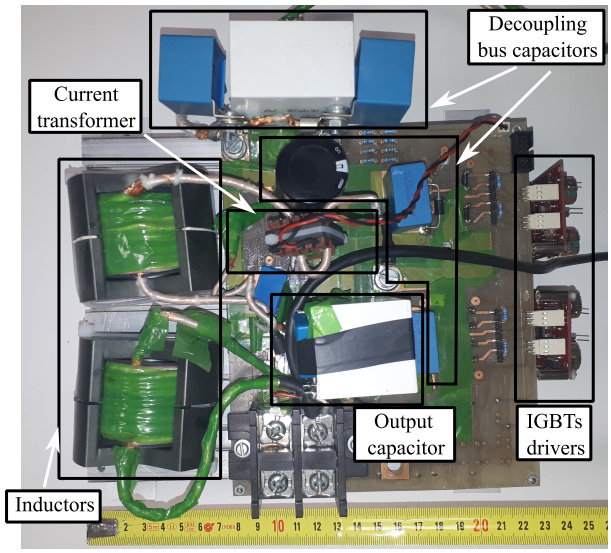

Fig. 5. The VSI prototype used in the experimental testing.

The VSI switches are IGBT 50MT060WTHA from Vishay. The output capacitor consists of two capacitors C4AEGBW5500A3LJ connected in parallel (2x50 μF), and a gapped ferrite cores wound with copper litz wire implements the power inductor (2x 200 μH). The CT is manually wound using a ferrite core of 3C90 material from Ferroxcube. The number of turns is 300, and the required value of L_x is adjusted adding an air gap to the core. Figure 5 shows a picture of the assembled power inverter.

The experimental results have been obtained for a resistive load and also when a diode rectifier is connected at the VSI output.

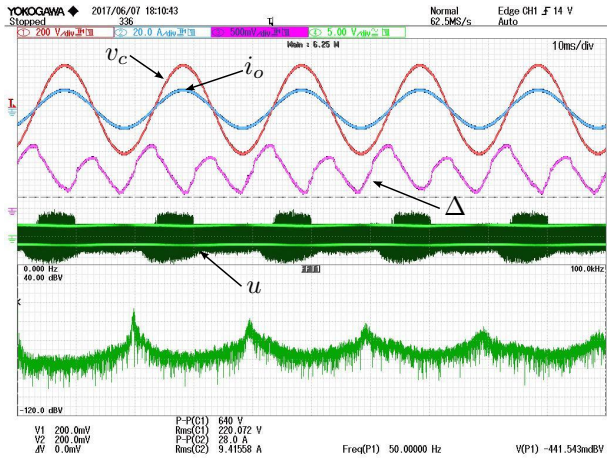

Fig. 6. Steady-state VSI response with a load of 2.2 kW; SFC with $\gamma = 2.5 \cdot 10^6$. Top: output voltage, v_c, output current, i_o, hysteresis value, Δ, and control signal, u. Bottom: FFT detail of the control signal, u.

A. Test 1: Resistive load

Figure 6 shows the system steady-state performance at nominal conditions, namely, 2.2 kW with resistive load. The output voltage, v_c, the output current, i_o, the hysteresis value, Δ, and the control signal, u, are presented in the top plot of the Figure. In turn, the bottom plot shows the Fast Fourier Transform (FFT) of the control signal. Notice that the output signal has a good behaviour, and achieves the desired switching frequency (confirmed by the FFT of the control signal) by adapting the hysteresis value. Table II shows the measured values of the THD (less than 0.3%) and the maximum voltage tracking error (less than 1.05%) for different values of the output power. Additionally, a power efficiency of 95% has also been measured in the inverter for the 2.2 kW load.

The VSI has also been tested when the load changes from 0 to 2.2 kW. The transient response can be seen in Figure 7, where the output voltage, v_c, the output current, i_o, and the voltage error, $v_c^* - v_c$ are shown. The voltage error has been computed by the μC, and loaded in a digital to analog converter, DAC, for visualization, with a resulting scale of 247.18 V/V. A maximum error of 4.5% of the output voltage amplitude can be observed in the transient. Notice that the transient has been produced in the worst case, where the peak current is maximum. As the implemented discrete-time SMC emulates the behaviour of the continuous-time one, the reaching time is minimum, since the control action does not change until the switching function reaches again the hysteresis band. This result confirms the theoretical prediction, thus validating all the assumptions made at the design and implementation stages.

The following test shows the SFC operation. Starting from a fixed hysteresis value, i.e. with the SFC disabled, the enabling

TABLE II
EXPERIMENTAL RESULTS OF THE VSI

Linear Load		
Output Power (kW)	THD[1] Voltage (%)	Voltage error (%)
0	0.2	0.59
0.5	0.3	0.73
1	0.3	0.89
1.8	0.3	0.97
2.2	0.3	1.04
Nonlinear Load		
Output power (kW)	THD Voltage/Nonlinear current (%)	Peak current/Crest factor (A)/ -
0.63	1.1/81.2	17.6/3.4

[1] FLUKE 434 Power quality analyzer

of the SFC results in switching frequency regulation. Figure 8 presents the behaviour of the output voltage, v_c, the hysteresis value, Δ_k, and the switching period, T. Notice, on the one hand, that the switching period is, as expected, time-varying when the hysteresis is fixed, and how it is properly regulated, with a smooth and fast transient response, to the desired value when the SFC is enabled. On the other hand, the output voltage dynamics is not affected by the hysteresis transient that appears when the SFC changes from the disabled state to the enabled one, thus confirming that the SFC does not have any impact in the SMC dynamics.

B. Test 2: Diode rectifier load

The diode rectifier produces a nonlinear current depending on the state of the diodes, which act as switches, the capacitor value and the applied load. This load has two different working states, one when there is no current consumption from the VSI (diodes open) and another one when the diodes are closed, thus behaving as a reactive linear load. The parameter values of the rectifier are $R_L = 132\ \Omega, r_s = 1\ \Omega, C_L = 6.6$ mF, and it provides a crest factor of 3.4 with a current peak of 17.6 A for an output voltage amplitude of $220\sqrt{2}$ V. Figure 9 shows the output voltage, v_c, the output current, i_o, and the voltage error, $v_c^* - v_c$. The bottom row of Table II presents the main performance parameters of this test. The results in Table II and Figure 9 confirm a very good performance of the VSI loaded with a the diode rectifier. The magenta signal shows the tracking voltage error, which achieves 21 V (peak to peak) in the worst case, corresponding to a 3.4 % of the reference value.

Figure 10 shows the output voltage, v_c, the output current, i_o, the hysteresis value, Δ, and the control signal, u, in the top plot, and the control signal FFT in the bottom plot. This test confirms that even in the face of a discontinuous current consumption, the control algorithm tracks the reference voltage and properly regulates the switching period. It should be noticed that, due to the operation of the diode rectifier, the SMC and the SFC undergo constant transients. As a

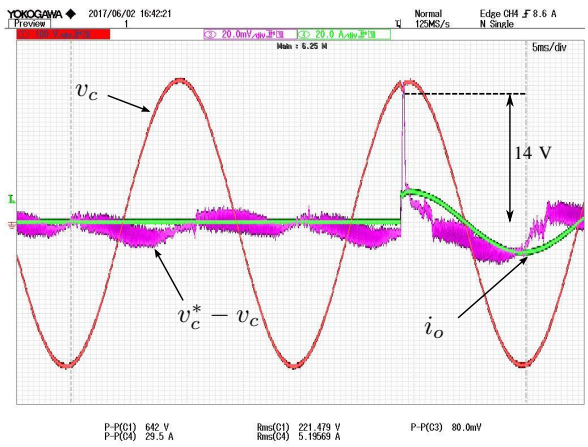

Fig. 7. Transient response when the load abruptly changes from no load to 2.2 kW; SFC with $\gamma = 2.5 \cdot 10^6$. Output voltage, v_c, output voltage error, $v_c^* - v_c$, and output current, i_o.

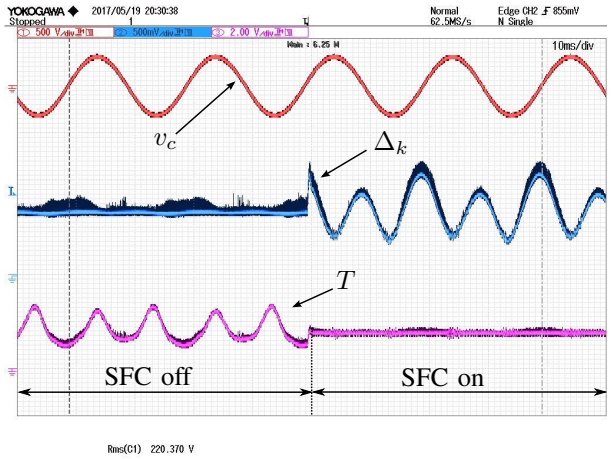

Fig. 8. VSI response in no load condition when the SFC is disabled and enabled; SFC with $\gamma = 10^7$. Output voltage, v_c, hysteresis value, Δ_k, switching period, T.

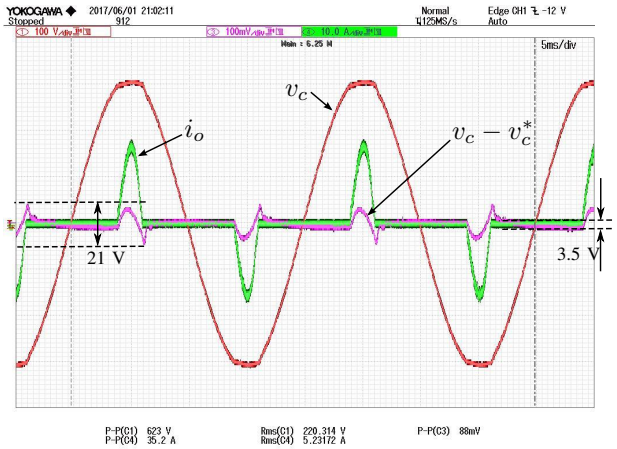

Fig. 9. VSI response with nonlinear load; SFC with $\gamma = 10^4$. Output voltage, v_c, output voltage error, $v_c^* - v_c$, and output current, i_o.

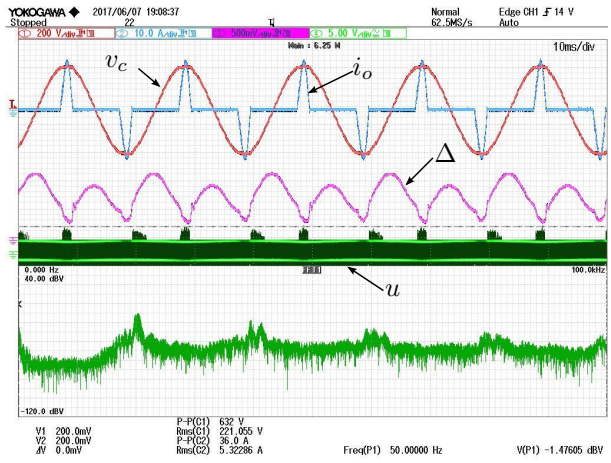

Fig. 10. VSI response with nonlinear load; SFC with $\gamma = 10^4$. Top: output voltage, v_c, output current, i_o, hysteresis value, Δ, and control signal, u. Bottom: FFT of the control signal, u.

consequence, the switching period slightly deviates from the desired one, generating small harmonics in the vicinity of the desired switching frequency, as indicated by the FFT of Figure 10. Nevertheless, even in these conditions the switching period can be considered constant.

VI. Comparative Analysis

The control algorithm has been compared with different controllers reported in the last 10 years. Table III shows the main figures of merit for the SMC-SFC, the discrete-time repetitive SMC with exponential-based bi-power reaching law (DRSMC) [18], the discrete time SMC (DSMC) [18], the standard first order sliding mode control (SMC) for single [16] and three phase inverter [20], terminal SMC with integral-compensation (TSMC-IC) [31] and two PWM-based controllers: the repetitive control (RC) [18] and the model predictive control (MPC) [32]. Notice that the SMC-SFC, the standard SMC and the TSMC-IC achieve the best THD indexes with a linear load. For the nonlinear load the DRSMC exhibits the best THD performance but the SMC-SFC and the SMC present indexes very close to the best one.

As regards the transient time after a load change, it should be remarked that the RC index highlights the well-known drawback of this control technique providing a long transient time. On the other hand, it has to be pointed out that the transient time is highly dependent on the output capacitor and for that reason the MPC and the SMC-SFC show longer transient time values. Concerning load regulation, the best index corresponds to the DRSMC, whereas SMC-SFC, DSMC and RC also present values bellow 0.5%, which are also very good.

The last two columns of the comparative table show the number of control parameters to be adjusted and the type of operations to be programmed in the software control routine. These items provide insight into the computing resources required by the controller and the control structure. Notice that the repetitive control algorithm manages a high number of delayed states, thus implying a high computational cost. Furthermore, with regard the power operation ($()^\alpha$) and dq transform, they also involve considerable computing cost and the rest of operations ($+$, x, $/$, sign()) can be considered simple and with reduced computational effort. Therefore, the DRSMC, TSMC-IC and RC are the ones with higher computational cost, being the SMC and SMC-SFC the lower ones.

Finally, for illustrative purposes, a set of numerical simulations comparing the proposed SFC-SMC with the DRSMC and the RC are presented. In order to make a fair comparison, each controller has been designed with the parameters of the VSI presented in Table I and the operating switching frequency is set to 20 kHz, which is the frequency regulated by the SFC in this work. Therefore, it is assumed that both the DRSMC and the RC can be executed in 50 μs. It has to be also remarked that the simulation setup has been carried out using the Matlab Simscape Power Systems Toolbox, and it has considered realistic experimental issues such as the dead-time of the transistor control signals, the computation delay (1 μs for the SMC-SFC and 50 μs for the DRSMC and the RC) and the ADC resolution. Dynamic and steady-state performances have been tested for linear load transients, bus voltage variations, and nonlinear load.

Specifically, two tests have been carried out. Test 1 consists of a start-up with a abrupt load changes from no load to 2.2 kW at $t = 0.025$ s and again to no load at $t = 0.035$ s, and a 20% bus voltage reduction at $t = 0.045$ s. Test 2 considers a nonlinear load corresponding to a diode rectifier with load parameters $R_L = 132$ Ω, $r_s = 0.35$ Ω, and $C_L = 6.6$ μF.

The simulation results are presented in Figure 11. Notice how the results for the SMC-SFC perfectly match the experimental results shown in Figure 7 for the response to a load change and in Figure 9 for a nonlinear load. From Figure 11 it can also be noticed that the steady-state error in the SMC-SFC is slightly better than that of the DRSMC and the RC for both linear and nonlinear tested loads, whereas all the controllers present quite similar transient responses. It has to be pointed out that the start-up of the RC controller requires more than 200 ms for reaching the steady-state; this is the reason why the simulation time of the RC has been extended with respect to the SMC-SFC and the DRSMC. Finally, with regard to the bus voltage variation, the SMC-SFC shows a more robust behaviour than the DRSMC and the RC.

Summarizing, from the data listed in Table III it can be inferred that the SMC-SFC shows the lowest THD for a linear load, while the other performance indexes are very close to the best ones, and the computational requirement is low. Moreover, the simulation results comparing SMC-SFC, DRSMC and RC performances obtained with the same VSI parameters indicate that the SMC-SFC presents the best steady-state behavior when operating with the tested linear and nonlinear loads. As a conclusion, the proposed SMC-SFC controller shows performance indexes very close, in some cases even better, to alternative solutions but allowing an easier implementation.

TABLE III
FIGURES OF MERIT OF THE SMC-SFC, THE DRSMC [18], THE DSMC [18], THE RC [18], THE SMC ([16] AND [20]), THE MPC [32] AND THE TSMC-IC [31]

	V_{dc}	V_{ac}	f_{sw}	C	L	P	THD (L)	THD (NL)	Transient time	Load regulation	Control parameters	Operations[1]
SMC-SFC	420 V	220 V_{rms}	20 kHz	100 μF	0.4 mH	2.2 kW	0.3 %	1.1 %	0.75 ms	0.45 %	3	+, x , /, sign()
DRSMC	750 V	380 V_{rms}	9 kHz	10 μF	2 mH	6 kW (3 phase)	0.7 %	1.0 %	0.3 ms	0.13 %	8	+, x , /, $()^{\alpha}$, RC
DSMC	750 V	380 V_{rms}	9 kHz	10 μF	2 mH	6 kW (3 phase)	1.9 %	2.8 %	2 ms	0.39 %	7	+, x , /, $()^{\alpha}$
RC	750 V	380 V_{rms}	9 kHz	10 μF	2 mH	6 kW (3 phase)	0.9 %	1.8 %	200 ms	0.26 %	2	+, x , /, RC
SMC	360 V	220 V_{rms}	15 kHz	9.4 μF	0.36 mH	1.76 kW	1.1 %	1.7 %	0.5 ms	1 %	3	+, x, /, sign()
SMC	390 V	110 V_{rms}	15 kHz	33 μF	0.88 mH	3 kW (3 phase)	0.4 %	1.7 %	0.3 ms	2.7 %	2	+, x, /, sign()
MPC	350 V	120 V_{rms}	4-6 kHz	60 μF	2.5 mH	1.2 kW (3 phase)	2.8 %	3.5 %	2 ms	5.4 %	5	+, x , /, dq
TMSC-IC	250 V	110 V_{rms}	20 kHz	10 μF	1 mH	0.6 kW	0.48 %	1.34 %	1.5 ms	- %	7	+, x , /, $()^{\alpha}$

[1] The symbols correspond to: addition (+), multiplication (x), division (/), sign function (sign()), power ($()^{\alpha}$), repetitive control (RC) and dq transform (dq).

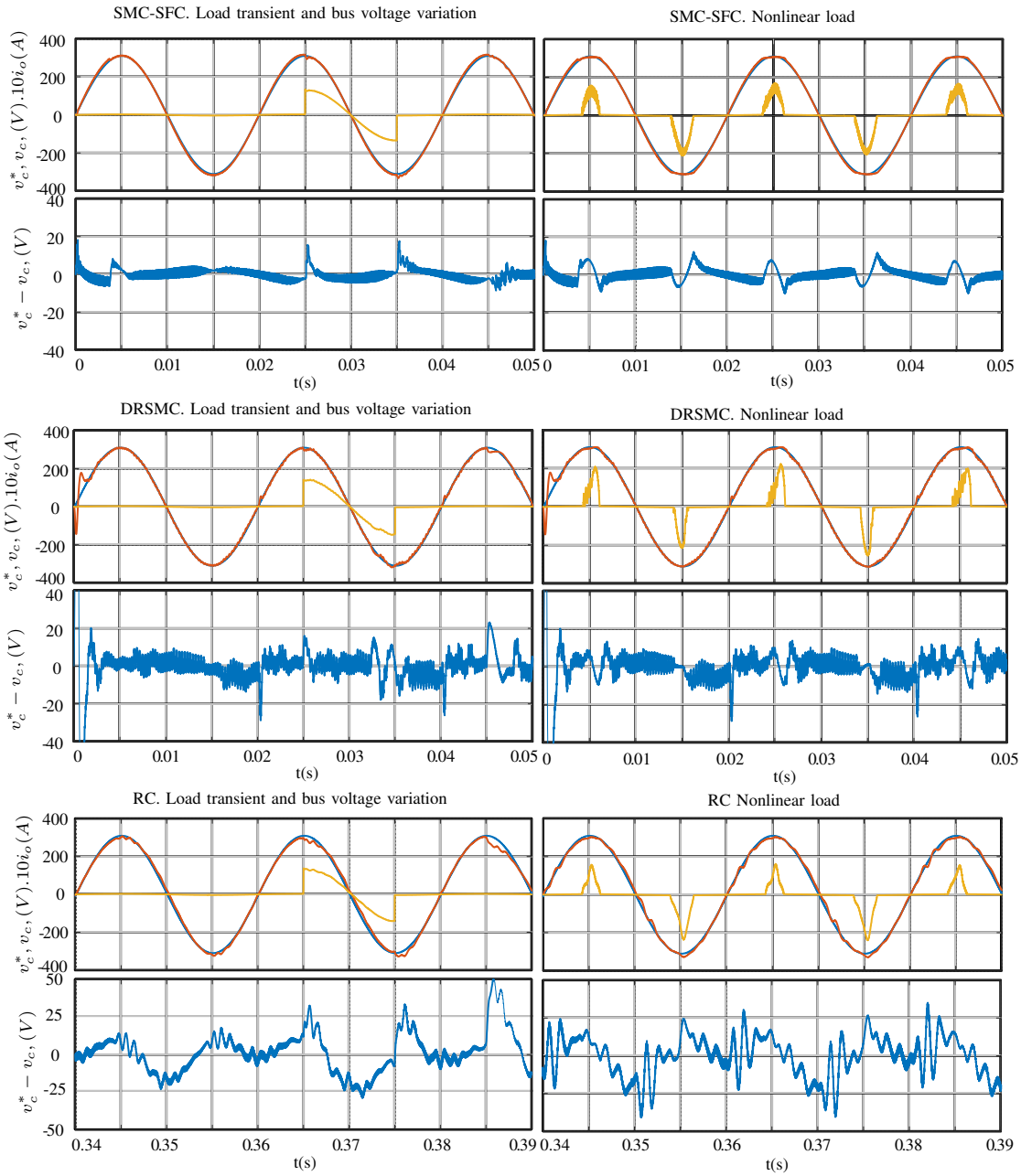

Fig. 11. Simulation result of SMC-SFC, DRSMC and RC. Top plot: response of SMC-SFC to Test 1 (left) and Test 2 (right). Middle plot: response of DRSMC to Test 1 (left) and Test 2 (right). Bottom plot: response of RC to Test 1 (left) and Test 2 (right).

VII. Conclusions

The design of a simple sliding mode control operating at fixed switching frequency in a VSI has been presented in this paper. The stability of the controlled system has been analysed for different loads. The sliding controller uses a first order switching surface and does not require any additional integral or resonant term. Moreover, the sliding parameters have been designed to ensure a good sliding motion performance for the different working scenarios. The sliding mode controller has been implemented by means of a hysteresis comparator, and the switching frequency has been regulated using an outer control loop that varies the hysteresis bandwidth.

A 2.2 kW VSI has been assembled and the controllers have been digitally implemented in a microcontroller. The prototype has been tested with a resistive load and with a diode rectifier, and the experimental results have confirmed the expected robustness and the fixed switching frequency regulation, showing low THD at the output voltage with small tracking error for all the tested loads.

Acknowledgements

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