ICT Systems Engineering

Microelectronics Exercises

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1 Introduction to integrated circuits and microelectronics

Exercise 1.1 Define what is meant by intrinsic and extrinsic semiconductor material. Indicate the types of current carriers present in each.

Exercise 1.2 Explain how pure silicon can be modified to exhibit electrical conductivity by means of electrons or by means of holes as the majority charge carriers. Compare electron mobility with hole mobility and justify the reasons behind the observed difference.

Exercise 1.3 Describe the main properties that characterize the following materials: monocrystalline silicon, polycrystalline silicon (polysilicon), silicon dioxide and amorphous silicon.

Exercise 1.4 Define what is meant by integrated circuit. Make a list of the advantages of this type of circuit compared to circuits made with discrete components. Please also indicate the difference between a monolithic integrated circuit and a hybrid integrated circuit.

Exercise 1.5 Explain the main physical phenomena that occur in a PN junction and its behavior as it is forward biased or reverse biased.

2 Fabrication Technology

Exercise 2.1 Describe the following processing steps in modern semiconductor device fabrication:

- Physical vapor deposition (PVD)
- Chemical vapor deposition (CVD)
- Oxidation (dry and wet)
- Photolithography
- Etching (dry and wet)
- Ion implantation
- Solid-state diffusion
- Metallization

Exercise 2.2 Define the following concepts and acronyms related to the field of microelectronics, providing application examples, images and any other information deemed relevant to their description:

- EDA Software
- DRC
- VLSI, ULSI, 3D-IC
- Full-Custom Layout Design
- Semi-Custom / Standard Cell Layout Design
- CPLD, FPGA
- Mixed-signal IC
- Monolithic integrated circuit
- Hybrid integrated circuit
- General-purpose integrated circuit
- ASIC
- ASSP
- SiP
- SoC

Exercise 2.3 Describe de following types of integrated-circuit packaging and look for some illustrative images. Note that many of the packaging configurations offer plastic and ceramic variants.

Through-hole (TH) packaging:

- Single-In-line (SIP)
- Dual-In-line (DIP)
- Quad-In-line (QIP)
- Zig-zag-In-line (ZIP)
- Pin-Grid-Array (PGA)

Surface-mount (SM) packaging:

- Small Outline (SO, SOIC)
- Leaded Chip Carrier (LCC)
- Flat Pack (FP)
- Quad Flat Pack (QFP)
- Ball Grid Array (BGA)

3 Active and passive devices in integrated circuits

EXERCISE 3.1 The diagram in Figure 1 shows the internal structure of an N-channel enhancement MOS transistor.

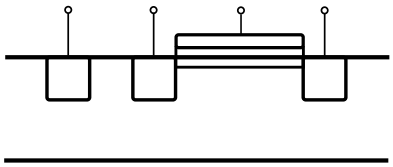

Figure 1

a) Complete the diagram describing each of the materials that constitute the transistor and the function performed.

b) Draw in detail how the diagram above changes in the different modes of operation of the transistor and explain qualitatively the behavior of the device in each case.

EXERCISE 3.2 Repeat the previous exercise for the following types of transistor:

a) P-channel enhancement MOST;

b) N-channel depletion MOST;

c) P-channel depletion MOST.

EXERCISE 3.3 We want to design an N-channel MOS transistor to be used as a switch. In particular, we need a conduction resistance $R_{DSon} = 1\ \Omega$ when $V_{GS} = 5$ V. Knowing that $K' = 20\ \mu\text{A/V}^2$ and $V_T = 1$ V, determine the ratio W/L (supose that conduction takes place with $V_{DS} \simeq 0$).

EXERCISE 3.4 In the design of an electronic circuit to be integrated in 2-µm CMOS technology, we want to use an N-channel MOS transistor to implement a linear resistor of 1.1 kΩ connected to the reference node (ground) through one of its terminals. To this end:

a) Based on the equations of the MOS transistor, indicate the requirements that V_{GS} and V_{DS} must accomplish so that the device behaves as a linear resistor (i.e., so that it exhibits I_D proportional to V_{DS}).

b) Knowing that the supply voltage is $V_{DD} = 5$ V, $K' = 20\ \mu\text{A/V}^2$ and $V_T = 0.5$ V, find the proper dimensions of the transistor.

c) Draw the resulting circuit schematic clearly indicating the terminals of the desired resistance.

d) Specify the range of voltages that can be applied to this resistance so that the transistor provides the expected behavior.

Exercise 3.5 Questions C8.1, C8.3, C8.4 and C8.11 (page 321) in Prat et al. [1].

Exercise 3.6 (NMOS inverter) Guided problem 6.3 (page 335) in Prat and Calderer [2].

Exercise 3.7 (CMOS inverter) Guided problem 6.4 (page 336) in Prat and Calderer [2].

Exercise 3.8 (CMOS inverter) Exercise 1.7 (page 1.15) in Castañer et al. [3]. The inversion voltage V_{INV} is defined in the same page of the exercise statement.

Exercise 3.9 For the circuit in Figure 2 find the operating point of the transistor, i.e., the variables v_{GS}, v_{DS} and i_D. Verify the results by means of simulation.

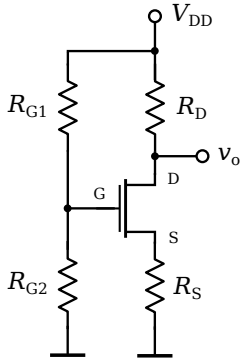

Figure 2

$V_{DD} = 20$ V, $R_{G1} = 100$ kΩ, $R_{G2} = 100$ kΩ, $R_S = 10$ kΩ, $R_D = 10$ kΩ,
$K' = 20$ μA/V^2, $W/L = 10$, $V_T = 1$ V.

Exercise 3.10 We want to design a logic inverter to be fabricated in 2-μm NMOS technology, according to the schematic in Figure 3, where $V_{DD} = 5$ V.

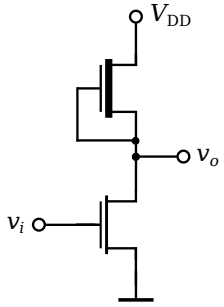

Figure 3

In particular it is required that when the output is at the low level the voltage does not exceed the value $v_o = 0.5$ V. The dimensions of the enhancement NMOSFET (transistor

below) are $W = 3$ µm, $L = 2$ µm, with a threshold voltage $V_T = 0.5$ V. The depletion NMOSFET (transistor above) has a theshold voltage $V_T = -0.5$ V. In both cases we have $K' = 20$ µA/V^2.

a) For each of the logical states available at the input ($v_i = 0$ V and $v_i = 5$ V), indicate in a reasoned manner the mode in which the transistors operate.

b) Determine the minimum dimensions of the depletion NMOSFET.

Exercise 3.11 Suppose that you have to design a CMOS voltage divider that provides an output voltage $v_o = 0.75$ V from a power supply voltage $V_{DD} = 1.5$ V, as shown in the schematic in Figure 4.

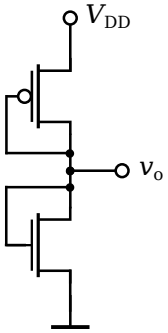

Figure 4

The technology used is 180 nm with the following parameters: minimum device width $W = 240$ nm, $K'_P = 10$ µA/V^2, $K'_N = 20$ µA/V^2, $V_{TP} = -0.5$ V and $V_{TN} = 0.3$ V.

a) Indicate de mode of operation of the transistors.

b) Determine the corresponding device dimensions, knowing that the current consumed by the divider must not exceed 10 µA.

Exercise 3.12 In this exercise you must determine the best strategy to implement resistors in an integrated circuit using 2-µm CMOS technology. The following table shows different techniques available with their characteristic parameters (sheet resistance R_s in the case of layers) and their minimum dimensions:

Layer / Device	Parameter	Minimum size
- N+ diffusion	$R_s = 35$ Ω/square	$W = L = 3$ µm
- Polysilicon	$R_s = 65$ Ω/square	$W = L = 2$ µm
- N well	$R_s = 2$ kΩ/square	$W = L = 10$ µm
- Enhancement NMOS transistor operated as a saturated load	$K' = 70,28 \times 10^{-6}$ A/V^2 $V_T = 0.7$ V	Channel: $W = 3$ µm, $L = 2$ µm

Knowing that the design requires to implement the following resistance values,

- 100 Ω
- 10 kΩ
- 1 MΩ

find the best option for each case. Set as the primary objective to occupy as little area as possible. In the case of the saturated load, assume that it supports a voltage of 2.5 V.

References

[1] Prat, Ll.; Bragós, R.; Chávez, J. A.; Fernández, M.; Jiménez, V.; Madrenas, J.; Navarro, E.; Salazar, J. *Circuitos y dispositivos electrónicos. Fundamentos de electrónica*. 6a ed. Barcelona, Edicions UPC, 1999. ISBN: 84-8301-291-X

Available online at:

http://upcommons.upc.edu/handle/2099.3/36340

[2] Prat, Ll.; Calderer, J. *Dispositius electrònics i fotònics. Fonaments*. 2a ed. Barcelona, Edicions UPC, 2006. ISBN: 84-8301-855-1.

Available online at:

http://ebooks.upc.edu/product/dispositius-electrnics-i-fotnics-fonaments

[3] Castañer, L.; Jiménez, V.; Bardés, D. *Fundamentos de diseño microelectrónico*. Barcelona, Edicions UPC, 2002. ISBN: 84-8301-613-3.

Available online at:

http://ebooks.upc.edu/product/fundamentos-de-diseo-microelectrnico

4 Digital integrated circuits

EXERCISE 4.1 Design a CMOS logic gate that implements with the minimum number of transistors the function

$$F = A + \overline{B}C + CD$$

EXERCISE 4.2 Design a logic gate that implements in CMOS technology the XOR (exclusive OR) function, $F = A \bigoplus B$.

EXERCISE 4.3 Given the truth table of function F, which depends on three inputs, A, B and C,

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

answer the following questions:

a) Get a simplified expression for the logic function $F = f(A, B, C)$.

b) Propose the schematic of a CMOS circuit that implements the aforementioned function.

c) Considering that the circuit is loaded with a capacitance much higher than the parasitic capacitances of the transistors, indicate the conditions under which the rise and fall times at the output will be higher (assume that all transistors have the same dimensions).

EXERCISE 4.4 Determine the logic function F performed by the circuit in Figure 5.

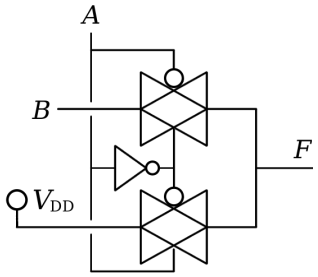

Figure 5

Exercise 4.5 One of the problems that some battery-powered electronic circuits exhibit is that the user may accidentally reverse their polarity, submitting the circuit to a reverse voltage able to damage some of its components. A solution to this problem is to incorporate a pass transistor, connected as shown in Figure 6.

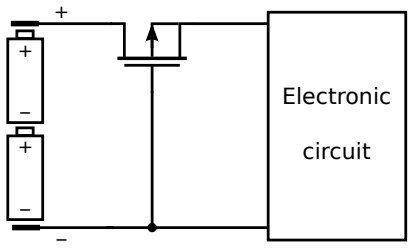

Figure 6

a) Prove that, with a suitable dimensioning, this transistor allows proper circuit operation when the polarity of the batteries is correct and, additionally, it protects the circuit when the polarity is reversed. Assume that the electronic circuit behaves for all purposes as a load resistor.

b) Knowing that the batteries provide a total voltage of 2.4 V and that, when switched on, the circuit draws a current of 100 mA, find the dimensions of the transistor so that the voltage drop between the drain and the source is not greater than 10 mV ($K' = 15$ μA/V^2, $V_T = -1$ V).

Exercise 4.6 Propose an alternative circuit to that in Figure 6 that protects the electronic circuit using an NMOS transistor. Which can be the advantage of using an NMOS transistor instead of a PMOS transistor?

Exercise 4.7 Figure 7 shows the symbol and the schematic of a CMOS transmission gate. Knowing that you want to use this gate in a digital circuit with a supply voltage $V_{DD} = 3.3$ V, that the maximum current which is expected to flow through the gate is 10 mA, and that the voltage drop introduced by the device must not exceed 50 mV at any of the logic levels to be transferred, determine the appropriate dimensions of the transistors.

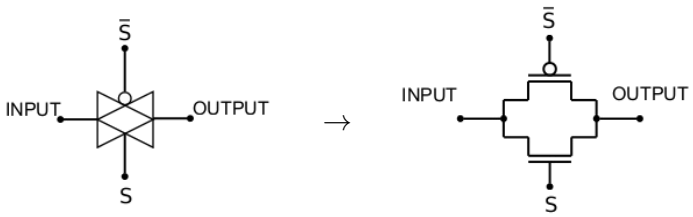

Figure 7

Additional data: CMOS technology: 900 nm; NMOS parameters: $K'_N = 50$ μA/V^2, $V_{TN} = 0.5$ V; PMOS parameters: $K'_P = 20$ μA/V^2, $V_{TP} = -0.7$ V.

EXERCISE 4.8 The diagram in Figure 8 corresponds to that of a single-output CMOS logic gate designed with Magic VLSI Layout Tool.

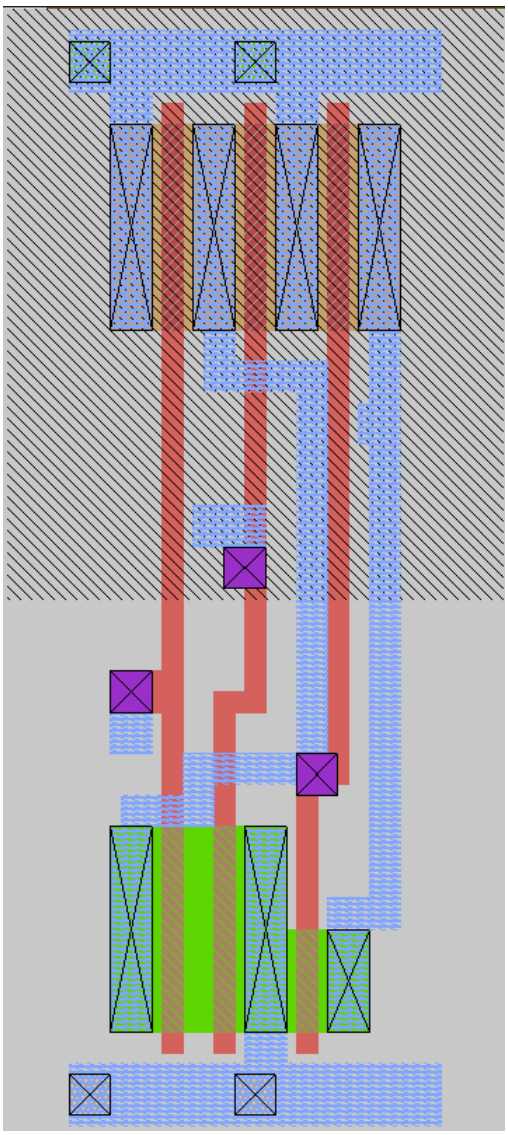

Figure 8

a) From the supplied diagram, plot the gate circuit schematic clearly identifying the inputs and the output.

b) Determine the truth table as well as the boolean expression of the logic function.

EXERCISE 4.9 The diagram in Figure 9 corresponds to that of a CMOS logic gate (*standard cell*) from the 0.35 µm libraries provided by the Oklahoma State University. For efficiency and occupied-area reasons, some of the transistors use a *fingers* layout.

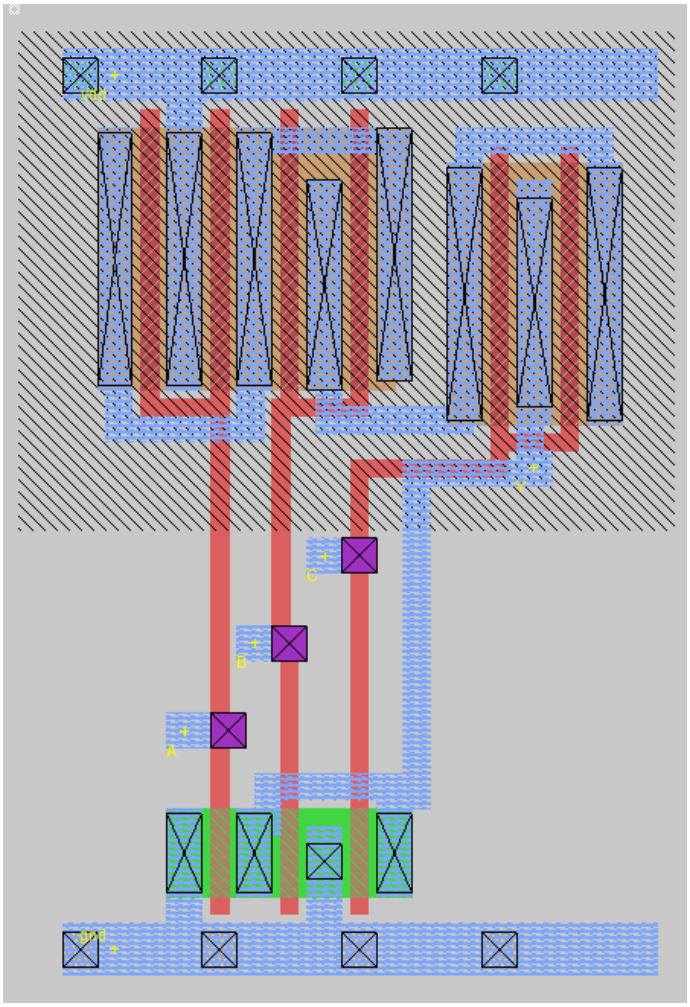

Figure 9

a) From the provided diagram and knowing that the gate has a single output, plot the circuit schematic clearly identifying the inputs and the output.

b) Determine the truth table as well as the boolean expression of the logic function.

EXERCISE 4.10 The website http://opencircuitdesign.com describes the digital synthesis tool Qflow as "*a complete tool chain for synthesizing digital circuits starting from Verilog source and ending in physical layout for a specific target fabrication process*". The site explains that the synthesis process is based on the use of various tools, namely:

- Qrouter: *Detail router*;
- Vhd2vl: *VHDL-to-Verilog translator*;
- Magic: *Final Layout generator/viewer*;
- Yosys: *Verilog parser/synthesis*;
- Graywolf: *Cell and pin placement.*

a) Indicate the order in which each of these programs is called and executed.

b) Explain in some detail the main function that each one performs.

Exercise 4.11 Propose a circuit schematic that corresponds to the layout in Figure 10 and identify its functionality.

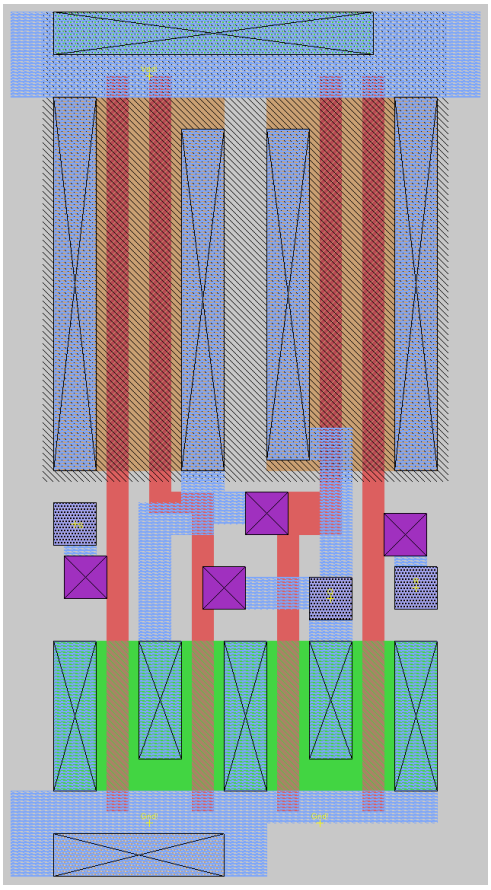

Figure 10

5 Analog integrated circuits

EXERCISE 5.1 This problem aims to follow the steps in the design of a MOS transistor amplifier that provides a voltage amplification $|A_v| = |v_o/v_i| = 10$.

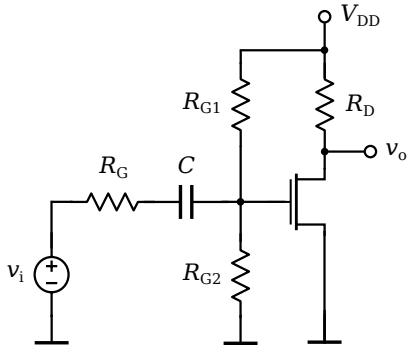

Figure 11

For the circuit in Figure 11, knowing that $V_{DD} = 5$ V, $R_G = R_D = 1$ kΩ, $K' = 20$ μA/V^2, $V_T = 1$ V and that C is large, so that it may be considered a shortcircuit except for the bias circuit:

a) Draw the corresponding bias and small-signal analysis circuits.

b) Find the drain current at the operating point of the transistor, I_{DQ}, imposing that the output voltage v_o at this point is half times the supply voltage (this guarantees the maximum dynamic range at the output, i.e., the maximum distance of the operating point to the limits imposed by ground and V_{DD}).

c) Obtain the voltage amplification of the circuit $|A_v| = |v_o/v_i|$ as a function of the transconductance of the transistor g_m. Assuming that the desired amplification is $|A_v| = 10$, determine g_m and, from it, the aspect ratio of the transistor W/L.

d) Find the gate-source voltage at the operating point V_{GSQ} and, from the obtained result, propose appropriate values for R_{G1} and R_{G2}.

e) Finally, provide the complete mathematical expression of the output voltage v_o.

EXERCISE 5.2 The goal of this problem is to redesign the circuit presented in the previous exercise (Figure 11) to replace the resistors by MOS transistors, thereby saving integration area. Assume that the minimum-size transistor available with the technology used has $W = 3$ μm and $L = 2$ μm.

a) Design a PMOS active load ($K'_P = 10$ μA/V^2, $V_T = -1$ V) to substitute the resistor R_D. Specifically, the active load must exhibit a small-signal resistance equal to 1 kΩ, and it must also provide an output voltage at the operating point that halves that of the supply. Note that for the operating point the active load behaves like a nonlinear

resistance, characterized by the equation of the MOS transistor in saturation, whereas for small signal it behaves like a linear resistor controlled by the transconductance of the transistor.

b) Find the new value of the NMOS transistor current at the operating point, I_{DQ}.

c) Determine the new dimensions of the NMOS transistor to achieve $|A_v| = |v_o/v_i| = 10$.

d) Determine the gate-source voltage of the NMOS transistor at the operating point, V_{GSQ}, and from it, design a CMOS bias network to replace R_{G1} and R_{G2} (impose that the current drawn by this network equals 10 μA).

e) Draw the complete circuit schematic of the final design.

EXERCISE 5.3 This problem aims to follow the steps in the design of a bipolar transistor amplifier.

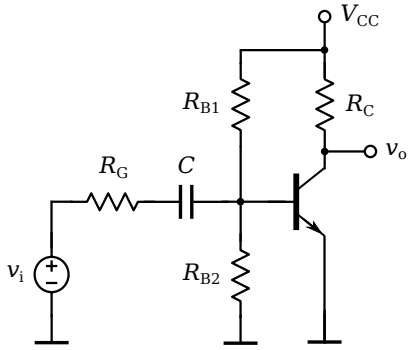

Figure 12

For the circuit in Figure 12, knowing that $V_{CC} = 5$ V, $R_G = 10\ \Omega$, $R_C = 1$ kΩ, $V_T = 25$ mV, $V_\gamma = 0.7$ V, $\beta = 100$ and that C is large, so that it may be considered a shortcircuit except for the bias circuit:

a) Draw the corresponding bias and small-signal analysis circuits.

b) Calculate the collector current at the operating point of the transistor, I_{CQ}, imposing that the output voltage v_o at this point is half times the supply voltage (this guarantees the maximum dynamic range at the output, i.e., the maximum distance of the operating point to the limits imposed by ground and V_{CC}).

c) Calculate the voltage amplification of the circuit, $A_v = |v_o/v_i|$, as a function of the transconductance of the transistor g_m. Prove that under the criterion applied in the previous question, the resulting amplification is $A_v = |v_o/v_i| = 20V_{CC} = 100$.

d) Taking into account that the transistor is in the conduction region and, therefore, it can be assumed that $v_{BE} \approx V\gamma$, find the base current at the operating point, I_{BQ}, and from this result propose appropriate values for R_{B1} and R_{B2}.

e) Finally, provide the complete mathematical expression of the output voltage v_o.

EXERCISE 5.4 For the amplifier with active load in Figure 13,

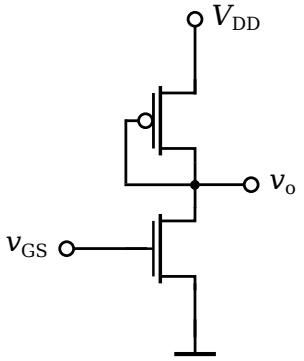

Figure 13

and knowing that $V_{DD} = 3$ V, $K'_P = 10$ μA/V^2, $K'_N = 20$ μA/V^2, $V_{TP} = -0.5$ V and $V_{TN} = 0.5$ V:

a) Design the PMOS active load so that the output voltage at the operating point is half times that of the supply, and so that the small-signal resistance equals 1 kΩ.

b) Find the dimensions of the NMOS transistor to achieve a small-signal voltage amplification $|A_v| = 5$.

c) Determine the value of the input voltage at the operating point, V_{GSQ}, necessary to achieve the desired performance.

EXERCISE 5.5 Figure 14 shows the schematic of a current mirror, a circuit commonly used in microelectronic design to set the current i_2 that flows through a given subcircuit from the current i_1 absorbed by the transistor M_1.

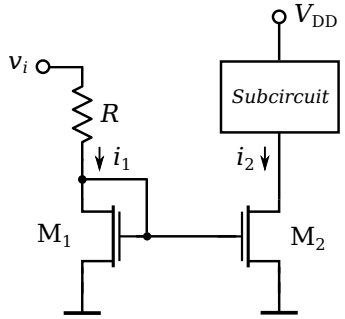

Figure 14

a) Demonstrate that if both transistors are identical and operate in saturation mode the currents i_1 and i_2 must necessarily be equal (hence the name of current mirror). This property ideally applies at low frequency when the capacitances of the transistors and other parasitic effects can be ignored.

b) Find the gain of the mirror, i.e., i_2/i_1, when the transistors exhibit different dimensions.

c) Knowing that $R = 10$ kΩ, $K' = 20$ μA/V^2, $V_T = 0.5$ V, that the technology allows $L_{min} = 1.8$ μm, $W_{min} = 2.4$ μm and that $v_i = V_{DD} = 5$ V, find the minimum dimensions of the transistors required to achieve $i_2 = 10$ mA.

EXERCISE 5.6 Figure 15 shows the schematic of an NMOS transistor amplifier.

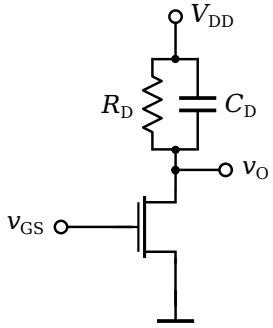

Figure 15

The supply voltage is $V_{DD} = 1.5$ V and the devices exhibit the following features:

- Transistor: $K' = 20$ μA/V^2, $V_T = 0.5$ V, $W = 14.94$ μm, $L = 0.18$ μm.
- Resistor: N well with sheet resistance $R_s = 4$ kΩ/square, $W = 0.24$ μm, $L = 0.6$ μm.
- Capacitor: Metal 1-Metal 2 structure with specific capacitance $C_s = 1$ fF/μm^2.

It is requested:

a) Knowing that the operating point of the voltage at the input of the transistor is $V_{GSQ} = 0.8$ V, find the corresponding drain bias current, I_{DQ}.

b) Calculate the small-signal amplification of the circuit at low and at high frequencies. In view of the results, what kind of filtering does the amplifier perform?

c) Design the capacitor so that the -3-dB cut-off frequency equals 8 MHz.

EXERCISE 5.7 The CMOS inverter is a basic component in digital circuits, where signals take two discrete levels. The inverter, however, also has other applications, e.g., an analog amplifier. Consider the CMOS inverter having the transfer characteristic shown in Figure 16.

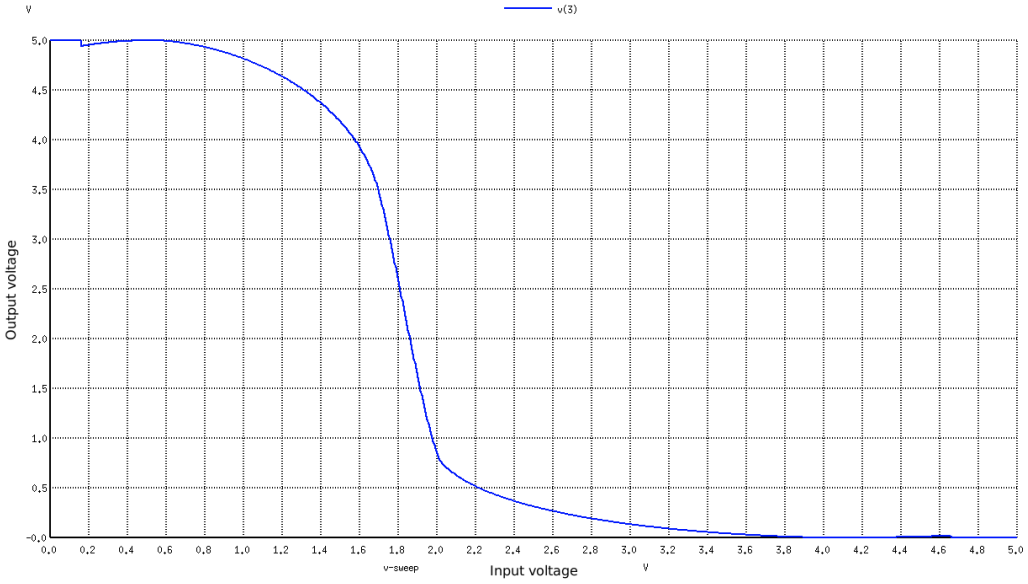

Figure 16

Assume that you want to use this inverter to amplify a low-frequency sinusoidal signal coming from a voltage source v_g exhibiting an amplitude of 100 mV.

a) Explain what needs to be done in order to properly amplify this signal with the CMOS inverter.

b) Give the schematic of a suitable circuit that, making use of the aforementioned inverter and other elements that provide suitable coupling of the signal v_g, achieves the desired function.

c) Determine the output amplitude, as well as the amplification provided by the circuit.