Impact of FinFET and III-V/Ge technology on logic and memory cell behavior

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***Abstract*—In this work, we assess the performance of a ring oscillator and a DRAM cell when they are implemented with different technologies (planar CMOS, FinFET and III-V MOSFETs), and subjected to different reliability scenarios (variability and soft errors). FinFET-based circuits show the highest robustness against variability and soft error environments.**

I. INTRODUCTION

Last decades, semiconductor industry has experienced a continuous improvement thanks to the use of planar CMOS devices usually build in silicon bulks. However, device process fluctuation has become critical as a consequence of the aggressive scaling towards technology nodes beyond 32nm. In this context, random doping distribution (RDD) appears as the principal source of variability [1], and their influence has been mainly reflected into a modification of the threshold voltage (V_T) of the devices. Additionally, dimension shrinking has largely degraded the carrier mobility, due to the higher electric fields present in scaled MOS devices. Another relevant reliability issue for deep technology nodes is soft errors [2] [3], since nodal capacitances are scaled down in the same way. Consequently, a larger soft error rate (SER) [3] is expected, which occurs as a radiation event causes enough charge disturbance to flip the data of a circuit node. One of the main parameters to study SER is critical charge (Q_{crit}), i.e. the minimum injected charge required to upset a circuit node [4], which it presents a marginal impact of temperature [5].

In order to overcome all these reliability drawbacks, some technology trends have been put in place. For instance, device mobility is enhanced by implementing the channel layers with high mobility materials [6]. Then, MOSFETs based on low band gap materials (e.g. Ge, III-V) are considered as future devices due to their relevant mobility improvement [6]. On the other hand, multi-gate devices (i.e. FinFETs) have emerged as the most promising candidates for very large-scale integrated (VLSI) circuits, due to their higher potentiality to push back the integration limits beyond 22nm [1], [7]. Moreover, FinFETs present a relevant variability mitigation due to a significant reduction of device doping [1], better short channel effects control, steeper sub-threshold slope, larger mobility and improved performance at low supply voltages (V_{DD}) [6].

So then, this study presents a behavioral analysis of two of the most relevant technology alternatives proposed nowadays (i.e. III-V/Ge MOSFETs and FinFETs) in front of different reliability scenarios, e.g. device variability and SER. In particular, we analyze the implication of both technology alternatives in logic and memory circuits. Thus, this work is organized as follows: Section II presents the different device models and the simulation framework. Section III manifests the impact of the different technology alternatives on the circuit performance. Section IV studies the impact of device variability. Section V carries out an analysis of soft error impact on each technology, and finally, Section VI summarizes the main conclusions of this work.

II. SIMULATION FRAMEWORK

A. Devices technologies and models

In order to show the comparative relevance of these new technologies with the conventional CMOS, we simulate with HSPICE [8] our circuits using three different devices models: i) FinFETs, ii) III-V/Ge MOSFETs, and iii) conventional planar bulk CMOS -as a reference technology. FinFETs are simulated using the High Performance Predictive Technology Models Multi-Gate (HP PTM-MG) [9]. In the case of the III-V/Ge MOSFET, we use models provided by the Device Modeling Group at University of Glasgow [10], developed using an atomistic simulator [11]. Finally, in the case of the planar devices, we utilize the HP PTM [9], based on high-k gate dielectrics and strained channel. For a fair comparison, we have used the same technology node (16nm) for all the device alternatives.

B. Test circuits under study

In order to get this comparison, we implement two different circuits on each technology: i) a seven-stage ring oscillator (ROSC), and ii) a dynamic memory cell. The former is a well-known test circuit, widely used to characterize device technologies [2], [12], due to its simplicity. We characterize their behavior in terms of: operating frequency, power consumption (PW) and switching energy.

On the other hand, we also analyze the impact of technology alternatives on the performance of a dynamic

memory cell. In this context, we select the 3T1D-DRAM cell that is becoming a promising memory cell to substitute the well-established 6T-SRAM cell in memory data caches [11]-[13]. The 6T static cell behavior is highly affected by device variability, which leads to a significant speed degradation and cell instability. Although the 3T1D cell is also affected by process variations, they do not have a critical impact on the operating frequency, unlike in the 6T case [13]. Further, 3T1D provides: lower cell area, non-destructive read process (in contrast to the conventional 1T1C-DRAM) and large retention time. Note that 3T1D cell is a Dynamic RAM, and the memory storage node is a capacitor (the gate capacitance of D1). Fig. 1 illustrates the conventional 3T1D cell. For all the technologies, a supply voltage of 1V is usually applied during all this work. Moreover, to measure the cell behavior, we analyze the following parameters:

a) Retention Time (RT), time required for the storage node voltage (V_S) in the cell to decay to V_{Smin} [14]. This is our reference parameter to analyze the cell as it is a DRAM.

b) Write Access Time (WAT) defined as the time elapsed between $V(WL_{write})=(0.5*V_{DD})$ and $V_S=(0.9*(V_{DD}-V_T))$.

c) Read Access Time (RAT) defined as the time elapsed between $V(WL_{write})=(0.5*V_{DD})$ and $V(BL_{read})=(0.9*V_{DD})$.

d) Dynamic Power consumption (PW) obtained by the average value along one complete cycle.

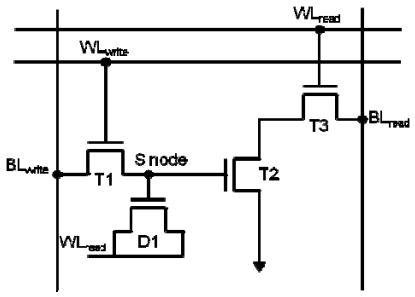

Figure 1. Schematic structure for a 3T1D-DRAM memory cell, where WL is wordline and BL is bitline.

C. Environment conditions for the reliability evaluation

Variability and soft error tolerance are considered in this study. For the former, we carry out 10000 Monte Carlo simulations. The process fluctuation is always reflected into a deviation of the threshold voltage (σ-V_T) of the transistors [1]. Table I depicts the variation levels assumed along this work for each technology [10], [11], [14] considering together all the variability sources. FinFET-based circuits present smaller V_T-shift ranges due to their lower doping [1], [6]. For the III-V/Ge MOSFETs, we assume the same process fluctuation levels as planar CMOS devices, since both are built in a similar way [10]. To analyze the variation level, the $3\sigma/\mu$ ratio (in percentage) is considered, where μ is the mean distribution and σ the standard deviation. For a more complete analysis of the memory cell, we also compute the manufacturing yield (at 99%) of a 2kB memory block, under the different variability scenarios. The circuit is evaluated with a reconfigurable array of 32 cells per column, 512 columns and 24 redundant columns as indicated in [14]. In this context, for yield analysis, a 3T1D cell with a retention time lower than 714ns is regarded as defective. Setting this minimum value for the retention time ensures the performance loss in a system with 3T1Ds will be within ~2% of an ideal 6T design [13].

TABLE I. V_T-VARIABILITY LEVELS STATED FOR EACH TECHNOLOGY TREND.

Variability levels	planar bulk	FinFETs	III-V MOSFETs
Moderate (M)	10%	7%	10%
High (H)	20%	15%	20%
Very high (VH)	40%	30%	40%

In the case of soft error study, we simulate the impact of an ion strike with a pulse wave current modeled with a double exponential function [4]. For a more accurate simulation of the ion impact, we assume different ion pulse shapes for each technology under study [12], [16]. Note that, we only focus on strikes occurring in the drain region of the nMOS, which accounts for most of the soft error upsets, even in scaled devices [17]. Moreover, we have analyzed SER at room temperature as a negligible impact on Q_{crit} is observed [5]. So then, in the SER study of the logic circuit we analyze the electrical masking, as well, which represents a common sign of a possible mitigation of the soft errors [12]. In fact, we obtain the minimal charge injected to upset the logic value at the strike node (output of the first inverter) and the observed related charge variation at the fourth stage of the inverter chain, when it is based on the different technologies. The difference depicts the relevance of the electrical masking, since the propagated pulse magnitude decreases and its width is widened. Fig. 2 illustrates the schematic representation of the SER simulation performed in the case of an inverter chain analysis, where the ion strike is produced in the first stage. In the case of the 3T1D cells, we simulate the impact of ion strike on the cell behavior. To the best of the authors' knowledge, this is the first time where SER is analyzed in FinFET or III-V-based 3T1D cell circuits.

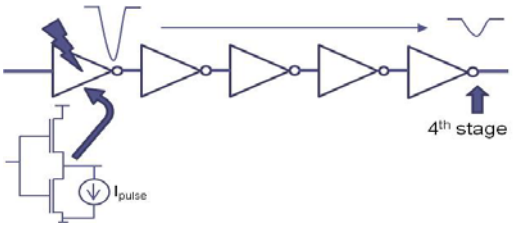

Figure 2. Schematic of the soft error analysis. The shrink of the propagated pulse illustrates the electric masking of each technology trend.

Finally, the influence of the environment temperature on the 3T1D memory cell behavior is analyzed as well for the three technologies. For this, the temperature is swept from 25º to 125ºC. It's worth noting that in all the FinFETs analysis the self-heating effect [18] is taken into account.

III. INFLUENCE OF TECHNOLOGY CHOICE

Throughout this section, we analyze the impact of the different technology alternatives in the performance for both circuit types (ROSC and DRAM cell).

A. Relevance on ROSC performance

First, we analyze the effects of reducing the supply voltage on the ROSCs performance. Fig. 3 shows the performance of

the different technology trends when V_{DD} is swept from 0.4 to 1V (bigger symbol means higher V_{DD} value). Fig. 3a depicts that FinFET-based ROSCs always present the highest frequency. Meanwhile, the III-V/Ge-based ROSCs point out lower values of frequency. When we compare the different technologies, we observe that FinFET circuits show better relationship between frequency and power consumption, since their performance is higher at low voltages. FinFETs have a significantly higher frequency (~8X), for smaller power consumption increase (~6X). This improvement observed in frequency, and penalty in power consumption in the FinFET-based circuits, is related to higher driving current capability of their structure for the same V_{DD} and also the reduction in their gate capacitances. In order to corroborate the outperforming behavior of FinFET-based ROSCs, Fig. 3b presents the switching energy, which represents the energy efficiency of a logic circuit, and it is related with the power-delay product. Thus, FinFET-based circuits depict the best performance, unlike planar bulk devices that present a slightly larger values, in accordance to the FinFET better electrostatic properties [6].

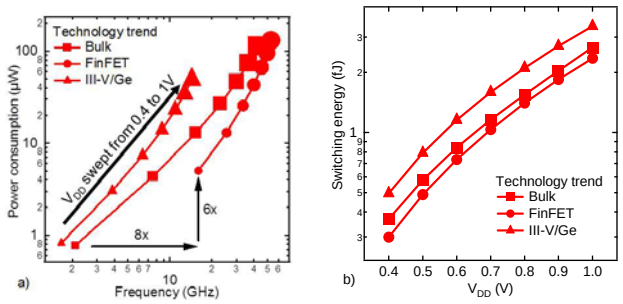

Figure 3. Relevance of the technology trend, i.e. bulk (square), FinFET (circles) and III-V/Ge (triangles), in ROSC under different scenarios: a) Relation between dynamic power consumption and operating frequency of the analyzed ROSCs. b) Switching energy as V_{DD} is reduced.

On the other hand, because the environment temperature is always considered a relevant factor (that may determine the final behavior of an electronic circuit), we analyze its impact on the different ROSCs behavior. Fig. 4a illustrates the performance of the ROSC when temperature is swept from 25 to 125ºC (bigger symbol means higher temperature). Both FinFET and III-V/Ge-based ROSCs present a frequency increase, and consequently power consumption, as temperature rises up, in contrast with the reduction observed in the planar devices. This behavioral difference is explained by the higher temperature dependence on mobility of planar

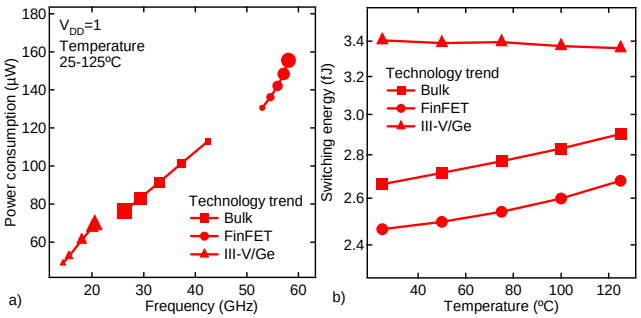

Figure 4. Impact of the environment temperature on ROSCs PW and frequency (a) and switching energy (b), when they are based on bulk (squares), FinFET (circles) and III-V/Ge (trtiangles) .

MOSFETs, because their higher doping deteriorates the mobility, unlike the significantly less doped FinFET devices [19]. Afterwards, Fig. 4b analyzes the temperature impact on the switching energy, and FinFET circuits present the lowest switching values proving again their better energy efficiency. While both FinFET and planar CMOS point out a slight energy increase as temperature rises, in III-V circuits it remains almost constant. This different behavior of the III-V circuits is caused by the different materials used. Note that, FinFET-based ROSCs present a worst ratio between power consumption and operating frequency as temperature increases, i.e. higher increase on power consumption than in operating frequency. This behavior is caused by the self-heating effect in FinFET devices [18].

B. Impact on 3T1D-DRAM cell performance

In the context of the 3T1D cells, Fig. 5 illustrates the memory behavior for each technology when V_{DD} is swept from 0.4 to 1V. FinFET-based memories show the best overall cell behavior since they present the highest RT and the smallest access times (WAT and RAT). On the other side, III-V/Ge-based cells present the lowest RT. We attribute these results to the higher leakage currents present in bulk and III-V/Ge technologies, in contrast to FinFET one [6]. In terms of access times, FinFET-based DRAM cells show the smallest values such as for WAT and RAT.

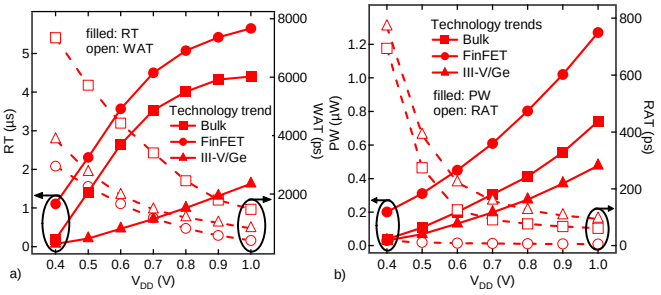

Figure 5. Impact of each technology trend on 3T1D-DRAM performance focused on RT–WAT (a) and PW-RAT (b), when V_{DD} is swept (0.4–1 V).

The 3T1D-DRAM cell performance study shows a clear dependence on temperature, since the stored voltage is highly dependant on it [7], and even more than the device degradation [15]. In this sense, Fig. 6 shows their impact on the 3T1D memory based on the different technology alternatives. Fig. 6a displays larger RT robustness for planar devices as temperature is swept (25-125ºC), in contrast to a relevant retention time reduction for the FinFET-based cells. This can be attributed to the self-heating effect produced in the

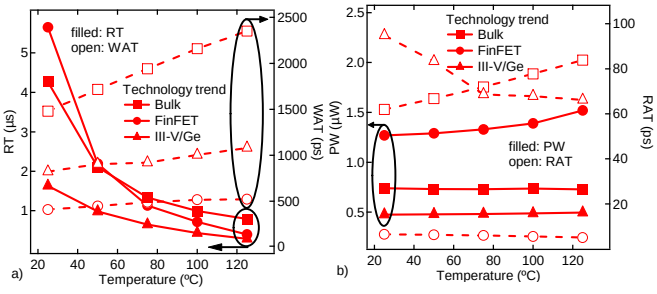

Figure 6. Impact of each technology alternative on 3T1D-DRAM performance measured as RT–WAT (a) and PW-RAT (b), when environment temperature is swept up to 125ºC.

FinFET structures [18] that when coupled with the high dependence of the retention time on temperature [7] lead to this significant RT reduction. Otherwise, FinFET cells show smaller impact on both access times, in contrast to the other two technologies.

IV. Variability Impact on the ROSC and 3T1D Cell

In this section, we analyze the impact of the random process fluctuations in both ROSC and 3T1D circuits, when they are based on the different technologies.

A. *Variability impact on the ROSC*

In this context, we focus on the oscillation frequency and power consumption for the different ring oscillators. Fig. 7 illustrates that as variability level increases larger parameter variation is observed. Moreover, the FinFET-based ROSCs are the circuits with lower influence of the V_T-shift, i.e. more robust against variability. This result can be attributed to the smaller σ-V_T observed in FinFET [1], due to the lower doping required. On the other side, although planar CMOS and III-V circuits are subject to the same variability levels a slightly smaller impact on circuit performance is observed for III-V.

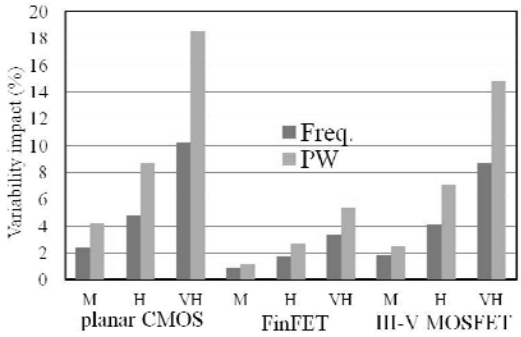

Figure 7. Variability impact on ROSC circuits for the three fluctuation levels considered, i.e. moderate (M), high (H) and very high (VH).

When considering the environment temperature on top of the V_T-variation, FinFET-based ROSCs again show the highest robustness in front of a moderate process variation level and temperature shift. Fig. 8 depicts higher variability impact for all circuits as temperature rises up. Again, the ROSCs based on FinFET devices present the smaller performance variation. Fig. 8a illustrates a reduction of the mean frequency for the circuits based on the conventional planar devices with temperature.

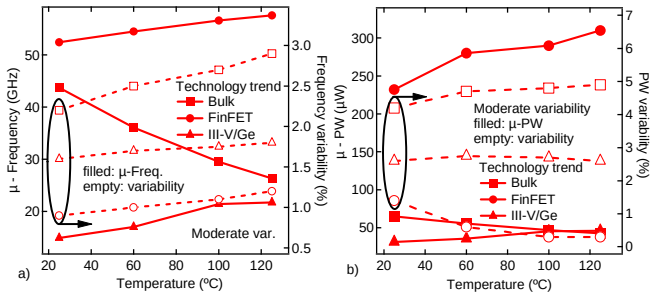

Figure 8. Impact of the environment temperature in the analyzed logic circuits, focusing on frequency (a) and PW (b), and when they are based on different technology trends and under a moderate variability scenario.

B. *Variability impact on the 3T1D-DRAM cell*

In order to avoid an excessive extension of the study of the 3T1D cell analysis, we only focus on retention time analysis albeit similar trends are obtained for the other cell factor metrics [14]. Fig. 9 depicts the FinFET-based results with reduction of half of the variability impact of the V_T-shift, i.e. more robust against process fluctuations. This result can be attributed to the smaller σ-V_T observed in FinFET [1].

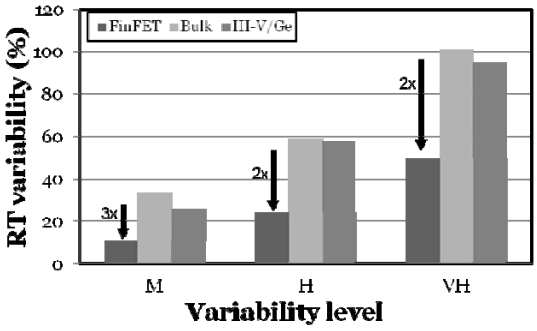

Figure 9. Impact of the process variation on 3T1D-DRAM cells, when it is subjected to different variability levels, i.e. moderate (M), high (H) and very high (VH).

Fig. 10a illustrates FinFET-based cells alternatives with the best variability robustness in comparison with both planar bulk and III-V/Ge MOSFETs as temperature rises up. Nevertheless, both FinFET and III-V/Ge-based cells show a slight RT variability reduction with temperature, in contrast to planar MOSFETs. This difference can be explained by the higher temperature dependence on mobility of bulk MOSFETs [19]. Since their higher doping levels deteriorates their mobility, unlike the significantly less doped FinFET devices. Additionally, we have also carried out a study on the performance of a 2kB memory block based on 3T1D-DRAM cells. In this context, Fig. 10b shows that in all cases the 2kB memory block proposals fulfill the time criterion (714ns) at moderate variability level. Note that each point represents the RT to achieve a 99% yield. Otherwise, when the environment temperature is raised to 60ºC (open symbols) solely FinFET-based memory blocks meet the criterion imposed. Moreover, we also sweep the memory block size (1-32kB), and we observe that the FinFET cells meet the time requirement even at 60ºC with a memory block of 32kB. In contrast, planar memory blocks only reach the time criterion for 1kB at 60ºC. Finally, III-V/Ge cells scarcely reach the imposed 714ns for a 2kB memory blocks at room temperature.

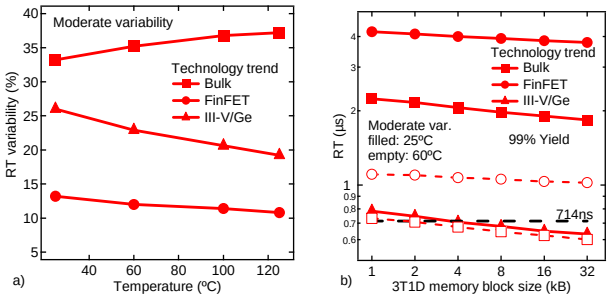

Figure 10. Impact of the environment temperature on 3T1D cells under a moderate variability scenario (a), and memory block (b).

V. SOFT ERROR IMPACT ON CIRCUITS

A. *Soft errors in logics circuits*

We consider the soft error test environment for the logic circuits and the different technologies. In order to analyze the relevance of the soft error rate, we simulate an inverter chain as it is pointed out in Fig. 2, since with this logic circuit we are able to observe the SER disturbance. First, we obtain the minimum injected charge (IC_{min}) required to upset the output of the primary node logic value. To do this, we use different nodes for all the technologies analyzed in this work, i.e. planar CMOS (32, 22 and 16nm), FinFETs (20, 16 and 7nm) and III-V/Ge MOSFETs (30, 22 and 16nm). Fig. 11a shows the minimum injected charge required as a function of technology node. We observe an IC_{min} reduction when the dimensions are shrunk down for all the technologies, as expected. So, the injected charge depends on the node capacitance of the circuit and that decreases with device scaling. The values obtained are in accordance to the predicted by ITRS [3], and similar ones are observed between all trends [16].Another relevant factor in a logic circuit is the electrical masking. This is evaluated by injecting a charge at the first stage, which causes a propagated pulse exceeding $0.5*V_{DD}$. This pulse propagates through the inverter chain and its charge is read at the strike node and also at the fourth stage of the logic circuit (Fig. 2). The reduction of this charge between the two nodes shows the masking efficiency of each technology. Fig. 11b shows the electrical masking effect for the different technologies as a function of V_{DD}. To analyze it, we compute the ratio between the injected charge that causes a pulse larger than $V_{DD}*0.5$ at both the strike node and at the fourth stage. In these terms, the III-V/Ge inverter chain outperforms the other two options at low supply voltage ranges, since it presents a larger ratio (~5X). This is caused by their higher drive current at low V_{DD}, and also to the reduced transient duration [12].

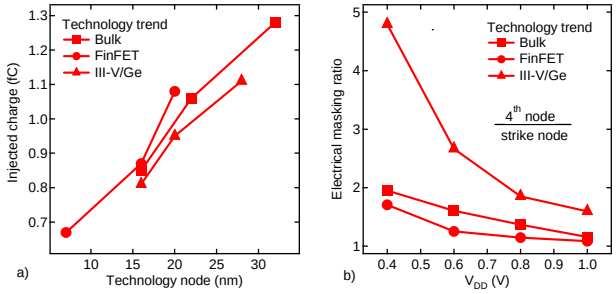

Figure 11. a) Minimum amount of injected charge required to trigger an upset event as device dimensions are reduced. b) Study of the electrical masking relevance in function of the different technology trends.

B. *Soft error in 3T1D-DRAM cells*

In the context of the dynamic memory cell, first, we observe that the drain region of the gated-diode (D1) and the read access transistor (T3) are connected to the word line read and bit line read of the cell (Fig.1), respectively. This involves high capacitance values at those nodes and, consequently, better robustness in front of soft errors. Thus, we only consider the relevance of an ion strike on the drain region of T1 (write access transistor) and T2. Hence, Fig. 12a depicts the impact of an ion strike on the storage node of the DRAM cell, during a write-read cycle. While an ion impact on the drain region of T2 (empty symbols) is negligible, their strike on T1 produces a significant reduction of the V_S as a function of the injected charge. This effect is critical to the cell performance, since this voltage is related with the retention time of the dynamic memory cell. For this reason, we concentrate on the SER impact on T1 for the rest of the paper. Then, when we compare the behavior of the different technology alternatives we observe that FinFET-based cells present a gentler slope of this V_S-shift in contrast to the other two alternatives. This means that a larger injected charge is required to shift the same amount of voltage, i.e. higher cell robustness. For instance, to obtain a V_S-shift about -0.5V the FinFET-based cells require a larger charge injection. On the other hand, we also study the impact of an ion strike when the cell is in retention mode (hold mode), i.e. no voltage applied to the cell and with logic 1 stored in the cell. Moreover, we have also analyzed the relevance of the environment temperature into SER. In this context, our simulations show a marginal impact of temperature into the critical charge determination [5]. Fig. 12b shows a negligible increase of the IC_{min} required for a V_S-shift of 0.5V as temperature increases.

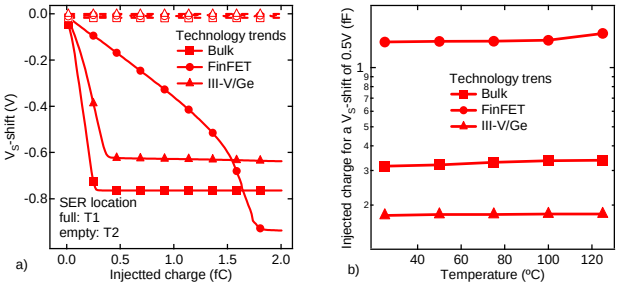

Figure 12. a) Impact of the injected charge in the storage node of the 3T1D cell at V_{DD}=1 in a write-read cycle, a reduction on V_S is observed. b) Negligible influence of environment temperature into the IC_{min} is observed.

Additionally, we analyze the SER relevance when the impact is produced at the beginning of the data retention period (1ps after the value is written). Then, Fig. 13a illustrates how the retention time is reduced as a function of the injected charge to the storage node. The larger the injected charge, the higher the RT reduction. In this sense, FinFET-based cells outperform the others once again, since they require a significantly larger injected charge (10X) to drop to the minimum retention time (714ns). This is caused by their topology, i.e. smaller area [2]. But this case cannot be considered the worst one in hold mode (no voltage applied to the cell), since a large amount of voltage is stored. For this, Fig. 13b shows the charge required to lose the data as a function of the instant where the ion impact is produced during the hold period. Thus, the larger the time in hold mode (less stored voltage), smaller the injected charge needed (more sensitivity to SER). In this study, when temperature is also considered all the technologies show similar tendency in the IC_{min} reduction required to upset the data when temperature is raised up (dashed lines), as it is observed in Fig. 13b for FinFET-based 3T1D cells. But, we mainly relate to the higher influence of temperature into the RT [14], as we observed in Fig. 6a, than to SER.

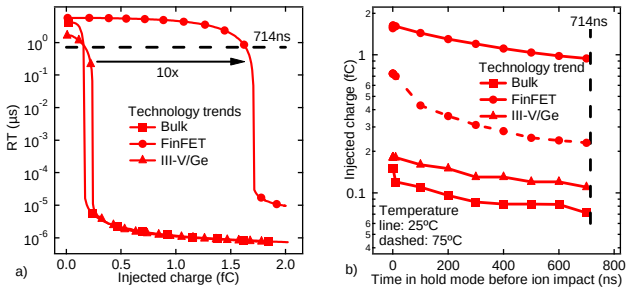

Figure 13. a) Reduction of RT in hold mode when a SER impact in the storage node of the 3T1D cell at V_{DD}=1. b) Influence of SER in hold mode for a logic 1, longer the time, the smaller the injected charge required to upset the node. In this context, temperature relevance (dasehd lines) is also analyzed, but the IC reduction is similar for all technologies, and it is related to the high tempretaure influence in RT.

VI. Conclusions

We have analyzed the performance of three device technologies (planar CMOS, and III-V/Ge MOSFETs FinFET), when they are used to implement different circuits, a ROSC and a dynamic memory cell, 3T1D-DRAM. In general, FinFET-based circuits outperform the other two technologies, since they present better overall behavior. Additionally, they deliver higher robustness against variability and soft error scenarios, thanks to their lower doping and device topology. This behavioral enhancement confirms FinFET as the most promising device for technology nodes beyond 20nm.

Acknowledgment

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