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Impact of Adaptive Proactive Reconfiguration Technique on Vmin and Lifetime of SRAM Caches

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Abstract

This work presents a test and measurement technique to monitor aging and process variation status of SRAM cells as an aging-aware design technique. We have then verified our technique with an implemented chip. The obtained aging information are utilized to guide our proactive strategies, and to track the impact of aging in new reconfiguration techniques for cache memory structures. Our proactive techniques improve the reliability, extend the SRAMs lifetime, and reduce the Vmin drift in presence of process variation and BTI aging**.**

Keywords

Process Variation, SRAM, reconfiguration, BTI, Vmin

1. Introduction

One of the main challenges in VLSI nano-scale technology nodes is the design for reliability, in presence of process variation and Bias Temperature Instability (BTI) aging mechanisms [1].

Process variation phenomenon causes with in chips are divided into two major types, i.e. systematic and random. With technology scaling down, the impact of random variations becomes more significant. Random variability in nano-scale integrated circuits, based on planar bulk CMOS is mainly due to Random Dopant Fluctuation (RDF) and some other phenomena such as the Line Edge Roughness (LER) [2]. These phenomena result in the variation of transistor parameters such as mainly the threshold voltage (V_T).

On the other hand, BTI aging is the result of devices being under electrical stress, when a negative voltage to gate of PMOS (NBTI), and positive voltage to NMOS (PBTI) is applied [3]. It also degrades the transistor parameters such as mainly shifting the V_T. Note that, some part of BTI wearout can be relaxed, if the device experiences some recovery phase [4]. This motivates some circuit design approaches that allow the devices to enter into recovery mode some period of time, to reduce their aging, and extend their lifetime [5].

Generally, SRAM cells are built with minimum device dimensions to increase the density of caches. This emphasizes their sensitivity to process variations. Furthermore, they might also store a bit for a long period of time (long stress time). Therefore, some SRAM cells might fail due to prolonged aging and process variation. Then, one possible solution to avoid early fails is to increase the supply voltage (V_{DD}); that makes the static noise margin (SNM) larger, but also causes a faster aging [4]. To allow the cache memory to keep performing its function and to improve the yield in cache memories the failed memory columns/rows are usually substituted with spare columns/rows, in a technique called reactive reconfiguration [5]. However, the reserved spares may never be used in some cases in the reactive technique, so instead of reserving all the spare units up to time of failure, they can also take part in the normal operation of the system in a technique called proactive reconfiguration. This technique, manages all the available resources in the system (the functional and the reserved spare units) in the normal operation of system. This concept firstly introduced by IBM [5], provides the possibility for the system elements to work on two modes, active and sleep modes, and slows down the overall system aging, by balancing the workload among all units. Note that, proactive reconfiguration in memories can be implemented in different granularity levels such as memory arrays, memory rows or columns. In this paper, memory columns are used as the reconfiguration elements, as they are more effective in repairing faults (i.e. bitline, sense amplifier, column multiplexer) [6]. The works [5, 7] utilize proactive reconfiguration to extend the cache lifetime by benefiting from BTI recovery properties, and [8] extends and improves the proactive reconfiguration concept by considering also process variation among memory cells. Our present work proposes a circuit technique to monitor the degradation and process variability of the 6T SRAM memory cells. We have implemented a chip prototype oriented to demonstrate the effectiveness of our proposal; the principles of the chip are also included in this work. We then analyze the impact of adaptive proactive reconfiguration in design parameters of 6TSRAM cells such as the SNM.

To save power, SRAM cache memories have two minimum operating voltages: one is applied at standby period (Vmin_standby), and the other at normal operation of memory (Vmin_active) [9]. In our work we consider the impact of these dynamic supply voltage levels on the device aging and propose an adapted proactive strategy. Therefore, the memory components may be in two modes: active and standby, affected by the applied voltage level, and their aging status. Note that, although applied to a given CMOS technology (32nm), our proactive strategy can be considered technology independent, as an efficient approach for improving reliability and reducing the Vmin drift in memories.

This work is organized as follows: Section 2 describes our modeling approach for the BTI aging and memory parameters. Section 3 presents the test and implementation methodology to monitor the SRAM cells in cache memory columns, with our implemented chip. Next, Section 4 analyzes the proactive approaches with dynamic voltages and their impact in cache memories, and finally Section 5 concludes the paper.

2. Analysis framework and modeling

In this section we present our modeling methodology for the parameters used in the paper, such as the BTI aging, the V_T fluctuations, the memory design parameters, like the SNM and the relation between memory Vmin drift and BTI aging.

2.1. BTI aging, stress and recovery phase parameters

One of the main impacts of the BTI aging is the increase of V_T, which magnitude depends on three variables: stress time (t), supply voltage (V_{DD}) and temperature (T). The BTI aging is usually considered in two different phases: stress and recovery. Several models have predicted the V_T shift in devices [10, 11] caused by BTI. Since our work is an analysis during a long period of time we simplify the model, explained in detail as follows. Note that, we have assumed high-k transistors in our work where both N and P transistors experience BTI aging [10].

In stress phase, the device experiences some V_T shift due to aging mechanisms affecting materials. Previous works have demonstrated that the V_T shift during the device lifetime is sub-linear, i.e. with a fast aging slope at the beginning, and a posterior slower slope. Therefore, we have modeled the BTI aging stress phase with piece-wise linear slopes. Figure 1.a illustrates the stress model with an initial sharp increase at the beginning of stress phase and some decreasing slopes in the following of the lifetime.

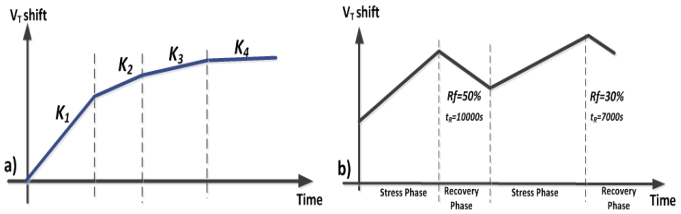

Figure 1: a) V_T shift and aging slopes of a device under stress during different time periods of device lifetime, b) BTI wear-out recovery behavior with different recovery factors

Note that, we assume a fixed temperature in this work, and do not insert it in our computational model. However, we consider the impact of V_{DD} in the V_T shift stress phase (higher V_{DD} results in higher V_T shift) as below:

$$\Delta V_T = A(V_{DD}) * K(t) * \Delta t_S \qquad (1)$$

where Δt_S is the stress time, K(t) is the aging slope (K(t) differs in each time period) and $A(V_{DD})$ is the supply voltage coefficient impact on the aging. The linear slopes and the supply voltage impact in aging are both obtained from previous experimental measurements [4, 11].

It has been demonstrated that when the device is released from stress, a wearout recovery occurs and relaxes some part of V_T shift as shown in Figure 1.b. We have modeled this wearout recovery in respect to different possible technologies with a parameter, named recovery factor, (Rf), which we define as the percentage of the V_T shift relaxation. We also compute the Rf, based on recovery period length, which depends on the proactive algorithm. For instance, Rf =50% means that 50% of the V_T shift from the previous stress phase would be recovered. Experimental measurements [4] have demonstrated that the device have a sharp recovery just after being released from stress phase and later the recovery gets slow and finally it will have the maximum possible of wearout recovery after a recovery time of t_R=10^4 seconds (in a non applied reverse voltage mode).

2.2. Memory Parameters

In order to analyze the impact of V_T changes, due to BTI aging in nano-scale 6TSRAM memory cells, we establish the dependence of V_T shift to memory reliability metrics. The metrics analyzed in this paper are the SNM and the Vmin, since previous works have demonstrated that these are the mostly affected by the BTI aging, and other metrics such as the cell write margin might be negligibly affected by the BTI aging [12]. We also consider a static stress for the SRAM cells in which the cells store the same data for a long period of time. It has been illustrated that SNM, under static stress varies linearly with V_T shifts in FETs [12, 13]. Therefore we have used a linear equation to relate the V_T shifts to the SNM, in our simulations:

$$\Delta SNM = -M * \Delta V_{TBTI} + C \qquad (2)$$

To calculate the M and C parameters in equation 2 (a line equation) we have simulated and computed the SNM at 2 points; one at time 0 (non-stressed), and the other after a V_T shift of 50mV in the corresponding stressed N and P FETs of 6T SRAM. Finally, to analyze the impact of BTI aging in Vmin drift of SRAM memory cells, we have considered a linear relationship between the memory SNM and the Vmin [13, 14, 15]. Therefore, SNM drop due to device aging, results in linear increase of Vmin. We will use these modeling approaches in section 4 to show the impacts of our proactive approach. Before, in the next section we present our aging monitoring technique for the SRAM cells in memory columns.

3. SRAM monitoring test and chip implementation

In this section we present a test procedure, as well as circuits and chip implementation details for our aging monitoring technique.

3.1. Aging monitor in SRAM cells

In order to evaluate the time zero variation and aging status (V_T value) of the SRAM cells in a cache memory array, an on chip monitoring circuit is required [16,17,18]. In this work, we propose a monitoring approach that can measure the BTI wearout of the individual SRAM memory cells in each memory column, which also considers the process variation among the SRAM cells. Our approach monitors the SRAM cells degradation in a column-by-column sequence, without effect on the normal memory operation, since it is applied when the specified memory column is in recovery mode and disconnected during the normal operation of the column. To implement the monitoring circuit for the 6T SRAM cells, two current mirrors are connected to the bitlines of a memory column. These measure the aging in the SRAM transistors (pull-down NMOS and pull-up PMOS) by tracking their current during the cell lifetime. The test process has two steps described as follows: i) a logic value ´1´ is written to all the cells in the column being tested (the column in recovery mode), then a counter enables each wordline one by one, to monitor the degradation in each one of the corresponding pull down (left (L)) and pull up transistor (right (R)) of a specific SRAM cell; ii) a ´0´ is written to all cells of the column, again the counter turns on each wordline one by one and this time the monitoring circuit measures the degradation in the other pair transistors of the SRAM cell. Figure 2 shows the scheme of our proposed monitoring circuit for the SRAM cells in the memory columns.

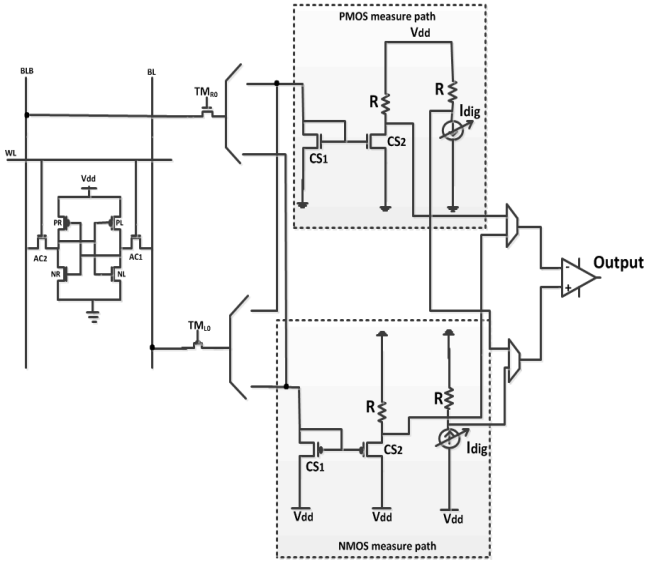

Figure 2: Process variation and aging sensing scheme

The current from the SRAM transistors (N/PMOS transistors except the access ones) is compared with the current of a digital current source, which is controlled, by a controller and the point where these two currents get equal the comparator´s output changes, and the value of current and its respective V_T value is recorded in a register.

Note that, the TM and the current mirror transistors are designed as long and wide channel transistors in order to avoid short channel effects in the devices and assure a perfect match of mirrored current (there is only a monitor circuit per a set of memory columns, so we expect a low overhead). The transistors (AC, TM) on the circuit path do not experience significant aging as they are only switched on for a short time, when a specific SRAM is accessed. Therefore, the value of the mirrored currents will be an indication of the corresponding SRAM transistors strength. Then the measured current will be digitalized and used by a global reconfiguration controller (Figure 3) for our proactive techniques.

Figure 3 shows the memory architecture proposed in this work with its proactive circuitry for a set of 17 columns (16+1 spare). We use one monitoring circuit per set of 17 columns and this avoids the impact of process variation and aging mismatch among the sensor devices, as the same measurement condition is applied among all the cells and columns in a reconfiguring

set. Our proposed architecture design keeps the original memory framework and it allows applying our proactive mechanism with just adding some circuitry to the memory. As an example, a 1kB SRAM memory consists of 128 columns divided into 8 groups of 16 columns and each memory column contains 64 6T SRAM cells. It can be assumed that the 1kB memory contains 8 unused spare columns and each one of the spare columns belongs to one set of the 16 columns.

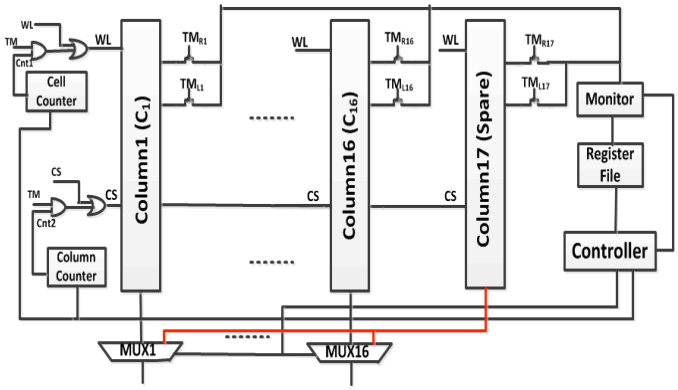

Figure 3: A group of 16+1 columns with adaptive proactive methodology

When all columns test finishes, the digital values representing the aging status of each column are recorded and used by the reconfiguration controller in order to let the columns be in the recovery mode with a specified time, adapted to their BTI aging and time zero process variability.

3.2. Our designed chip

To demonstrate the effectiveness of our technique we have designed and fabricated an integrated chip in CMOS 350nm technology node. Note that, the purpose of our chip is not to compare the aging and variability between 32nm and 350nm technology nodes, but to experimentally analyze our technique as a verified aging (V_T shift) monitoring technique in SRAM PMOS transistors (SiO_2). Therefore, we emulate the V_T shift in our 350nm transistors by modifying the device body bias, since the process variation and BTI aging is not significant in the 350nm technology node.

Figure 4 depicts a detailed schematic for testing one of the PMOS transistors along with the current path for our monitoring approach (dotted line). Moreover, it shows the implemented approach to digitalize the current with a slight modification in comparison with Figure 2. The current from the analyzed SRAM`s PMOS transistor (PL) is first mirrored by the current mirror, and then it would be compared with a digital voltage value which is adjusted by the controller through a comparator. The point where these voltages get equal the output of the comparator changes the state. The controller monitors the state change of the comparator and the current value at this point, and then the digital value of the V_T in respect to it is recorded in a register file.

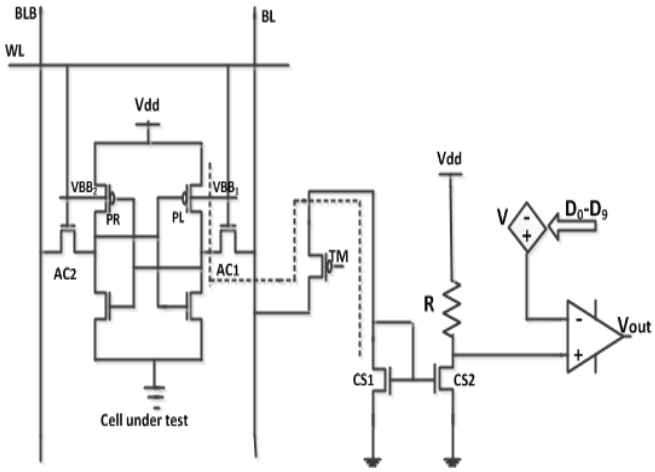

Figure 4: SRAM degradation monitoring scheme, the dotted line exhibits the path for monitoring the aging in one of the pull-up PMOS transistors

Figure 5 shows a picture of our manufactured chip, which contains three separate sections: i) Part one (P_1) is our monitoring technique with one SRAM cell sized with the minimum technology node (350nm), ii) part 2 (P_2) is same as the former but with bigger transistors for the SRAM cell (to increase the current and reduce the mismatch effect in our measurements), and finally iii) part 3 (P_3) contains 8 SRAM cells in a column and our monitoring sensor to be switched separately for each SRAM cell.

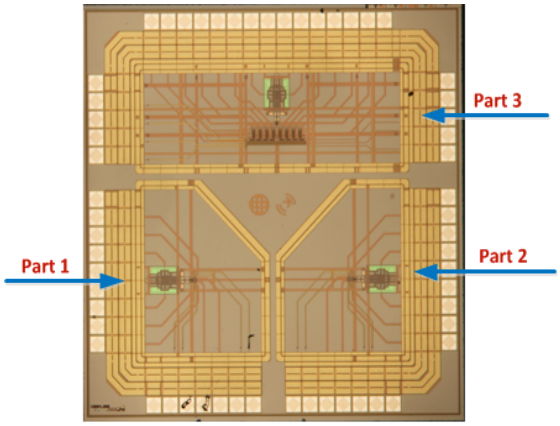

Figure 5: Our manufactured chip

Our objective for P_1 and P_2 is to prove our monitoring concept experimentally, and P_3 will show the benefits of our proactive methodology with an externally software controlled adaptive proactive technique. Figure 6.a depicts some of the monitoring datagrams of our P_1 chip simulation in Cadence, where we monitor the degradation in one of the SRAM PMOS transistors. In this test sequence of datagrams, first we write a ´1´ inside the SRAM storage node and later we sense (read) the current through the respective PMOS, when this current passes a known threshold, the comparator output changes and we can measure the aging status of the specified FET. Figure 6.b depicts the impact of changing the PMOS body bias in our monitoring technique.

We have performed a parametric analysis in Cadence and increased the PMOS body bias step by step. As depicted, this causes that the comparator output to change state at different time points regarding the V_T shift in PMOS and its current.

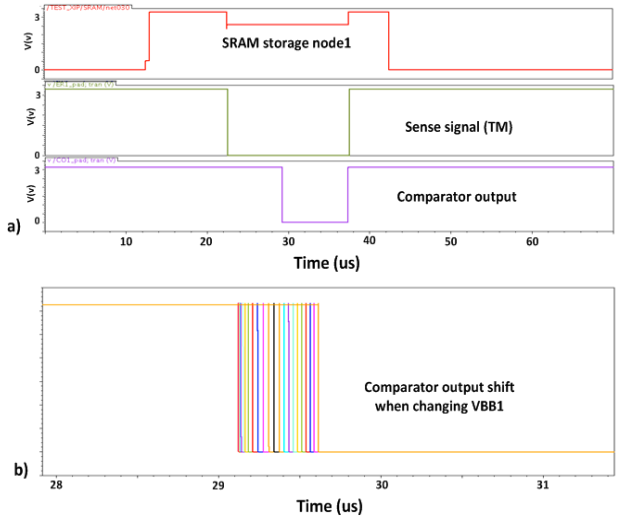

Figure 6: a) A test sequence of writing the value one in one of SRAM storage nodes and sensing the aging in the corresponding PMOS, b) Comparator output shift when changing body bias voltage of PMOS PL

4. Adaptive proactive techniques and their impact

In this section we will use the section 2 modeling and section 3 monitoring information, to implement our proactive techniques in Matlab.

4.1. Adaptive proactive approach in presence of single VDD

Our first approach of proactive reconfiguration relies on adaptive recovery periods of memory columns in which each memory column will experience different recovery period in respect to its weakest cell´s SNM. All the memory columns will experience recovery periods along their lifetime by a round robin method in which all columns (spare and operational columns) participate in the memory operation and have recovery ratios in function of their V_T and SNM value, affected by process variation and BTI degradation [8]. We implement our approach in Matlab by generating random V_Ts and calculating each cell SNM at time zero. Then, each column is recognized by the lowest SNM (weakest cell) on the column. During the memory lifetime, a test (described in previous section) is applied to all SRAM cells in all columns and calculates the SNM drift and determines the weakest cell and column. Note that, this operation does not necessarily causes an idle time in the memory system because the measurement can be performed while the corresponding column is in the recovery phase. Next, in a set of

columns, with one spare column among them, a loop allows the columns to enter in recovery mode, one at each time (for a specified respective time period). When we have more than one spare, the columns with close SNM values constitute one class and the loop is between different classes of columns. Depending to the number of available spares, a number of columns can go on recovery mode. The round robin loop is called a reconfiguration cycle and each step of it is named a reconfiguration step. In this approach, we assume the system has only one supply voltage and a memory column fails when the SNM of one SRAM cells becomes zero. Also we assume that each reconfiguration step will take at least 10^4 seconds of recovery time (for the maximum possible wearout recovery). Therefore, the reconfiguration cycle could present a magnitude of several days. In a single spare mode of column reconfiguration, at each step the spare column will replace a working column that goes to recovery and the column´s data is copied in the spare column. This copied data will be written back to the column before next column reconfiguration step. Figure 7 shows the convergence of SNM values, computed in Matlab, in a system consisting of 4 functioning and 1 spare column. This system is based on presence of one supply voltage (Vmin_active) and the wearout recovery (Rf) is assumed at 30%. The adaptive proactive approach balances the activity distribution between all SRAM cells, thus demonstrating the benefits of using adaptive recovery phase ratios during the columns' lifetime. It can extend SRAM memory columns' lifetime in comparison with no-adaptive proactive memories [8]. Also while the no proactive memories need to increase the Vmin of the memory to keep it functional, our approach can reduce this Vmin drift (because of slower SNM drop) along a specific period of time (5 years in our analysis).

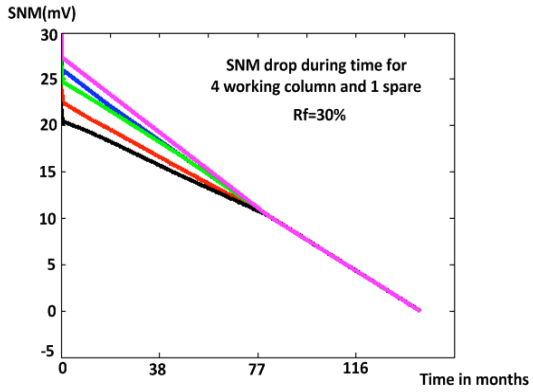

Figure 7: Degradation behaviour of weakest SRAM SNMs of memory columns due to BTI aging by utilizing our adaptive proactive reconfiguration

To show the benefits of our technique, we have performed 1000 Monte Carlo simulations in Matlab to compare our adaptive proactive approach versus the non adaptive approach with various number of operational (O) and spare (R) memory columns (O+R) and presented the results in Table I. The adaptive technique depicts a relevant reduction of the Vmin drift and extends the memory columns' lifetime.

Table I. Relative lifetime extension and Vmin reduction drift obtained by the proactive over the non-proactive technique for a memory based on different number of spare and operational columns

Configuration	Lifetime	Vmin drift reduction
4+1	3.5X	30%
8+2	3.2X	27%
16+1	1.5X	15%
16+4	3X	25%

4.2. Adaptive proactive approach in presence of dual VDD

Our previous analysis considers a cache memory system with only one Vmin. Nevertheless, usually cache memories are designed with two Vmins to save the power consumption, one supply voltage for when the cache is at standby mode and another when the cache is at active mode [9]. Figure 8 illustrates the memory operation along the time and with two Vmins.

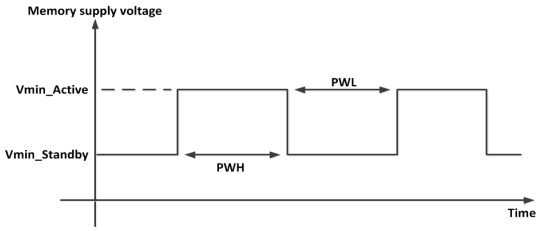

Figure 8: Memory operation during its lifetime consists of two mode of active and standby

As noted in section 2, a higher supply voltage causes more BTI aging in devices, so in our analysis we have taken into account different aging speeds at the cache standby and active mode. The value of SNM also depends on the supply voltage so we assume two different SNMs in our analysis, one is the SNM at Vmin_active and another one is the SNM at Vmin_standby. Considering the assumptions as above, we have reanalyzed our adaptive proactive strategy explained in the previous section. Figure 9.a depicts the BTI aging behavior of the weakest SRAM memory cells SNMs in the cache memory columns, and its comparison with no proactive (dashed lines) approach.

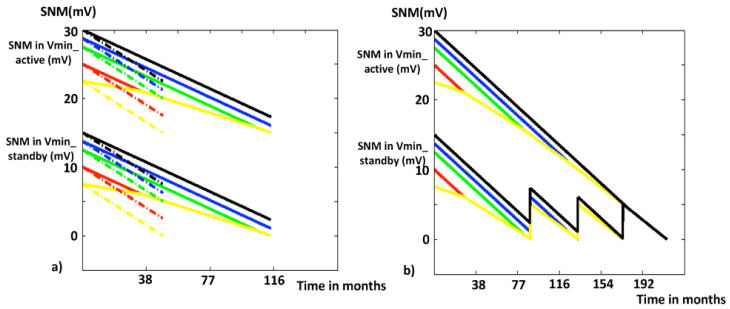

Figure 9: a) Aging behavior of SRAM SNMs in Vmin active and Vmin standby mode and comparison between proactive and no proactive b) Step by step Vmin standby increase during the memory lifetime

The memory fails when one of its columns SNMs reach to value '0', as the memory has lower supply voltage at hold mode and consequently smaller SNMs, it is more likely that the hold SNMs reach to the value ´0´. On the other hand, to keep the memory functioning and maintain the data at hold mode, memory designers usually consider performing some tests during the memory lifetime and increase the standby supply voltage [19]. Increasing the supply voltage step by step improves the hold SNMs and keeps the memory functional at lower voltages than active supply voltage. Figure 9.b shows the step-by-step supply voltage increase among the memory columns. The results illustrates that our adaptive proactive technique results in a final convergence of SNM at Vmin_active and the SNM at Vmin_standby and extends the SRAMs lifetime.

4.3. Supply aware adaptive proactive approach

The adaptive proactive approaches explained in sub-sections 4.1 and 4.2 are based on dynamic recovery periods of memory columns in respect to their time zero process variability and BTI aging along their lifetime. However, in order to enhance the reduction of Vmin drift and to improve the columns lifetime we should also consider the status of the supply voltage in the proactive round robin strategy. The Vmin_active induces more aging than the Vmin_standby, therefore in a system with high periods of active mode it is more efficient to put the weakest column\s to recover during the Vmin_active mode and to let them operate during the Vmin_standby mode. So, we propose a round robin method among the memory columns that is aware of supply voltage too. We put the weakest column\s to recover in Vmin_active while the other columns function. In Vmin_standby mode the weakest columns operate while the other columns experience recovery one by one in round robin. We also make a test in a specific sequence, e.g. once per day, to determine the weakest SRAM cell and its corresponding memory column. Figure 10 presents the recovery datagram for such approach, with 5 columns (C_1-C_5) where C_5 is considered the weakest column (has the SRAM cell with lowest SNM) that recovers in Vmin_active.

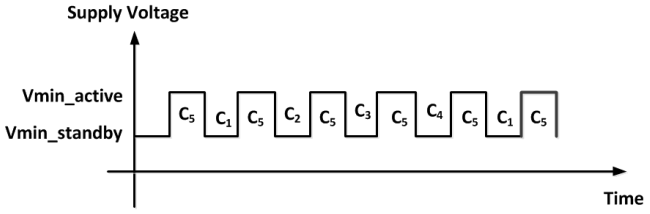

Figure 10: Round robin in respect to supply voltage showing at each moment the column under recovery

We have implemented our approach in Matlab, and Table II presents the impact of such strategy to reduce the Vmin drift of the memory system and extending the memory columns' lifetime obtained from 1000 Monte Carlo simulations. It depicts

that this technique can also reduce the Vmin drift (we only consider Vmin_standby drift) and extends the memory columns lifetime.

Table II. Relative lifetime extension and Vmin reduction drift obtained by the proactive over the non-proactive technique for a memory based on different number of spare and operational columns

Configuration	Lifetime	Vmin drift reduction
4+1	3.8X	35%
8+2	3.5X	31%
16+1	1.9X	20%
16+4	3.5X	30%

5. Conclusions

This work presents a test and measurement approach to monitor aging in SRAM cells. We have verified its applicability by a chip prototype. Many of used resources, such as the multiplexers, utilized in our proactive technique already exist in the memory for fault tolerant techniques; however our monitoring circuits take 10% area of the SRAM memory and have no performance loss, since it is applied when the memory column is in recovery. Then we show the application of our monitoring technique in a proactive scenario, based on adaptive recovery periods of memory columns. Moreover, we have introduced the proactive strategies in presence of dual supply voltages. Our proactive approaches extend the cache lifetime (1.5-3.5X) and reduce the Vmin drift (15-35%), depending to the configuration, along the memory lifetime.

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