Test of Dual Axis Accelerometers Based on Specifications Compliance

Álvaro Gómez-Pau, Luz Balado, Joan Figueras

Departament d'Enginyeria Electrònica, Universitat Politècnica de Catalunya
Av. Diagonal 647, 9th floor, E-08028 Barcelona (Spain)
{alvaro.gomez-pau, luz.m.balado, joan.figueras}@upc.edu

***Abstract*—Testing microelectromechanical systems (MEMS) devices is a challenging and time consuming task demanding high amount of resources. Devices targeting safety critical applications need to be efficiently tested in order to deliver reliable units to the market. MEMS systems require non electrical excitations inherent to their transduction functions what difficults even more the testing procedure. In this work, an accelerometer testing technique using octrees to encode the specifications compliance region is presented. The test proposal is based on the application of two phases [1], namely, training and testing. In the former phase, the acceptance region is generated according to device specifications and encoded using octrees. In the testing phase a novel test strategy is applied to a candidate device taking advantage of the benefits of evaluating octree structures. The method is applied to test dual axis accelerometers under parametric defects with encouraging results. Incurred test escapes and test yield loss as a function of the number of bits used to encode the octree have been statistically evaluated.**

***Index Terms*—Accelerometer Testing, Specifications Compliance Test, Octrees, Quadtrees, Test Escapes, Test Yield Loss, Lissajous Compositions.**

I. Introduction

Testing analog and mixed-signal circuits is a challenging task due to the limitations of current analog automatic test equipment (ATE) and the partial availability of systematic procedures to such purpose. Similar challenges are encountered when testing MEMS devices. Such systems present the same difficulties of M-S circuits plus the requirements of non electrical excitations due to their inherent sensing characteristics. These facts cause a significant increase of the testing costs of the final product and therefore the need for developing effective, reliable and low cost testing techniques to cope with these drawbacks [2]–[4].

MEMS accelerometers devices are commonly used in safety critical applications requiring the highest reliability levels. For that reason, novel solutions have been proposed in the literature as BIT/BIST techniques. For instance, Analog Devices outfits its accelerometers with a digital pin which electrostatically actuates the inertial mass for functional testing [5].

Several techniques have been proposed for testing MEMS accelerometers [4], [6]–[9]. A calibration method based on device models is presented in [10] while a pseudo random generator in order to obtain the input-output transfer function is used in [11]. The work in [12] targets device calibration by performing different sets of measurements considering several device orientations. An indirect testing method is proposed in [13] using regression techniques to map the parameters space to the measure space.

In this work, a testing technique for dual axis IC accelerometers based on specifications compliance is presented. To that purpose, the device is spun in a vertical spinning wheel and both orthogonal outputs are composed to yield a Lissajous composition [14]. The test is performed by checking whether the Lissajous trace lies in the specifications compliance region or not. This region is previously characterized and encoded using octrees. Such codification has been used by the authors in previous works with successful results [1].

The paper is organized as follows. Section II presents a brief description of integrated capacitive accelerometers and its behavioral modeling. Section III describes the two phases in the proposed specifications compliance test for dual axis accelerometers. Section IV introduces the concept of octree data structure and how it can be used to encode the specifications compliance region of MEMS accelerometers. In section V, the procedure of testing a candidate device using the octree data structure is explained and discussed. In section VI, the testing proposal is evaluated in terms of *test yield loss* and *test escapes* as a function of the number of bits used to perform the encoding. The *test application time* has been also studied. Finally, section VII summarizes the work and concludes the paper.

II. Dual Axis IC Accelerometers

MEMS accelerometers are composed by a set of three functional subsystems, namely, mechanical, capacitive transducer and electronic conditioning subsystems as depicted in Fig. 1. First and second stages correspond to the mechanical and capacitive subsystems where the transduction from acceleration to mass displacement and then to capacitance difference takes place. The latter stage corresponds to the electronic conditioning subsystem which generates the output signal. The transduction chain is replicated according to the number of device sensitive axes. In the following subsections each of these subsystems is briefly explained.

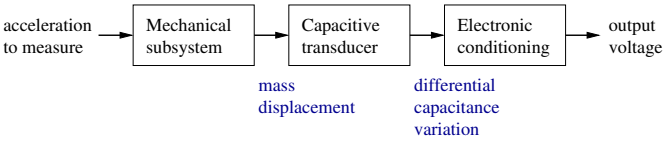

Fig. 1. Functional diagram of an integrated capacitive accelerometer. Three subsystems can be identified in the acceleration to voltage transduction chain. The involved magnitudes in the sensing process are also shown.

A. Mechanical Subsystem

The sensing principle in capacitive MEMS accelerometers is based on the displacement of an inertial mass attached by means of springs to the fixed substrate as Fig. 2 illustrates. When an acceleration a_{in} is applied, the intertial mass experiments a displacement x. The dynamics of such structures are complex, but they are usually approximated by the following second order motion equation, $\ddot{x} + \frac{b}{m}\dot{x} + \frac{k}{m}x = a_{\text{in}}$. Where m is the inertial mass, k is the spring constant and b is a damping coefficient. In quasi static operation or steady state, the mass displacement is approximated by $x = m/k\, a_{\text{in}}$.

Mechanical parameters usually determine the frequency response of the device thus the characteristic frequency of the system can be written as $\omega_0 = \sqrt{k/m}$. This frequency is usually in the range of units or tenths of kHz. The Q factor is determined by the characteristic frequency and the damping factor as $Q = m/b\,\omega_0$.

B. Capacitive Transducer Subsystem

The capacitive transducer structure is formed by a set of interdigitated fingers attached to the inertial mass as Fig. 2 depicts [15]. Fingers movement translate in a capacitance variation in both sides of the differential capacitive voltage divider formed by capacitors C_1 and C_2.

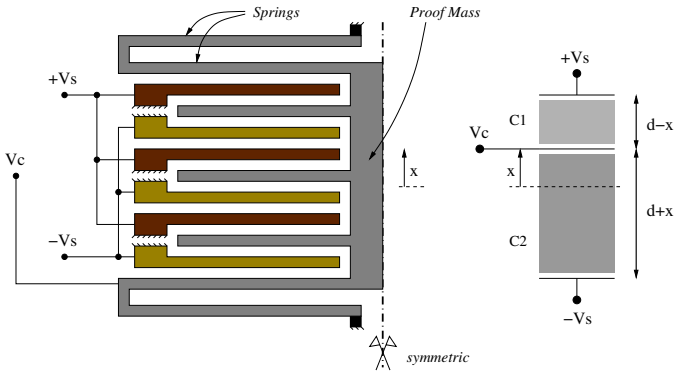

Fig. 2. Sketch of inertial mass and interdigitated fingers of the capacitive voltage divider. Inertial mass moves along x direction by means of the anchoring springs therefore unbalancing the capacitive voltage divider.

The capacitive transducer is usually supplied with a high frequency AC signal, denoted here as $\pm V_{\text{s}}$. Each of the capacitors in Fig. 2 depend on the medium permittivity ε, total plate area A and rest distance between plates d. The effective distance between plates depends on the mass displacements in opposite directions for both capacitors. When x is positive, effective d_1 decreases while d_2 increases and vice versa. Capacitive transducer output can be written as [15],

$$V_{\text{c}} = \frac{C_1 - C_2}{C_1 + C_2}\, V_{\text{s}}, \quad C_1 = \frac{\varepsilon_1 A_1}{d_1 - x}, \quad C_2 = \frac{\varepsilon_2 A_2}{d_2 + x} \tag{1}$$

Under the assumption of a fault free device, $\varepsilon_1 A_1 = \varepsilon_2 A_2$ and also $d_1 = d_2 = d$. The previous considerations make equation (1) simplify to $V_{\text{c}} = x/d\, V_{\text{s}}$.

C. Electronic Conditioning Subsystem

The electronic conditioning subsystem accommodates the output signal according to device specifications. As mentioned, it is usual to supply the capacitive transducer with a high frequency AC signal for mitigating resistive effects, so the electronic conditioning subsystem also performs the demodulation and filtering of the analog signal coming out from the capacitive transducer subsystem.

For the case of analog output accelerometers and assuming an ideal AC signal demodulation, the electronic conditioning subsystem can be supposed to act as a signal boosting stage with a certain gain G, therefore, $V_{\text{out}} = G\, V_{\text{c}}$.

The output signal is normally affected by an offset voltage V_{off}, which is also added in the electronic conditioning subsystem. Gathering the contribution of each of the subsystems in one single expression yields device output voltage, V_{out}, to a given input acceleration, a_{in},

$$V_{\text{out}} = V_{\text{off}} + \underbrace{G\frac{V_{\text{s}}}{d}\frac{m}{k}}_{\text{Sensitivity}}\, a_{\text{in}} \tag{2}$$

The term $S = G\frac{V_{\text{s}}}{d}\frac{m}{k}$ is the sensitivity of the device. Sensitivity is the most important functional parameter of an accelerometer and it distributes following a normal distribution as can be checked in different Analog Devices products datasheets [5]. In this work, both axes sensitivities are considered as functional specifications.

III. Test Based on Specifications Compliance

Conventional integrated accelerometers testing is carried out by means of horizontal spinning tables or tilt tables. Horizontal spinning tables use centripetal acceleration as input excitation since it is a well controlled parameter due to its dependence on the angular velocity and spinning radius. On the other hand, tilt tables take advantage of gravity acceleration to apply a static excitation to the device. In previous works, the authors have explored the possibilities of testing and diagnosing dual axis accelerometers using a vertical spinning setup [14], [16].

The vertical spinning proposal consists on rotating the device in a vertical plane following an arbitrary angular velocity profile, $\dot{\theta}(t)$, as Fig. 3 illustrates. While the device is rotating, both orthogonal device outputs are sensed and composed to yield a Lissajous composition. These traces are sensitive to catastrophic and parametric defects the device under test (DUT) may present and therefore become a suitable tool for testing such devices.

The test proposal departs from a Lissajous composition generated by the previously presented vertical spinning setup. Therefore, the classification of pass/fail devices is translated in taking the decision if a given Lissajous composition corresponds to a device which fulfills functional specifications or not. To this purpose, the proposed testing methodology is divided into two phases. The former corresponds to a training phase in which the specifications compliance region is computed using statistical and corner samples with the aid of octrees. The latter is related to the testing procedure itself.

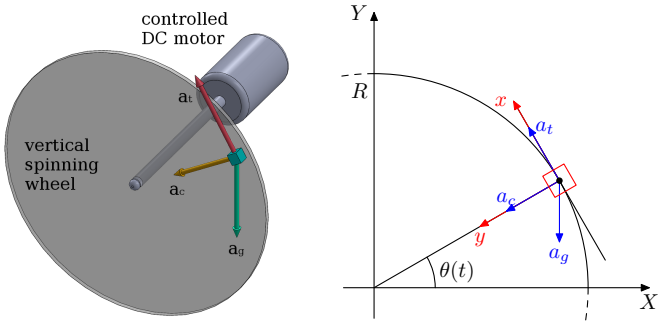

Fig. 3. Sketch of a dual axis accelerometer mounted in a vertical spinning wheel. The device senses three different accelerations while it spins: centripetal, tangential and gravity. Refer to [14] for more details.

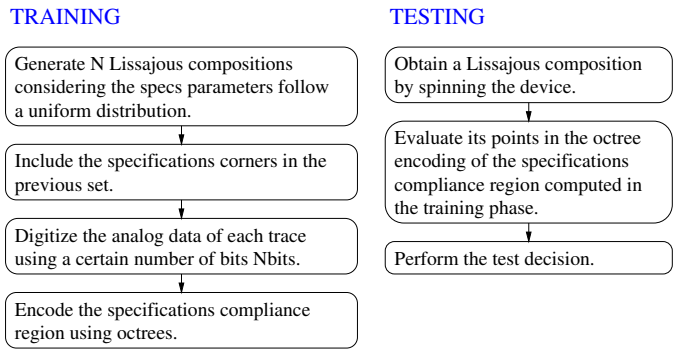

Fig. 4. Flow diagram showing an overview of the steps that characterize the training and testing phases. The training phase, which may be computationally intense, only needs to be performed once.

Fig. 4 shows an overview of the method which is described in detail in the following two sections.

IV. Training Phase

A. Introduction to Octrees

Researchers have been using octrees data structures since they were proposed in [17]. Their main applications include image color quantization, rendering, object identification and data clustering [18]. In this work, we will used them to encode the specifications compliance region of dual axis accelerometers.

An octree data structure of dimension n is a tree in which each node has 2^n children and represents a geometric partition of an n dimensions space. Octrees are extensively used in computer graphics for 3D modeling, therefore each node has exactly $2^3 = 8$ children, what gives its name. Octrees can be used in 2D geometries too therefore being denoted as quadtrees since each node owns $2^2 = 4$ children. The concept can be easily generalized to n dimensional spaces where sometimes are referred to 2^n-trees.

Octrees are easy to compute. As an example, consider the set of bivariate data points shown in Fig. 5 each of them belonging to a certain cluster (green or red). Initially, the orange theoretical boundary is unknown, so the presented algorithm is solely based on the green/red data points. The first step is to consider a square (an n-cube in n dimensions) containing all the data points. Then, this square is tessellated in 4 (2^n in n dimensions) equally sized smaller squares. For each of the squares, if it exclusively contains red or

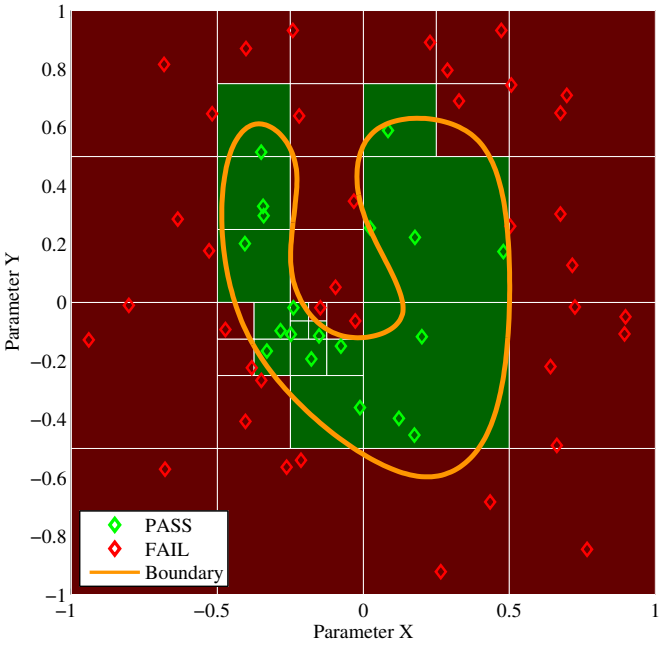

Fig. 5. Example of octree (quadtree) generated using 57 bivariate samples. The achieved octree depth is 5 levels what implies the initial square at level 0 has been scaled by a factor of $2^5 = 32$ in the smallest square.

green points, the square is tagged accordingly and no further partitioning is performed. Otherwise is marked as decision pending (white nodes in Fig. 6). The procedure continues until all the generated squares only contain equal class data.

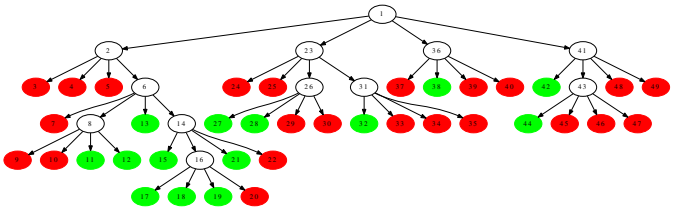

Fig. 6. Graph of the 5 levels depth octree (quadtree) depicted in Fig. 5. Green nodes correspond to specification compliance regions, red ones correspond to specification violation regions and white nodes correspond to decision pending regions.

Squares with no data points inside may occur in deep octree levels. In this situation a decision must be taken. The way to proceed is to label the cell according to a criterion of proximity depending on the assigned clusters to its neighboring cells.

B. Octree Encoding of the Specifications Compliance Region

As stated before, the training phase consists on the generation and encoding of the specifications compliance region for further usage in the testing phase. The training phase may be computationally intense since the computation time is exponentially related to the data dimensionality and the required number of bits (upper bound), but it only needs to be computed once. Given a device with sensitivities S_x and S_y for each of its axes, it is called to be within (functional) specifications if and only if $S_{\text{min}} \leq S_x \leq S_{\text{max}}$ and $S_{\text{min}} \leq S_y \leq S_{\text{max}}$.

The previous subset of devices can be visualized in the Lissajous composition space by performing a statistical sampling of specifications compliance devices among all the possible ones and representing them in the XY plane. In Fig. 7, 50

Lissajous compositions are plotted. Devices sensitivities have been drawn from non correlated uniform distributions. Voltage outputs can be easily computed using equation (2).

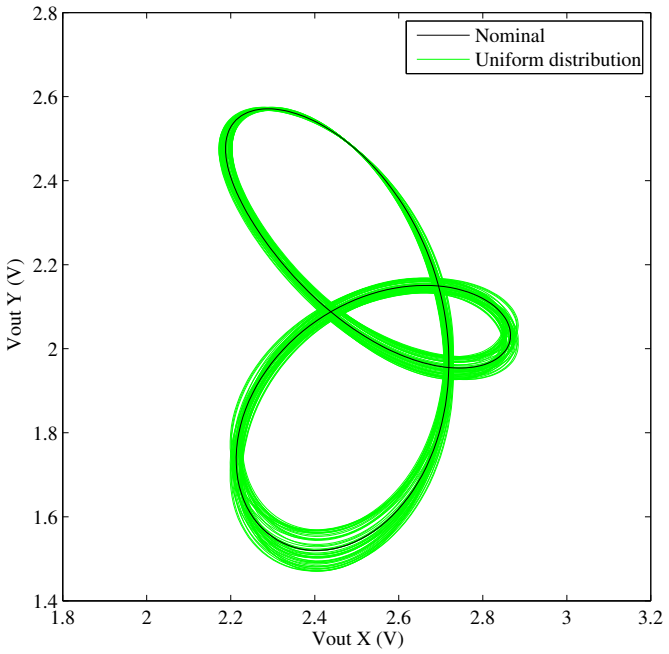

Fig. 7. Set of 50 Lissajous compositions generated with devices which sensitivities have been drawn from non correlated uniform distributions. Distributions spread has been assumed to be $\pm 5\%$ of the nominal value.

Test limits have been established to $\pm 5\%$ of the nominal value of 0.29 V/g ($S_{\text{min}} = 0.2755$ V/g and $S_{\text{max}} = 0.3045$ V/g). In order to accurately determine the specification compliance region, the four corners have been also included in the dataset.

In order to encode the analog data of Fig. 7 using octrees, a digitalization process has to be performed. For illustration purposes, Fig. 8 shows the resulting digitalization of the previous set of Lissajous compositions using 6 bits. As can be seen, the digitalization process allows getting rid of a large number of redundant data points which do not provide any extra information according to the required resolution or noise level.

After digitalization, the octree algorithm detailed in the previous subsection can be applied to pass/fail data points. Fig. 9 shows the resulting octree encoding using 6 bits. Note that the maximum achieved octree level matches the number of bits since each new level corresponds to a bisection operation.

If the number of bits is increased, the maximum number of levels also increases and therefore the number of octree cells. Such situation can be checked in Fig. 10 in which the Lissajous information of Fig. 7 has been encoded using an 8 bits octree.

V. Testing Phase

A. Octree Evaluation Overview

Octree data structures are time efficient to evaluate. Consider the case example of Fig. 5. For a candidate data point (x_c, y_c), the clustering to one class or another is performed using the octree graph representation of Fig. 6. Assuming the

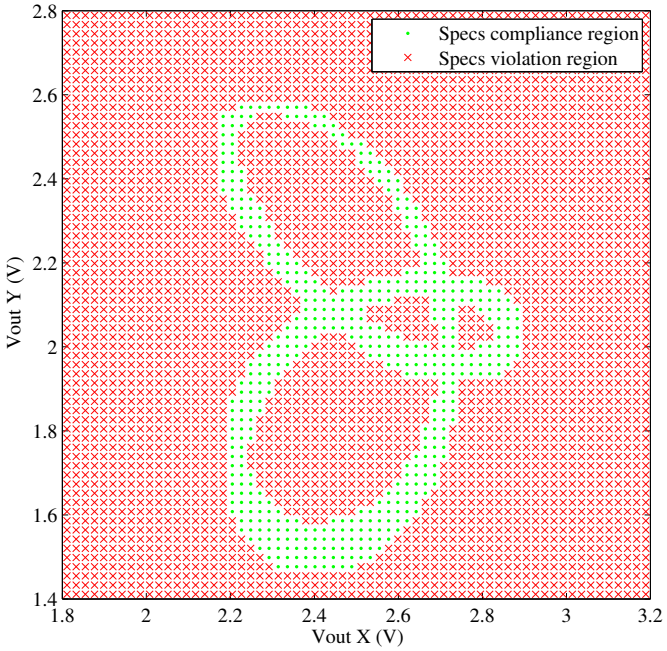

Fig. 8. Resulting specifications compliance and violation regions after digitizing the analog information of the Lissajous compositions shown in Fig. 7. The digitalization has been carried out using 6 bits.

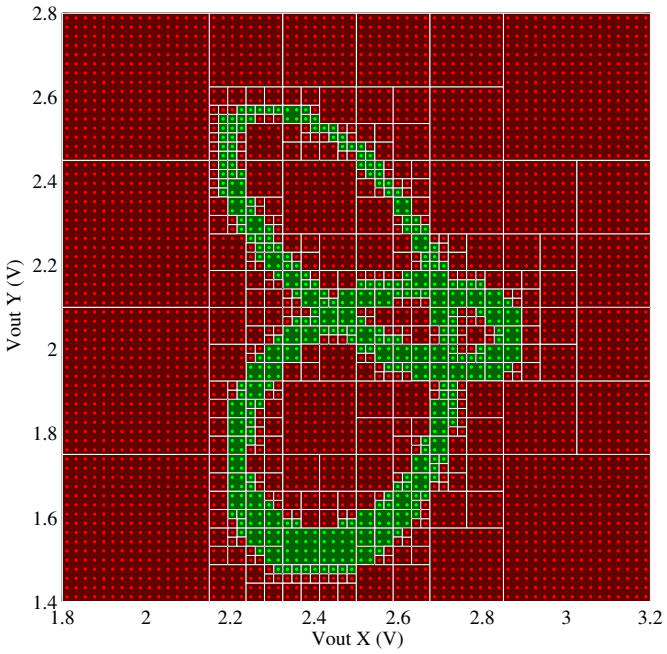

Fig. 9. Octree encoding of the specifications compliance/violation regions for the case study presented in Fig. 8 using 6 bits. The maximum octree level achieved is 6.

(x_c, y_c) data point is within the initial square, it is checked to which quadrant it belongs to (SW, NW, SE or NE). This decision brings the (x_c, y_c) point to a new bound thus a deeper octree level is achieved. If the current node is tagged, the point is mapped to that class and the evaluation ends. If not, the evaluation algorithm repeats the decision operation through the graph until a tagged node is found.

The evaluation of octrees, particularly in the topic this work presents, is very time efficient because the probability of having a device near the test decision boundary is quite small. Additionally, the octree depth is only higher in the boundary

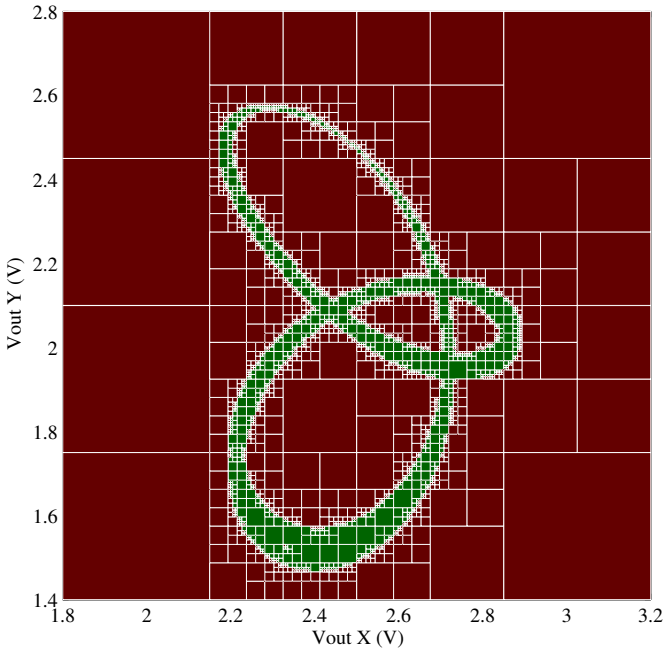

Fig. 10. Octree encoding of the specifications compliance/violation regions for the case study presented in Fig. 9 using 8 bits. The maximum octree level achieved is 8.

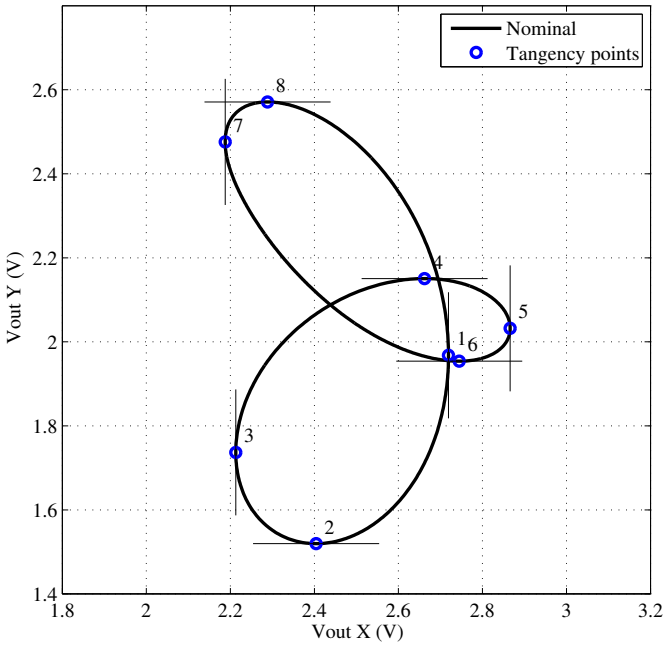

Fig. 11. Lissajous trace information is replaced by its points of tangency with vertical and horizontal tangent lines. These set of points are used to perform the test decision by evaluating them in the octree data structure.

region so the average time to perform an evaluation is far from the maximum theoretical exponential upper bound. The proposal presents an advantage over other clustering methods since the required number of operations to evaluate the device is highly decreased.

B. Selection of Lissajous Evaluation Points for Testing

The test strategy consists on the evaluation of a Lissajous composition in the previously computed octree encoding the specifications compliance region. To this purpose, only a few points of the trace are chosen to be evaluated in the octree improving this way the test application time.

Consider the Lissajous composition of Fig. 11. The points taken in consideration correspond to the tangency points of vertical and horizontal tangent lines to the Lissajous composition. The selection of such points allows an easy and systematic approach, therefore facilitating further data processing while keeping the information of the Lissajous trace [14].

Given a set of n Lissajous data points, the test strategy establishes a device as PASS if all the n points are clustered as specification compliant by the octree data structure, otherwise, the device is classified as FAIL.

VI. Simulation Results

In order to validate the proposal, several simulations have been performed as a function of the number of bits. To that purpose, a set of 10000 device samples have been generated considering their sensitivities distribute as normal and non correlated random variables.

The testing technique is evaluated against *test yield loss* and *test escape* metrics. *Test yield loss* is defined as the probability of classifying a functional device as non functional and therefore being discarded. *Test escapes* is defined as the probability of classifying a non functional device as functional and therefore being served to the customer. If the number of simulations is high enough, these indicators can be estimated.

Regarding test yield loss, simulation results can be seen in Fig. 12. As can be observed, the maximum value does not exceed 0.05%. The increase of test yield loss as the number of bits increase is because a finer approximation of the specifications compliance region boundary is achieved. This fact increases the probability of classifying a functional device as non functional, situation reflected in Fig. 12.

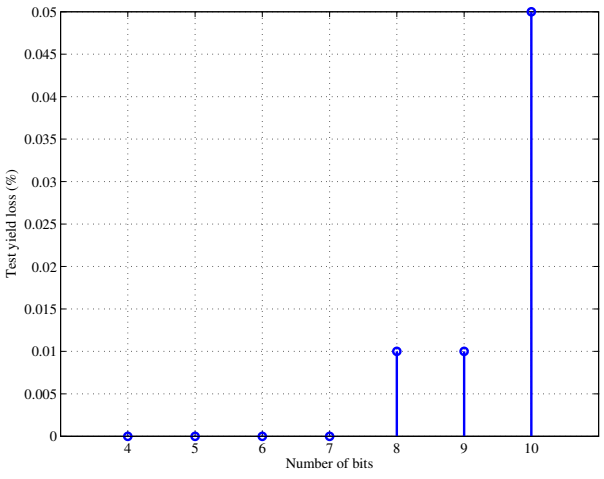

Fig. 12. Test yield loss as a function of the number of bits used to encode the octree data structure. The finer the encoding, the larger the probability of classifying a functional device as non functional.

Test escapes values are upper bounded by 2.4% as Fig. 13 illustrates. As expected, the number of non functional devices passing the test decreases as the resolution (i.e. the number of bits) of the octree increases. Of course, there is a trade off between the required resolution and required test escapes level since they strongly affect the octree computation time.

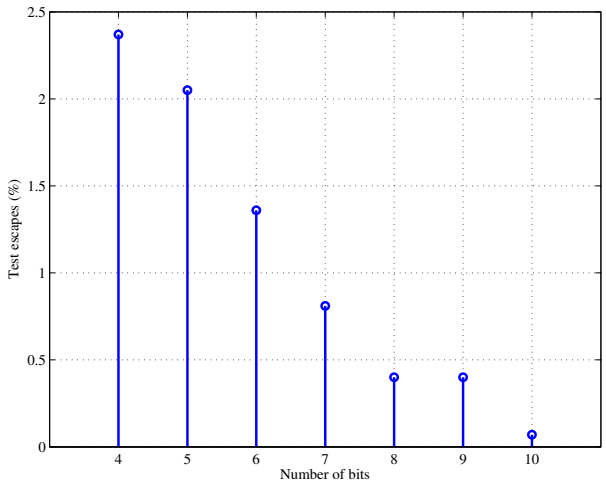

Fig. 13. Test escapes as a function of the number of bits used to encode the octree data structure. The finer the encoding, the probability of classifying a non functional device as functional decreases.

Fig. 14 shows the test application time considered as the computational time used to evaluate the octree for a given candidate device. As can be observed, the largest time is about 5 ms using 10 bits for octree encoding. It is important to note that the computational time logarithmically depends on the number of bits. This fact makes the octree data structure an interesting option in terms of time efficiency.

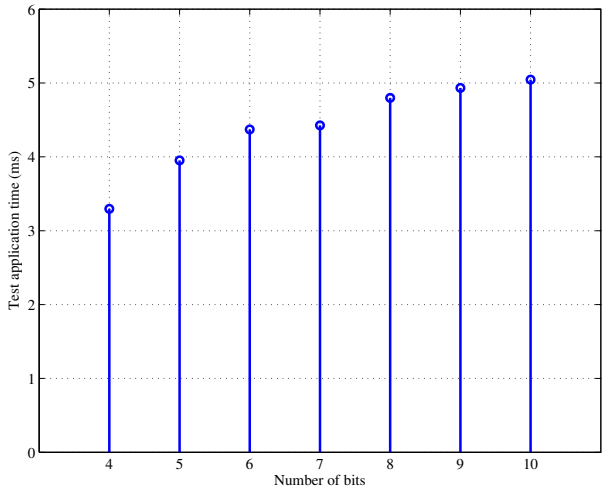

Fig. 14. Test application time as a function of the number of bits used to encode the octree data structure. As can be checked, increasing the resolution does not implies a significant overhead in evaluating the octree.

VII. Conclusions

A test strategy based on validating DUT specifications using octrees has been proposed. The method relies on a training phase aiming the generation of the specifications compliance region using statistical and corner samples. In this work, the method has been applied to test a dual axis accelerometer with promising results.

The test is performed by simply checking in which octree region the candidate device lies on. The test is performed using data samples from a Lissajous composition sensitive to parametric defects. To such purpose, the octree representation has many benefits due to its sparse data structure what makes its evaluation time efficient.

Several simulation have been conducted in order to evaluate the incurred test yield loss and test escapes of the testing proposal. These metrics have been studied as a function of the number of bits used to encode the octree data structure. The obtained encouraging results validate the proposal.

Acknowledgments

This work has been partially supported by the Spanish Ministry of Economics and Competitiveness (project reference is TEC2010-18384) and European Union FEDER funds.

References

[1] A. Gómez-Pau, L. Balado, and J. Figueras, "Mixed-Signal Test Based on Specification Validation using Octrees in the Measurement Space," in *Proceedings of European Test Symposium (ETS)*, Avignon, France, May 2013, pp. 70–75.

[2] "International Technology Roadmap for Semiconductors (update)," 2012, http://www.itrs.net/Links/2012ITRS/Home2012.htm.

[3] S. Devarakond, S. Sen, S. Bhattacharya, and A. Chatterjee, "Concurrent device/specification cause-effect monitoring for yield diagnosis using alternate diagnostic signatures," *Design Test of Computers, IEEE*, vol. 29, no. 1, pp. 48 –58, feb. 2012.

[4] S. Dasnurkar and J. Abraham, "Characterization and testing of micro-electromechnical accelerometers," in *Proceedings of the 14th International Mixed-Signals, Sensors and Systems Test Workshop*, 2008, pp. 1–6.

[5] *ADXL203 dual axis accelerometer datasheet*, Analog Devices, 2010.

[6] R. Puers and S. Reynthens, "RASTA: Real-acceleration-for-self-test accelerometer: A new concept for self-testing accelerometers," *Journal of Sensors and Actuators*, vol. 97–98, pp. 97–98, April 2002.

[7] B. Charlot, S. Mir, F. Parrain, and B. Courtois, "Electrically Induced Stimuli for MEMS Self-Test," in *VLSI Test Symposium, 19th IEEE Proceedings on*, 2001, pp. 210 –215.

[8] S. Mir, L. Rufer, and A. Dhayni, "Built-in-self-test techniques for MEMs," *Microelectronics Journal*, vol. 37, no. 12, pp. 1591–1597, December 2006.

[9] X. Xingguo, W. Yu-Liang, and J. Wen-Ben, "A Dual-Mode Built-In Self-Test Technique for Capacitive MEMS Devices," in *VLSI Test Symposium, 2004, 22nd IEEE Proceedings on*, April 2004, pp. 148–153.

[10] N. Dumas, F. Azaïs, F. Mailly, and P. Nouet, "Evaluation of a fully electrical test and calibration method for MEMS capacitive accelerometers," in *Proceedings of International Mixed-Signals, Sensors and Systems Test Workshop*, Vancouver, Canada, June 2008.

[11] L. Rufer, S. Mir, E. Simeu, and C. Domingues, "On-Chip Pseudorandom MEMS Testing," *Journal of Electronic Testing: Theory and Applications*, vol. 21, no. 3, pp. 233–241, June 2005.

[12] J. Yang, W. Wu, Y. Wu, and J. Lian, "Thermal Calibration for the Accelerometer Triad Based on the Sequential Multiposition Observation," *IEEE Transactions on Instrumentation and Measurement*, vol. 62, no. 2, pp. 467–482, February 2013.

[13] V. Natarajan, S. Bhattacharya, and A. Chatterjee, "Alternate Electrical Tests for Extracting Mechanical Parameters of MEMS Accelerometer Sensors," in *Proceedings of the VLSI Test Symposium*, April 2006.

[14] A. Gómez-Pau, L. Balado, and J. Figueras, "Nondestructive Diagnosis of Mechanical Misalignments in Dual Axis Accelerometers," in *Proceedings of Design, Test, Integration & Packaging of MEMS/MOEMS (DTIP)*, Barcelona, Spain, April 2013, pp. 229–234.

[15] K. Lee, *Principles of Microelectromechanical Systems*. Wiley, 2011.

[16] A. Gómez-Pau, L. Balado, and J. Figueras, "Testing Dual Axis IC Accelerometers Using Lissajous Compositions," in *Proceedings of Design of Circuits and Integrated Systems Conference (DCIS)*, Albufeira, Portugal, November 2011.

[17] D. Meagher, "Octree Encoding: A New Technique for the Representation, Manipulation and Display of Arbitrary 3-D Objects by Computer," Rensselaer Polytechnic Institute, New York, Tech. Rep., 1980.

[18] H. Medellin, J. Corney, J. Davies, T. Lim, and J. Ritchie, "Octree-based production of near net shape components," *Automation Science and Engineering, IEEE Transactions on*, vol. 5, no. 3, pp. 457 –466, july 2008.