

Micropower thermoelectric generator from thin Si membranes

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Abstract

We report the development of a Si-based micro thermogenerator build from silicon-on-insulator by using standard CMOS processing. Ultrathin layers of Si, 100 nm in thickness, with embedded n and p-type doped regions electrically connected in series and thermally in parallel, are the active elements of the thermoelectric device that generate the thermopower under various thermal gradients. This proof-of-concept device produces an output power density of $4.5 \mu\text{W}/\text{cm}^2$ under a temperature difference of 5 K across the hot and cold regions.

Keywords: Low-dimensional Si, Planar thermoelectric generator, Power output, Si membrane.

1. Introduction

The potential decrease of fossil fuel supplies and the urgent need to reduce green-house gas emissions drives mankind into the necessity to search for alternative, greener, sources of energy. Among the various available energy sources, waste-heat energy is universally present since any heat engine, from biological entities at nearly room temperature to high-temperature combustion processes, will dissipate part of its energy in the form of heat. An efficient conversion of this excess heat into useful forms of energy, i.e. electricity, remains a challenge and it is the object of intense investigation [1-4]. In this respect, thermoelectric materials that convert heat differences across the material into electricity could help meeting the energy challenge of the future. The efficiency of this energy conversion relies on the capacity of the material to transport electrical charges while impeding the flow of heat. A useful indicator of the goodness of a TE material is the Figure-of-Merit, ZT , an adimensional parameter that relates the Seebeck coefficient, S , the electrical conductivity, σ , and the thermal conductivity, κ , at a given temperature, as $ZT=(S^2\sigma/\kappa)*T$. A material with large ZT can be termed phonon glass-electron crystal, but unfortunately, no material in nature fulfills these requirements to the desired level. Currently, heavy semiconductors of the BiSbTe family with consistent values of ZT up to 1.5 are the best thermoelectric materials at medium-to-low temperatures [5,6]. However, Bi(Sb)Te, already used in commercial Peltier devices, lacks proper integration with standard CMOS processing. Therefore, integration of these materials into chip-harvesting devices is technically challenging. On the contrary, doped bulk-Si may be appealing but its figure-of-merit is remarkably low, $ZT=0.01$ at 300 K, precluding its use as a thermoelectric converter. In fact, poly-silicon

thermoelectric devices with many elements per device have been fabricated in an augmented BiCMOS process [7,8], however their low power output limit the range of applications. Nanostructuring can be a convenient route to improve the figure of merit [9] and a recent breakthrough has challenged the view that Si is a poor thermoelectric [10,11]. It was shown that Si nanowires exhibit a figure of merit enhanced by 100x compared to its bulk counterpart. This remarkable behavior is mainly due to the reduction of the thermal conductivity associated to phonon scattering with the boundaries of the NW, while preserving bulk values for the electrical conductivity and the Seebeck coefficient. Although still insufficient for many applications that require ZT in excess of 3, this finding opens the use of low-dimensional Si as a thermoelectric material in miniaturized chips that can be monolithically integrated into CMOS-compatible devices for low-power applications. There are already several examples that employ low-dimensional Si obtained from bottom-up or top-down approaches in planar or vertical geometries [12-14]. The most extended device structure has a vertical configuration with the n-p legs connected thermally in parallel and electrically in series. Several vertical n-p type TEG using top-down Si NWs were recently fabricated and tested [12, 13]. The output power in the device fabricated by Li et al. was limited to few μW per device due to the reduced $\Delta T=0.12\text{K}$ achieved across the $1\ \mu\text{m}$ Si NWs [12]. A power output of $29.3\ \mu\text{W}$ with ΔT of $56\ \text{K}$ for a $50\ \mu\text{m} \times 50\ \mu\text{m}$ device was achieved by Bowers and coworkers in a unileg device using a highly ordered Si nanowire array composite [13]. A planar device also based on Si NWs was fabricated by Davila et al [14]. The NWs were grown by the VLS method at high temperature. This unileg device has a high density of NWs with a total distance between the hot and cold regions up to $90\ \mu\text{m}$. Power outputs of $9\ \mu\text{W}/\text{cm}^2$ and $1.4\ \text{mW}/\text{cm}^2$ were achieved under temperature differences of 27 and $300\ \text{K}$ across the device, respectively.

Thin films can also be used to build a thermoelectric generator [6, 15]. In this case the vertical geometry is sometimes not adequate since the temperature of the cold side increases rapidly by heat conduction and radiation from the hot side. A planar configuration has been shown to be more effective for a thin film TEG since the heat flow is parallel to the thin film and larger ΔT can be achieved [15]. The reduction of film thickness to the nm range will increase phonon scattering with the boundaries compared to bulk materials, enabling higher temperature differences and therefore higher power outputs.

Bottom-up approaches to fabricate the desired nanostructured material integrated in the chip-harvesting module often lack enough reproducibility to guarantee the required fabrication yield. Therefore, we propose a top-down strategy in combination with a planar configuration to fabricate a TEG device that uses low-dimensional Si as the main thermoelectric material. In this article we detail the fabrication procedure and the critical steps towards obtaining a reliable and efficient TEG comprising n and p-type legs made from an ultrathin Si membrane. We model the thermoelectrical behavior of the device and characterize the power output at various ΔT by measuring IV curves under different loads.

2. Material and Methods

2.1. Device design and microfabrication procedure

The design of the TEG is shown in Figure 1. It consists on a planar device with a suspended very thin Si platform at the center ($500 \times 500 \mu\text{m}^2$) contacted to a Si frame through ultrathin n and p-type Si membranes, 50um wide x 150 um long. The distance between hot and cold regions is also approximately 100 μm . In this particular design, 20 np couples are distributed along the 4 sides of the central platform.

We start the microfabrication process (See Figure 2) with a Silicon on Insulator, SOI, wafer with a Si thickness of 340 nm and buried oxide of 400 nm. The upper Si layer is reduced to 100 nm by wet oxidation and subsequent HF etching. This layer is patterned and etched (RIE) until the buried oxide is reached, to create a central squared silicon region of 500 μ m \times 500 μ m (undoped region) and 40 50 μ m \times 150 μ m “legs” surrounding it (doped n,p regions). A thin, 50 nm, low-stress SiN_x layer is grown by low-pressure chemical vapor deposition, LPCVD, at the top and bottom surfaces of the wafer. The bottom SiN_x layer is patterned by photolithography and then etched by reactive ion etching (RIE), leaving windows to facilitate the removal of the Si wafer in the last step. The n, p regions are defined by using a photoresist mask, followed by sequential implantation of Boron and Phosphorous and Rapid Thermal Annealing RTA at 900°C. Details of this step will be covered in the next section. After dopant activation, vias are opened at the edges of the doped regions to permit contacts with the metal and also in the middle of the n, p regions to decrease the thermal link between the Si_{frame} and the suspended membrane. Ni, 50 nm thick, is grown by sputtering, followed by a thermal treatment at 300°C to form NiSi and achieve ohmic contacts with the doped Si regions. The final step consists on a KOH wet etching of the back side to leave the central Si platform suspended.

2.2. n and p-type doping of ultrathin Si layers

Ion implantation followed by rapid thermal annealing to recrystallize the material and activate the dopants is the standard technique to increase carrier concentration in semiconductors. Although the microscopic processes behind an effective doping are complex, very well established recipes exist for bulk Si. However, unlike their bulk counterpart, doping ultrathin layers require additional strategies to achieve the adequate carrier concentration without compromising the stability of the film. Since the high

mobility of the carriers depends on the crystalline quality of the material, epitaxial recrystallization must be ensured by appropriate post-processing annealings. This requires that a single-crystalline layer, free of defects, that will act as a seed for epitaxial ordering of the damaged region during rapid thermal processing, must be ensured at the bottom of the implanted layer. We use SRIM software packaging to determine the doses and energies required to achieve the desired carrier concentration, and guarantee a low-damaged region at the bottom of the Si layer. The temperature of the rapid thermal processing is another key aspect of impurity activation when dealing with very thin layers of Si on SiO₂. Temperatures above 950°C will rupture the film by dewetting induced by the surface tension between crystalline Si and SiO₂ [16, 17]. As the best compromise to facilitate activation and avoid structural damaging of the layer we have adopted a RTA procedure with T=900°C.

3. Finite Element Modeling

3D modeling of the output power under different temperature loads is realized by COMSOL Multiphysics simulation package, which allows the solution of common arbitrary partial differential equations (PDEs) of a field variable on a given volume. Finite Element Modeling, FEM, was carried out with the cold region at room temperature and the materials parameters listed in Table I. The main results are shown in figure 4. Figure 4 show the voltage output (a) and the output power density (b) as a function of current, measured by varying the R_{load}. Maximum power densities of 6.7 and 168 μW/cm² are attained at R_L=R_{int} for ΔT=5 and 25 K, respectively. The inset of Figure 4b shows the 2D Temperature contour in the device. The structure yields a Seebeck voltage at open circuit of 285 μV/K, which reflects S is dominated by the n and p-type doped Si regions embedded in the Si membrane.

Table I. Material properties, thermal conductivity κ , electrical resistivity ρ , and Seebeck coefficient S , used in the Multiphysics modeling of the TEG.

Material	κ [W/mK]	ρ [Ωcm]	S (V/K)
SiO ₂	1.4	10^{16}	
SiN _x	3	1000	
Ni	93	6.24×10^{-8}	-15×10^{-6}
Si (central region)	150	14-22	0
Si (doped legs)	60	1×10^{-2}	4.0×10^{-4}
Contact resistance Ni/NiSi/Si = $1.7 \times 10^{-6} \Omega\text{cm}^2$			

4. Experimental results on TEG behavior

The experimental conditions to achieve a good contact resistance between Ni and n and p-type doped Si were evaluated by using specific test structures to determine the contact resistance. As briefly mentioned in section 2.1, after Ni growth, the devices were annealed at 300°C to form NiSi. This procedure reduced the interfacial contact resistance to values around $1.7 \mu\Omega \text{ cm}^{-2}$. The resistance of the Si layer and the mobility of the carriers were evaluated with a Hall setup. In the n-type material for a doping level of $2 \times 10^{19} \text{ cm}^{-3}$ we measured a mobility of $80 \text{ cm}^2/\text{Vs}$, and for p-type Si with a doping of $6.5 \times 10^{18} \text{ cm}^{-3}$ we obtained $\mu=50 \text{ cm}^2/\text{Vs}$. Those values are compatible with bulk Si [18] and reinforce the epitaxial regrowth of the thin Si layer in the conditions stated above. The internal resistance of a single device with 20 np regions connected electrically in series is about 40 k Ω . This value closely agrees with the calculated one,

38 k Ω , based on the dimensions of the material and the electrical resistivity of both n and p-type regions.

4.1 TE characterization

We impose a temperature gradient between the hot and cold regions of the device by contacting the Si frame to a hot plate, that served as a heat-source in harvesting configuration, while cooling the central part of the chip (suspended Si membrane) by convective cooling with a fan (Figure 5a). In steady-state the temperatures of the central and outside regions of the device are measured by means of two metal resistances located at both sides. The Seebeck voltage at open circuit was quantified under various temperature differences across the structure ranging from 1 to 5.5 K. The length of the active region of the device is 150 μm . The results for the 100 nm thin Si membrane are shown in Figure 5b-d. The measured Seebeck coefficient, obtained from the slope of the open circuit voltage versus the temperature difference (Figure 6b), is 354 $\mu\text{V/K}$ per a unileg (7.1 mV across a 10 μm legs device). Previous studies have shown that the Seebeck coefficient of SOI wafers with Si thicknesses above 6 nm is similar to bulk Si [19]. As the Seebeck coefficient of the structure is largely dominated by the n,p Si regions, we infer an average doping level of $\sim 10^{19} \text{ cm}^{-3}$, that roughly matches our estimations from the test structures. Since, in a 100 nm thick single-crystalline layer the electrical resistivity is also analogous to bulk Si, the main impact of the reduced thickness of the Si membrane on the figure of merit is the decrease of the thermal conductivity by approximately 3-fold compared to bulk Si [20]. That basically means the device is able to withstand higher temperature differences under the same applied temperature loads compared to previous devices that used much thicker films of poly-Si

[7,8]. Further reduction of the Si thickness will diminish the thermal conductivity even further at the expense of an increase of the internal resistance which may require complex signal conditioning steps to power output devices.

The thermoelectric characterization of the microdevice is accomplished by using a load resistor connected in series with the TE generator. I-V curves are obtained by changing the value of the load resistor. The results for various temperature differences are shown in figure 6b and c. As expected and shown above in Figure 4 from the modeling of the thermoelectric response, the maximum power output occurs at $R_{load} \sim R_{int}$. From the measured data a power output of $4.5 \mu\text{W}/\text{cm}^2$ under a temperature difference of 5.5 K is obtained, which is comparable to the value obtained from Finite Element Modeling of the structure. This value compares well to previously reported Si-based micro/nanogenerators [12-14, 21]. Considering that the maximum power output increases parabolically with ΔT , $P \propto \Delta T^2$ [1], the power output achieved with our device at $\Delta T = 5$ K is higher than those found in other planar Si-based thermo generators, such as the one based on Si-Al thermopiles [7] or on bottom-up Si NWs [14]. In future devices optimization of the structure could improve the power output. A simultaneous reduction of the Si thickness together with an improved design that maximizes the parallel configuration of the n,p regions to reduce the internal resistance will certainly result in improved power outputs and thermal gradients across the structure. Thermal coupling of the central membrane to a heat sink and encapsulation of the device are also important considerations for practical applications. Under optimum conditions the microgenerator could ultimately be used as an energy harvester to power small devices such as mobile and wireless electronics. For sensing applications requiring discontinuous monitorization, the proposed device can be integrated into wearable thermoelectrics for body scavenging purposes or into higher temperature sources such

as exhaust hot pipes. A back-of-the-envelope calculation shows a 10 cm^2 TEG device could provide power outputs around $50 \text{ }\mu\text{W}$ during energy body scavenging in appropriate ambient conditions. Collecting energy for about 2 min would provide about 6 mJ, that is enough to run a low power device such as a heart rate monitor.

Conclusions

We have fabricated a first prototype of a CMOS compatible planar microthermoelectric generator that contains ultrathin Si membranes as the active TE material and therefore can be integrated into standard Si chips. A power output of $4.5 \text{ }\mu\text{W}/\text{cm}^2$ was achieved under a temperature difference of 5.5 K. Patterning the membrane into Si nanowires or reducing its thickness to few nm could result in substantial improvements by reducing the thermal conductivity of the structure. In addition, the proposed design permits the fabrication of multiple optimized generators on a single wafer to be connected in series to boost the voltage performance or in parallel to increase current output to match the desired application.

References

- [1] Rowe DM. Thermoelectric Handbook: From Macro to Nano. 2010.
- [2] Shakouri A. Recent Developments in Semiconductor Thermoelectric Physics and Materials. *Annu. Rev. Mater. Res.* 2011;41:17.1–17.33
- [3] MRS Bulletin, Volume 31 (3), March 2006: Issue's Topic: 'Harvesting Energy through Thermoelectrics: Power Generation and Cooling'
- [4] Bell LE, Cooling, Heating, Generating Power, and Recovering Waste Heat with Thermoelectric Systems. *Science* 2008; 321:1457.
- [5] Harman TC, Taylor PJ, Walsh MP, LaForge BE. Quantum Dot Superlattice Thermoelectric Materials and Devices. *Science* 2002;297:2229.

- [6] Venkatasubramanian R, Siivola E, Colpitts T, O'Quinn B. Thin-film thermoelectric devices with high room-temperature figures of merit. *Nature* 2001;413: 597.
- [7] Strasser M, Aigner R, Lauterbach C, Sturm TF, Franosch M, Wachutka G. Micromachined CMOS thermoelectric generators as on-chip power supply. *Sensors and Actuators A* 2004;114:362-70.
- [8] Glosch H, Ashauer M, Pfeiffer U, Lang W. A thermoelectric converter for energy supply. *Sensors and Actuators A* 1999;74:246-50.
- [9] Dresselhaus MS, Chen G, Tang MY, Yang R, Lee H, Wang D, Ren Z, Fleurial JP and Gogna P. New Directions for Low-Dimensional Thermoelectric Materials. *Adv. Mat.* 2007;19:104353.
- [10] Boukai AI, Bunimovich Y, Tahir-Kheli J, Yu J-K, Goddard III WA, Heath JR, and Goddard WA. Silicon nanowires as efficient thermoelectric materials. *Nature* 2008;451:168.
- [11] Hochbaum AI, Chen R., Delgado RD, Liang W, Garnett EC, Najarian M, Majumdar A. and Yang P. Enhanced thermoelectric performance of rough silicon nanowires. *Nature* 2008;451:163.
- [12] Li Y, Buddharaju K, Singh N, Lo GQ and Lee SJ. Chip-Level Thermoelectric Power Generators Based on High-Density Silicon Nanowire Array Prepared With Top-Down CMOS Technology. *IEEE Electron Dev Lett* 2011;32:674-6.
- [13] Curtin BM, Fang EW and Bowers JE. Highly Ordered Vertical Silicon Nanowire Array Composite Thin Films for Thermoelectric Devices. *J Electronic Mat* 2012;41:887-94.
- [14] Dávila D, Tarancón A, Calaza C, Salleras M, Fernández-Regúlez M, San Paulo A, Fonseca L. Monolithically integrated thermoelectric energy harvester based on silicon nanowire arrays for powering micro/nanodevices. *Nano Energy* 2012;1:812-819.

- [15] Fan P, Zheng Z-hao, Cai Z-k, Chen T-b, Liu P-j. The high performance of a thin film thermoelectric generator with heat flow running parallel to film surface. *Appl. Phys. Lett.* 2013;102:033904.
- [16] Danielson DT, Sparacin DK, Jurgen M, Surface-energy-driven dewetting theory of silicon-on-insulator agglomeration *J Appl Phys* 2006;100:083507.
- [17] Garcia G, Lopeandía AF, Bernardi A, Alonso MI, Goñi AR, Lábár JL, Rodríguez-Viejo J, Crystallisation of Amorphous Germanium Thin Films, *J. Nanosci Nanotech* 2008;9:1-7.
- [18] Jacoboni C, Canali C, Ottaviani G, Quaranta AA. *Solid State Electron* 1977;20:77-89.
- [19] Salleh F, Asai K, Ishida A, Ikeda H. Seebeck Coefficient of Ultrathin Silicon-on-Insulator Layers. *Applied Physics Express* 2009;2:071203.
- [20] Liu W and Asheghi M. Thermal conduction in ultrathin pure and doped single-crystal silicon layers at high temperature. *J Appl Phys* 2005;98:123523.
- [21] G.J. Snyder, *Thermoelectrics Handbook: Macro to Nano*, in: D.M. Rowe (Ed.), CRC/Taylor & Francis, 2006.

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FIGURES

FIGURE 1. Schematics of the device. (a) Front view. Gray colour show the metal lines. Red and blue represent the n, p Si regions. Purple represents the SiN_x membrane. In this version of the device the central region is filled with a metal for heating/sensing purposes. (b) Back view after etching the bulk Si of the SOI wafer.

FIGURE 2. Sketch of the main microfabrications steps: 1. Thining of the Si layer. 2. Patterning of the Si membrane. 3. Growth of SiN_x. 4. RIE in the backside to open window. 5&6. n,p implantation. 7. Post annealing to activate dopants. 8. Photolithography to define metal lines and contacts. 9. Deep RIE to suspend the central region.

FIGURE 3. Optical microscope images of a fabricated device before opening the back side (a,b) and after (c,d). Figure d shows a detailed view of the n,p regions and the open vias used for contacts.

FIGURE 4. Finite Element Modeling of the thermoelectric microgenerator. Output voltage (a) and Power density (b) as a function of current for two temperature differences across the structure. The inset in figure b shows the 2D map use for the simulations.

FIGURE 5. (a) Schematic design of the experimental setup to measure thermoelectric behavior. (b) Voltage at open circuit as a function of the temperature difference Measured voltage (c) and power generation per unit area (d) versus current for the TEG device Different values of temperature difference were used for each series as shown in the legend.

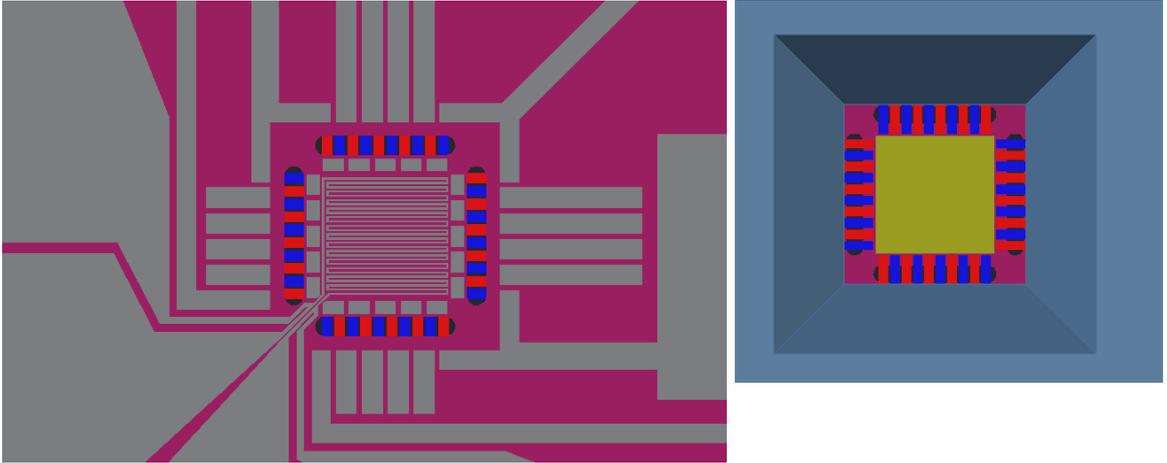


Figure 1

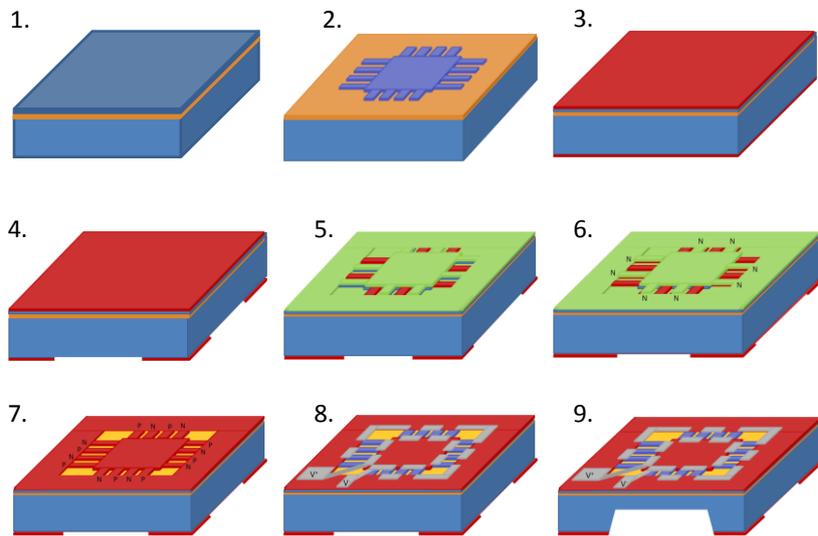


Figure 2

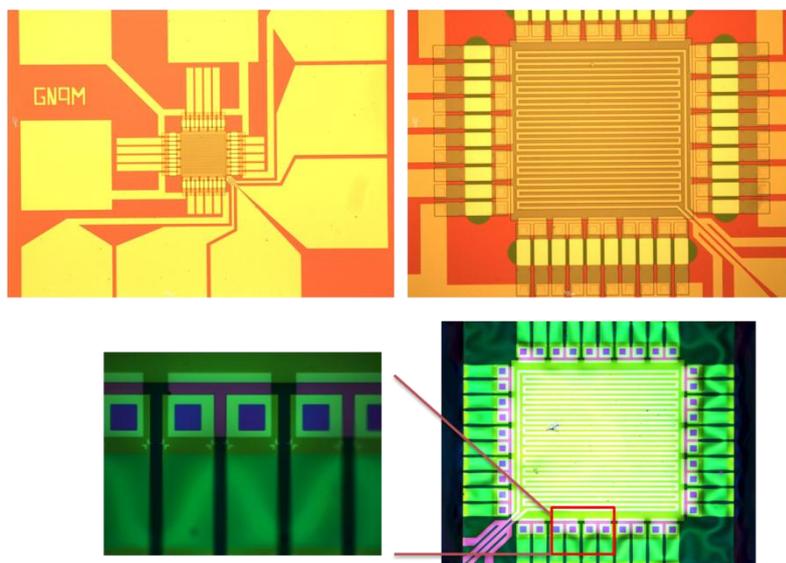


Figure 3

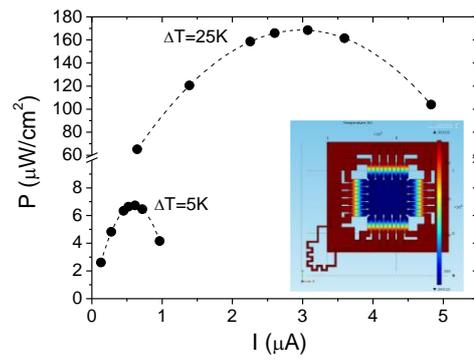
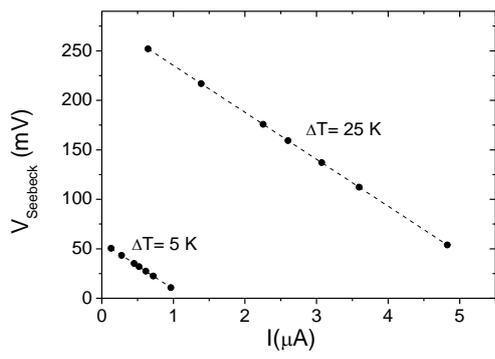


Figure 4

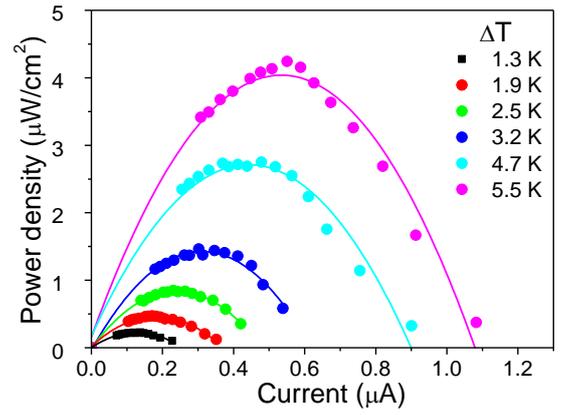
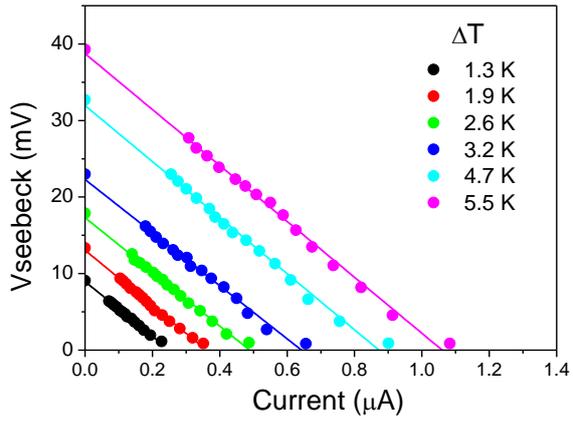
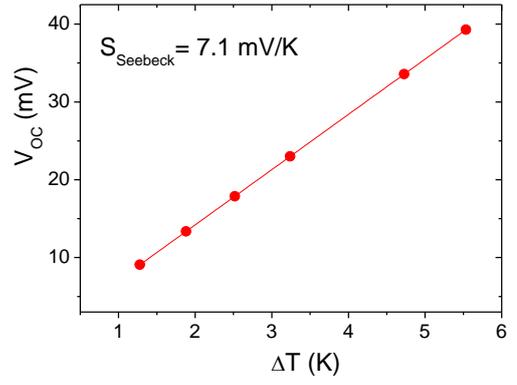
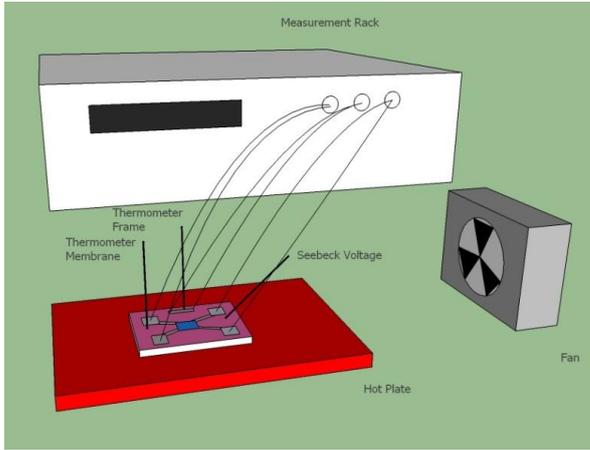


Figure 5

Highlights

- We describe the microfabrication of a planar CMOS compatible Si-based generator.
- The device contains a 100 nm thick Si membrane with embedded n,p doped regions.
- A power output of $4.5 \mu\text{W}/\text{cm}^2$ is achieved for a temperature difference of 5.5 K.
- The chip could be suited for body-energy scavenging to feed low-power devices.