A High-efficiency Matching Technique for Low Power Levels in RF Harvesting

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Abstract— Radiofrequency (RF) energy can be harvested in order to power autonomous sensors either from the surrounding environment or from dedicated sources. A conventional RF harvester is mainly composed by an antenna, a matching network and a rectifier. At low power levels, e.g., −10 dBm and below, the corresponding voltage amplitude at the antenna is low and comparable to the voltage drop of the diodes used in the rectifier. In order to boost the voltage at the rectifier input and thus the rectifier efficiency, an L-network optimized for an input power of −10 dBm at 868 MHz is proposed in this work. As for the rectifier, a half-wave rectifier with a single zero-bias Schottky diode (HSMS2850) was selected. First, a theoretical analysis was performed followed by simulations with ADS (Harmonic Balance). Simulations show efficiencies of 75% for an input power of −10 dBm with ideal components but using the actual model of the diode rectifier. The incorporation of the PCB layout effects and the actual components decreases the efficiency to below 50%. Finally, a PCB implementation was performed using a 0.5 pF capacitor and a 27 nH inductor for the L network. The input power was generated by an RF generator. The RF-to-DC efficiency was of 45% at 868 MHz with an optimum load of 2.5 kΩ. Efficiencies of 34.5% and 22.5% were achieved at −15 dBm and −20 dBm, respectively.

1. INTRODUCTION

The possibility of powering low power devices (e.g., RFID tags/sensors or autonomous sensors) from electromagnetic waves has been widely proposed in the literature [1–13]. Radiofrequency (RF) energy can be harvested either from the surrounding environment or from dedicated sources. Fig. 1 shows the main building blocks of a conventional RF energy harvester, which is composed of an antenna, an impedance matching block, and a rectifier.

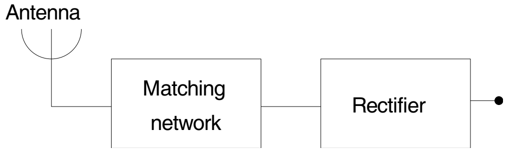


Figure 1: A conventional RF energy harvester.

An antenna can be roughly modelled as an AC voltage source (v_s) with a series impedance. The series impedance basically comprises a radiation resistance (R_s), a loss resistance and a reactive part. The amplitude of the voltage generated on the antenna is given by [6]

$$\hat{v}_\mathrm{s} = 2\sqrt{2R_\mathrm{s}P_\mathrm{AV}} \tag{1}$$

where P_AV is the available power at the antenna. As can be deduced, lower values of P_AV lead to lower values of v_s.

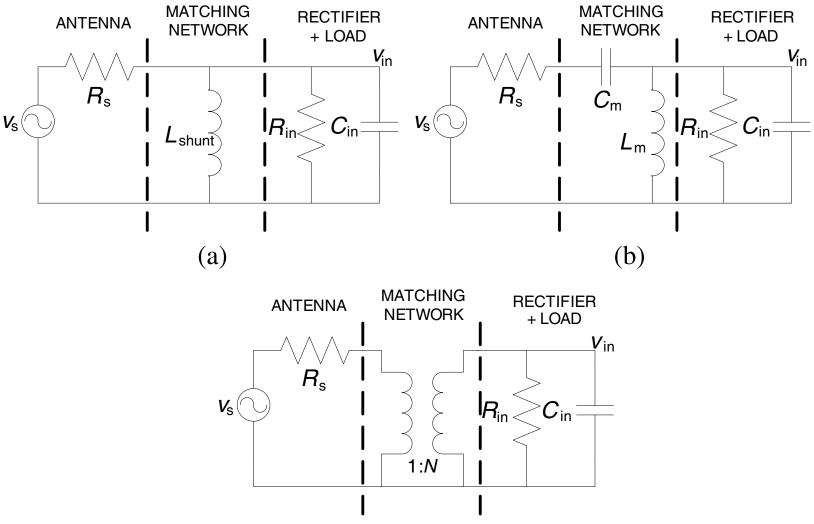
Rectifier circuits provide a dc output voltage. Several topologies have been reported such as a single series- or shunt-mounted diode [3, 4, 8, 9, 13], a bridge rectifier [3] and single or multistage voltage doubler structures [2, 5–7, 10–13]. The input impedance of the rectifier can be modelled as a capacitance (C_in) in parallel with a resistance (R_in) [1, 6, 7, 11–13]. Accurate expressions of the input impedance are not straightforward [11]. As an approximation, C_in, apart from the parasitic capacitances introduced from the layout, is mainly given by the addition of the parasitic capacitances of the diodes [6, 7] whereas R_in is proportional to the output load [6, 13].

The objective of the impedance matching network is to match the input impedance of the rectifier to the antenna impedance so that maximum power may be transferred. In this condition, the antenna sees at its output the complex conjugate of the antenna impedance. Fig. 2 shows three different types of matching networks where v_{s} and R_{s} model the antenna and R_{in}-C_{in} model the input impedance of the rectifier plus the ensuing load (e.g., autonomous sensor) to be powered.

In Fig. 2(a) a shunt inductor (L_{shunt}) is placed in parallel with the input of the rectifier, whose value is given by

$$L_{\mathrm{shunt}} = \frac{1}{\omega_r^2 \cdot C_{\mathrm{in}}} \tag{2}$$

whereby ω_r is the angular resonant frequency. A shunt inductor is used in [11, 13]. Maximum power will be transferred for $R_{\mathrm{in}} = R_{\mathrm{s}}$, being the voltage at the rectifier input (v_{in}) half v_{s}. From (1), low values of P_{AV} (e.g., $< 0\,\mathrm{dBm}$) lead to low values of v_{s} and thus of v_{in}. Thus, due to the voltage drop of the diodes the rectifier efficiency will be low. This issue can be partialy solved by using antennas with higher radiation resistance (e.g., a folded dipole has a radiation resistance of roughly $300\,\Omega$) which, from (1), lead to a higher value of v_{in}. Another approach is to use an L-matching network, an example of which is shown in Fig. 2(b). Here, a voltage boosting in v_{in} can be achieved whenever using a relative high-Q network, which results in higher efficiencies of the rectifier [10–12]. These types of matching networks have been used, for example, in [6, 7, 12]. In order to achieve the same effect, transformers have also been proposed (Fig. 2(c)), as in [1].



(a) (b)

(c)

Figure 2: Three types of matching networks: (a) shunt inductor, (b) L network, (c) transformer.

In this work, in order to achieve high efficiencies at low RF input powers, the use of the matching network of Fig. 2(b) is proposed. A series-configured Schottky diode (HSMS2850, Avago Technologies) with a low threshold voltage will be used for the rectifier. The circuit will be optimized for an input power of $-10\,\mathrm{dBm}$ at a resonant frequency of 868 MHz (ISM band).

2. L-MATCHING NETWORK

For the circuit of Fig. 2(b), the required values of the matching network are given by

$$C_{\mathrm{m}} = \frac{1}{\omega_{\mathrm{r}} R_{\mathrm{s}}} \sqrt{\frac{R_{\mathrm{s}}}{R_{\mathrm{in}} - R_{\mathrm{s}}}} \tag{3}$$

$$L_{\mathrm{m}} = \frac{R_{\mathrm{in}}}{\omega_{\mathrm{r}}} \frac{1}{\omega_{\mathrm{r}} R_{\mathrm{in}} C_{\mathrm{in}} + \frac{1}{\sqrt{\frac{R_{\mathrm{s}}}{R_{\mathrm{in}} - R_{\mathrm{s}}}}}} \tag{4}$$

being the voltage gain [1, 12]

$$G = \frac{v_{\mathrm{in}}}{v_{\mathrm{s}}} = \frac{1}{2} \cdot \sqrt{\frac{R_{\mathrm{in}}}{R_{\mathrm{s}}}} \tag{5}$$

Thus, for $R_{\mathrm{in}} > R_{\mathrm{s}}$, the voltage will be boosted. The drawback is that the circuit becomes more selective since the circuit Q is given by [7]

$$Q = \sqrt{\frac{R_{\mathrm{in}}}{R_{\mathrm{s}}} - 1} \tag{6}$$

In order to maximize the power efficiency, the following procedure will be followed. First, a suitable gain will be selected in order to achieve a relative high value of v_{in}. Then, from (5), and assuming a given value of R_{s}, the value of R_{in} will be obtained. Finally, for given values of ω_{r} and C_{in}, the component values of the matching network will be obtained from (3) and (4).

3. SIMULATIONS AND EXPERIMENTAL RESULTS

Figure 3 shows the circuit schematic of the simulated circuit. Simulations were carried out using the Harmonic Balance module of ADS software (Agilent). As can be seen, the antenna is modelled by v_{s} and R_{s} and ideal lumped components were used for rest with the exception of the diode, where the actual model has been used. The output load is composed by a filter capacitor of 1 nF (C_{Load}) in parallel with a resistive load (R_{Load}).

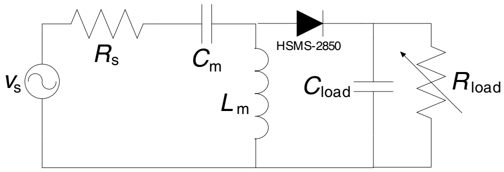


Figure 3: Circuit schematic with ADS of the RF harvester.

The design was optimized for $P_{\mathrm{AV}} = -10\,\mathrm{dBm}$ at 868 MHz (ISM band) and $R_{\mathrm{s}} = 50$. From (1), $\hat{v}_{\mathrm{s}} = 0.2\,\mathrm{V}$. Then, in order to boost v_{in} to a suitable voltage, we selected $G = 5$, which leads to $\hat{v}_{\mathrm{in}} = 1\,\mathrm{V}$, high enough compared to the voltage drop of the diode (0.15 V for a forward current of 0.1 mA). Thus, from (5), $R_{\mathrm{in}} = 5\,\mathrm{k\Omega}$ will be required. From the manufacturer data, the diode presents a parasitic capacitance of 0.18 pF, which for this circuit will be assumed as C_{in}. Thus, from (3) and (4) the following values for the L-matching network are obtained: $C_{\mathrm{m}} = 0.368\,\mathrm{pF}$ and $L_{\mathrm{m}} = 61.7\,\mathrm{nH}$.

As for L_{m} and R_{Load}, a parametric sweep was performed in order to find the best performance in terms of efficiency (η), where

$$\eta = \frac{P_{\mathrm{Load}}}{P_{\mathrm{AV}}} \tag{7}$$

being P_{Load} the power dissipated at R_{Load}. Fig. 4 shows the results where a sweep of L_{m} from 55 nH to 65 nH with steps of 1 nH was performed. A maximum efficiency of nearly 75% was found for $L_{\mathrm{m}} = 60\,\mathrm{nH}$ and $R_{\mathrm{Load}} = 8.5\,\mathrm{k\Omega}$. The value of L_{m} nearly matches that found theoretically. On the other hand, as the value of R_{Load} directly influences the equivalent resistance R_{in}, an optimum value is also found. Techniques for automatically controlling the value of R_{in} have been presented in [8] but are outside the scope of this paper.

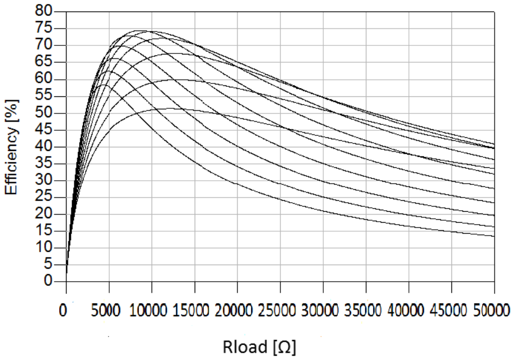


Figure 4: Efficiency versus L_{m} and R_{Load} with ideal lumped components.

Then, a FR4 PCB was designed (Fig. 5) and the S parameters corresponding to the layout were incoporated into the simulation. Commercial components were also added. As for C_{Load}, a capacitor of value 1 nF (ATC) was selected. As for L_{m} and C_{m}, a trial and error procedure was followed, starting from the values found before, in order to achieve the highest efficiency. Finally, $C_{\mathrm{m}} = 0.5\,\mathrm{pF}$ (AVX) and $L_{\mathrm{m}} = 27\,\mathrm{nH}$ (Coilcraft) were selected. Fig. 6 shows the simulated efficiency versus R_{Load}, where a maximum efficiency of 48% was achieved for $R_{\mathrm{Load}} = 3.1\,\mathrm{k\Omega}$.

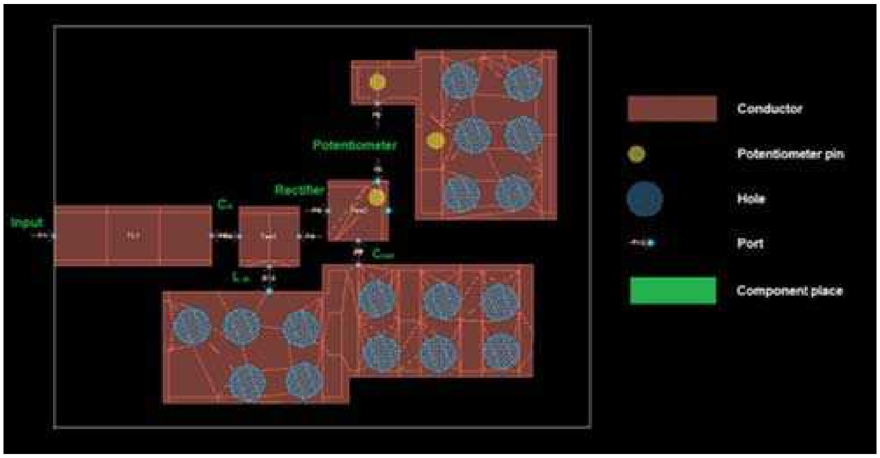


Figure 5: PCB layout.

The designed circuit was implemented using a potentiometer for R_{Load}, in order to find out the optimum load. An RF signal generator was used at the input in order to emulate the antenna. Fig. 7 shows the results for an input power of $-10\,\mathrm{dBm}$, where an efficiency of 45% was achieved for a load of $2.5\,\mathrm{k\Omega}$. So, experimental results largely agree with simulations. Bandwidth (half-power) was found to be 122 MHz. Efficiency drecreased to 34.5% and 22.5% at $-15\,\mathrm{dBm}$ and $-20\,\mathrm{dBm}$, respectively. A fair comparison with other works is rather difficult but measured efficiencies are among the highest achieved in the literature at that power levels.

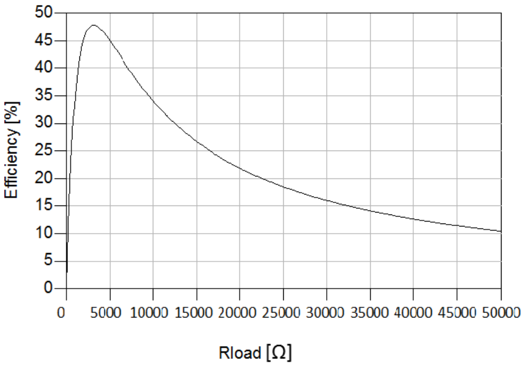


Figure 6: Efficiency vs R_{Load} with commercial components and layout effects.

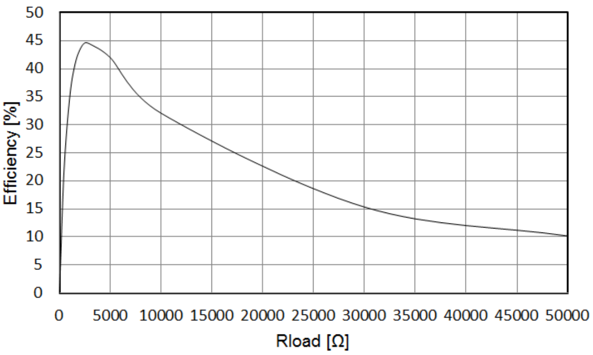


Figure 7: Measured efficiency vs R_{Load}.

4. CONCLUSIONS

A matching technique using a simple L-network has been proposed in order to boost the efficiency of RF harvesters at low power levels. A theoretical approach in order to find out suitable values of the capacitance and inductance of the matching network has been presented. Simulations have shown efficiencies of 75% for an input power of $-10\,\mathrm{dBm}$ with ideal components but using the actual model of the diode rectifier. The incorporation of the PCB layout effects and the actual components decreases the efficiency to below 50%. Experimental results largely agree with simulations showing an efficiency of 45% at $-10\,\mathrm{dBm}$. Efficiency decreases to 34.5% and 22.5% at $-15\,\mathrm{dBm}$ and $-20\,\mathrm{dBm}$, respectively.

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