Design of an On-Chip Linear-Assisted DC-DC Voltage Regulator

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***Abstract*—This article shows the design of an on-chip CMOS linear-assisted DC-DC regulator. It results a good alternative topology to classic switching DC-DC power converters. In the presented technique, an auxiliary linear regulator is used to cancel the output voltage ripple and provides fast responses for load and line variations. On the other hand, a switching converter, connected in parallel, allows supplying almost the whole output current demanded by the load. The objective of this linear-assisted regulator or hybrid topology is to achieve a high efficiency of switching converters, with suitable load and line regulation features, typical of linear regulators. In this kind of on-chip applications, CMOS is the current prevailing technology. Thus, in order to implement on-chip power supply systems and on-chip power management systems with low-to-medium current consumption, this structure has good features.**

I. INTRODUCTION

Series linear regulators have been structures widely used for decades in power supply systems providing supplies with low or moderate currents and consumes [1], [2]. These voltage regulators have several advantages that lead their use. However, they suffer from some serious disadvantages: the efficiency of these structures hardly exceeds 50%. Their series-pass transistor has to support all current required by the load and, therefore, in high power applications, this component has to be dimensioned (both electrically and thermically) in order to dissipate high power. Since the minimum permissible dropout voltage of a linear regulator defines the maximum achievable efficiency, in order to improve the efficiency of this circuit, the use of LDO (low dropout) regulators has been extended in last years. Although this increase in efficiency is achieved, the cost of a compromise in stability of the regulator is paid. However, nowadays, the emphasis on efficiency has made LDO regulators the most popular class of linear regulators [3], [4].

The alternative to linear regulators is DC-DC switching converters. Many of these structures [5], [6] have been designed, and their main advantage is their high efficiency that, although not reaching 100% due to omnipresent circuit losses, is near this optimal figure. However, they present some important problems: the design and implementation of this sort of converters is a more complex process than in linear regulators, especially their control loops. In addition, the intrinsic switched nature of these converters increments EMIs in neighboring electronic systems due to significant ripples in currents and voltages in the converter. In order to minimize the aforementioned output ripple voltage, it is necessary to include both a bulky and expensive inductor and an output capacitor.

Linear-switching hybrid regulators (also known as linear-switching hybrid regulators or converters) are compact circuit topologies that preserve the well-known advantages of the two typical alternatives for the implementation of DC/DC voltage regulators, namely, achieving both moderately high efficiencies –by virtue of the switching regulator– together with fast wideband ripple-free regulation –thanks to the linear regulator–. They are circuit topologies of strong interest when designing power supplies requiring as design specifications both: (1) High slew-rate of the output current, and, (2) high current consumption by the output load. This is the case of systems based on modern microprocessors and DSPs, where both requirements converge [7], [8]. This interest is also applicable to wideband adaptive supply of RF power amplifiers.

In this paper, a linear-assisted strategy is applied to an on-chip regulator. CMOS technology has rapidly embraced the field of analog integrated circuits, providing low-cost, high performance solutions and tending to dominate the market of integrated circuits. Thus, in this article, a CMOS design of a DC-DC regulator based on a linear-assisted topology is presented for an on-chip application. The design must guarantee the electric power supply for a critical load that needs a constant 1.1 V supply. This load is an analog design (included in the same chip) that consists of a continuous time filter for MEMS signal filtering with its central-frequency and quality-factor control loops. The regulator input voltage (chip input voltage) can vary from 1.6 V to 1.8 V.

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With the compact structure designed, the output ripple is negligible without any output capacitor for a wide range of output currents. In addition, some of the aforementioned disadvantages are minimized as the low efficiency and the high power dissipation present in linear regulators, or the complexity in the design of the control for switching converters.

II. Proposed Arquitecture for the On-Chip Linear-Assisted DC-DC Regulator

Let us consider a series linear regulator that supplies a load R_L with constant output voltage V_{out}. With the objective of reducing the dissipated power in the series-pass transistor of the regulator, it is also necessary to reduce the current through the regulator as far as possible below a maximum value. In case the load current should be higher than this maximum value, it is possible to introduce a buck (or step-down) switching converter into the structure. This second block will be connected in parallel with the first one, and will provide the excess current that the series linear regulator fails to supply. The original idea, which is presented and analyzed in [9], [10] and [11], needs a clock signal for the switching converter.

Nevertheless, the proposed configuration in this paper (Fig. 1) makes use of the analog hysteretic comparator CMP_1 that controls the conduction or cut of transistor Q_1, and fixes its switching frequency. Notice that the main objective of the switching converter is to provide the excess of current that the linear regulator fails to supply. Consequently:

$$I_{out} = i_{reg}(t) + i_L(t)\,. \tag{1}$$

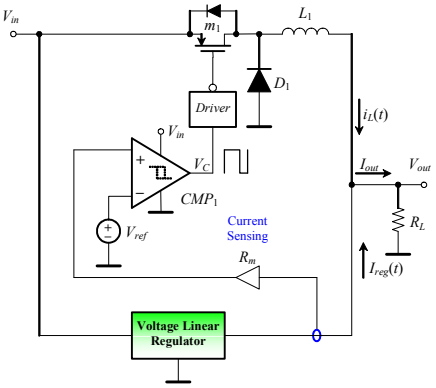

Figure 1. Basic structure of the proposed linear-assisted voltage regulator or hybrid DC-DC regulator.

In a first approximation, consider CMP_1 without hysteresis. If the load current is below a boundary current, named *switching threshold current*, I_γ, the output of CMP_1 is held low. Thus, the switching converter will be disabled and the current through inductor L_1 will be zero. As a result of this, the linear regulator supplies the load R_L, providing all the output current (I_{reg}=I_{out}) (Fig. 2). However, when the load current increases and goes slightly beyond this limit current I_γ, comparator output will pass to high level, increasing $i_L(t)$ in a linear form. Taking into account (1) and that output current I_{out} is constant (equal to the quotient V_{out}/R_L), $i_{reg}(t)$ will tend to decrease also linearly, reaching a value below I_γ. At this moment, the comparator changes its output from high to low, cutting off transistor Q_1 and forcing $i_L(t)$ to decrease. Therefore, when $i_L(t)$ decreases so that $i_{reg}(t)>I_\gamma$, CMP_1 changes from low to high, repeating the cycle again.

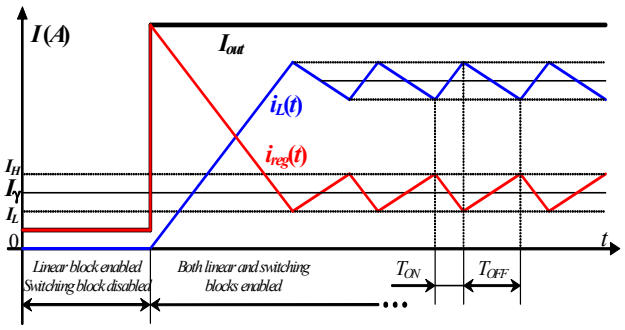

Figure 2. Principle of operation of the proposed linear-assisted DC/DC regulator: Currents through the load (black color), inductance L_1 (blue) and linear regulator (red).

It is important to highlight that both the reference voltage V_{ref} and the sensing current element R_m determine the switching threshold current I_γ. In this way, the switching instant of the DC/DC converter is controlled by I_γ. This control signal can be adjusted thanks to the gain of the current sensing element, R_m, and the reference voltage V_{ref}, according to the expression:

$$I_\gamma = \frac{V_{ref}}{R_m}\,. \tag{2}$$

With the objective of reducing the dissipated power by the internal transistor of the linear regulator to the utmost, and increasing the efficiency of the whole system, even with significant load currents, this current I_γ has to be, ideally, equal to zero. However, in a practical voltage regulator, this current should be slightly positive in order not to penalize its good regulation features.

In addition, with the objective of fixing the maximum value of this switching frequency to a suitable value (in order to avoid increasing the switching losses significantly), it is convenient to add a hysteresis to the analog comparator CMP_1. In this way, designating V_H and V_L to the upper and lower switching threshold levels of CMP_1, respectively, the value of the switching frequency f_S in steady state is given by:

$$f_S = \frac{R_m}{L_1}\frac{V_{out}}{V_H - V_L}\left(1 - \frac{V_{out}}{V_{in}}\right). \tag{3}$$

On the other hand, the ON time, T_{ON}, and OFF time, T_{OFF}, in every steady-state switching period is given, respectively, by the following expressions:

$$T_{ON} = \frac{L_1}{R_m}\frac{V_H - V_L}{V_{in} - V_{out}}\,,\ \text{and,}\ T_{OFF} = \frac{L_1}{R_m}\frac{V_H - V_L}{V_{out}}\,. \tag{4}$$

As an additional advantage, it is important to highlight that typical low-pass filtering capacitors at the output terminal of the switching converters (which capacities can be important in some high-current applications), are not necessary in the proposed structure because the linear regulator implements an efficient low-pass filtering function [12]-[14].

III. Design of the Proposed Linear-Assisted Regulator

A. Design of the Linear Voltage Regulator

The CMOS implementation of the linear voltage regulator used in the topology of the linear-assisted DC-DC regulator is shown in Fig. 3. It consists of a classical three-stage operational amplifier. On the one hand, the first stage is a *p*-MOS differential input pair (m_{19} and m_{20} transistors) with an *n*-channel current mirror active load (m_{21} and m_{22} transistors). Transistor m_{23} provides the suitable bias current for this differential pair. On the other, the second gain stage is a simple CMOS inverter with m_{24} as the driver of the output stage, and m_{25} being its active load. The output of this second stage is connected to its input by means of a Miller compensation capacitance C_C in order to assure regulator stability. Finally, the output stage is a classical class-B push-pull output buffer (transistors m_{26} and m_{27}). It should be noted that this final stage (in particular, the ratio W/L of the output transistors) determines the output current capability of the linear regulator. In the presented case, for the considered maximum output current, this ratio is 300 μm/0.36 μm. These two devices are transistors with low threshold voltage (V_t), in order to improve their input dynamic ranges (gate-source voltage).

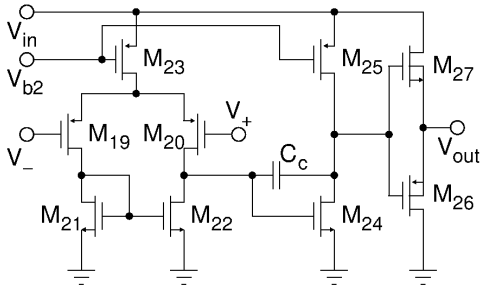

Figure 3. Circuit of the CMOS operational amplifier used in the linear-assisted regulator.

B. Design of the Analog Comparator

The main core of the controller is an analog comparator with a suitable hysteresis. This analog comparator is presented in Fig. 4. It consists of a first stage, an *n*-channel differential input pair (transistors m_1 and m_2), with their associated current mirrors that act as active loads (m_4 and m_5), and transistor m_3, a current source that provides the bias current for the differential pair. The output of this first stage is applied to a second one (m_6 to m_{11}) that assures a suitable hysteresis to the analog comparator thanks to transistors m_6 to m_9. Its output is applied to a second differential pair (m_{12} to m_{16}) that boosts the total gain of the comparator. Finally, the fourth stage, transistors m_{17} and m_{18}, assures the output current capability. They have a reasonable value for the transistor widths in order to drive the switch gates of the switching DC-DC converter.

C. Complete Linear-Assisted Regulator

Finally, Fig. 5 shows the final implementation of the CMOS linear-assisted regulator, in which the operational amplifier *OA* is given in Fig. 3, and the analog comparator *CMP* is shown in Fig. 4. Resistors R_1 and R_2 determine the reference voltage V_{ref} given in Fig. 1. Notice that this voltage fixes the value of the switching threshold current I_γ (according to (2)), limiting the maximum current through the linear regulator at the steady state. Finally, transistors M_p, and M_n, diodes D_1 and D_2, and an off-chip inductor L define the buck converter structure. Although transistor M_n could be removed from the circuit, the linear-assisted DC-DC regulator includes a synchronous buck converter with transistors M_p and M_n. The use of the synchronous step-down converter improves the total efficiency of the linear-assisted regulator.

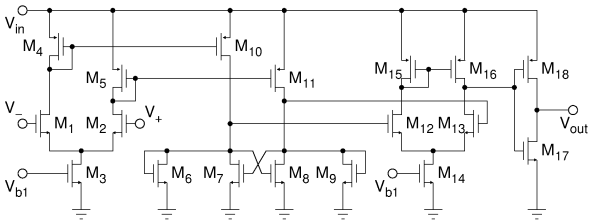

Figure 4. Proposal of the circuit for the CMOS analog comparator used in the control loop of the switching DC-DC converter.

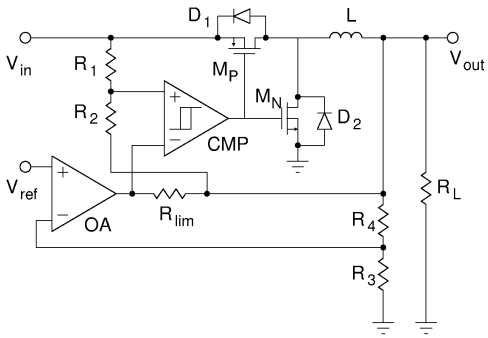

Figure 5. CMOS implementation of the linear-assisted DC-DC regulator.

IV. Simulation Results

With the objective of validating the correct operation of the proposed circuital structure, the CMOS on-chip linear-assisted regulator presented in Fig. 5 has been simulated using a standard CMOS 0.18–μm technology. The parameters of this model have been obtained from UMC (United Microelectronics Corporation®). The design must guarantee the power supply for an analog design included in the same integrated circuit with a constant voltage of 1.1 *V*. In our case, this load is an analog design that consists of a low-power continuous time filter for MEMS signal filtering with its central-frequency and quality-factor control loops. The regulator input voltage (chip input voltage) can vary from 1.6 *V* to 1.8 *V*. The total consumption of the aforementioned load is around 15 *mA*.

In order to corroborate and validate the functionality of the proposed linear-assisted structure, Fig. 6 shows the voltage and current waveforms of the topology at the steady state. In particular, the output voltage V_{out} (top trace), the comparator output V_{CMP} (middle), and load $i_{out}(t)$, inductor $i_L(t)$ and linear regulator $i_{reg}(t)$ currents (bottom axis).

Finally, Fig. 7 shows the transient response of the same voltage and current waveforms shown in the previous figure, when the load current is a sinusoidal pulse between 0 and 15

mA. Notice that when the output current is below the threshold current ($I_{out}<I_\gamma$), the output current is provided by the linear regulator. However, when $I_{out}>I_\gamma$, the inductor current follows the load current; that is, almost all the load current is provided by the switching converter. In addition, the output voltage is determined by the linear regulator, which guarantees a good voltage regulation and only provides a small percentage of the total load current, remaining a good efficiency of the whole linear-assisted regulator.

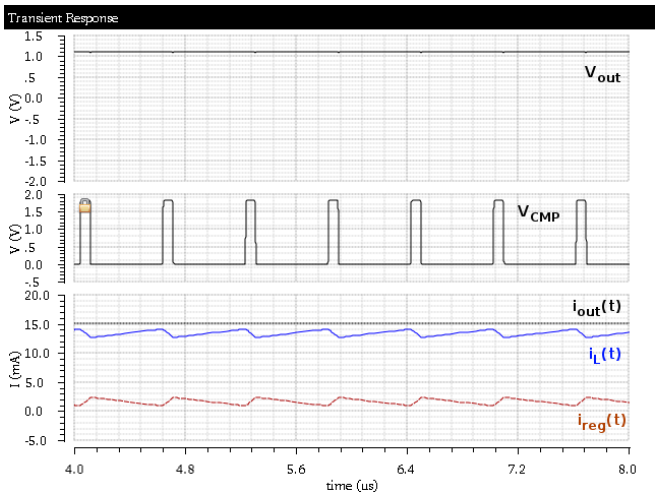

Figure 6. Voltage and current waveforms of the proposed linear-assisted DC-DC regulator at the steady state.

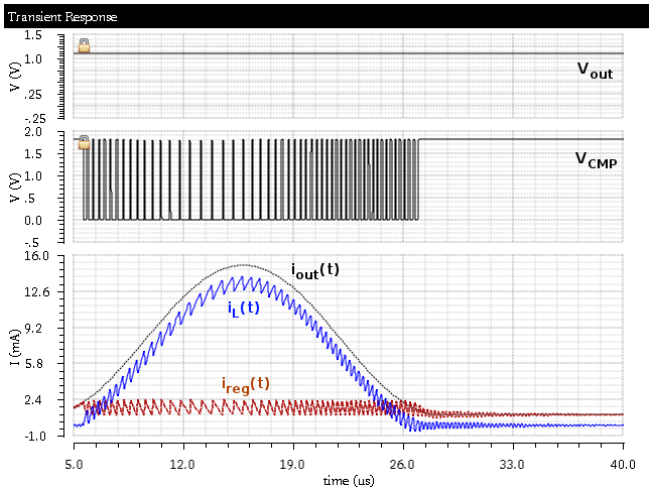

Figure 7. Voltage and current waveforms of the proposed linear-assisted DC-DC regulator when load current is a sinusoidal pulse.

V. CONCLUSIONS

Taking into account the advantages of the CMOS technology to implement on-chip power supply subsystems for integrated circuits, this article has shown the design of an on-chip CMOS implementation of a hybrid or linear-assisted DC-DC regulator. On the one hand, the article has shown the suitable regulation features of the output voltage for the presented structure with low-to-medium current consumption. On the other hand, the efficiency of the whole structure should be hardly penalized for the limitations of the linear regulators. Besides, the inclusion of a linear regulator in parallel with the switching converter achieves a good performance with fast responses to transients of load current and input voltage. Note that without output capacitance, the linear-assisted regulator achieves good dynamic and static characteristics.

Simulation results have demonstrated the feasibility to make an excellent and simple on-chip CMOS linear-assisted DC-DC regulator. Surely, the final experimental implementation of the on-chip regulator will degrade some specification. However, this technology allows being optimist for its expansion into commercial integrated circuits.

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