Voltage Balancing Method Using Phase-Shifted PWM for Stacked Multicell Converters

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***Abstract*—This paper proposes an active voltage balancing method for stacked multicell converters (SMC) using phase-shifted pulse-width modulation, which is easy to implement and extend to high number of levels. The proposed method balances the voltages of the capacitors by modifying the duty cycle of each switch of the SMC using a proportional controller. The crossed effect between capacitor currents and duty cycles is considered and is used for optimal capacitor voltage balance. The performance of the proposed voltage balancing method is verified by simulation for different operating conditions, such as unbalanced linear loads, non-linear loads and load transients.**

***Index Terms*—Multilevel converter; Stacked multicell converter; Capacitor voltage balancing; Pulse-width modulation.**

I. Introduction

Multilevel converters allow higher voltage/power ratings, lower total harmonic distortion (THD), and lower losses, when compared with the conventional two-level converter [1], [2]. The most popular multilevel toplogies are the cascaded multi-modular converter [3], the modular multilevel converter (MMC) [4], the neutral-point-clamped (NPC) converter [5], and the flying capacitor (FC) converter [6]. Most of these topologies are well established by industry.

Multilevel topologies with more than five levels, require to store large amounts of energy, which strongly impacts on the converter size and price. Recently, hybrid multilevel converters has been introduced and are considered as competitive solution, since they require less energy storage when compared with the popular multilevel topologies [7]. One of the hybrid multilevel topology is the stacked multicell converter (SMC) which consist of two multilevel FC converters that are stacked together to generate multilevel voltage waveforms, as shown in Fig. 1. This $Y(cell) \times Z(stage)$ SMC allows higher voltage, with reduced FCs in the converter, when compared with the conventional multilevel FC converter.

Like the other multilevel topologies, the SMC also requires capacitor voltage balancing for the acceptable performance of the converter. In [9]–[15], phase-shifted pulse-width modulation (PS-PWM) was proposed, which provides natural voltage balance. However, natural voltage balance depends on the load conditions. The dynamics of the converter slow down with different types of load conditions. Some references in [9], [11], [12], [14] proposed a balance booster to achieve fast voltage balance dynamic. This balance booster consists of a passive RLC filter, which introduces additional power losses.

There are a few active voltage balancing methods found in the technical literature [16]–[18]. In [16], a direct torque control method was proposed. This method regulates the FC voltage; however, no line-to-line voltage is shown and analyzed in the paper. Another active balancing method was proposed in [17], which makes use of a sliding mode observer. This method performs well as it does not require any voltage sensors. However, the method is complicated and requires a lot of computation. Finally, an active voltage balancing method which was proposed in [16], consists on evaluating a cost function for the redundant states using space vector modulation (SVM) in a four-level hybrid SMC. However, some limitations have been reported when operating with high modulation indices. The authors suggest increasing the number of voltage levels to extend the operating range of the converter, which is obviously not an optimal solution.

The majority of the solutions discussed above are complex from the implementation point of view and not easy to extend to higher number of levels. The main objective of this paper is to present a novel active voltage balancing method for the SMC that is efficient and can be easily extended to any number of levels. It is implemented using PS-PWM and is based on a proportional (P) controller. The effects between the FC currents and the duty cycles of the switches are considered and used to optimize the voltage balancing process. Furthermore, the voltage balancing dynamic performance is very good. Although the proposed method has been applied to the seven-level (3×2) SMC, it can be easily extended to any number of levels.

The rest of the paper is organized as follows. Section II describes the operating principle of the SMC. Section III explains the proposed FC voltage balancing method. Section IV presents simulation results from a seven-level SMC to verify the effectiveness of the proposed method. Finally, the conclusions are summarized in Section V.

II. Operating Principle of the SMC Converter

Fig. 1 shows a circuit diagram of a three-phase seven-level SMC. It consist of three cells $(Y = 3)$ of FC units,

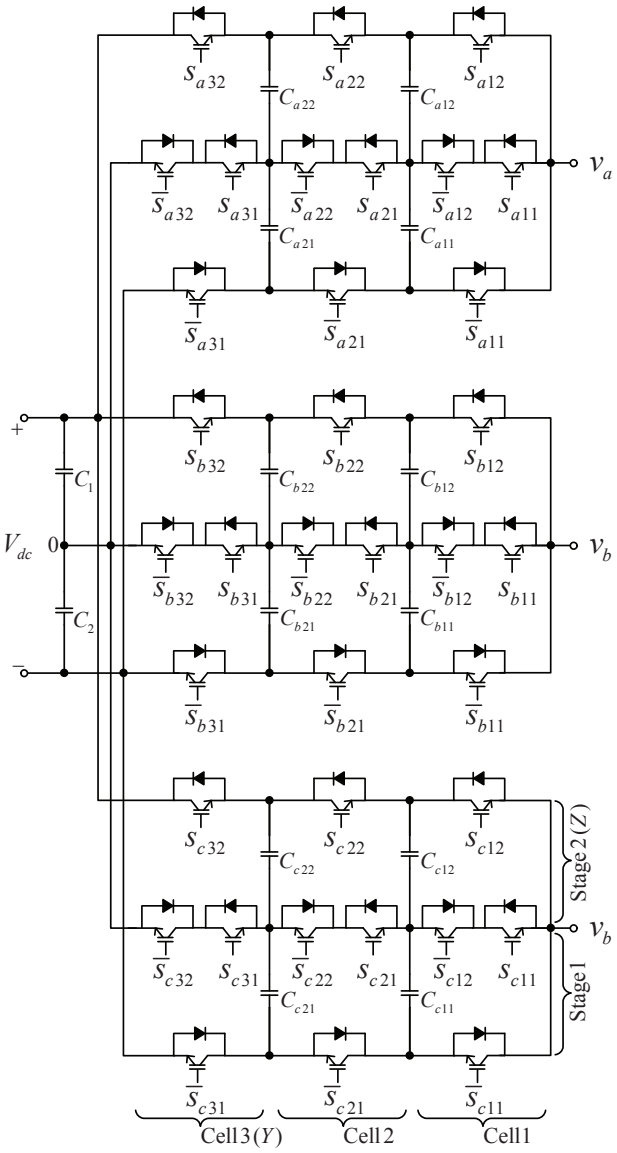


Fig. 1. Circuit diagram of a three-phase 3×2 SMC.

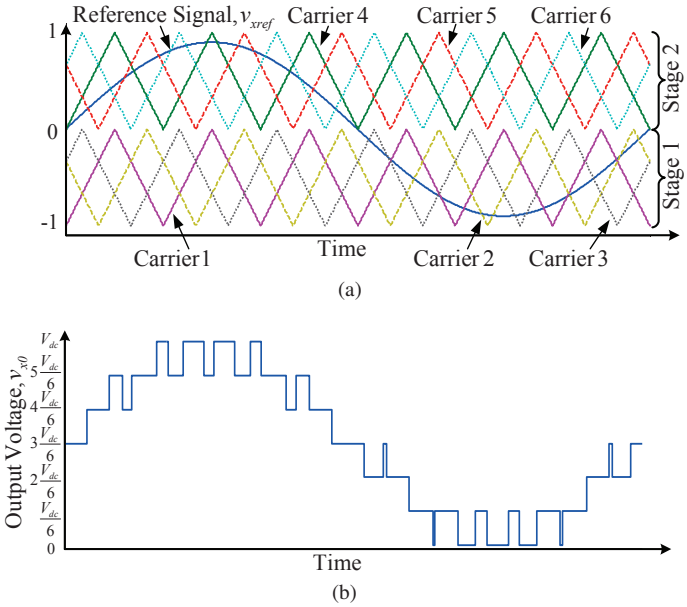


Fig. 2. PS-PWM technique for 3×2 SMC: (a) reference sinusoidal signal with six carriers and (b) output voltage.

which are integrated to form two stages/stacks ($Z = 2$). It is called as 3×2 SMC. The converter includes four FCs, the upper FCs, i.e, C_{x12} and C_{x22}, are in the Stage 2, while the lower FCs C_{x11}, C_{x21} are in the Stage 1, where the subscript x is used for phase identification x=$\{a, b, c\}$. The dc bus consists of two capacitors, C_1 and C_2, each of them regulated to have a half of the dc-link voltage ($V_{dc}/2$). During normal operation, the mean voltages of the FCs C_{x11} and C_{x12} have to be maintained at $V_{dc}/6$, whereas for FCs C_{x21} and C_{x22} have to be maintained at $V_{dc}/3$. The output voltage v_{x0} can produce seven voltage levels ($3 \times 2 + 1$), i.e. 0, $V_{dc}/6$, $V_{dc}/3$, $V_{dc}/2$, $2V_{dc}/3$, $5V_{dc}/6$, and V_{dc}. The switch control function are defined as $s_{x\,yz}$, where y denotes the switch number corresponding to a particular cell in the phase-leg x of the SMC converter $y = \{1, .., Y\}$ ($Y = 3$), and z defines a particular switch associated with the stage $z = \{1, .., Z\}$ ($Z = 2$). The switch control functions can take two values $s_{x\,yz} = \{0, 1\}$, meaning "0" and "1" that the switch is off and on, respectively. The switch pairs in each phase-leg ($s_{x\,yz}$ and $\overline{s}_{x\,yz}$) operate in a complementary manner.

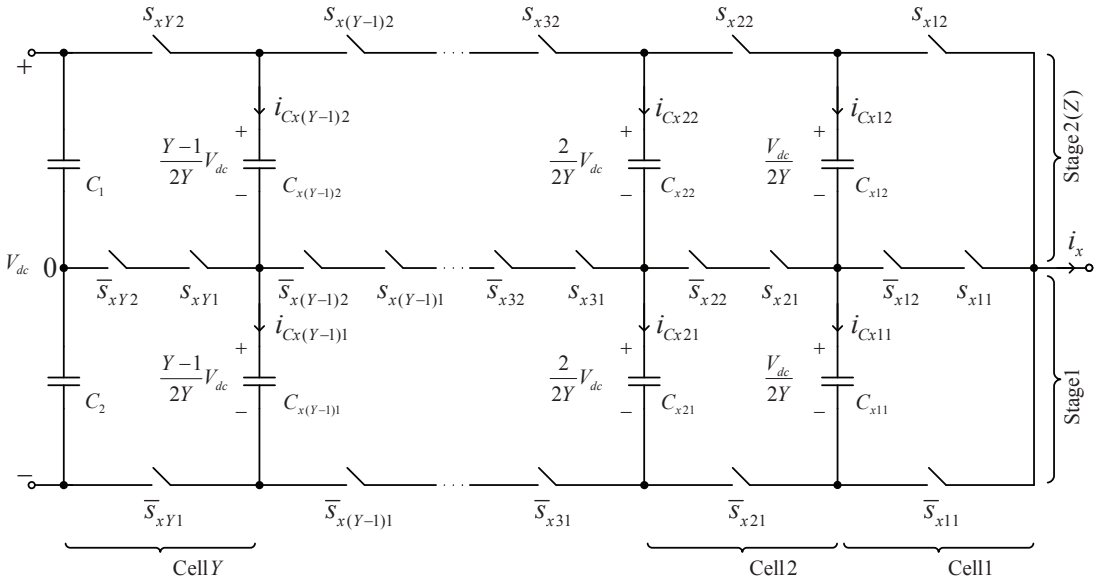
Fig. 2 shows a sinusoidal reference signal and the carrier signals using PS-PWM applied to a 3×2 SMC. In this converter, PS-PWM requires six carriers. The upper three carriers in Stage 2 are phase-shifted 120° between consecutive carriers. The same characteristics apply to the three lower carriers in Stage 1. A sinusoidal reference signal (v_{xref}) has been normalized to range in the interval [-1, 1] under linear modulation mode. It is compared with all six triangular carriers to define the voltage level that has to be generated at the output. Using this method, natural voltage balancing can be achieved. However, the voltage balancing process is usually slow and depends on the loading conditions. Therefore, an active balancing method is required to regulate the FC voltages at their desired levels with improved dynamics, especially under transient conditions and unbalanced linear/non-linear loads.

III. Proposed Voltage Balancing Method

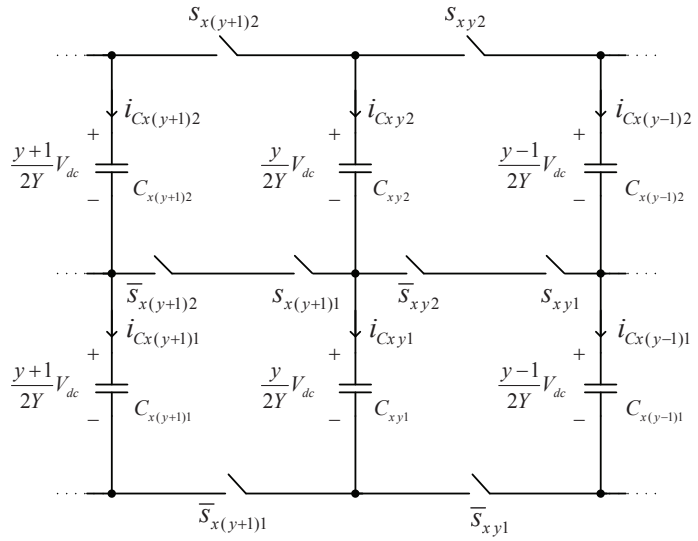
Fig. 3(a) shows a general $Y \times Z$ SMC phase-leg chain. The proposed voltage balancing method is developed based on the analysis of a generic cell section of the SMC as shown in Fig. 3(b). In this analysis $Z = 2$ is considered for simplicity. Assuming $v_{x\,ref} > 0$, where the switches $s_{x\,y1}$ and $s_{x\,(y+1)1}$ are turned on. Therefore, the current through capacitor $C_{x\,y2}$ is represented by [19]:

$$i_{Cx\,y2} = (s_{x\,(y+1)2} - s_{x\,y2})i_x. \tag{1}$$

It can be observed that during $v_{x\,ref} > 0$, the current through a capacitor is affected by the control signals associated



(a)



(b)

Fig. 3. One phase-leg of an SMC: (a) General $Y \times 2$ cell chain representation and (b) a section of the chain.

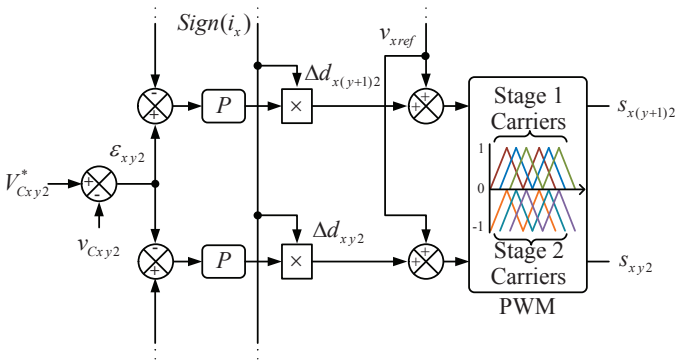


Fig. 4. Development of the proposed voltage balancing method based on (2).

to the two adjacent switches. The locally-averaged representation of the capacitor current calculated over a switching period is:

$$\bar{i}_{Cx\,y2} = (d_{x\,(y+1)2} - d_{x\,y2})\bar{i}_x, \tag{2}$$

where $\bar{i}_{Cx\,y2}$ and $\bar{i}_x$ are the locally-averaged currents of the capacitor $C_{x\,y2}$ and the output current, respectively, and $d_{x\,(y+1)2}$ and $d_{x\,y2}$ are the duty cycles of the switches $s_{x\,(y+1)2}$ and $s_{x\,y2}$ for Stage 2, respectively.

Assuming a positive output current $(i_x > 0)$, (2) shows that by increasing the duty cycle $d_{x\,(y+1)2}$ the locally-averaged current through the capacitor will increase, while the opposite effect will be produced if $d_{x\,y2}$ is increased. If the voltage of the capacitor $C_{x\,y2}$ is greater than its reference value, a negative current should be imposed to this capacitor. Therefore,

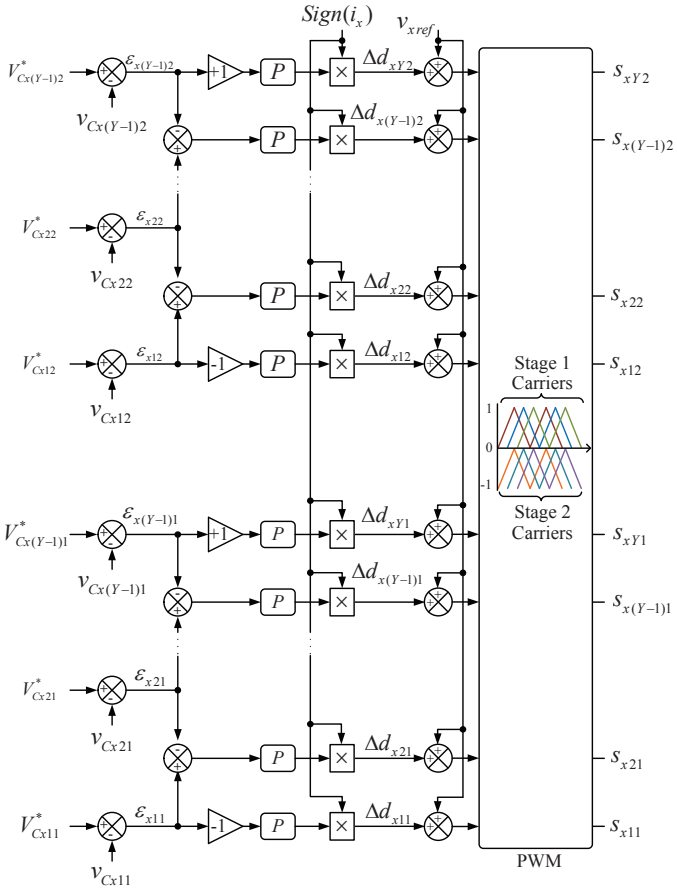


Fig. 5. Proposed voltage balancing method for a general $Y \times 2$ SMC.

the duty cycles $d_{x\,y2}$ and $d_{x\,(y+1)2}$ should be increased and decreased, respectively. On the other hand, if the output current is negative (i_x<0), the duty cycles should be manipulated in the opposite direction to help for voltage balance. Based on this analysis, the control method for voltage balancing is developed for the upper cells located in the Stage 2. A similar analysis can be performed for the bottom capacitor $C_{x\,y1}$ to achieve voltage balance, which is in the Stage 1. In this case $v_{x\,ref} < 0$, and the switches $\overline{s}_{x\,(y+1)2}$ and $\overline{s}_{x\,y2}$ are turned on. Fig. 4 shows the proposed voltage balance method for a general case, where $\Delta d_{x\,y2}$ and $\Delta d_{x\,(y+1)2}$ are control magnitudes added to the reference signal $v_{x\,ref}$ to compensate for voltage balance. Fig. 5 shows the complete voltage balancing method for a $Y \times 2$ SMC.

Assuming $v_{x\,ref} > 0$, the switches $s_{x\,y1}$ and $s_{x\,(y+1)1}$ are turned on, the voltage balancing dynamic of capacitor $C_{x\,y2}$ can be analyzed based on:

$$\bar{i}_{Cx\,y2} = C_{x\,y2}\frac{d\overline{v}_{Cx\,y2}}{dt} \Leftrightarrow \frac{d\overline{v}_{Cx\,y2}}{dt} = \frac{\bar{i}_{Cx\,y2}}{C_{x\,y2}}. \tag{3}$$

From (2) and (3), one can obtain:

$$\frac{d\overline{v}_{Cx\,y2}}{dt} = \frac{\bar{i}_x(d_{x\,(y+1)2} - d_{x\,y2})}{C_{x\,y2}}, \tag{4}$$

TABLE I
SMC CONVERTER PARAMETERS

Circuit Parameter	Value
DC Link Voltage (V_{dc})	100 V
Flying Capacitors (C_{x1}, C_{x2})	400 μF
Load Resistance (R)	44 Ω
Load Inductance (L)	6 mH
Carrier Frequency (f_s)	2 kHz
Fundamental Frequency (f)	50 Hz
Control Parameter (P)	0.04

where,

$$d_{x\,(y+1)2} = v_{x\,ref} + \Delta d_{x\,(y+1)2}, \tag{5}$$

$$d_{x\,y2} = v_{x\,ref} + \Delta d_{x\,y2}. \tag{6}$$

Assuming small variations around the operating point, using (5) and (6) in (4), one can obtain:

$$\frac{\Delta\overline{v}_{Cx\,y2}}{\Delta t} = \frac{\bar{i}_x(\Delta d_{x\,(y+1)2} - \Delta d_{x\,y2})}{C_{x\,y2}}. \tag{7}$$

The variations of the duty cycles are given by a proportional controller, as follows:

$$\Delta d_{x\,(y+1)2} = sign(i_x)(\varepsilon_{x\,y2} - \varepsilon_{x\,(y+1)2})P, \tag{8}$$

$$\Delta d_{x\,y2} = sign(i_x)(\varepsilon_{x\,(y-1)2} - \varepsilon_{x\,y2})P, \tag{9}$$

where $\varepsilon_{x\,(y-1)2}$, $\varepsilon_{x\,y2}$, and $\varepsilon_{x\,(y+1)2}$ are the voltage errors of the capacitors $C_{x\,(y-1)2}$, $C_{x\,y2}$, and $C_{x\,(y+1)2}$ at Stage 2, respectively, and P is the proportional control parameter. $sign(i_x)$ is the sign of the output current defined as 1 and -1 when i_x is positive and negative, respectively. Substituting (8) and (9) into (7):

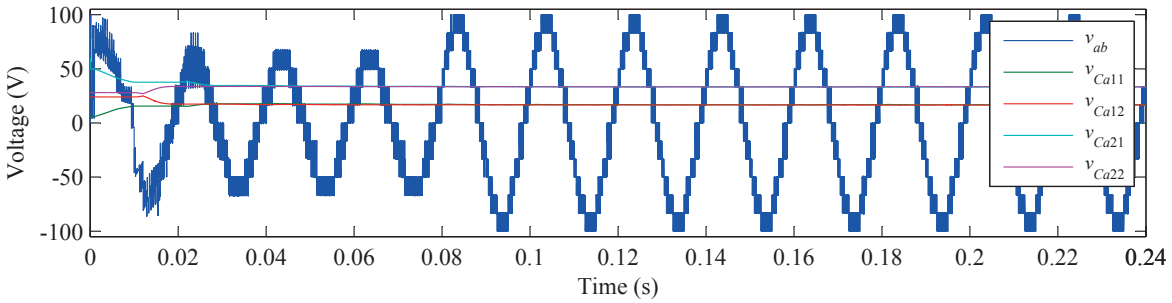
$$\frac{\Delta\overline{v}_{Cx\,y2}}{\Delta t} = \frac{|\bar{i}_x|P(2\varepsilon_{x\,y2} - \varepsilon_{x\,(y+1)2} - \varepsilon_{x\,(y-1)2})}{C_{x\,y2}}. \tag{10}$$

Equation (10) defines the balancing dynamic of the proposed voltage control for $Y \times 2$ SMC when $v_{x\,ref} > 0$ and can be used to tune the controller gain parameter P to achieve a satisfactory converter performance. A similar kind of analysis can be performed for $v_{x\,ref} < 0$, when switches $\overline{s}_{x\,(y+1)2}$ and $\overline{s}_{x\,y2}$ are turned on, for the voltage balance of the bottom capacitor $C_{x\,y1}$ in Stage 1.

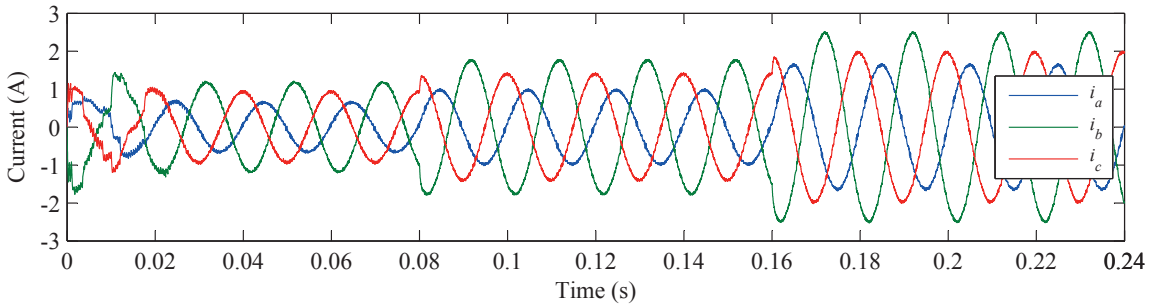
IV. PERFORMANCE EVALUATION

Simulation tests are performed on a three-phase 3×2 SMC converter as shown in Fig. 1. The converter has been simulated using the MATLAB/Simulink [20] and PLECS Toolbox [21]. The parameters of the converter are shown in Table I.

The dynamic behavior of the proposed voltage balancing method is shown in Fig. 6. In this test, the SMC is operating over a linear unbalanced RL load ($R_a = 70.4\Omega, R_b = 17.6\Omega, R_c = 44\Omega$). The line-to-line voltage v_{ab} and the capacitor voltages ($v_{Ca\,11}$, $v_{Ca\,12}$, $v_{Ca\,21}$, and $v_{Ca\,22}$) are shown in Fig. 6(a). In this simulation, the initial capacitor voltages are set to $v_{Ca\,11} = 6$V, $v_{Ca\,12} = 24$V, $v_{Ca\,21} = 28$V,

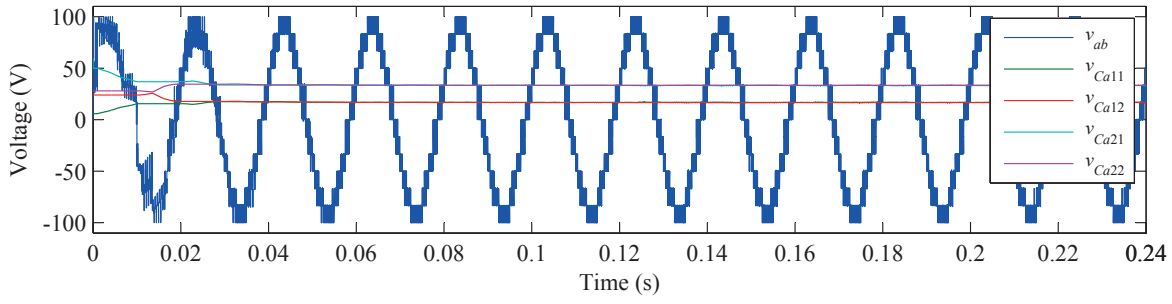


(a)

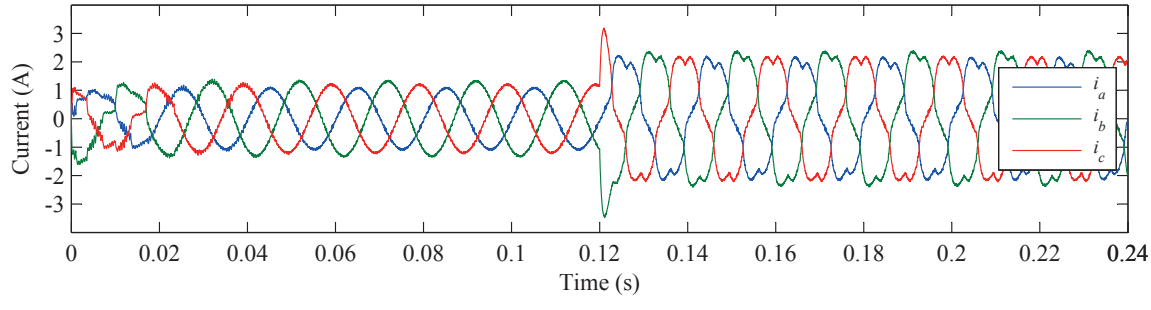


(b)

Fig. 6. 3x2 SMC operating over an unbalanced linear load. A step change in the modulation index from $m = 0.6$ to $m = 0.9$ occurs at 80 ms, and at 160 ms a three-phase Y-connected resistive load is added in parallel ($R_x = 88\Omega$): (a) line-to-line voltage (v_{ab}) and FC voltages ($v_{Ca11}, v_{Ca12}, v_{Ca21},$ and v_{Ca22}), and (b) output currents ($i_a, i_b,$ and i_c).



(a)



(b)

Fig. 7. 3x2 SMC operating over an unbalanced linear load and at 120 ms an non-linear load is added: (a) line-to-line voltage (v_{ab}) and FC voltages ($v_{Ca11}, v_{Ca12}, v_{Ca21},$ and v_{Ca22}), and (b) output currents ($i_a, i_b,$ and i_c).

$v_{Ca\,22} = 60$V and regulated to the desired voltages, i.e. 16.67 V, 16.67 V, 33.33 V, and 33.33V, respectively, in about 30 ms. It can be observed that the proposed voltage balancing method is capable of maintaining the capacitor voltages at the reference value under this unbalanced condition. There is a step change in the modulation index from $m = 0.6$ to $m = 0.9$ at 80 ms, and later at 160 ms, a three-phase Y-connected resistive load is added in parallel ($R_x = 88\Omega$). Observe that during the transients the voltages in the FCs remain unaffected. In Fig. 6(b), the load currents increase as expected during these transients. The proposed voltage balancing method proves to be robust under unbalanced loads and transients. Furthermore, although the proposed voltage balancing method is based on a proportional controller, the capacitor voltages are properly regulated at the reference values with no zero-order errors in the steady-state. This is because no control action is required ($\Delta d_{x\,y1} = 0$ and $\Delta d_{x\,y2} = 0$ for $y = \{1, 2, 3\}$) when the capacitor voltages are at the reference values.

In Fig. 7, the converter is tested against a non-linear load. Initialy, the converter operates over a linear unbalanced RL load ($R_a = 44\Omega, R_b = 35.2\Omega, R_c = 52.8\Omega$) with a modulation index of $m = 0.9$. At 120 ms, a non-linear load consisting of a three-phase diode rectifier with a filter capacitor of 30μF and a load resistor of 88Ω is added. It can be observed in Fig. 7(a), that the capacitor voltages are maintained to the desired references. The load currents shown in Fig. 7(b), are highly distorted as expected, but no effects on the FCs is seen. Hence, the proposed voltage balancing method is quite robust, as the capacitor voltages are maintained at their reference values under such a non-linear load and unbalanced conditions.

V. Conclusion

A new voltage balancing method for SMC operating with PS-PWM has presented which ensures the acceptable performance of the converter by maintaining the capacitor voltage levels. The method has been formulated for a $Y \times 2$ SMC and is tested on 3×2 SMC which produces seven levels. The proposed method is based on a proportional controller which is able to remove the steady-state errors. This is because when the capacitor voltages are at their reference values, i.e. the voltage errors are zero, no control action is required. It can regulate the capacitor voltages to their reference values, even under unbalanced load, non-linear load and transients. Moreover, it is simple and easy to implement in any $Y \times Z$ SMC configuration.

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