Control Strategy to Balance Operation of Parallel Connected Legs of Modular Multilevel Converters

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***Abstract*—Connecting legs of modular multilevel converters (MMCs) in parallel can assist an MMC-based high-voltage direct current (HVDC) to increase its current ratings and hence overall power handling capability. Consequently, each phase of the MMC would be integrated by several legs or sets of upper and lower arms (ULAs). This paper proposes a current control strategy for each ULA in order to ensure balanced current sharing among them. In addition, each ULA has its own circulating current control that follows a reference obtained from the instantaneous magnitudes of the output current and the modulation signal. All the proposed control actuations do not distort the phase output voltage of the MMC which follows the reference voltage. The performance of the proposed control strategies is evaluated by simulation studies in the PLECS Blockset under MATLAB/Simulink software platform.**

***Index Terms*—Modular multilevel converter, Circulating current control, Parallel legs, Current balance.**

I. Introduction

MULTILEVEL converters have attracted significant interests for medium/high power applications. Among various multilevel converter topologies [1], [2], the modular multilevel converter (MMC) [3], [4], offers several salient features which make it a potential candidate for various applications including high-voltage direct current (HVDC) power transmission systems [5], [6], flexible alternating current transmission system (FACTS) controllers [7], and motor drives [8]. The most attractive features of an MMC are (i) its modularity and scalability to handle different power and voltage levels, and (ii) its capacitor voltage balancing capability [9], [10].

Proper operation of the MMC necessitates an active voltage balancing scheme to carry out the voltage balancing task among the submodule (SM) capacitors. Capacitor voltage balancing of the MMC does not have the limitations and complexities associated with other multilevel converters [6]. However, with the benefits of no limitations and complexities come at a price of having to deal with the circulating currents in each phase-leg of the MMC. These circulating currents if not properly controlled, can affect semiconductor ratings, losses, and also the magnitude of the capacitor voltage ripples. Analysis of the circulating currents of an MMC has been reported in the technical literature and, correspondingly, various open- and closed-loop remedial measures have been proposed to minimize/eliminate them [11]–[13]. The open-loop strategies rely on the exact parameters of the MMC which cannot be as realistic in practical applications [12].

In [13], a closed-loop control strategy based on elimination of the second order harmonic of the arm currents has been proposed, while other strategies are focused on the injection of proper current harmonics in order to minimize capacitor voltage oscillations [14], [15].

Connecting phase-legs of MMCs in parallel can assist an MMC-based HVDC to increase its current ratings and hence overall power handling capability. Inductors are the passive components to connect in parallel several phase-legs in voltage source inverters (VSIs). They not only qualify for averaging the voltage from several legs to form the output voltage, but also for limiting circulating currents among the phase-legs. In the case of the MMC, the inductors are already integrated in the structure of the legs; therefore, no extra inductors are required. Making sure that the output currents are evenly shared among the legs connected in parallel is an important issue. Several techniques can be applied to achieve current balance among the legs. In [16], a fast current balancing strategy is presented. The exact modification of the modulation signals is calculated and applied. The method is performed without distorting both the output voltages and currents.

In this paper, in addition to the individual circulating current control of each leg, a control loop based on [16] is added to achieve even current sharing among the legs that integrate each phase. The effectiveness of the proposed strategy in terms of balancing the output currents in the legs of an MMC is presented. The studies are carried out based on simulations in the PLECS Blockset and MATLAB/Simulink environment. The analysis and conclusions of this paper are general and applicable to MMC converters with any number of voltage levels and phase-legs connected in parallel.

The rest of the paper is organized as follows. Section II

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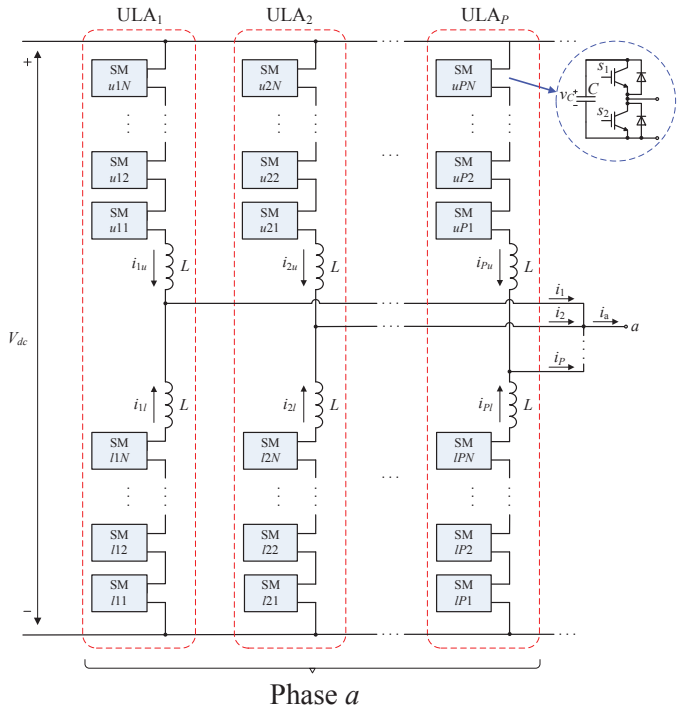


Fig. 1. MMC phase-leg with parallel-connected ULAs.

presents the structure of the MMC with legs connected in parallel. Section III presents the equivalent common- and differential-mode circuits of an MMC leg. Section IV introduces a differential current reference for each leg of the converter to produce low ripple amplitudes for the capacitor voltages. Section V describes the proposed control strategies for this system. Section VI reports the simulation results, and Section VII concludes this paper.

II. The MMC with Legs Connected in Parallel

Fig. 1 shows an MMC phase-leg with P sets of upper and lower arms (ULAs) connected in parallel. Each leg has two arms that include N series-connected, identical, half-bridge submodules (SMs). The output voltage of each SM is either equal to its capacitor voltage (v_C) or zero, depending on the switching states of the switch pairs s_1 and s_2 in each SM. Reactors L are inserted in the circuit to control the circulating currents and to limit the fault currents. They are also necessary to connect the ULAs in parallel.

To synthesize the output voltage waveform at the ac-side of the converter, a phase-disposition pulse-width modulation (PD-PWM) strategy can be applied. The PD-PWM technique requires N in-phase carrier waveforms displaced symmetrically with respect to the zero-axis [6].

Fig. 2 shows the equivalent circuit of an MMC phase-leg with parallel-connected ULAs, where the voltages v_{u_p} and v_{l_p} for $p = \{1, 2, ..., P\}$ are provided to the extremes of the series inductors of each ULA. The number of activated SMs in each arm define the instantaneous value of the variable capacitors C_{u_p} and C_{l_p}. Although this way of representing the ULAs is

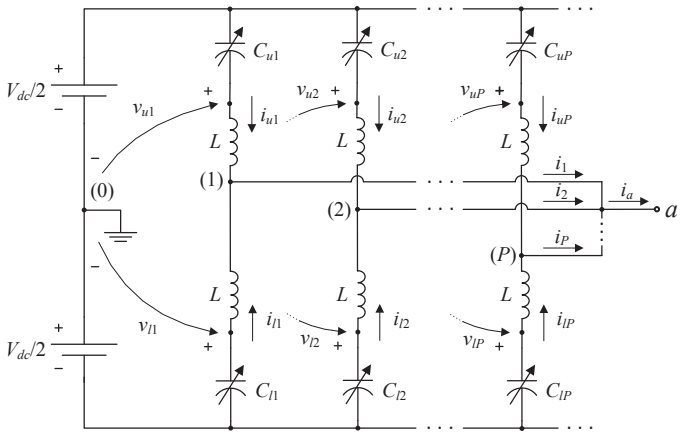


Fig. 2. Equivalent circuit of an MMC phase-leg with parallel-connected ULAs.

not acceptable to evaluate the energy in the arms because the capacitors of the non-activated SMs are not considered, this model is useful to study the voltages and currents in the arms.

III. Common- and Differential-Mode Circuits of the ULAs

The output currents of the ULAs can be balanced by using the controller proposed in Section V. The proposed balancing controls does not affect the output phase voltage and the circulating currents of the ULAs. Therefore, the circulating currents can be independently controlled irrespective of the number of ULAs in parallel.

In this section, equivalent common- and differential-mode circuits of an ULA are obtained. These are used later for the control of the circulating currents. Because of independence between control actions, a single ULA is represented.

Assuming a grid-connected MMC, the circuit of an ULA can be seen as in Fig. 3(a), where z_{out} represents the impedance between the converter and the grid voltage e_a. The same circuit can also be seen in Fig. 3(b), where the common- and differential-mode voltages of the ULA are given by:

$$v_{comm_p} = \frac{v_{u_p} + v_{l_p}}{2} \quad \text{and} \tag{1}$$

$$v_{diff_p} = \frac{v_{u_p} - v_{l_p}}{2}. \tag{2}$$

Applying the principle of superposition, common- and differential-mode mode circuits can be separated, as they are shown in Fig. 3(c) and (d), respectively. The common and differential arm currents in each ULA will be:

$$i_{comm_p} = \frac{i_{u_p} + i_{l_p}}{2} = \frac{i_p}{2} \quad \text{and} \tag{3}$$

$$i_{diff_p} = \frac{i_{u_p} - i_{l_p}}{2}. \tag{4}$$

From (3) and (4) the arm currents can be deduced as follows:

$$i_{u_p} = i_{comm_p} + i_{diff_p} = \frac{i_p}{2} + i_{diff_p}, \tag{5}$$

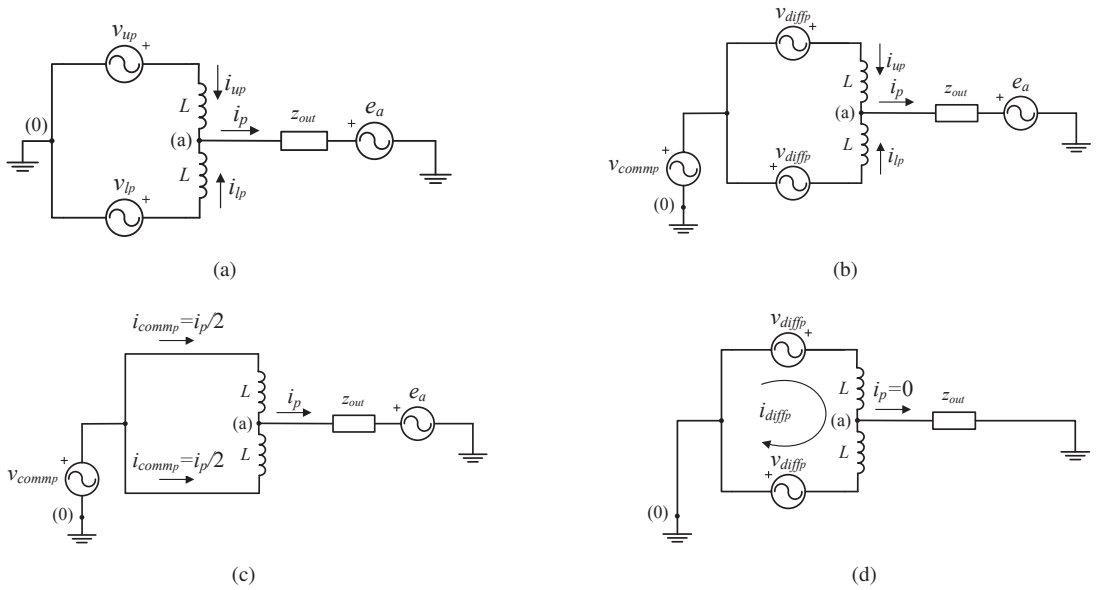


Fig. 3. Equivalent circuits: (a) original circuit including voltages v_{u_p} and v_{l_p}, (b) with common- and differential-mode voltages, (c) common-mode circuit, and (d) differential-mode circuit.

$$i_{l_p} = i_{comm_p} - i_{diff_p} = \frac{i_p}{2} - i_{diff_p}. \tag{6}$$

The two circuits in Fig. 3(c) and (d) can be analyzed independently. Therefore, some differential voltage can be introduced to control the differential (or circulating) current within the ULA without producing any distortion to the output current of the ULA.

According to Fig. 3(d), the differential current will be:

$$i_{diff_p} = \frac{1}{L}\int_0^t v_{diff_p} dt + I_{diff0_p}, \tag{7}$$

where I_{diff0_p} is the initial value of the differential current of the ULA. The differential current contains a dc component that is essential to keep the arms energized; i.e. maintain the capacitor voltages around the reference value [14]. On the other hand, ac current components can be defined freely to meet some objectives, such as minimizing the voltage ripples of the SM capacitors [15] or the rms value of the arm currents in order to improve the MMC efficiency.

IV. Differential Current Reference

The differential current reference for each ULA can be determined from the instantaneous value of the ULA output current. The target is not only to determine the dc current needed, but also an ac component capable of reducing the capacitor voltage ripple amplitudes. The reasoning behind this is explained in the following.

In order to produce low ripple to the capacitor voltages, the arm that inserts fewer capacitors connected in series (i.e. higher equivalent capacitance) should carry more current. This is equivalent to assume that the inductors L in the model in Fig. 2 are zero and the output current of each leg flows naturally within the arms [17]. Although this is not a realistic situation, the inductors are always used in a practical system, the currents produced in the arms under this assumption will be very convenient. Therefore, those currents will be determined and used as reference values for the arm currents.

If the variables u_p and l_p, where $p = \{1, 2, ..., P\}$, are the number of series connected SMs in the upper and lower arms at any time, respectively, the value of the equivalent capacitors C_{u_p} and C_{l_p} are:

$$C_{u_p} = \frac{C}{u_p} \quad \text{and} \tag{8}$$

$$C_{l_p} = \frac{C}{l_p}. \tag{9}$$

The output current of each ULA (i_p where $p = \{1, 2, ..., P\}$) is shared between the upper and the lower arms based on the following equations:

$$i_{u_p} = i_p \frac{C_{u_p}}{C_{u_p} + C_{l_p}} = i_p \frac{l_p}{u_p + l_p} \text{ and} \tag{10}$$

$$i_{l_p} = i_p \frac{C_{l_p}}{C_{u_p} + C_{l_p}} = i_p \frac{u_p}{u_p + l_p}. \tag{11}$$

The locally averaged value of u_p and l_p, calculated over a switching period, can be represented by:

$$u_p = N(1 - v_{am}) \text{ and} \tag{12}$$

$$l_p = N(1 + v_{am}), \tag{13}$$

where v_{am} is the modulation or reference signal of the leg normalized in the interval [-1,1]. In the steady state and under sinusoidal operation mode, the modulation signal is:

$$v_{am} = v_{am1} + v_o = m_a cos(\omega t) + v_o, \tag{14}$$

m_a being the modulation index, and v_o a normalized zero-sequence signal introduced to extend the linear operation mode

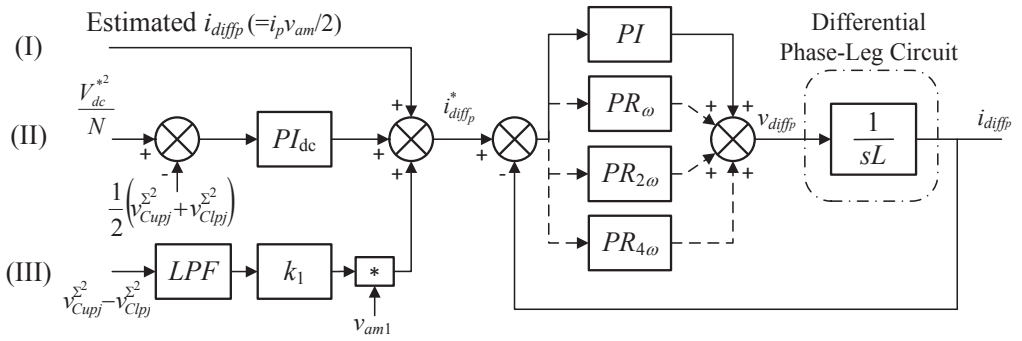


Fig. 4. Scheme of the differential current control.

of a multiphase system (up to m_a=1.1547 in the case of a three-phase MMC).

Substituting (12) and (13) into (10) and (11), the arm currents become:

$$i_{u_p} = i_p \frac{1+v_{am}}{2}, \tag{15}$$

$$i_{l_p} = i_p \frac{1-v_{am}}{2}. \tag{16}$$

Equations (15) and (16) provide the instantaneous references for the arm currents of the ULA. Considering (4), the differential term is:

$$i_{diff_p} = \frac{i_p v_{am}}{2}. \tag{17}$$

Equation (17) provides the differential current reference obtained from the instantaneous value of the output current of the ULA$_p$ and the modulation signal of the phase.

V. Voltage and Current Controls

A. Control of the Differential Currents

The differential current of each ULA can be controlled using the scheme shown in Fig. 4. In this control scheme, there are three signals that define the reference for the differential current $i^*_{diff_p}$:

I. The estimated instantaneous reference current given by (17). This reference contains an ac current component, mostly integrated by a second order harmonic and a dc current. The harmonic components help to reduce the capacitor voltage ripple amplitudes. The dc component matches the value needed to keep power balance in the ULA assuming that the efficiency of the MMC were 100 %. This is, therefore, a draft estimation of the dc current component and thus, an additional control for the dc current is needed.

II. An extra dc current component able to lead the average energy stored in the SM capacitors to the reference value. The sum of all the quadratic voltages in the capacitors is measured, which is proportional to the energy stored in the capacitors. The error goes through a proportional-integral controller (PI_{dc}) where the integral part is needed to eliminate steady state errors.

III. A fundamental-frequency current component. This current will transfer energy between the upper and lower arms of each ULA; therefore, this control loop will help to keep energy balance between the arms. To achieve optimal performance of the balancing algorithm, this term has to be synchronized with the fundamental component of the modulation signal. The fundamental component is obtained from the original modulation signal (v_{am1}) before a zero sequence to extend the linear modulation index range is added (v_o). On the other hand, a low pass filter is needed in this loop because there is energy fluctuation between the upper and lower arms, even when the total energy within the ULA is constant. This control loop is not provided with an integrative part but only with a proportional one (k_1). This is because the control action required from this controller when the upper and lower arms are balanced is zero. Therefore, the error is canceled in the steady state.

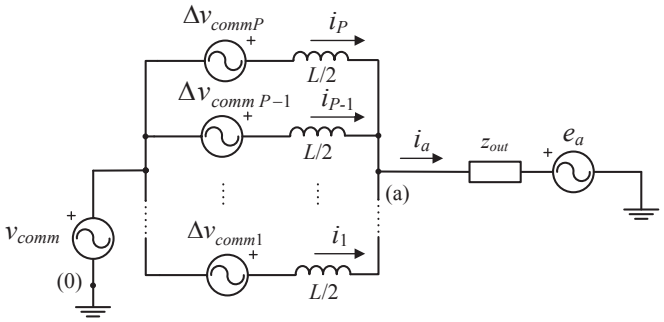


Fig. 5. Common-mode scheme of P MMC ULAs connected in parallel.

The reference obtained for the differential current ($i^*_{diff_p}$) is provided to the current controller (Fig. 4). Since the current reference contains not only a dc term but also certain harmonics, a set of proportional-resonant (PR) controllers may be included in addition to a proportional-integral (PI) controller. Each of them is tunned at the main frequency components of the current reference (ω, 2ω, and 4ω). The harmonic component 3ω is not tracked although it may appear in the current reference. This is because the third harmonic component would produce ripples in the dc bus current that cannot be canceled by the other phase-legs of a three-phase system [14].

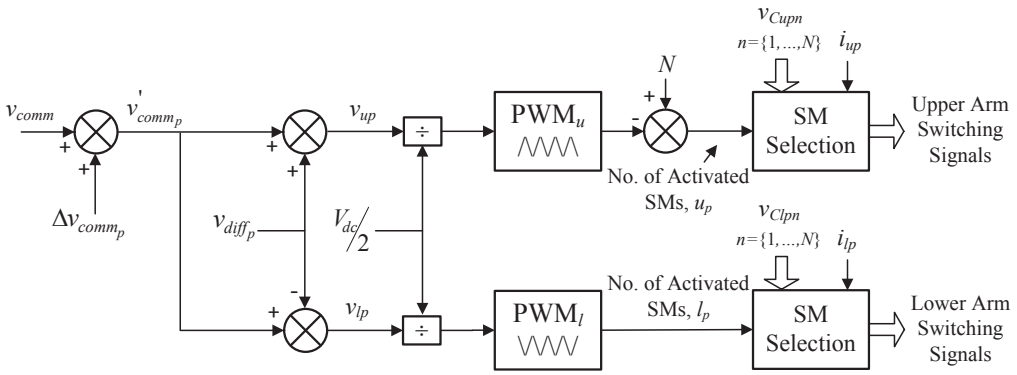


Fig. 6. Proposed modulation scheme with the modification of the modulation signal for each arm within an ULA.

B. Capacitor Voltage Balancing Control

A voltage balancing algorithm is used to keep voltage balance among the capacitors in the SMs of each arm [6]. It is based on the following principles:

- If the number of activated SMs in the arm increases, the new activated ones will be those that have lower/higher voltages if the arm current direction is such that it would charge/discharge the capacitors.

- If the number of activated SMs in the arm decreases, the deactivated ones will be those that have higher/lower voltages whenever the arm current direction is such that it would charge/discharge the capacitors.

Whenever there is a change in the output voltage level, a voltage balancing strategy that allows to change the minimum number of required modules can be used to reduce the switching frequency of the power devices. In other words, if the arm has to increase a single level, only one SM should be activated and no other combination can happen, such as activation of two SMs and deactivation of one SM simultaneously.

C. Current Balancing Among the Legs

Some additional control actions have to be included to achieve balanced current sharing among the ULAs. In Fig. 5, each ULA has been substituted by its equivalent common-mode or Thevenin circuit. This circuit is similar to the parallel connection of inverter legs described in [16]; therefore, the same control law can be applied. In order to achieve current balance, the modulation signal of each ULA is modified at any switching period (T_s) by adding the following term:

$$\Delta v_{comm_p} = -\frac{L}{2T_s}\Delta i_p, \tag{18}$$

where Δv_{comm_p} is the control variable that should be applied to the ULAp, and Δi_p the measured current error given by:

$$\Delta i_p = i_p - \frac{i_a}{P}. \tag{19}$$

According to [16], the output voltage will not be distorted if the sum of the control variables Δv_{comm_p} meets the following condition:

$$\sum_{p=1}^{P} \Delta v_{comm_p} = 0. \tag{20}$$

The control variable Δv_{comm_p} is added to the phase voltage reference v_{comm} ($= v_{am} V_{dc}/2$), as follows:

$$v'_{comm_p} = v_{comm} + \Delta v_{comm_p}, \tag{21}$$

considering (18):

$$v'_{comm_p} = v_{comm} - \frac{L}{2T_s}\Delta i_p. \tag{22}$$

This modification of the reference signal is equivalent to shifting the voltages of each ULA in the same direction:

$$v'_{u_p} = v_{u_p} + \Delta v_{comm_p} \tag{23}$$

$$v'_{l_p} = v_{l_p} + \Delta v_{comm_p} \tag{24}$$

and therefore the differential voltage is not affected:

$$v_{diff_p} = \frac{v'_{u_p} - v'_{l_p}}{2} = \frac{v_{u_p} - v_{l_p}}{2}. \tag{25}$$

As a consequence, the differential current within each ULA is not affected by this current balancing control. Similarly, the equivalent phase voltage (i. e. Thevenin voltage of the entire phase), given by:

$$v'_{comm} = \frac{\sum_{p=1}^{P} v'_{comm_p}}{P} = \frac{\sum_{p=1}^{P} (v_{comm} + \Delta v_{comm_p})}{P}, \tag{26}$$

will not be affected either if restriction (20) is applied:

$$v'_{comm} = \frac{\sum_{p=1}^{P} v_{comm}}{P} = v_{comm}. \tag{27}$$

Fig. 6 presents a scheme on how the control signals have to be applied to properly modify the modulation signals of each ULA. Firstly, current balance among the ULAs is achieved by adding Δv_{comm_p} to the general modulation signal for the phase v_{comm}. The differential current of each ULA is controlled by the control signal v_{diff_p}, which is applied with opposite signs to the upper and lower arms. Then, both modulation signals are normalized within the range [-1, 1]

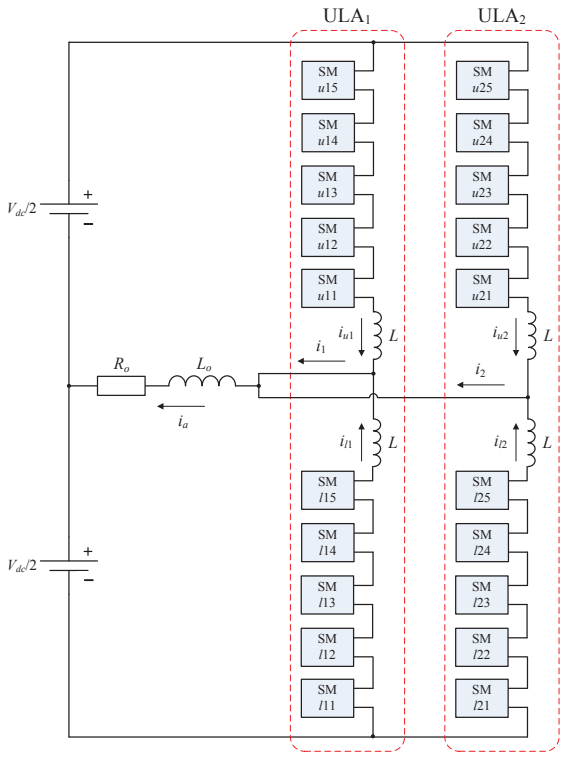


Fig. 7. Single-phase configuration based on two ULAs connected in parallel.

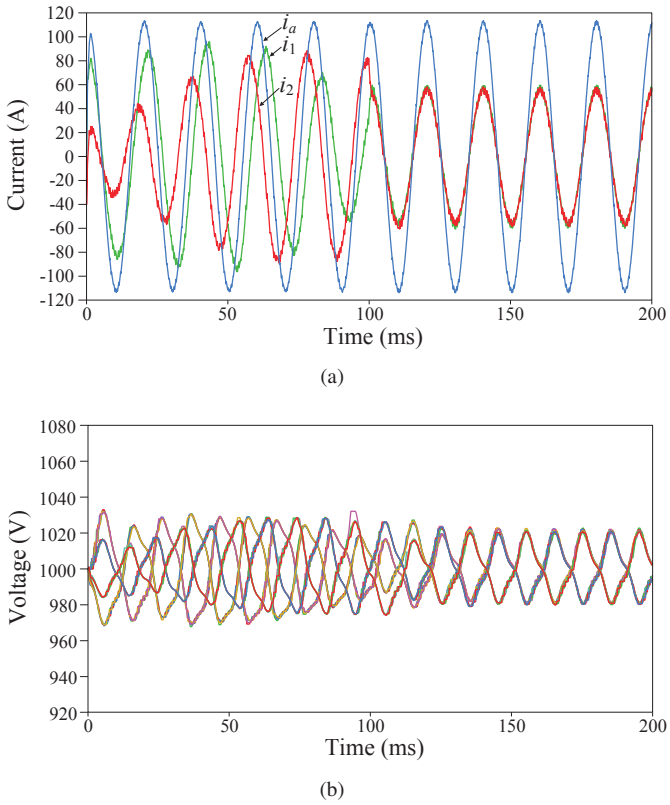


Fig. 8. Simulation results operating over an RL load (Load 1 in Table I). The current balance control is activated at the instant t= 100 ms: (a) currents of ULA$_1$ and ULA$_2$ (i_1 and i_2, respectively) and output current (i_a), (b) voltages in the SM capacitors.

by dividing by V_{dc}/2. Each modulation signal goes through a PWM block with N level-shifted carriers. The carriers used for the upper and lower arms are phase-shifted by 180 degrees to achieve the interleaving effect and thus improve the quality of the output voltages and currents. Phase-shifting among the carriers of the different ULAs can also be performed to achieve further improvements of the output waveforms.

VI. Simulation Results

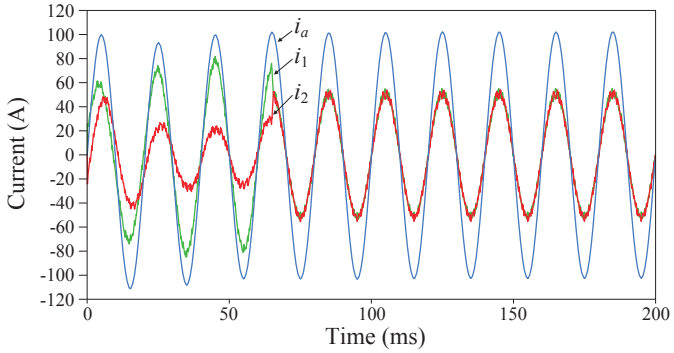
A single-phase converter with two ULAs connected in parallel has been modeled using PLECS Blockset under Matlab-Simulink environment. Fig. 7 shows the scheme of the modeled system and Table I provides the specifications of the test converter for the simulations.

Fig. 8 shows results for a converter operating with an RL load (Load 1 in Table I). The system starts starts with an initial current imbalance between the two ULAs and with the current balancing control deactivated. At the instant t= 100 ms the proposed balancing control is activated. Fig. 8(a) shows the currents of ULA$_1$ and ULA$_2$ (i_1 and i_2, respectively), and also the output current (i_a). Observe that the two output currents remain unbalanced while the current balancing control is deactivated. Both currents become balanced quickly under the proposed balancing control. Fig. 8(b) shows the voltages in all the SM capacitors. In this case there is a tendency to balance the voltages while the current balancing controller is deactivated. This is due to the independent energy balancing control between the arms that each ULA has. In addition to that, the voltages of the SMs in the arms are quickly balanced when the current balancing controller is activated.

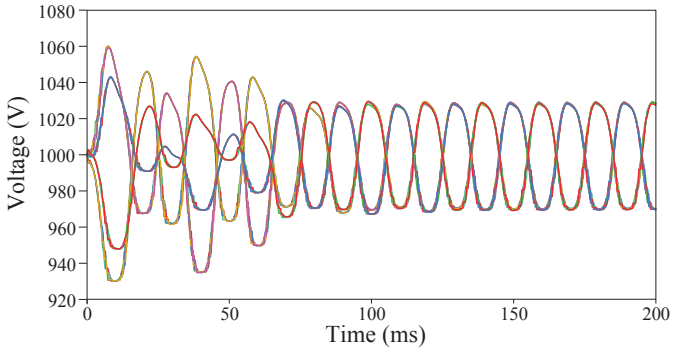
TABLE I
Specifications of the Test Converter for the Simulations

Parameter	Value
Number of SMs per Arm, N	5
Number of Legs in Parallel, P	2
SM Capacitors, C	1 mF
Arm Inductors, L	10 mH
Load 1	R_o= 20 Ω, L_o= 5 mH
Load 2	R_o= 0 Ω, L_o= 70 mH
DC-Link Voltage, V_{dc}	5 kV
SM Voltage, V_C	1 kV
Modulation Index, m_a	0.9
Carrier Frequency, f_s	5 kHz

Fig. 9 shows a similar simulation analysis, but in this case the load is purely inductive (Load 2 in Table I). The system starts with the same initial current imbalance as the test performed in Fig. 8. The current balancing control is activated at t= 65 ms and Fig. 9(a) shows that both currents become balanced quickly. Fig. 9(b) shows the voltages in all the SM capacitors. Again the voltages balancing dynamic of the SMs in the arms is accelerated when the current balancing controller is activated.



(a)



(b)

Fig. 9. Simulation results operating over a purely inductive load (Load 2 in Table I). The current balance control is activated at the instant t= 65 ms: (a) currents of ULA_1 and ULA_2 (i_1 and i_2, respectively) and output current (i_a), (b) voltages in the SM capacitors.

VII. Conclusion

The MMC is a topology able to deal with high voltage and power. The connection of MMC ULAs in parallel allows to increase further the rated power of the system. Although the parallel connection of ULAs can be performed directly because they already contain inductors, such a connection requires a current balancing controller otherwise overcurrent in some ULAs may be produced. The current balancing strategy proposed in this paper is able to achieve current balance and stabilize the system. This technique is general and can be applied to an MMC with any number of ULAs per-phase connected in parallel. Furthermore, the current balancing control action does not affect the output voltage and the differential current control.

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